MAPS and LGAD ...

Motivation

> Current Trend for all detectors

- High Granularity
- Precision timing
- Low Material

> Past

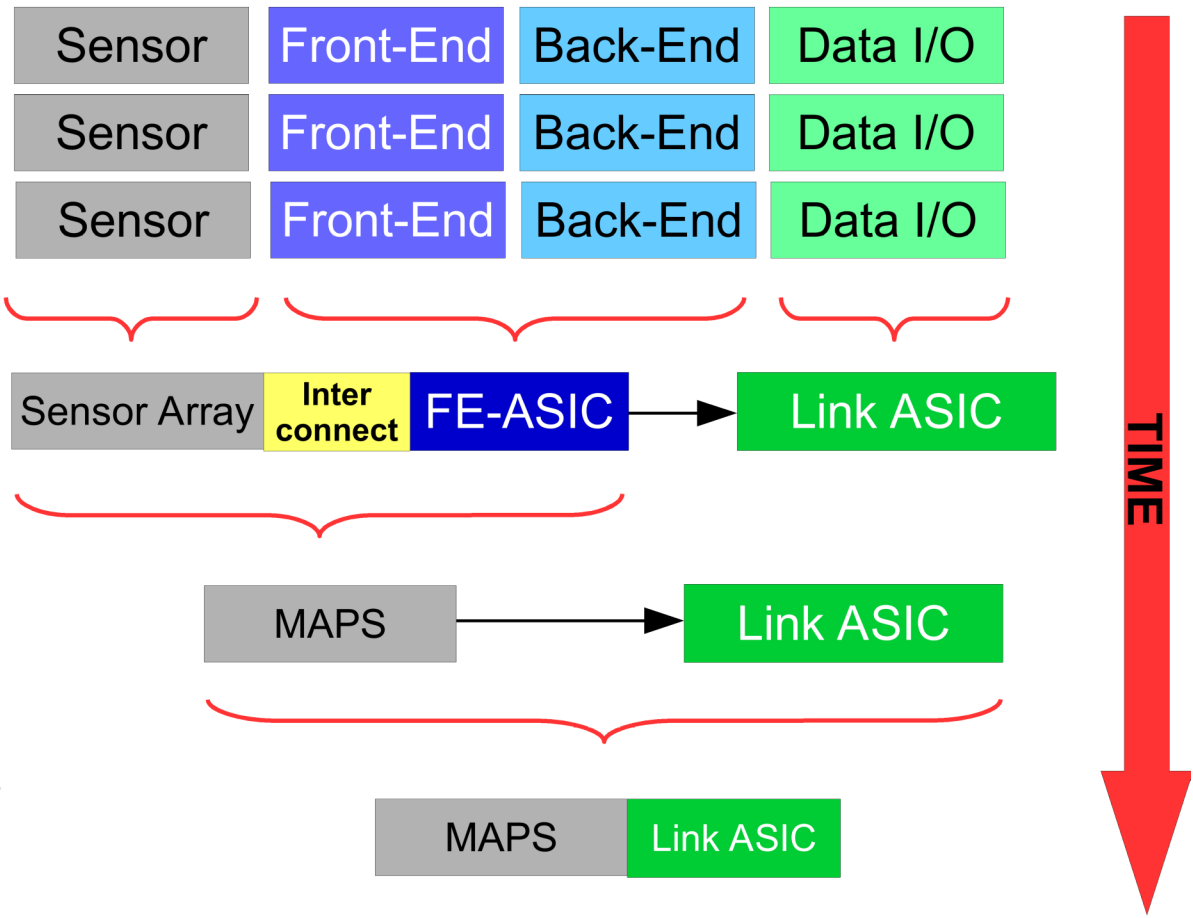
- Individual Building Blocks put together
- “Systems Expertise”

> Present

- ASICS & Interconnects are the focus

> Future needs

- Higher granularity not possible with current “present” approach
  - Power cabling, Interconnects
- Fully Monolithic and/or Advanced Interconnects
- Snappy Timing with “ok” spatial resolution → LGAD



The Status at DESY

MAPS

- **Mostly "system builder" → e.g. telescope**
  - Mimosa26-based telescope
  - ALPIDE Integration
  - CHESS effort for ATLAS Upgrade
- **Expertise**
  - Lots of people with MAPS experience (both at FH & FS)
- **Lessons learned**
  - Design expertise crucial to have impact on the entire system already early on
- **Status**
  - In MAPS we're a late-comer
  - Strong statements in POF

LGAD

- **Ideas & Conceptual studies**
- **Expertise**
  - Not as widespread as for MAPS
- **Status**
  - LGAD features prominently in "Quantum Universe" & POF

Processes in Use at DESY

Foundry	Node	Option	Layer/Substrate	MPW	Cost	Application
GF (IBM)	130 nm		low R	no	high	old CMOS Workhorse
TSMC	65 nm	RF	low R	yes	low	new CMOS Workhorse
TJ	180 nm	CIS	high-R ≤18-µm Epi	yes	medium	MAPS Workhorse, SPAD
TJ/Panasonic	65 nm	CIS	low-R 5-µm Epi	no	high	CIS Highlight, MAPS ?
TJ	65 nm	RF	low R	yes	medium	
LFoundry	150 nm		high R	yes	very low	MAPS, SPAD
LFoundry	110 nm		high R	yes	low	MAPS, SPAD
GF	90 nm		low R (SOI)	yes	medium	CMOS + Si Photonics
AIM*	65 nm		low R (SOI)	yes	medium	Si Photonics

*: NDA under way

The Future

MAPS

- **In POF we identified MAPS as a way forward to meet future requirements**
  - Need to build-up design expertise
  - Need to look ahead for the next 10 years
- **65 nm is the "next big thing"**
  - 180 nm is going to disappear on a timescale of ten years.
  - Note, it took 12 years from a first MAPS in TJ180 to ALPIDE and a lot of "process goodies" did not exist in 2006
  - It will require significant investments
  - Cooperation to organize MPWs
- **3D Stacks**
  - Always been the next big thing
  - But Industry is getting interested
  - Merge a MAPS with a "silicon photonics layer or an LGAD

LGAD

- **Timing Plane for the Telescopes**
  - Together with QU
- **Explore the limits of LGAD**
  - How precise can we time-stamp ?
  - Understand the limits of the technology
  - Explore the radiation hardness
- **Telescope as a tool to explore LGAD and its limitations**
  - Real user demand
  - Get the "System experience"

Challenges and Risks

- **Currently we are not ideas-limited**
  - And compared to many other groups we are quite “well-fund”
  - Unique here: We have our “own” test beam
- **But an ambitious R&D program will require a strong technical base**
  - ASIC Design effort
  - Any new chip needs testing environment - DAQ, PCB’s Firmware, mechanical support
  - We already tight there in many areas
- **Risk in Technology choices**
  - It is probably prudent to follow the CMOS industry trends
  - Single-vendor not-standard process carry theirs risks (remember the DEPFETS)
- **Cost**
  - ASIC and MAPS development will require significant budget for submissions
- **People**
  - Next generation of detector experts → long-term job perspective