TCAD Simulation of High Voltage Monlithic Active Pixel Sensors

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für Bildung
und Forschung

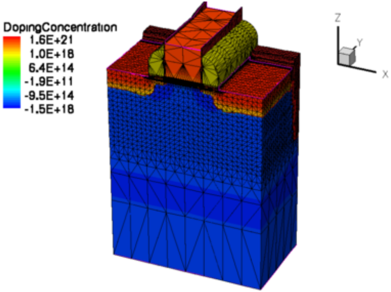
HighR

TCAD

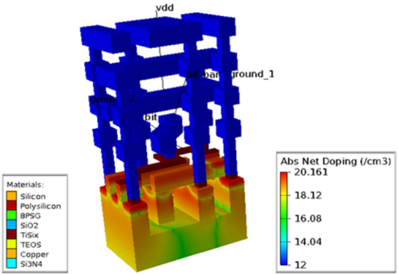
Technology Computer Aided Design

Simulation of semiconductor processing technology and device operation for development, manufacturing and characterization

SYNOPSYS® ✓



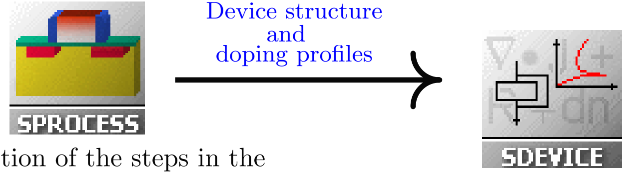
SILVACO



TCAD

What do TCAD tools do?

- Simulation of tiny and complex structures in 2D and 3D.



Device structure
and
doping profiles

Reproduction of the steps in the fabrication process

- Deposition of layers
- Etching
- Ion implementation
- Diffusion
- Etc ... (almost any process perform in a real clean room)
- Used for the foundry to evaluate the technological process

Simulation of electrical, thermal, and optical characteristics using a FEM

- Physical models: mobility, recombination, avalanche, ...
- Quasistationary simulation (Capacitance, Electric Field ...)
- Transient simulation of Minimum Ionizing Particle (MIP)

TCAD

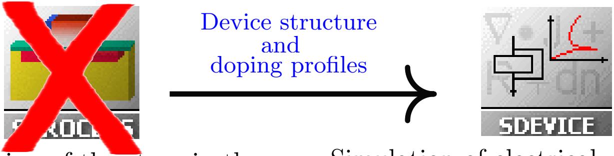
Why use TCAD?

1. Reduce the iteration process, saving time and money
2. Help to estimate essential properties in the sensor performance, as
    - Breakdown Voltage
    - Pixel Capacitance
    - Charge collection time
3. Complement to laboratory measurements

TCAD

In our case ...

1. We are not developing a technological process
2. In most of the cases, the foundry does not reveal the process



Device structure
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Reproduction of the steps in the fabrication process

Simulation of electrical, thermal, and optical characteristics using a FEM

TCAD

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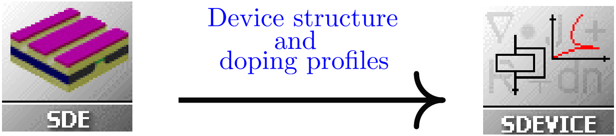


Device structure and doping profiles

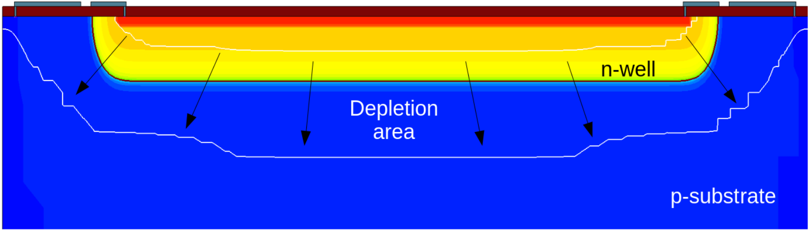
Reproduction of the device structure and doping profiles using geometric shapes

Simulation of electrical, thermal, and optical characteristics using a FEM

3. The mesh (SNMESH) is the most time consuming step (Trial and error)
    - Should be fine (have small elements) in areas that are important for the subsequent calculations
    - Too many points cause very long simulation and memory errors

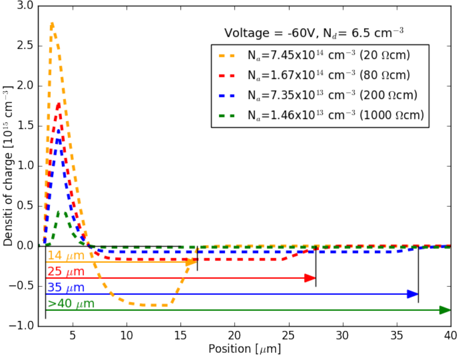
Substrate resistivity

- Pixel simple structure (p-n junction reversely biased)

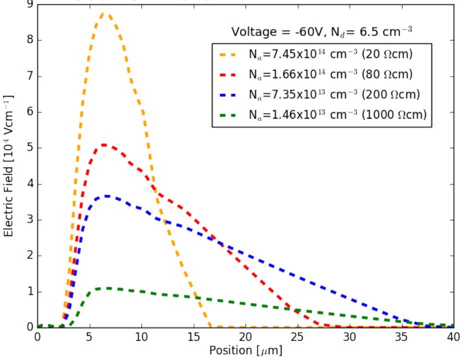


Substrate resistivity

- Space of charge



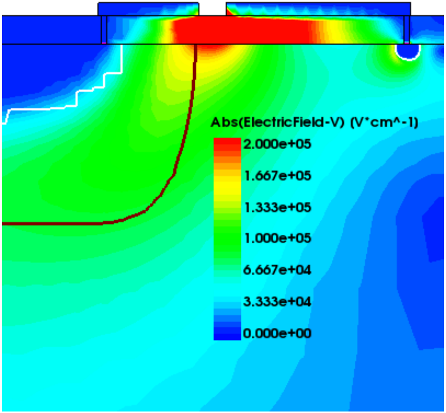
- Electric Field



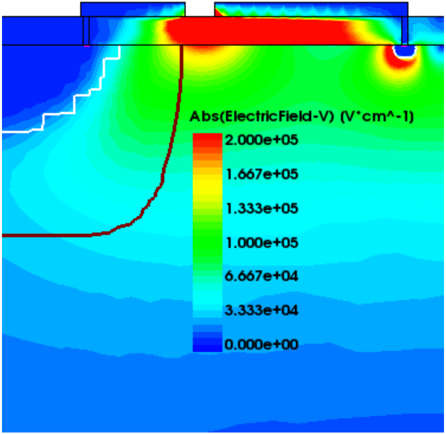
1. Depletion depth
   - Higher resistivity → Thicker depletion zone (More sensitive area)
2. Electric Field
   - Lower resistivity → Higher Electric Field (Faster collection charge)

Substrate resistivity

- 80 Ωcm



- 1000 Ωcm

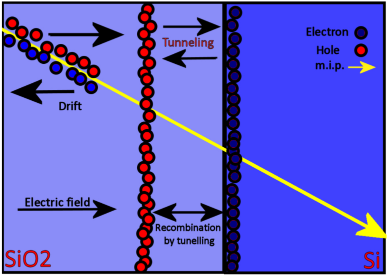


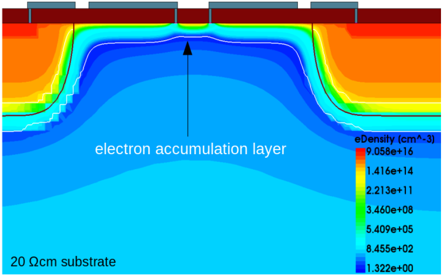
@ -100 V

Pixel Isolation

Why do we need isolation between pixels?

- SiO2 used for surface passivation, protecting from moisture and atmospheric contaminants (also as active gate electrode in MOS devices)
- Crystal structure highly irregular, displacement of single atoms do not lead to macroscopic changes, but is the main material damaged by ionizing radiation
- If the holes arrive to the transition region between Si and oxide where many hole traps exist, they may be kept there permanently
- The positive oxide charge have an influence in the electric field in the Si bulk close to the surface, inducing a compensating electron accumulation layer

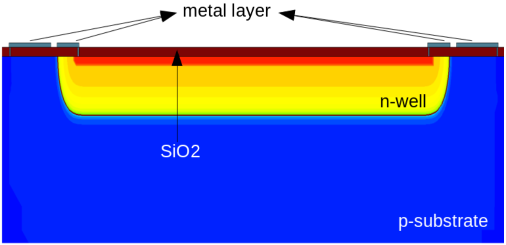




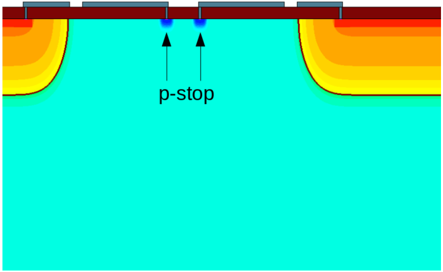
*Charge density in Si-SiO2 interface from 10^{11} cm^{-2} to 10^{12} cm^{-2} between 0 and 10^{8} Rad

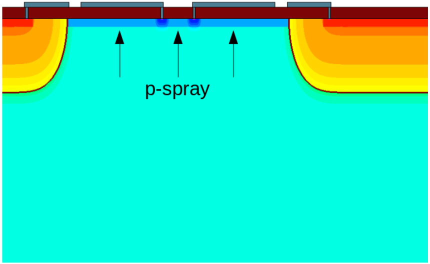
Pixel Isolation

- Simple Pixel Structure



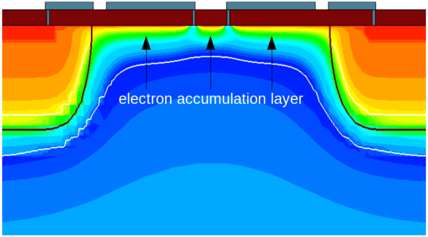
- Pixel Isolation



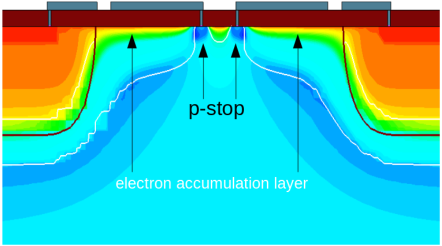


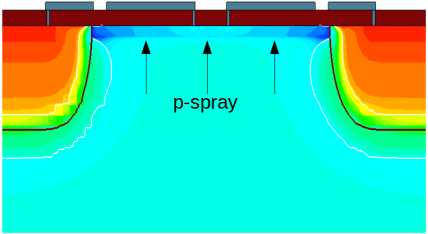
Pixel Isolation

- Simple Pixel Structure



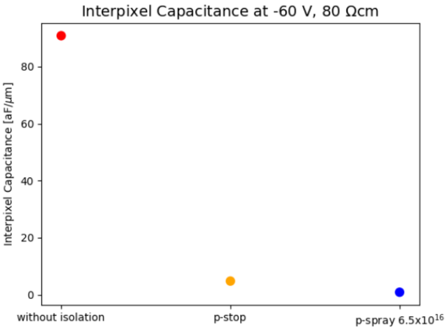
- Pixel Isolation

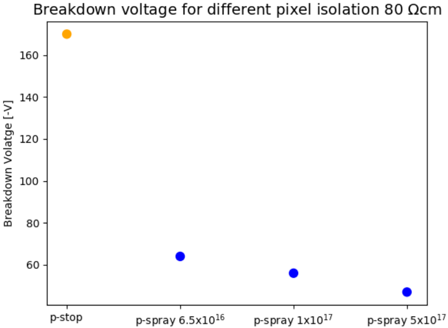




eDensity @ 20 Ωcm @ 10^{11} density of charge in Si-SiO2 interface

Pixel Isolation

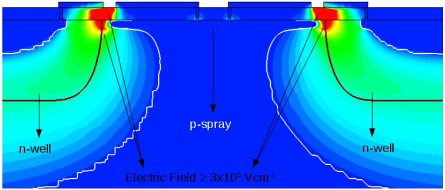




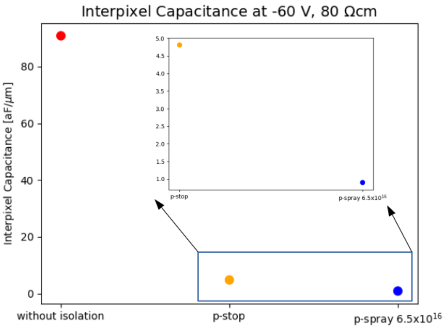
1. InterPixel Capacitance
   - lower → p-spray

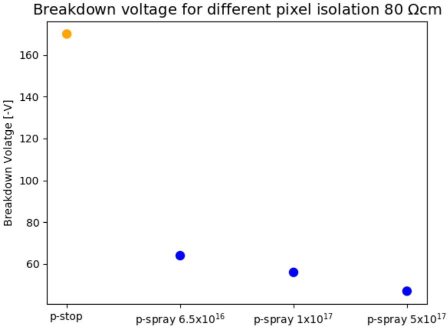
   Example: Mupix8
   - without isolation: 21.56 fF
   - p-stop: 1.39 fF
   - p-spray 6.5x10^{16}: 0.61 fF

2. Breakdown Voltage
   - lower → p-spray



Pixel Isolation





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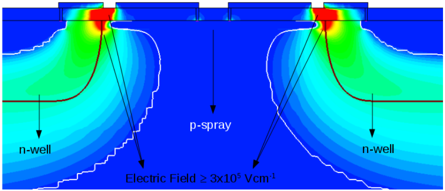
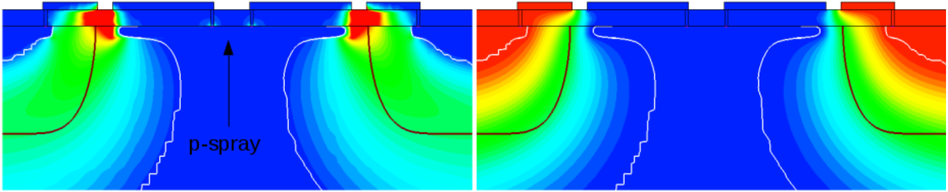


Pixel Isolation

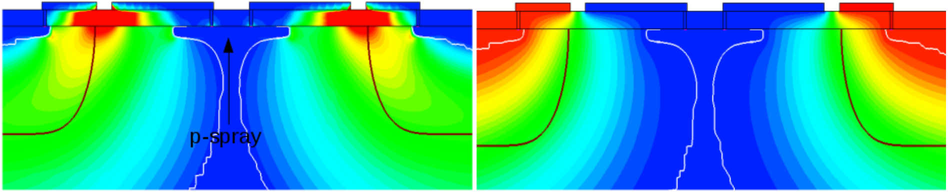
Electric Field

Electrostatic Potential

- 1 μm mask

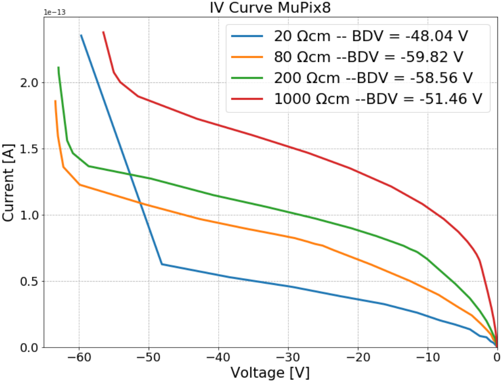


- 4 μm mask



@ 20 Ωcm @ 10^{11} Si-SiO2 interface charge

Experimental Breakdown Voltage

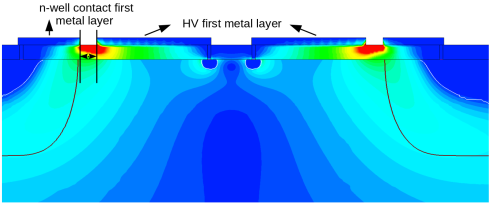


$[\Omega cm]$	Expe.[V]	TCAD [V]
20	-48.0	-48.0
80	-63.0	-59.8
200	-60.2	-58.5
1000	-46.4	-51.4

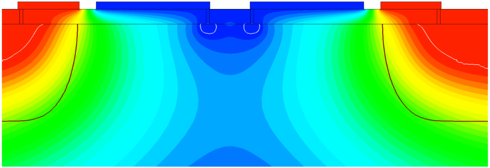
The use of p-spray in the MuPix8 structure reproduce the experimental results

First Metal Layer

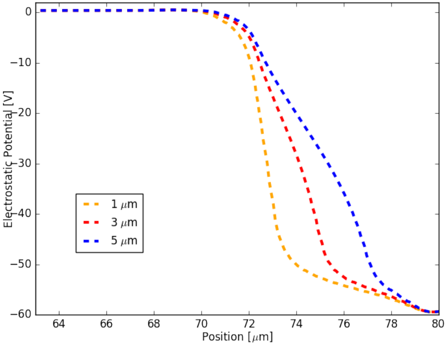
- Electric Field



- Electrostatic Potential



@ -60 V @ 80 Ωcm @ 10^{11} Si-SiO2 interface

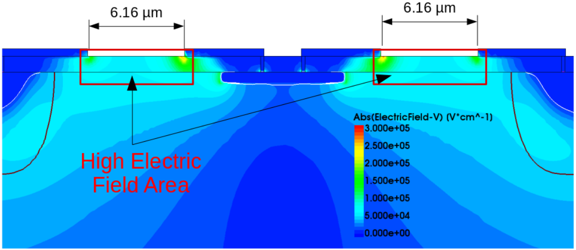


- MuPix8 → 1 μm
- AtlasPix3 → 6.16 μm

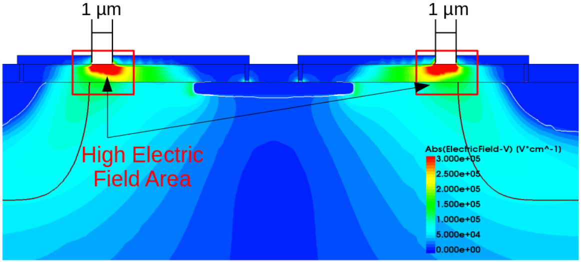
Simulation result shows that a distance of 3.5 create a Break Down Voltage above -120 V

First Metal Layer

- AtlasPix3 (200 Ωcm at -60 V)

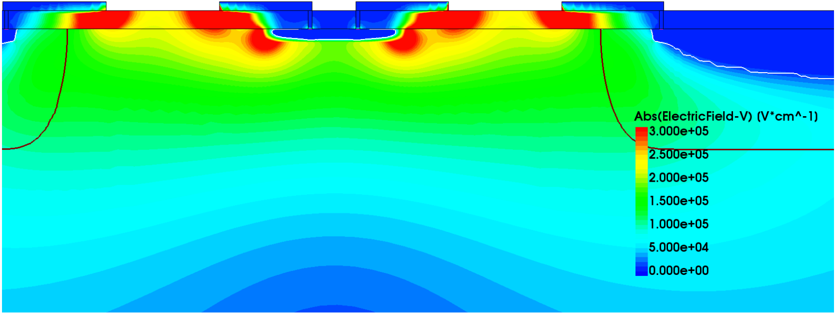


- MuPix8 (200 Ωcm at -60 V)



AtlasPix3 Breakdown Voltage

- AtlasPix3 (200 Ωcm)



Breakdown Voltage:

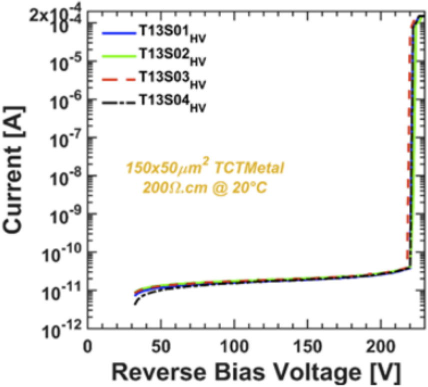
- 2D Simulation:

without mask: -59 V
with mask: -250 V

- Experimental: -65.8 V (Rodolph reported measuring)

AtlasPix3 Breakdown Voltage

- Result from Geneva (Sultan)



Break Down Voltage:
-222 V @ 20°C

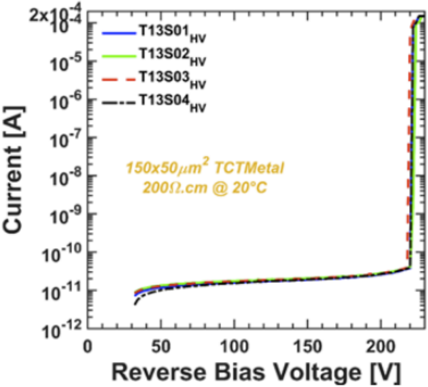
☐ TCT structures holding 3x3 pixels with similar pixel flavor of ATLASPix3 matrix

☐ All connections from electronics have been removed

☐ Shallow n-well (holds CMOS) sits upon the deep n-well is connected to GNDA pad

AtlasPix3 Breakdown Voltage

- Result from Geneva (Sultan)



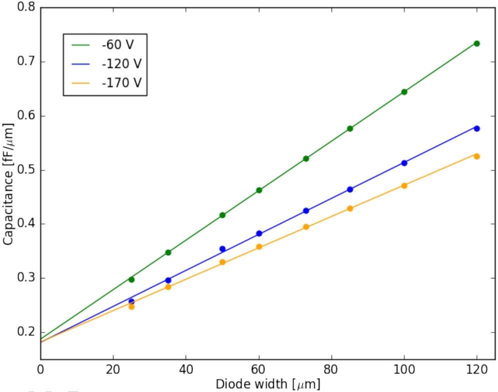
Break Down Voltage:
-222 V @ 20°C

Structure more similar to simulation

☐ Simulations including NMOS and PMOS transistors

Pixel Dimensions

Diode Capacitance (C_0) in 80 Ωcm

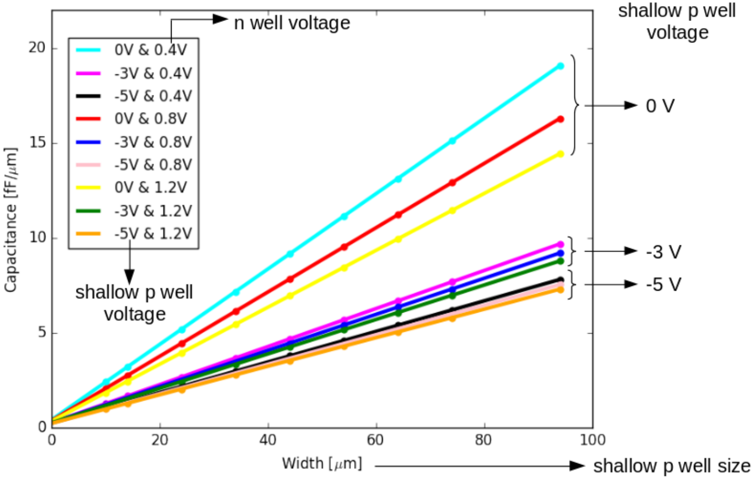


- Design like MuPix8
- Linear function of the diode width
- Capacitance increases with diode size and decreases with HV

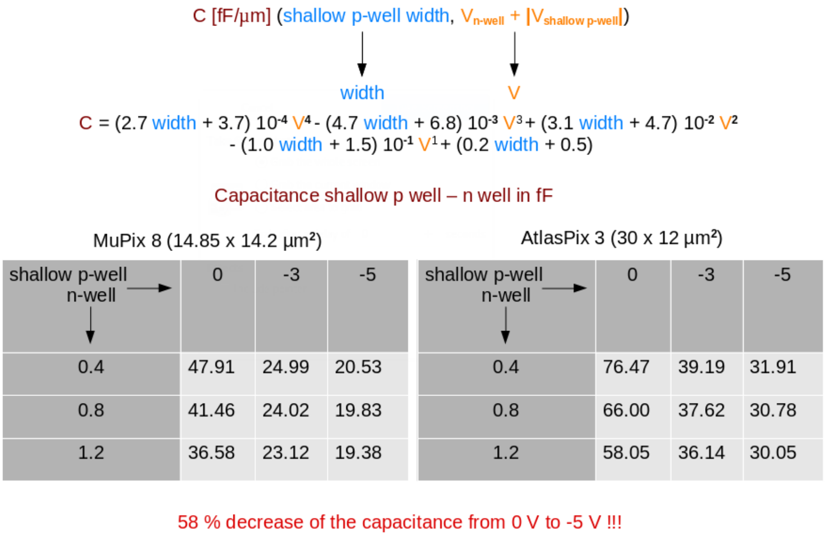
$$C_0[\frac{fF}{\mu m}] = (-1.538 * |V| + 539) * 10^{-5} * diode\ width + 0.18$$

Shallow p-well

Shallow p-well capacitance (C_1)



Shallow p-well



C [fF/µm] (shallow p-well width, $V_{\text{n-well}} + |V_{\text{shallow p-well}}|$)

width V

$$C = (2.7\,\text{width} + 3.7)\,10^{-4}\,V^{4} - (4.7\,\text{width} + 6.8)\,10^{-3}\,V^{3} + (3.1\,\text{width} + 4.7)\,10^{-2}\,V^{2} - (1.0\,\text{width} + 1.5)\,10^{-1}\,V^{1} + (0.2\,\text{width} + 0.5)$$

Capacitance shallow p well – n well in fF

MuPix 8 (14.85 x 14.2 µm²)

shallow p-well → n-well ↓	0	-3	-5
0.4	47.91	24.99	20.53
0.8	41.46	24.02	19.83
1.2	36.58	23.12	19.38

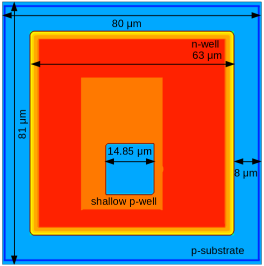
AtlasPix 3 (30 x 12 µm²)

shallow p-well → n-well ↓	0	-3	-5
0.4	76.47	39.19	31.91
0.8	66.00	37.62	30.78
1.2	58.05	36.14	30.05

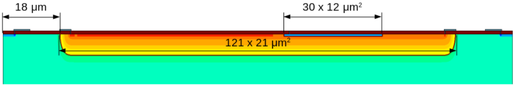
58 % decrease of the capacitance from 0 V to -5 V !!!

Prototypes

- MuPix8



- AtlasPix3



- Total pixel capacitance (@ -60 V n-well = 1.2 V shallow p = 0 V)

☐ 80 Ωcm

$$C_t = 29.07fF + 36.58fF$$
$$C_t = 65.65fF$$

$$C_t = 15.13fF + 58.05fF$$
$$C_t = 73.18fF$$

☐ 200 Ωcm

$$C_t = 20.34fF + 36.58fF$$
$$C_t = 56.93fF$$

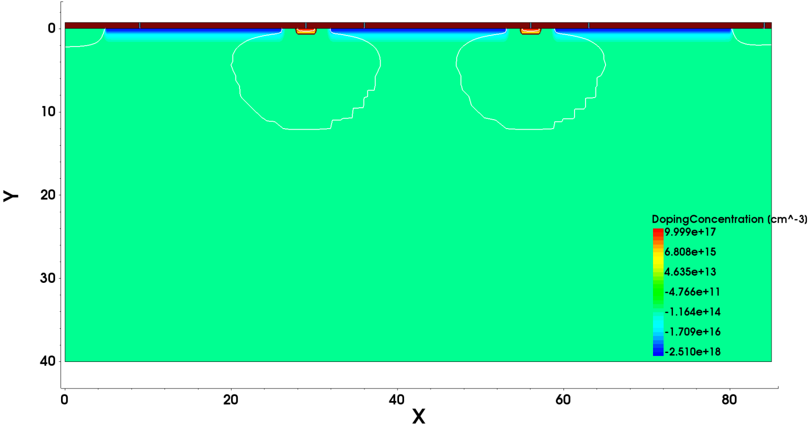
$$C_t = 9.62fF + 58.05fF$$
$$C_t = 67.66fF$$

Conclusions and Outlook

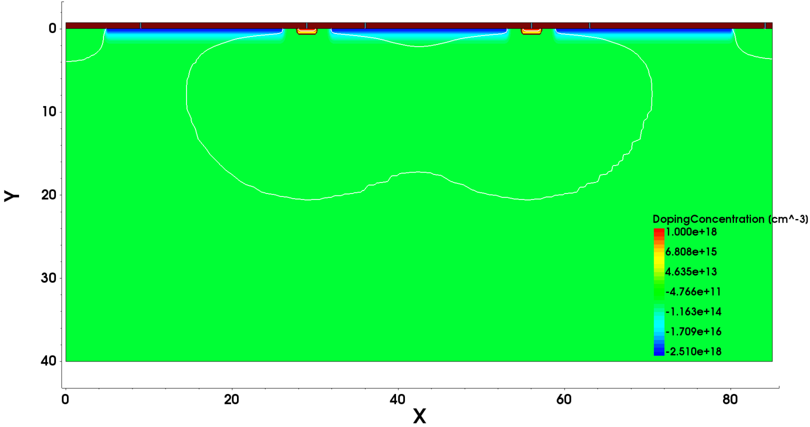
- TCAD simulation is a powerful tool for designing and optimizing semiconductor detectors.
- Ongoing studies:
  - Pixel structure in 3D
  - Electric Field for AllPix2
  - Small fill factor structures

Backup

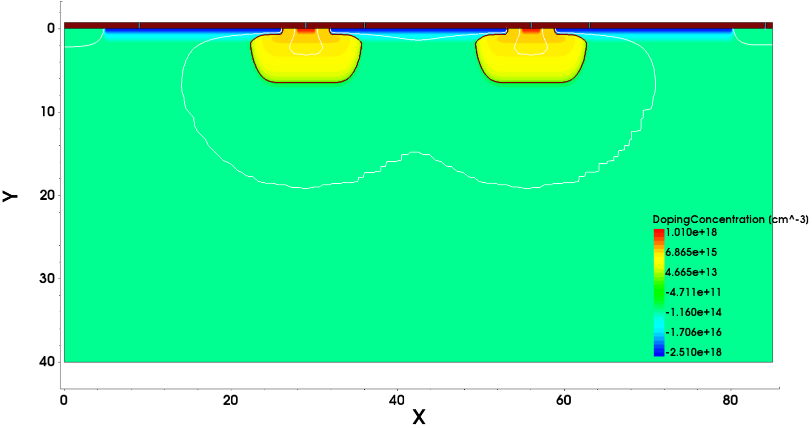
Shallow p-well



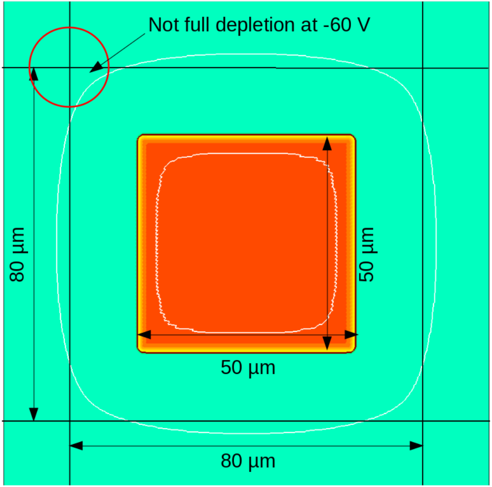
Shallow p-well

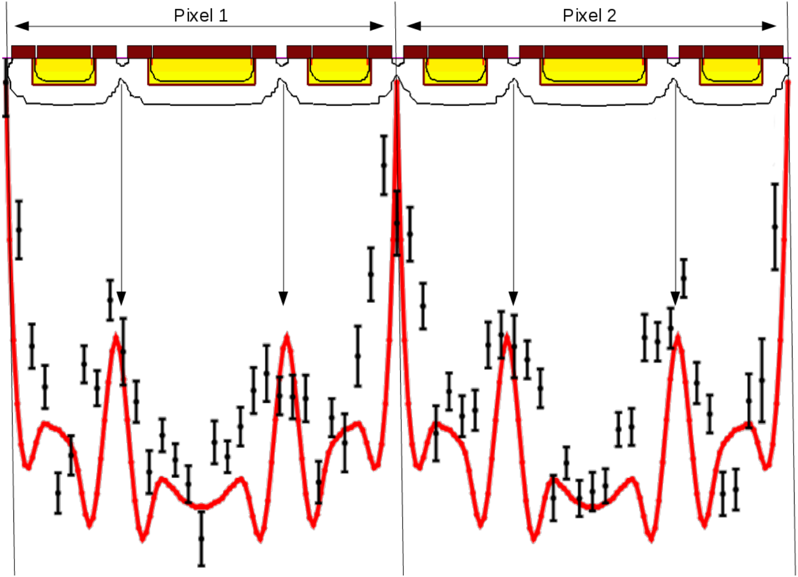


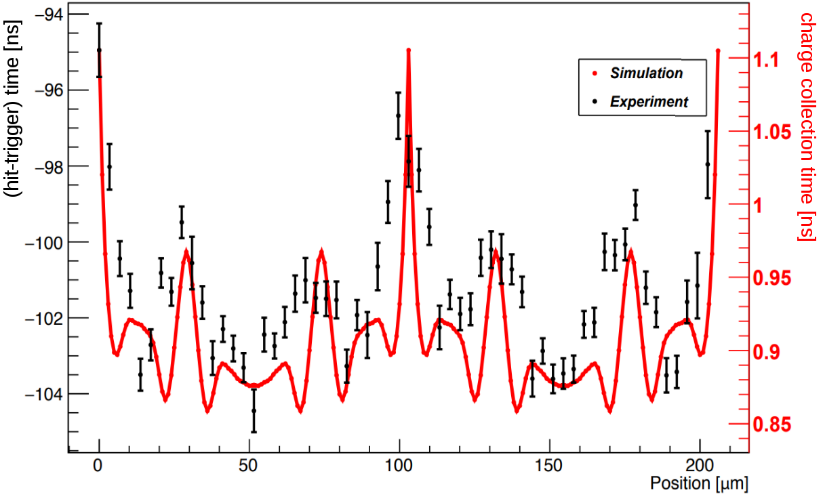
Shallow p-well



Shallow p-well




Pixel 1
Pixel 2


(hit-trigger) time [ns]
−94
−96
−98
−100
−102
−104
charge collection time [ns]
1.1
1.05
1
0.95
0.9
0.85
Simulation
Experiment
0
50
100
150
200
Position [μm]