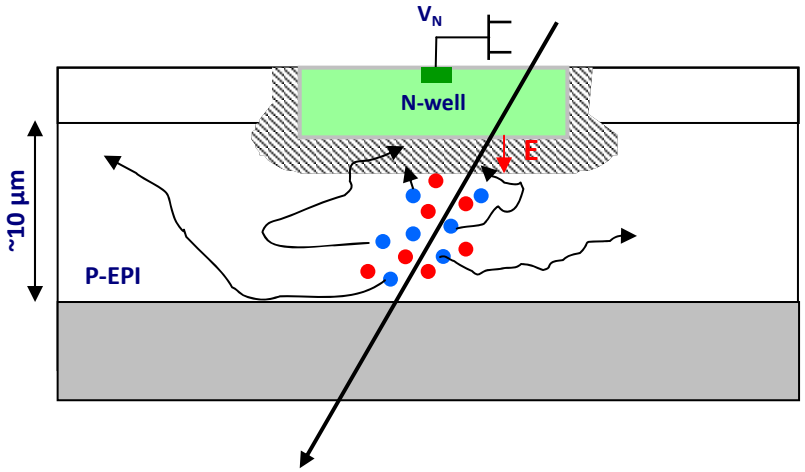
Issues of FEE Designs Integrated in CMOS Pixel Sensors

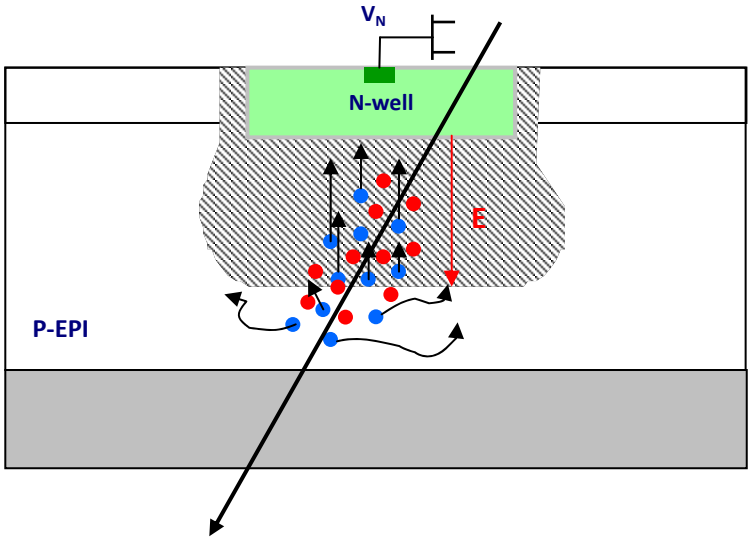
Christine Hu-Guo (on behalf of the PICSEL team of IPHC-Strasbourg)

Outline

- *Introduction to CMOS Pixel Sensors (CPS)*
  - *Twin, (triple), Quadruple well (deep P-well) processes*
- *Design criteria: S/N, power, …*
- *A typical readout chain*
  - *Synchronous readout architecture: Rolling shutter readout*
    - *In-pixel pre-amplifier, filter*
    - *Column-level and pixel-level discriminator*
    - *Zero suppression logic & data transmission*
  - *Asynchronous readout architecture: ALPIDE*
- *Summary & Conclusion*

CMOS Pixel Sensors





Standard Epitaxial Layer

- *Standard CMOS OPTO Process: EPI ~10 Ω*cm*
- *Charge collection: thermal diffusion*
- *Collection time: O(100 ns)*

High resistivity Epitaxial Layer

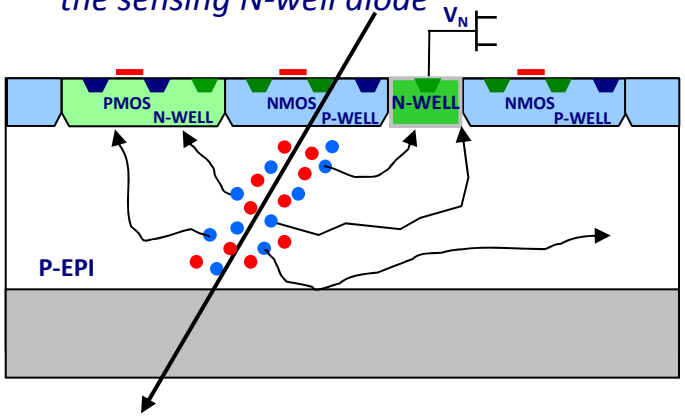
- *High resistivity >1 kΩ*cm & thicker (~40 µm) EPI layer*
- *Charge collection: drift/thermal diffusion*
- *Collection time faster, less recombination ➔ radiation tolerant*
- *Depletion depth depends on bias*

- *Low signal value: ~ 80 e^-h^+ pairs/µm ➔ signal O(1 Ke^-) collected by a cluster of ~3-5 pixels*
  - *Need very low noise in-pixel front end circuitry*
- *High granularity ➔ small pixel pitch ➔ large number of pixels*
  - *Need low power consumption per pixel*
  - *Require data compression*
  - *Call for high speed data transmission*

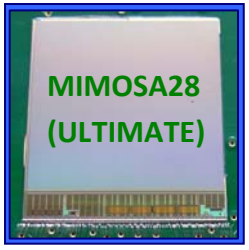
➡ *Analogue signals have to be converted to digital signal (ADC)*

CMOS Process Evolution

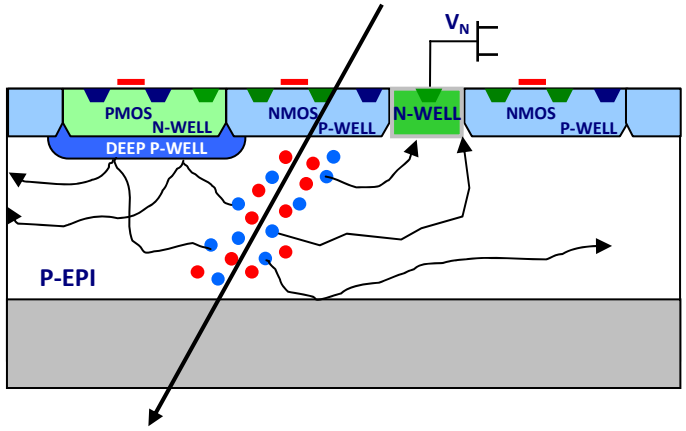
- *Twin well process: 0.6-0.35 µm*
  - *Use of PMOS in pixel array is not allowed because any additional N-well used to host PMOS would compete for charge collection with the sensing N-well diode*



  - *Limits choice of readout architecture strategy*
  - *Already demonstrate excellent performances*
    - *STAR PXL detector: MIMOSA28 are designed in this AMS-0.35 µm process*
      - ✓ $\varepsilon_{eff} > 99.5\%$, $\sigma < 4$ µm
    - *1st CPS based VX detector at a collider experiment*



- *Quadruple well process (deep P-well): 0.18 µm*
  - *N-well used to host PMOS transistors is shielded by deep P-well*
  - *Both types of transistors can be used*



  - *Widens choice of readout architecture strategies*
    - *Ex. ALICE ITS upgrade: 2 sensors R&D in // using TOWER CIS 0.18 µm process (quadruple well)*
      - *Synchronous Readout R&D:*
        - ✓ *proven architecture = safety*
      - *Asynchronous Readout R&D: challenging*

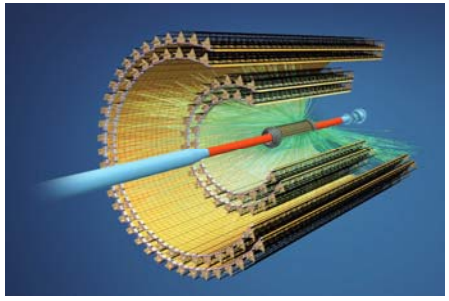


Figure of Merit S/N vs Design Optimisation (1)

- **Signal :** $S(\mathrm{v}) = \frac{Q}{C}$ $\quad C = C_{diode} + C_{Tin} + C_{connection}$
  - *Small collection electrode, small input transistor, short inter connection for low C*
  - *BUT too small diode does not favour the charge collection*

- **Noise:**
  - *Input Transistor* *in **W**eak inversion:* $dv_{eq}^{\ 2} = \left(\frac{K_F}{WLC_{cx}^2 f^{\alpha}} + \frac{4K_B T\, n}{g_m}\right) df$ $\quad g_m \sim I$

    Flicker noise (1/f) *Thermal noise*

    ***S**trong inversion* $dv_{eq}^{\ 2} = \left(\frac{K_F}{WLC_{cx}^2 f^{\alpha}} + \frac{2K_B T\, \gamma}{g_m}\right) df$ $\quad g_m \sim \sqrt{I}$

    - *To minimise*

      - Flicker noise: large input transistor → large C_{Tin}

      - Thermal noise Large g_m, → high power

      - Both of two noise: Use a filter (band-pass):

      $$N \sim \frac{1}{\sqrt{g_m}}$$

    → *1. trade-off between Noise & Power*

    2. need a filter

K_F	*Technology dependent constant*
W, L	*MOS transistor width and length*
C_{ox}	*Gate oxide capacitance per unit area*
g_m	*Transistor transconductance*
K_B	*Boltzmann constant*
T	*Absolute temperature*
n	*Weak inversion slope*
γ	*Often around ½ - 2/3 in strong inversion*

Figure of Merit S/N vs Design Optimisation (2)

- *Collection diode: shot noise due to leakage current, especially after irradiation*
  - *I_{leak} is proportional to diode dimensions* $di_N^2 = 2qI_{leak}df$
  - *Leakage noise is proportional to integration time*
    - ✓ *Negligible for very short integration time O(1 µs)*

- *Reset noise:* $v_N^2 = \frac{kT}{C}$

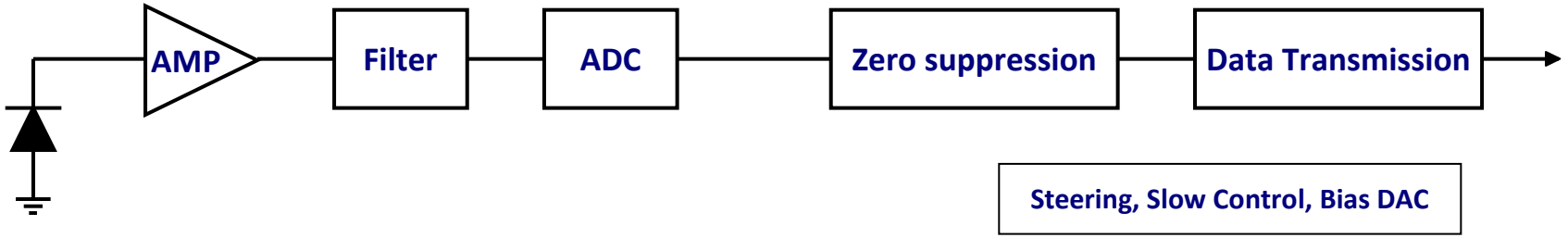
- *Contributions from:*
  - *Other transistors in pre-amplifier stage is not negligible*
  - *Next stages*

$$N_{total} = N_1 + \frac{N_2}{G_1} + \frac{N_3}{G_1 G_2} + \ldots$$

➔ *High gain G1 in the first stage tends to mitigate the total noise*

- *RTS (Random Telegraph Signal) noise*
  - *RTS noise increases as the feature size of the devices is scaled down*
    - ✓ *Impact on dimensions (W and L) of the in-pixel transistors*
    - ✓ *PMOS has better performance than NMOS*
    - ✓ *Negligible if integration time is small enough*

A Typical Readout Chain



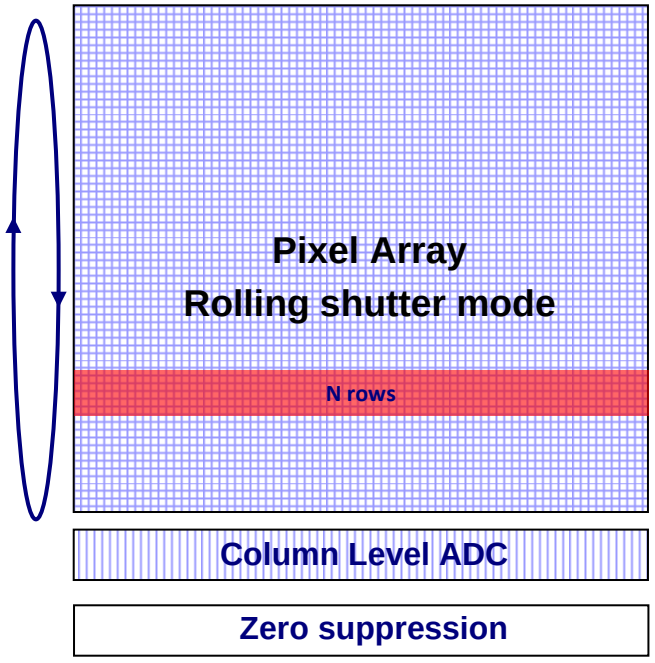
- *AMP:* *In-pixel low noise pre-amplifier*
- *Filter:* *In-pixel filter*
- *ADC:* *Analogue to digital conversion (1 bit: discriminator)*
  - *it may be implemented in-pixel level or at column level underneath the pixel array*
- *Zero suppression:* *Only hit pixels information is sent*
  - *Its location is usually at chip edge level underneath the pixel array but it may be implemented in-column level*
- *Data transmission:* *~Gbit/s link at chip edge level*

- *Readout: synchronous (Rolling Shutter) or asynchronous*
- *Using a twin-well process, the Rolling Shutter readout architecture is the best trade-off between performance, design complexity, pixel dimension, power, …*
  - *MIMOSA26, MIMOSA28*

Synchronous Readout Architecture: Rolling Shutter Mode

- *Design addresses 3 issues:*
  - *Increasing S/N at pixel-level*
  - *A to D Conversion: at column-level (twin well, 0.35 µm process)*
    at pixel-level (quadruple well, 0.18 µm process)
  - *Zero suppression (SUZE) at chip edge level*
- *Power vs speed:*
  - *Power: only the selected rows (N=1, 2, …) to be read out are powered ON*
  - *Speed: N rows pixels are read out in //*
    - *Integration time = frame readout time*

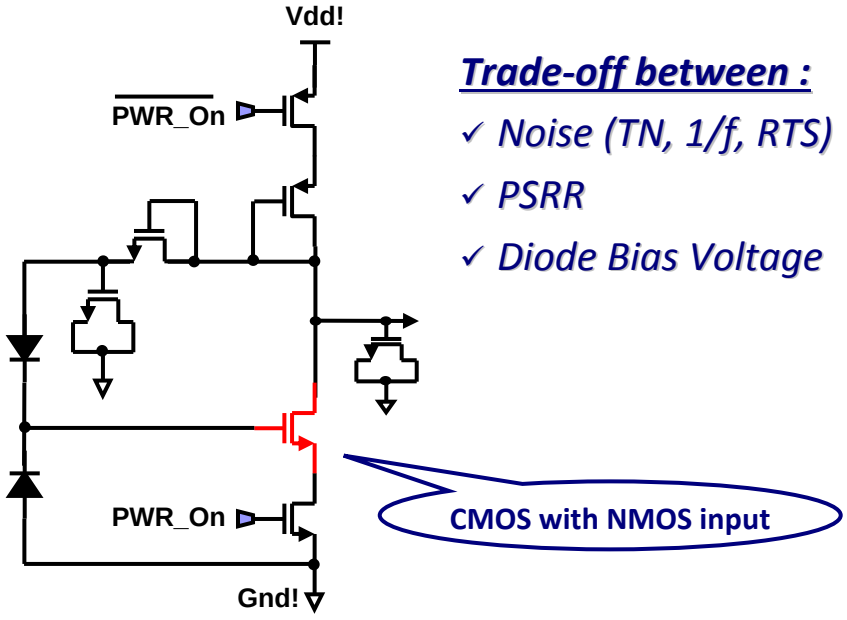
$$t_{\text{int}} = \frac{\left(Row\ readout\ time\right)\times\left(No.\ of\ Rows\right)}{N}$$



- *Mature & Validated architecture*
  - *In 0.35 µm, twin well process :*
    - *MIMOSA26 equipping EUDET telescope*
    - *MIMOSA28 equipping STAR PXL detector*
  - *In 0.18 µm, quadruple well process:*
    - *FSBB-M (for MISTRAL)*
    - *FSBB-A (for ASTRAL)*

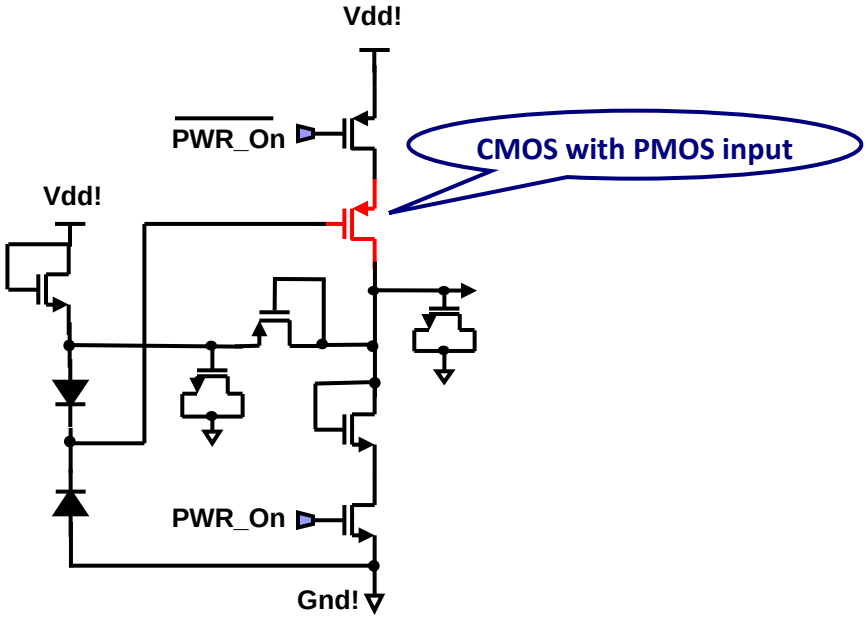
Synchronous Readout Architecture: AMP

- *Pre-amplifier:*
  - *It is only active when the row is selected to be read*
  - *High readout speed (~100 ns/row) ➔ short time from start to steady*
    - *Requires current to drive ➔ increase power consumption*
    - *Large bandwidth ➔ noise*
  - *Short start-up time leads to a moderate gain*
    - *Typical gain value: < 5*
  - *Using a Twin-well process: only NMOS transistors can be used while in a process with deep P-well, both types of transistors (CMOS) can be used*



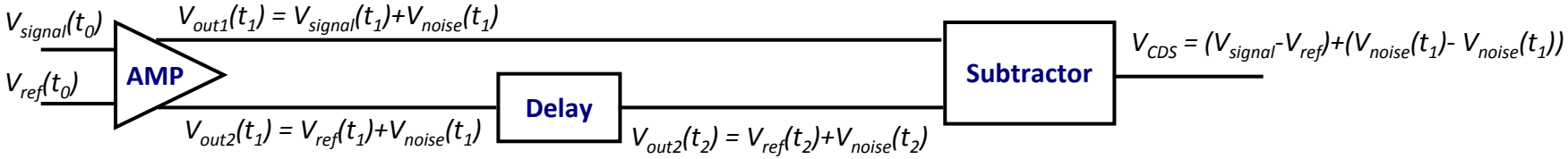
Trade-off between :

- ✓ *Noise (TN, 1/f, RTS)*
- ✓ *PSRR*
- ✓ *Diode Bias Voltage*

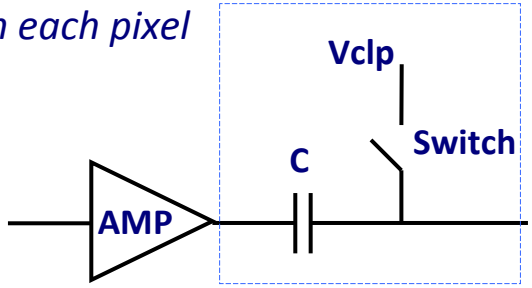


Synchronous Readout Architecture: Filter

- *Filter = cDS (correlated Double Sampling) in the design*
  - *CDS: the output voltage (or current) is sampled twice: once with signal and once with a reference, then the value from signal is subtracted from the value from the reference*



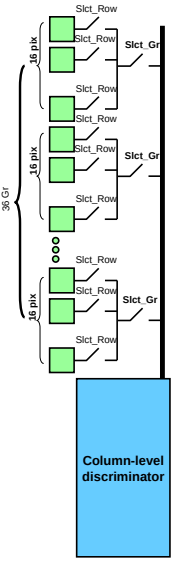
  - *Signal is not affected by CDS operation*
  - *For noise, CDS acts as a high pass filter*
    - *Low-freq. cut-off is promotional to the sample frequency (~2 * f_{sample})*
    - *It can provide suppression of low frequency noise*
      - ✓ *ex. reset noise, 1/ f noise, fixed pattern noise*
    - *White noise is sampled twice, their power is quadratically added*
  - *cDS is achieved by a clamping technique which is implemented in each pixel*
    - *Simple design & layout*
      - ✓ *1 capacitor + 1 switch*
    - *Need 2 phases to perform cDS*
      - ✓ *Phase 1: info. of the frame N-1 (V_{N-1}) stored in C*
      - ✓ *Phase 2: signal is subtracted from charge previously stored (V_N - V_{N-1})*



Synchronous Readout Architecture: ADC

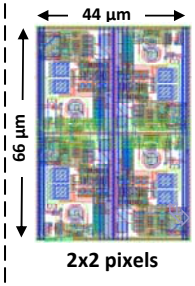
- *Choice of number of ADC bits depends on the required spatial resolution and the pixel pitch*
  - *Some applications ➔ 1 bit ADC ➔ discriminator*
  - *R&D on 3-bit ADC both in pixel and column level*
    - *3-4 bits suffice in achieving ~ analogue resolution (see talk by A. Besson)*

- *Column-level discriminator*



  - *Developed in a twin-well process in which only NMOS can be used in pixel array*
    - *At periphery: CMOS circuitry admit*
  - *Less constraints in pixel layout*
  - *Need power to drive analogue signal to the bottom of the pixel array (~cm long)*
  - *Readout time may be relatively long due to analogue signal transfer*
    - *A-D conversion time ~200 ns/row*
  - *For N rows read out at once, one has to implement N discriminator per column*

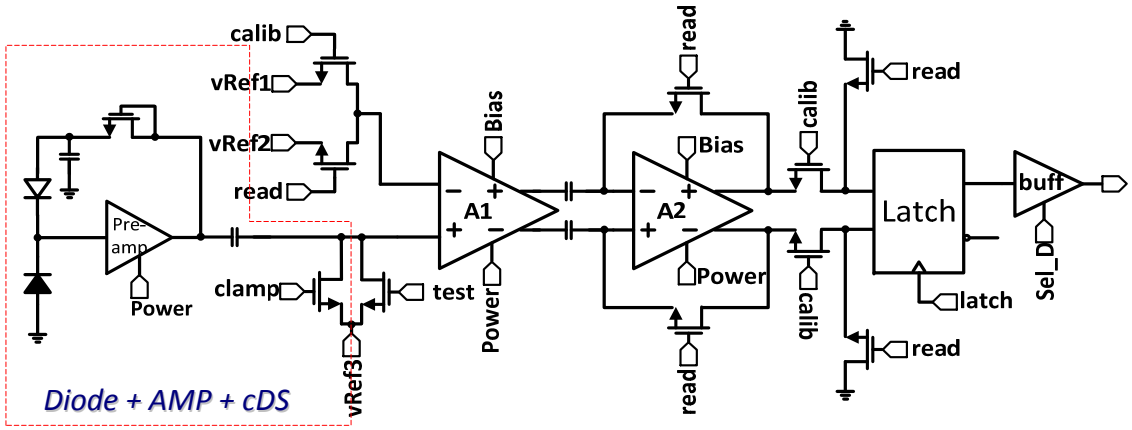
- *Pixel-level discriminator*

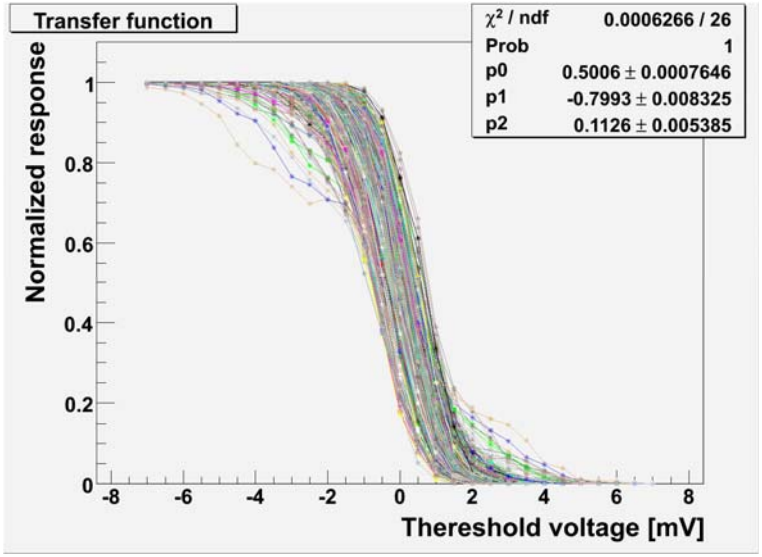


  - *Thanks to the deep P-well, smaller feature size process, more complex designs may be implemented*
  - *Pixel layout very compact*
  - *Analogue buffer driving the long distance column line is no longer needed*
    - *Static current consumption reduced from ~120 µA (in column-level discrimination) to ~15 µA per pixel*
  - *A-D conversion time can be halved down to 100 ns due to small local parasitics*
  - *Space dedicated for column-level discriminators is removed*

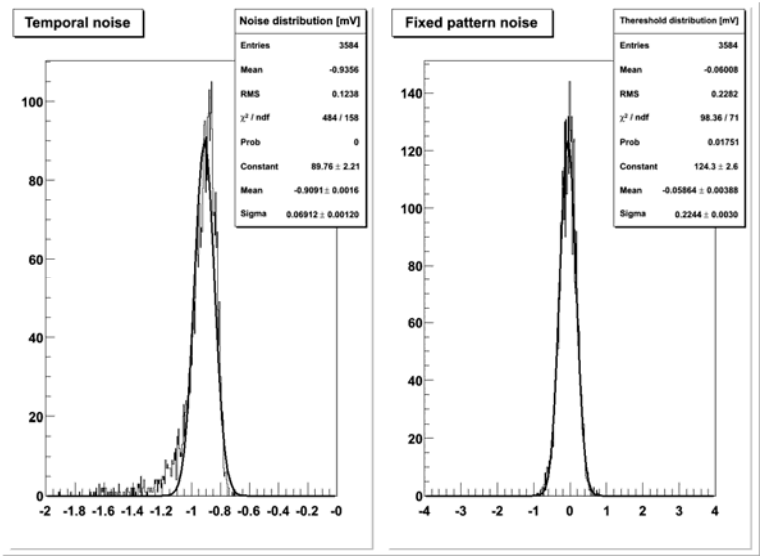
- *Because the gain in the pre-amplifier stage is not high enough, both column and pixel level discriminators need to use an offset compensation technique*

Synchronous Readout Architecture: In-Pixel Discriminator



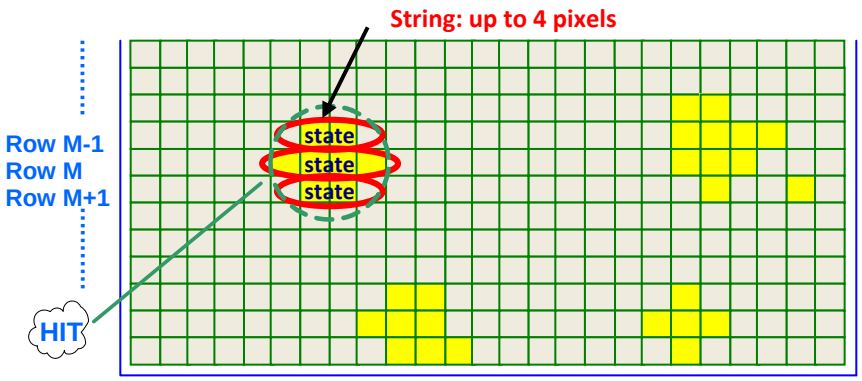


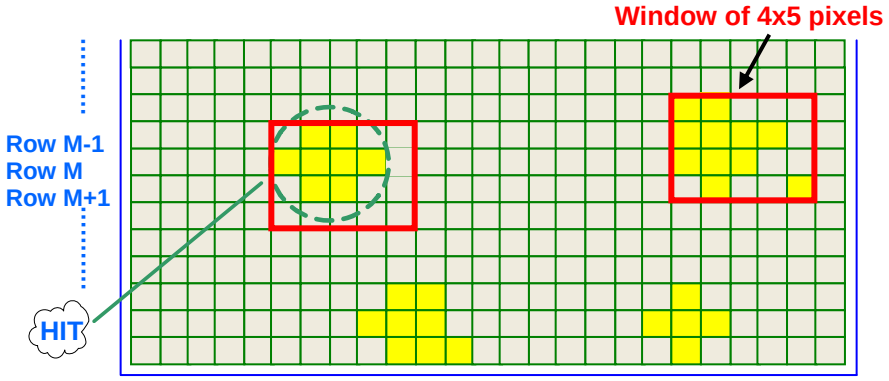
- *To provide adequate performance within small pixel*
  - *Structure selection: speed & power & offset mitigation vs area*
    - *Differential structure: preferable in mixed signal design*
    - *Two auto-zero amplifying stages + dynamic latch*
      - ✓ *OOS (Out Offset Storage) for the first stage and IOS (Input Offset Storage) for the second*
    - *Gain and power optimized amplifier*
  - *Very careful layout design to mitigate cross coupling effects*
  - *Conversion time: 100 ns; current: ~14 µA/discriminator*
- *Test results of in-pixel discriminator:*
  - *Discriminators alone: TN ~ 0.29 mV, FPN ~ 0.19 mV*
  - *Discriminators + FEE: TN ~ 0.94 mV, FPN ~ 0.23 mV*



Synchronous Readout Architecture: Zero Suppression Logic (SUZE)

- *SUZE finds groups of hit pixels and sends their address and the corresponding encoded pattern*

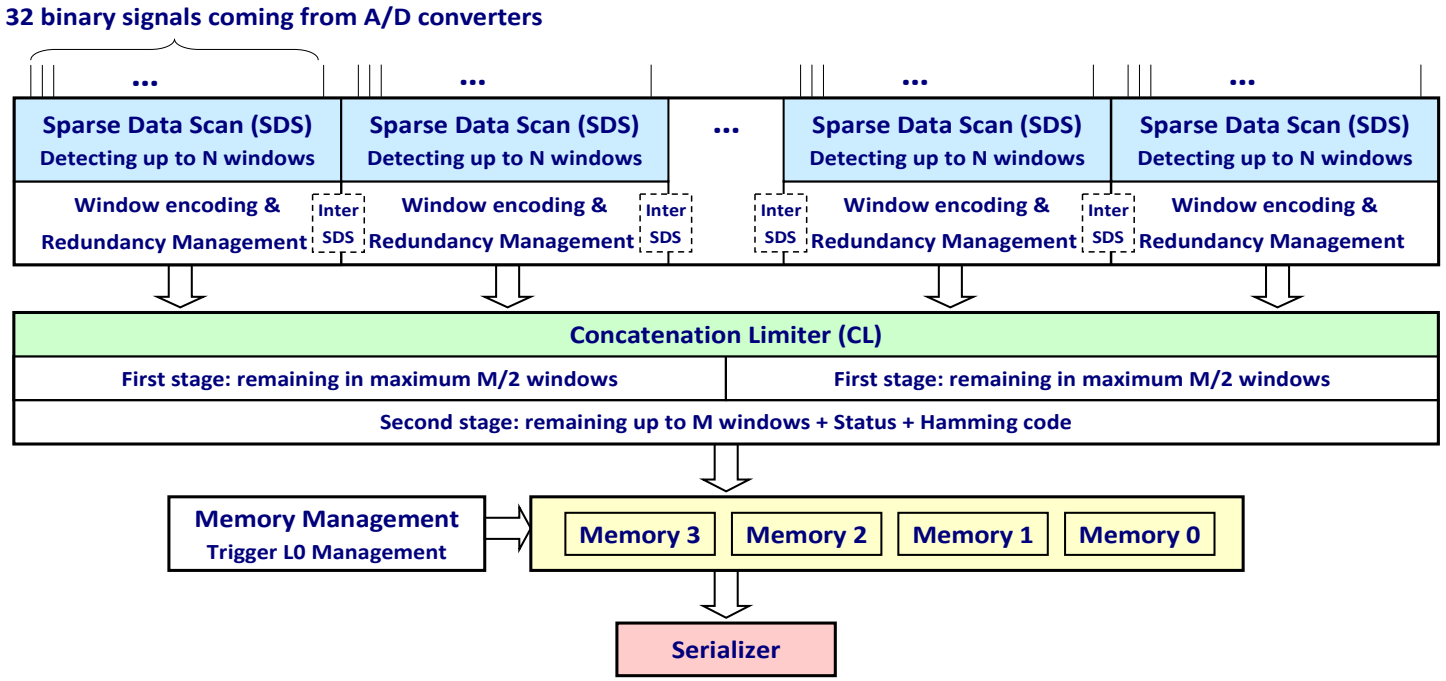




- *1st generation: SUZE-01*
  - *A hit is encoded in 1, 2, 3 even 4 states of 2 bits (up to 4 contiguous hit pixels)*
    - *1 address for 1 state*
      - ✓ *More memory space*
      - ✓ *Redundant info. sent*
  - *Row by row readout: 200 ns/row*
  - *Simple design, compact layout*
  - *Processing capability: 0.5x10⁶ hits /cm²/s*

- *2nd generation: SUZE-02*
  - *A hit cluster is identified in a window of 4x5 pixels (20 bits)*
    - *Need only 1 address*
      - ✓ *Compact data*
  - *2-row by 2-row readout: 100 ns/2-row*
  - *Space to implement the logic*
  - *Power to perform the logic*
  - *Processing capability: 15x10⁶ hits /cm²/s*

SUZE-02



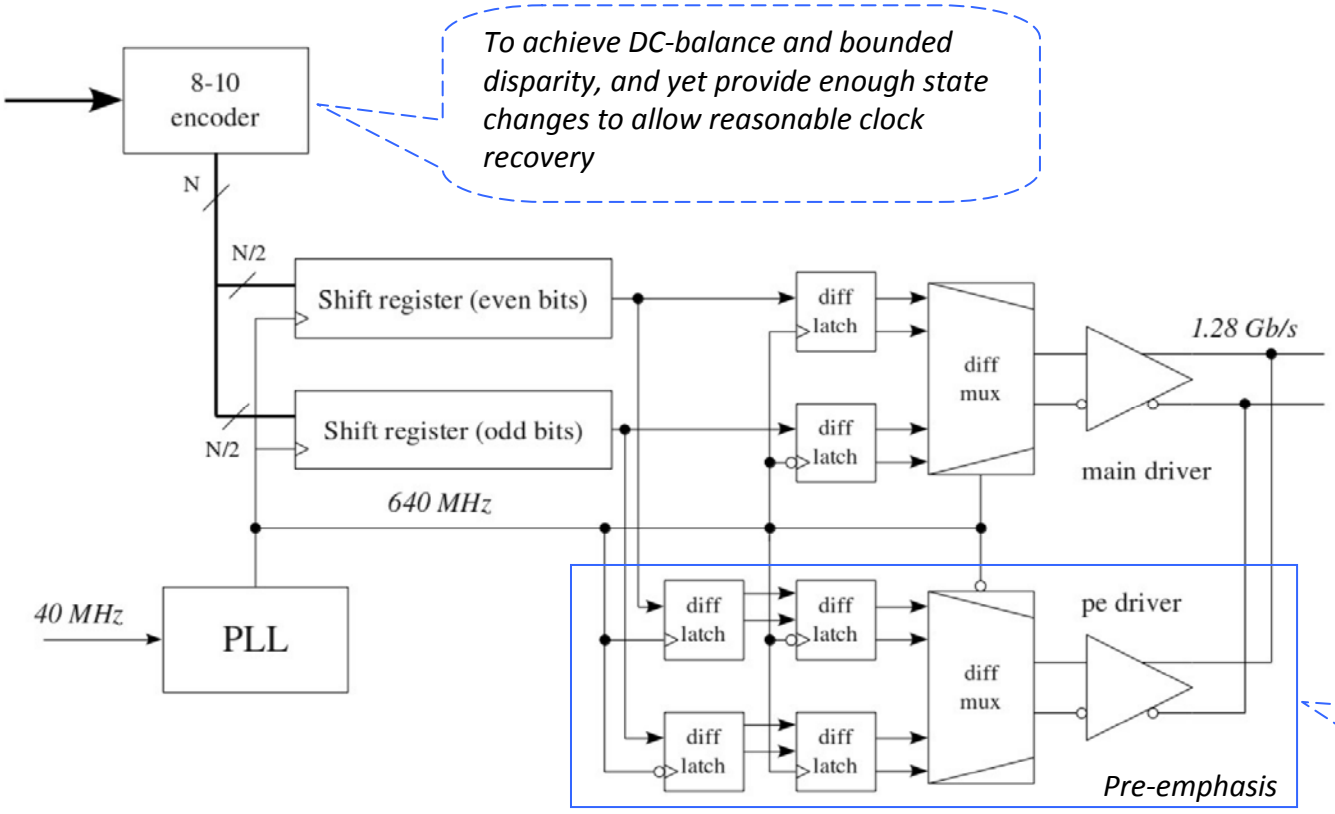
- *SUZE features a pipelined process organised in three stages :*
  - *Sparse Data Scan (SDS): searches windows of 4x5 pixels in 4 consecutive rows*
    - *The search is performed in // in banks of 32 columns and each bank can contain up to N windows*
  - *Concatenation: abuts the windows identified in all banks*
    - *It retains only M windows*

  N, M: according to the hit density defined by the estimated (simulated) amount of events
  - *Storage: results of the second stage will be stored in the memories*

N and M, the memory capacity and the transfer frequency must be customized for each application

Data Transmission

- *Data transmission rate can reach up to several Gbit/s per sensor*
- *Choice of transmission technologies (LVDS, CML, …) depends on system design*
  - *Number of transmission channels per sensor*
  - *Distance to drive*
- *ALICE-ITS Data Transmission Unit (DTU) developed by INFN Turin (G. Mazza)*

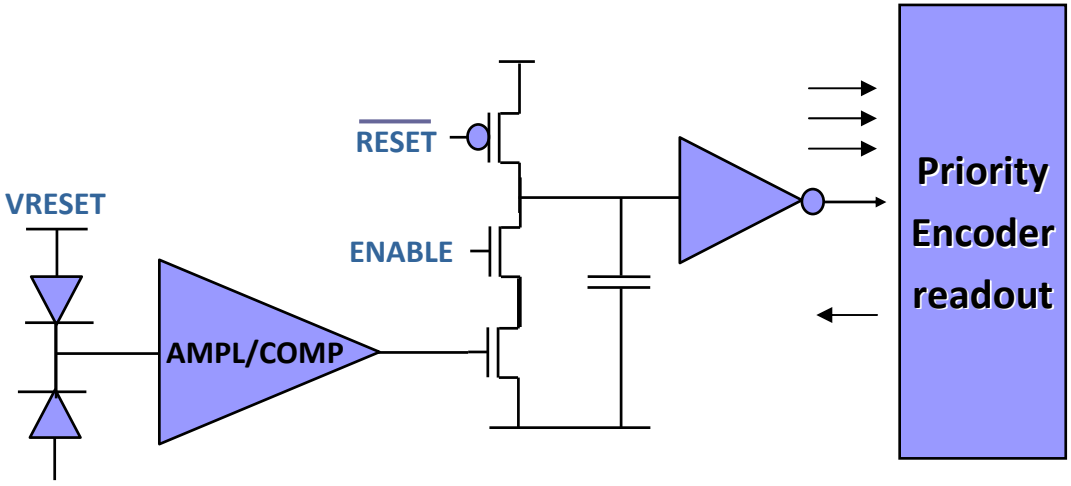


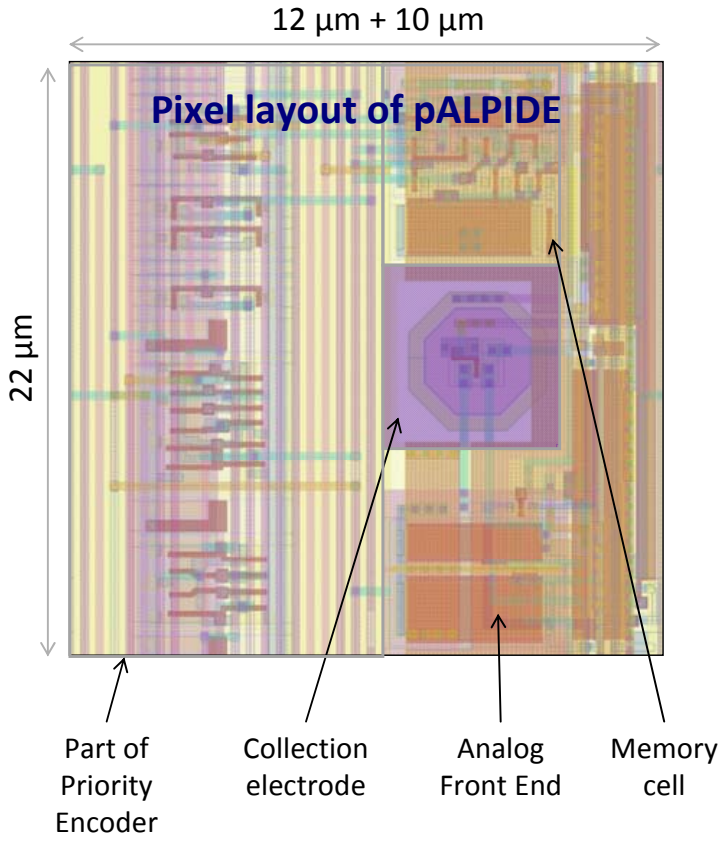
To achieve DC-balance and bounded disparity, and yet provide enough state changes to allow reasonable clock recovery

Pre-emphasis is an output overdrive technique that compensates for cable losses and extends transmission distance

Asynchronous Readout Architecture: ALPIDE (ALice PIxel Detector)

- *Design concept similar to hybrid pixel readout architecture thanks to availability of Tower CIS quadruple well process: both N & P MOS can be used in a pixel*
- *Each pixel features a continuously power active:*
  - *Low power consumption analogue front end (Power < 50 nW/pixel) based on a single stage amplifier with shaping / current comparator*
    - *High gain ~100*
    - *Shaping time few µs*
  - *Dynamic Memory Cell, ~80 fF storage capacitor which is discharged by an NMOS controlled by the Front-End*
- *Data driven readout of the pixel matrix, only zero-suppressed data are transferred to the periphery*

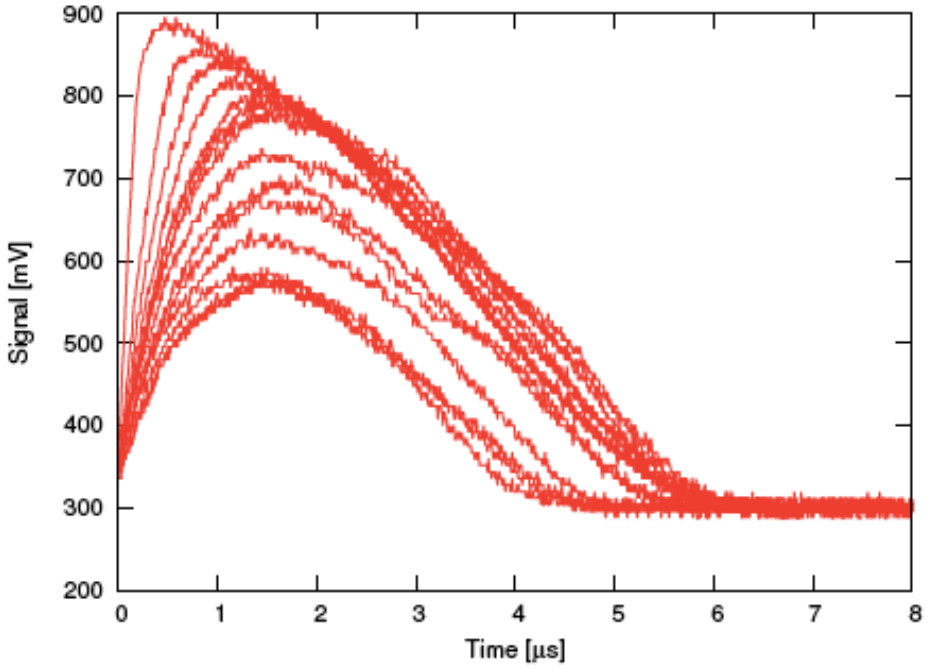




Courtesy of W. Snoeys / TWEPP-2013

pALPIDE: Analogue Response & Noise and Threshold Distributions

Analog output of one pixel under ^{55}Fe



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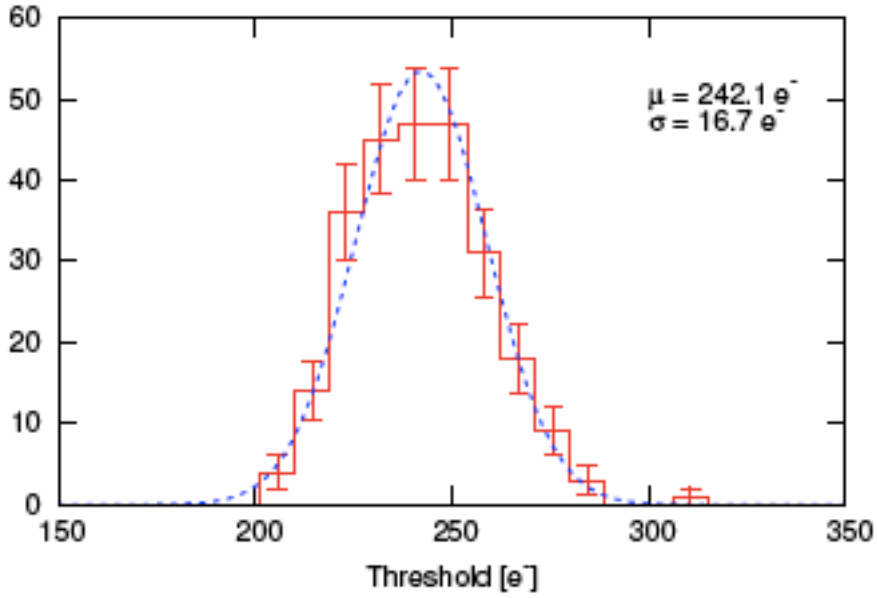
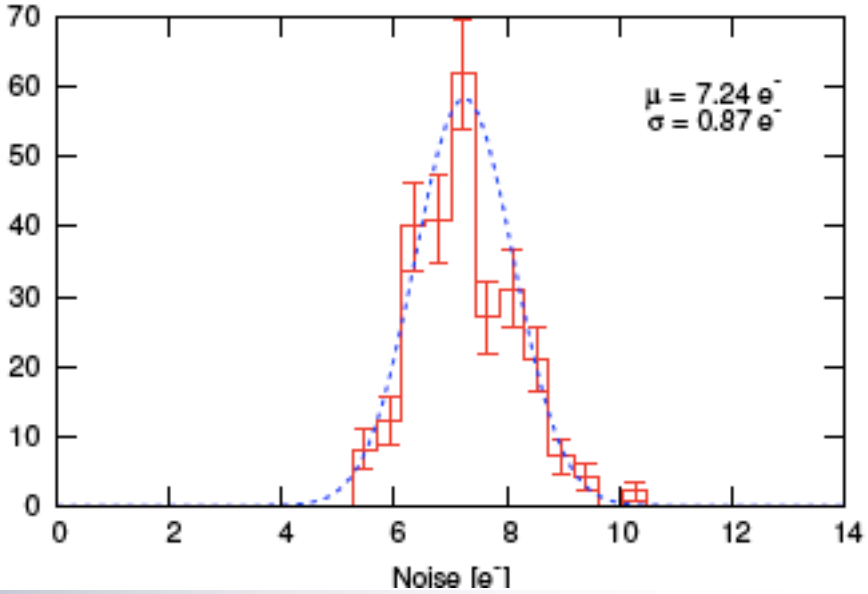
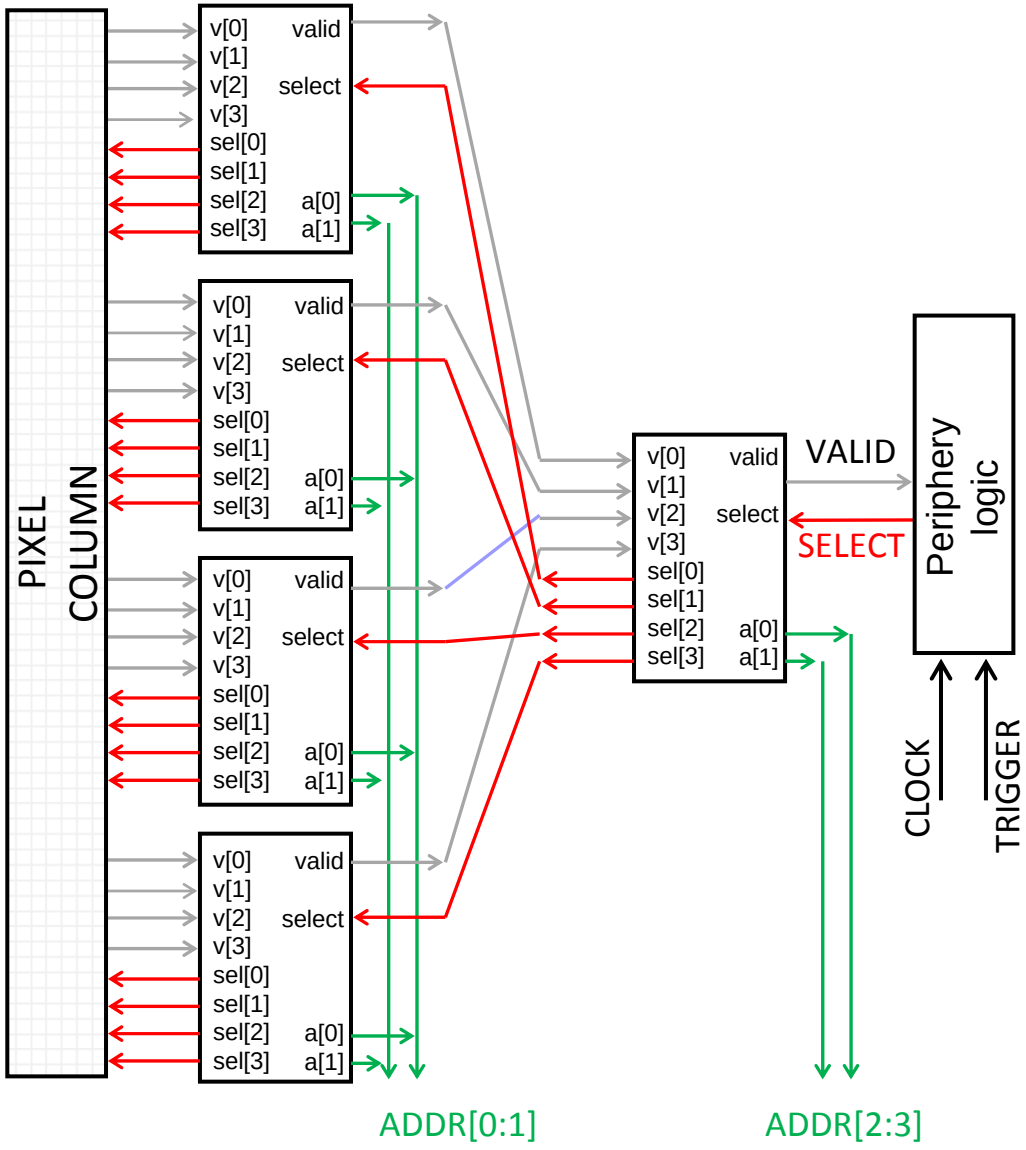




- *Minimum detectable charge <130 e-*
- *At nominal bias (20.5 nA/pixel) and threshold setting:*
  - *Threshold spread 17 e-*
  - *Noise ~ 7 e-*

ALPIDE: Priority Encoder readout

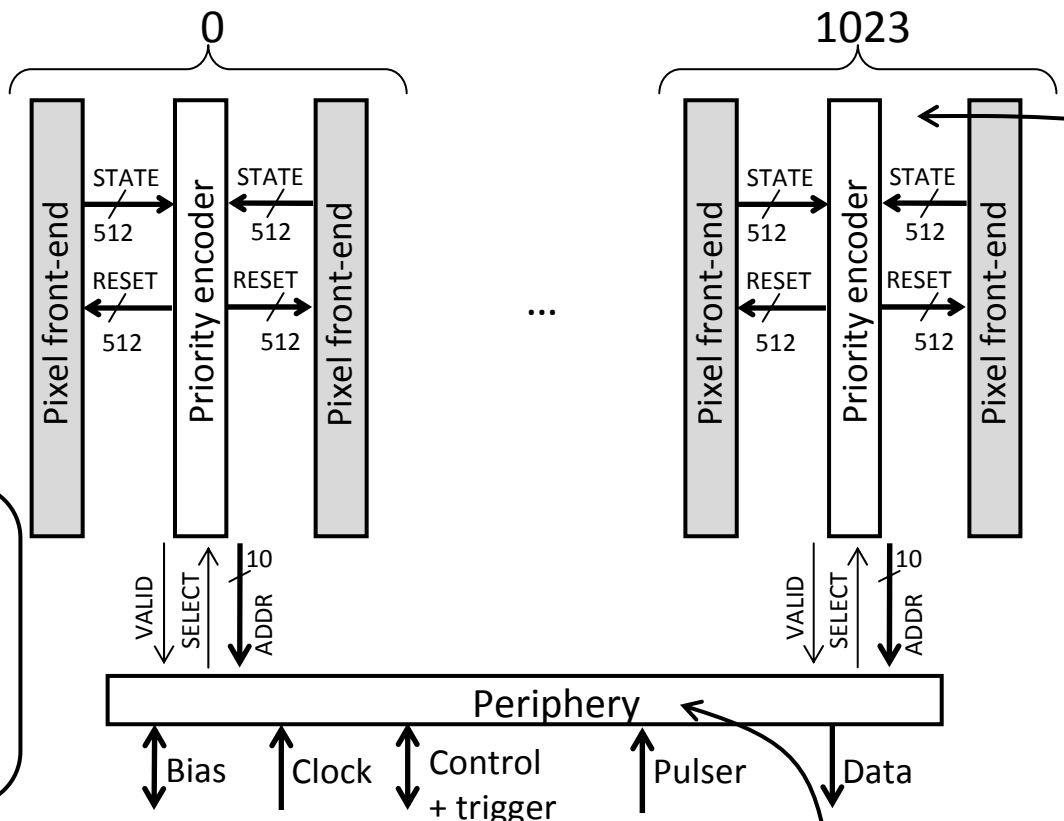
Courtesy of W. Snoeys / TWEPP-2013



- *Hierarchical readout: 1 encoder per double column (2^{10} pixels)*
- *4 inputs basic block repeated to create a larger encoder*
- *1 pixel read per clock cycle*
- *Forward path (address encoder) in gray*
- *Feed-back path (pixel reset) in red*
- *Asynchronous (combinatorial) logic*
- *Clock only to periphery, synchronous select only to hit pixels*

ALPIDE Top Level

Courtesy of W. Snoeys / TWEPP-2013



- low power in-pixel discriminator
- current comparator (bias of ~20 nA)
- storage element for hit information

- in-matrix address encoder
- tree structure to decrease capacitive load of lines
- outputs pixel address and resets pixel storage element

- loss-less data compression de-randomizing circuit
- compresses cluster information in the column
- multi-event memory

Summary & Conclusion

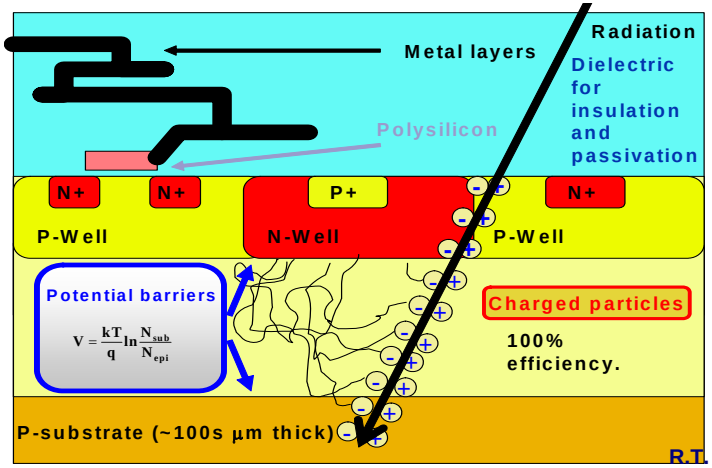
- *Two readout architectures (synchronous and asynchronous) are being developed for CMOS Pixel Sensors adaptable to the ILC vertexing (& tracking)*
- *Synchronous (rolling shutter) readout architecture is a proven architecture*
  - *MIMOSA26 = EUDET beam telescope*
  - *MIMOSA28 = STAR PXL detector*
  - *Still improving performances such as readout speed, power consumption, data compression efficiency …*
    - *Double row readout, In-pixel ADC, New zero suppression logic*
- *Asynchronous readout architecture (ALPIDE) is an emerging architecture being developed*
  - *It would be a breakthrough in the development of CPS*
  - *Low power front-end (20.5 nA/pixel) with data-driven readout, integration time of a few µs determined by shaping time of the front end*
  - *According to applications, it may need more than 1 in-pixel memory buffer to minimise dead time effects*
- *Significant work in CPS architecture design in progress*
  - *Attractive perspective for an ILC vertex detector (i.e. single bunch tagging)*

BACK-UP SLIDES

Development of MAPS for Charged Particle Tracking

- ***In 1999, the IPHC CMOS sensor group proposed the first CMOS pixel sensor (MAPS) for future vertex detectors (ILC)***
  - *Numerous other applications of MAPS have emerged since then*
  - *~10-15 HEP groups in the USA & Europe are presently active in MAPS R&D*

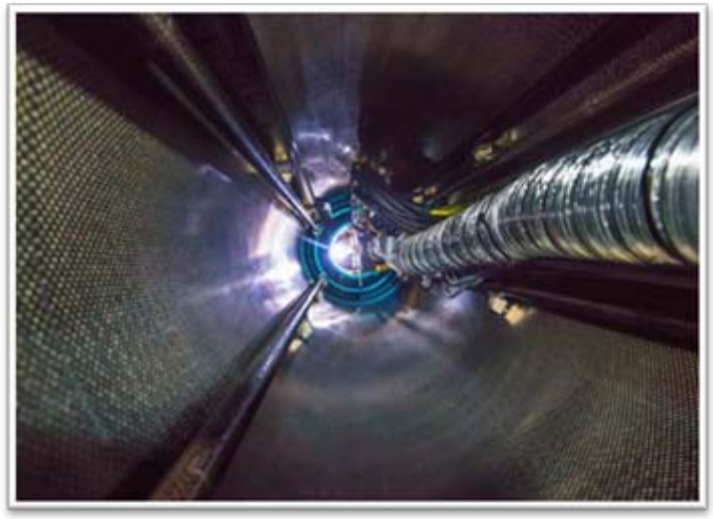
- ***Original aspect: integration sensitive volume (EPI layer) and front-end readout electronics on the same substrate***
  - *Charge created in EPI, excess carries propagate thermally, collected by N_{WELL}/P_{EPI}, with help of reflection on boundaries with P-well and substrate (high doping)*
    - *Q = 80 e^-h / µm ➔ signal < 1000 e^-*
  - *Compact, flexible*
  - *EPI layer ~10–15 µm thick*
    - *thinning to ~30–40 µm permitted*
  - *Standard CMOS fabrication technology*
    - *Cheap, fast multi-project run turn-around*
  - *Room temperature operation*

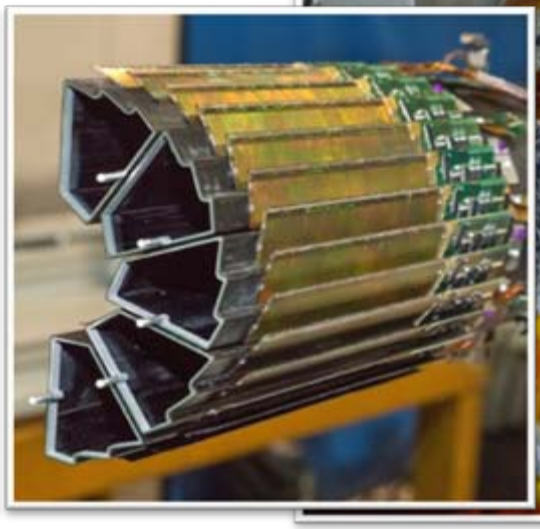


- ***➔ Attractive balance between granularity, material budget, radiation tolerance, read out speed and power dissipation***

  BUT
  - *Very thin sensitive volume ➔ impacts signal magnitude (mV!)*
  - *Sensitive volume almost un-depleted ➔ impacts radiation tolerance & speed*
  - *Commercial fabrication (parameters) ➔ impacts sensing performances & radiation tolerance*
  - *N_{WELL} used for charge collection ➔ restricts use of PMOS transistors*

Starting point: Ultimate chip in STAR





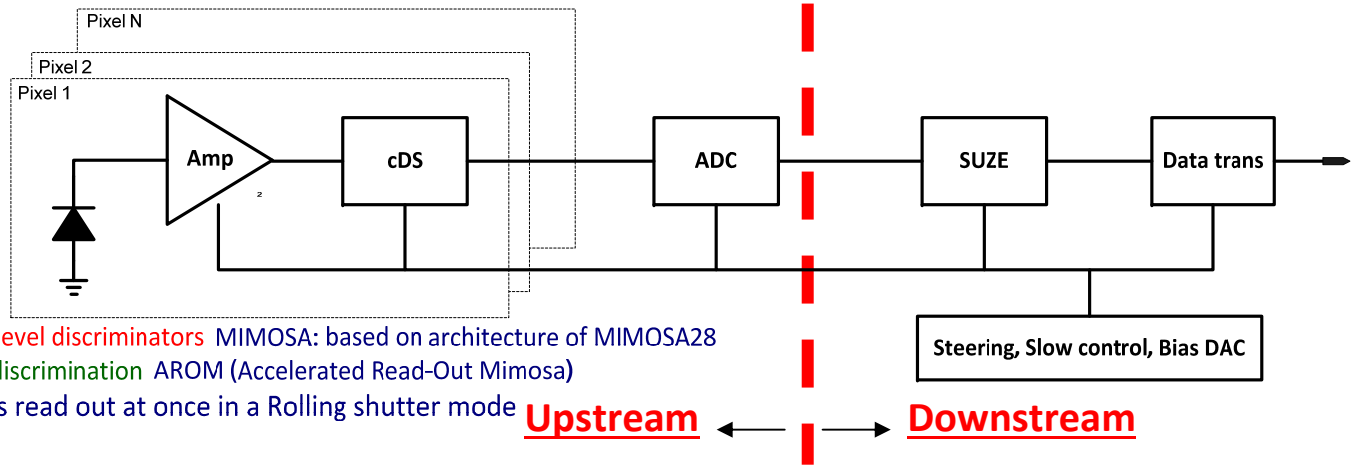
Towards Higher Read-Out Speed and Radiation Tolerance

- Next generation of experiments calls for improved sensor performances:

Expt-System	σ_t	σ_{sp}	TID	Fluence	T_{op}
STAR-PXL	<~ 200 µs	~ 5 µm	150 kRad	$3x10^{12}$ n_{eq}/cm^2	30 °C
ALICE-ITS	10-30 µs	~ 5 µm	700 kRad	10^{13} n_{eq}/cm^2	30 °C
CBM-MVD	10-30 µs	~ 5 µm	<~10 MRad	<~ 10^{14} n_{eq}/cm^2	<<0 °C
ILD-VXD	<~2 µs	<~ 3 µm	O(100) kRad	O(10^{11} n_{eq}/cm^2)	<~30 °C

- Main improvements required while remaining inside the virtuous circle of spatial resolution, speed, material budget, radiation tolerance ➔ move to **0.18 µm** process
  - To enhance the radiation tolerance
    - High resistivity epitaxial layer
    - Smaller feature size process
  - To accelerate the readout speed
    - More parallelised read-out
    - Optimised number of pixels per column
    - New pixel array architectures
    - Smaller feature size process

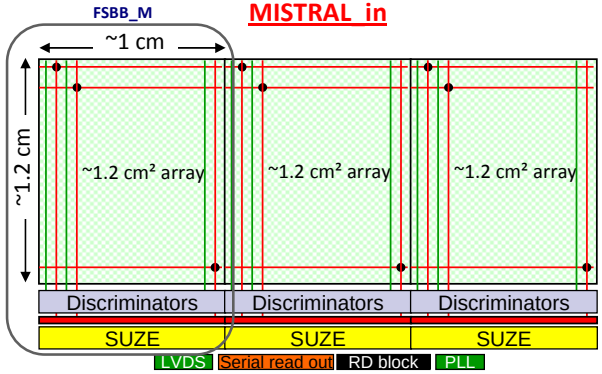
Sensors R&D for the upgrade of the ITS: Our Strategy

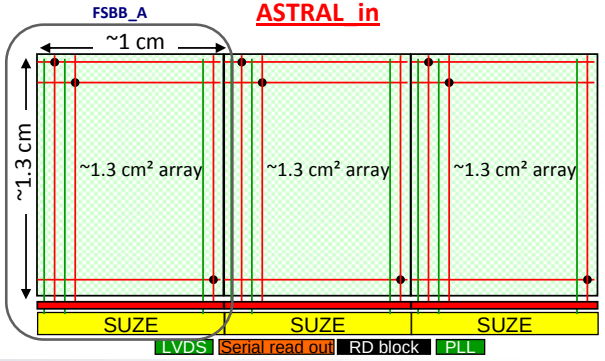


- R&D of up- & down-stream of sensors performed in parallel at IPHC in order to match the ITS timescale

for 2 final sensors (~3x1.3 cm²)

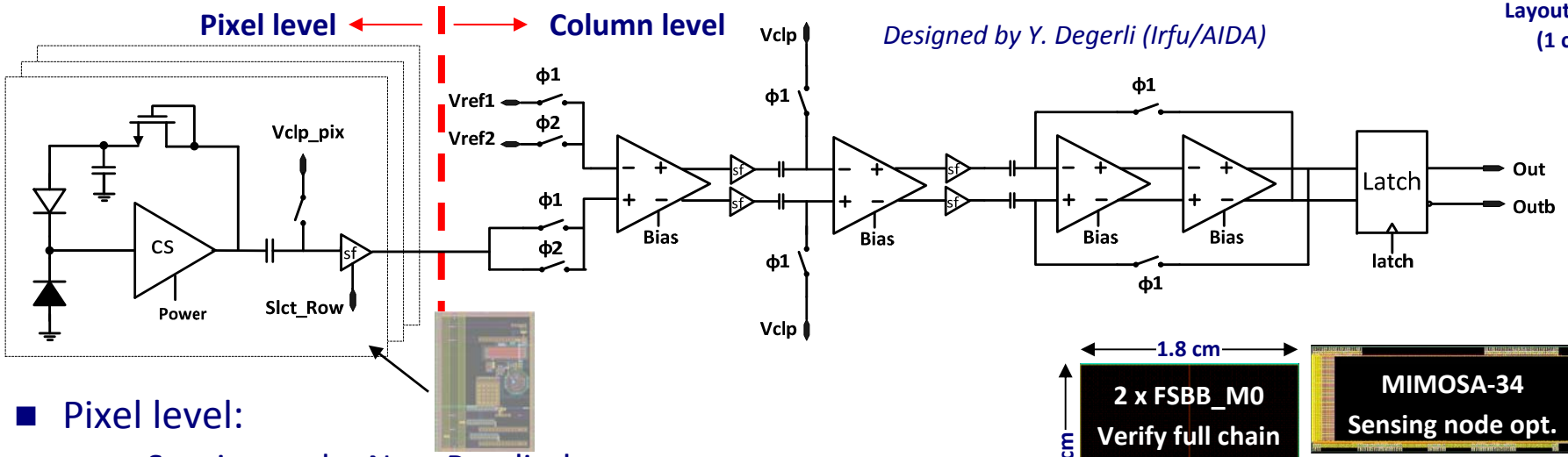
- Mature architecture: MISTRAL = **MI**MOSA **S**ensor for the inner **TR**acker of **AL**ICE
  - Relatively moderate readout speed (200 ns/ 2rows)
    - ~ 200 mW/cm² , σ_{sp} ~ 5 µm for inner layers
    - ~ 100 mW/cm² , σ_{sp} ~ 10 µm for outer layers
- Improved architecture: ASTRAL = **A**ROM **S**ensor for the inner **TR**acker of **AL**ICE
  - Higher speed (100 ns/ 2rows) + Lower power
    - ~ 85 mW/cm², σ_{sp} ~ 5 µm for inner layers
    - ~ 60 mW/cm², σ_{sp} ~ 10 µm for outer layers

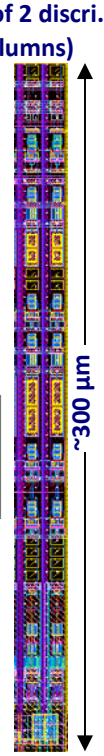


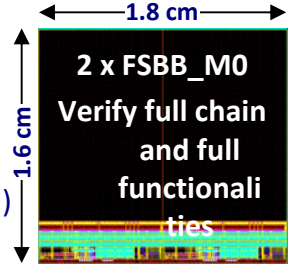


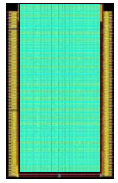
- Modular design + reused parts ➔ optimising R&D time
- Several groups involved in the ITS design
  - ➔ see Magnus Mager (CERN) talk in this conference

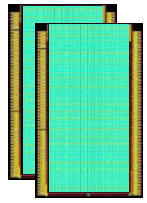
Upstream of MISTRAL Sensor

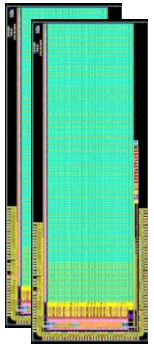


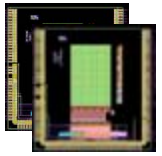










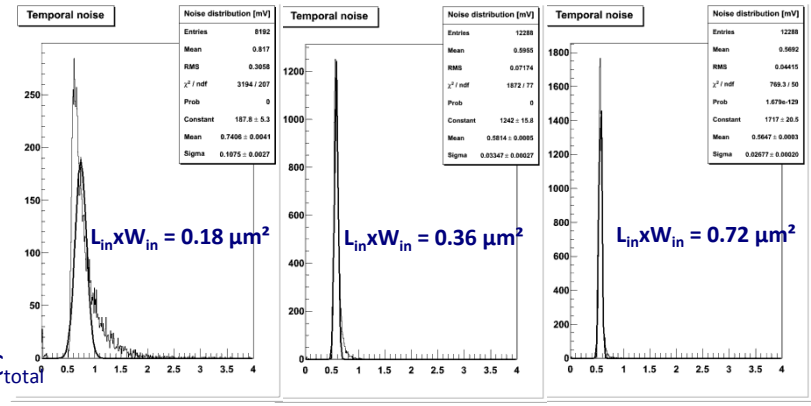


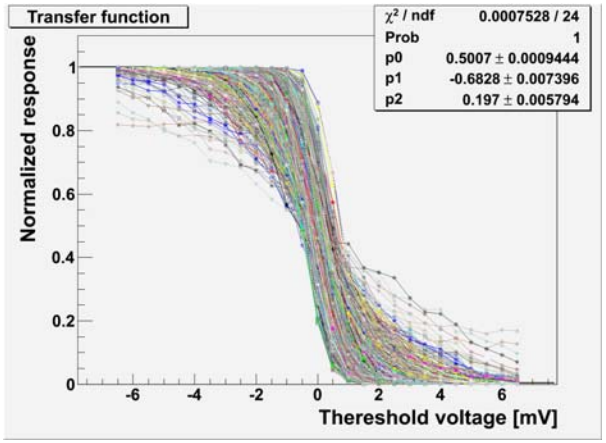
- Pixel level:
  - Sensing node: N_{well}-P_{EPI} diode
    - Optimisation = f (diode size, shape, No. of diodes/pixel, pixel pitch, EPI)
  - In-pixel amplification and cDS:
    - Limited dynamic range (supply 1.8 V) compared to the previous process (3.3 V)
    - Noise optimisation especially for random telegraph signal (RTS) noise
      - Sensing diode: avoid STI around N-well diode
      - RO circuit: avoid using minimum dimensions for key MOS & avoid STI interface
      - ➔ Trade off between diode size, input MOS size w.r.t. S/N before and after irradiation
- Column level:
  - Discriminator: similar schematic as in MIMOSA26 & 28
    - Offset compensated amplifier stage + DS (double sampling)
    - 200 ns per conversion
  - Read out 2 rows simultaneously ➔ 2 discriminators per column (22 µm)

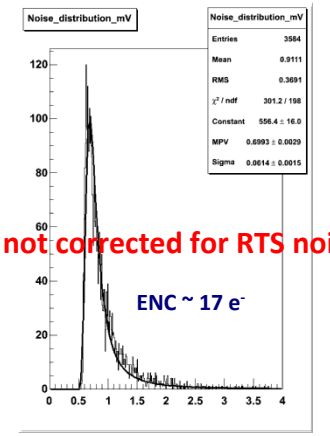
Test Results of the Upstream Part of MISTRAL Sensor

- Lab test results @ 30 °C (MIMOSA22-THRa1 & 2, MIMOSA22-THRb) :
  - Diode optimisation
    - CCE optimisation: surface diode of 8-11 µm² (22x33 µm²)
  - In-pixel amplification optimisation
    - Reduction of RTS noise by a factor of 10 to 100
  - MISTRAL RO Architecture: (single & double raw RO)
    - 2-row RO increases FPN by ~1 e⁻ ENC ➔ negligible impact on ENC_{total}

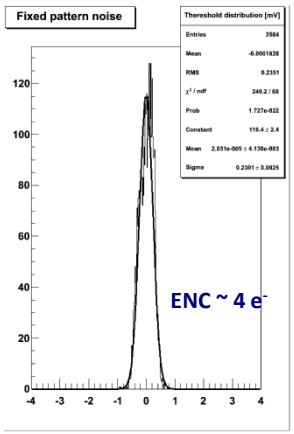
    ➔ Design of the upstream of MISTRAL validated







Pixel not corrected for RTS noise

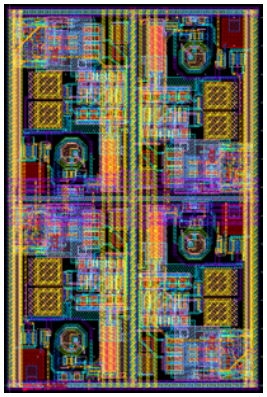


- Beam test results (DESY):
  - SNR for MIMOSA-22THRa close to MIMOSA 34 result
    - 8 µm² diode features nearly 20 % higher SNR (MPV)
  - Detection efficiency ≥ 99.8% while Fake hit rate ≤ O(10^{-5})
  - 22×33 µm² binary pixel resolution: ~5 µm as expected from former studies
  - Final ionisation radiation tolerance assessment under way

Upstream of ASTRAL sensor

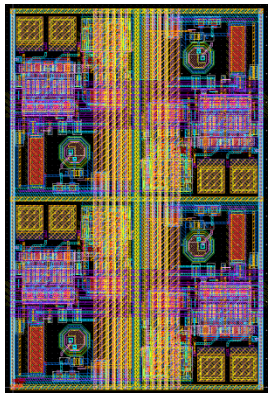
- Thanks to the quadruple-well technology, discriminator integrated inside each pixel
  - Analogue buffer driving the long distance column line is no longer needed
    - Static current consumption reduced from ~120 µA up to ~14 µA per pixel
  - Readout time per row can be halved down to 100 ns (still with 2 rows at once) due to small local parasitics
- Sensing node & in-pixel pre-amplification as in MISTRAL sensors
- In-pixel discrimination
  - Topology selected among 3 topologies implemented in the 1st prototype AROM-0
  - Several optimisations on the 2 most promising topologies in AROM-1
  - One third of final sensor (FSBB_A0) coming back this week from dicing/thinning

AROM-1a
2x2 pixels



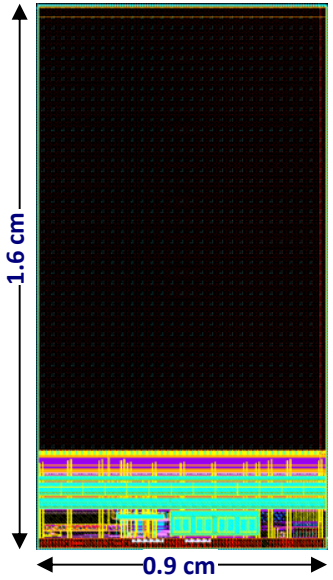
Horizontal controls shared between 2 rows

AROM-1b
2x2 pixels

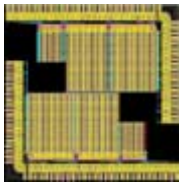


Horizontal controls in each row

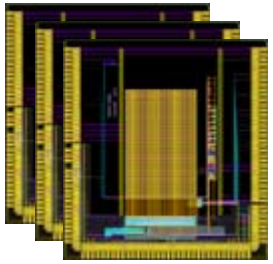
FSBB_A0
1/3 of final sensor



AROM-0



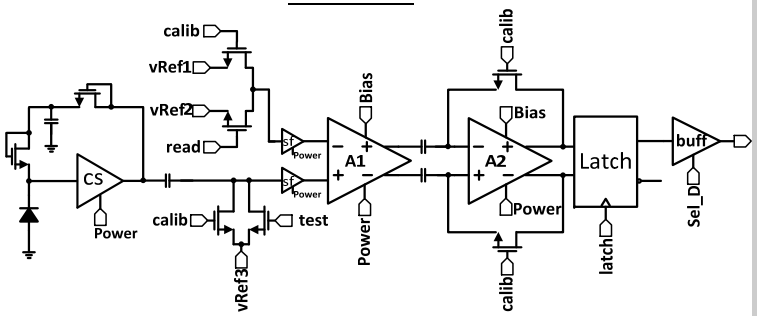
AROM-1



Summary of the AROM-1 development

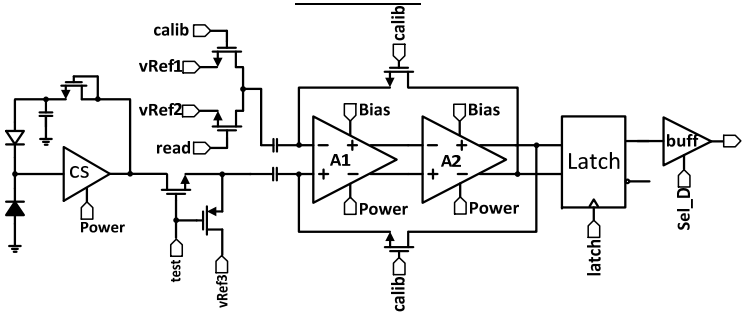
AROM-0 submission Feb. 2013

Version 1



- 32 x32 pixels (22x33 µm²) Single row readout

Version 2



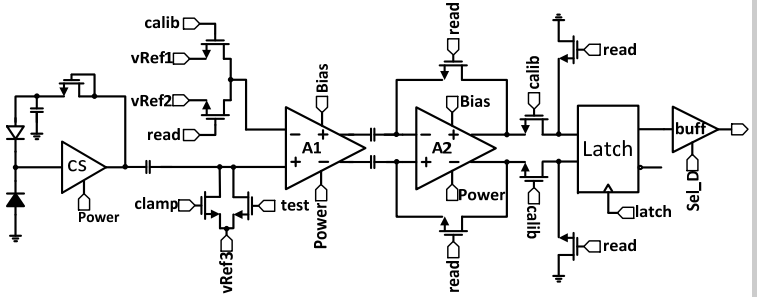
- 32 x32 pixels (22x33 µm²) Single row readout
- 16 x16 pixels (22x33 µm²) Double row readout

AROM-1_e/f
More stable
Less compact → more noise

AROM-1_a/b/c
More compact
Less stable → more noise

AROM-1 series

AROM-1e/f submission Nov. 2013



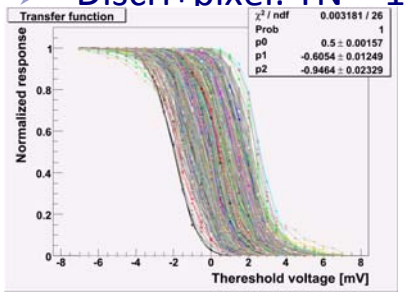
- 64 x64 pixels Double row readout
  - e: 22x33 µm²
  - f: 27x27 µm²
- Noise and power consumption optimized
- Slightly different timing configuration
- Tests in progress

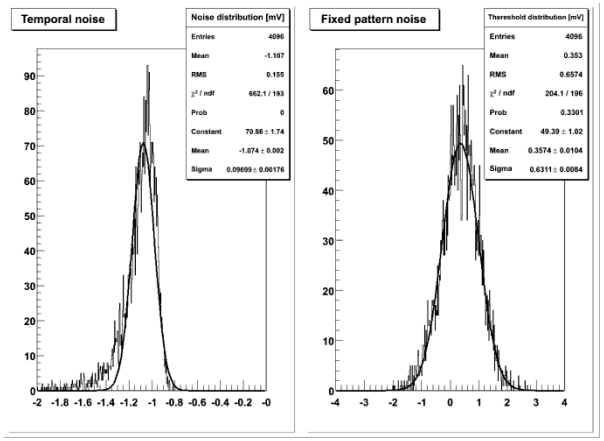
AROM-1a/b/c submission Aug. 2013

- 64 x64 pixels Double row readout
  - a: 22x33 µm² (similar layout as AROM-0v2)
  - b: 22x33 µm² (optimized layout)
  - c: 24x33 µm² (study impact of pixel pitch)
- RTS noise mitigated
- Thermal noise from switches optimized
- Optimized layout to minimize cross talk and asymmetry
- Performance validated already in laboratory

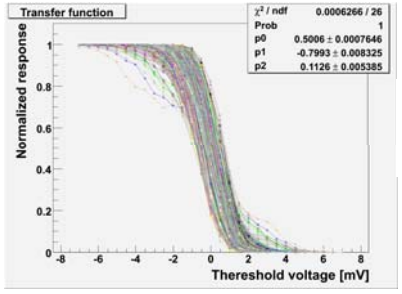
Test Results of the Upstream Part of ASTRAL Sensor

- Preliminary lab test results @ 30 °C and @ 100 MHz (instead of 160 MHz)
  - Current acquisition board limitation
- AROM-1b/c
  - Discri alone: TN ~ 0.75 mV, FPN ~ 0.63mV
  - Discri+pixel: TN ~ 1.1 mV, FPN ~ 0.66mV

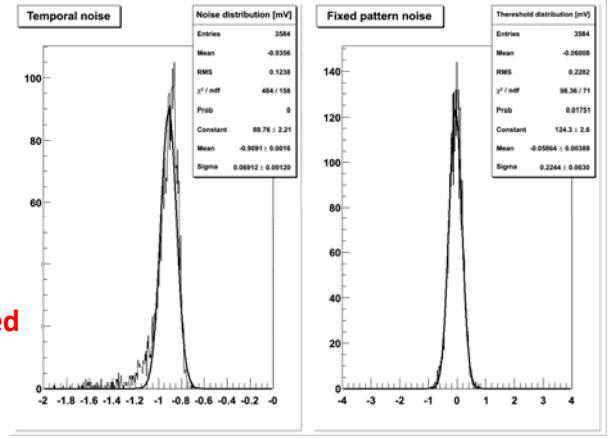




- AROM-1e tests are ongoing
  - Discri alone: TN ~ 0.29 mV, FPN ~ 0.19mV
  - Discri+pixel: TN ~ 0.94 mV, FPN ~ 0.23mV

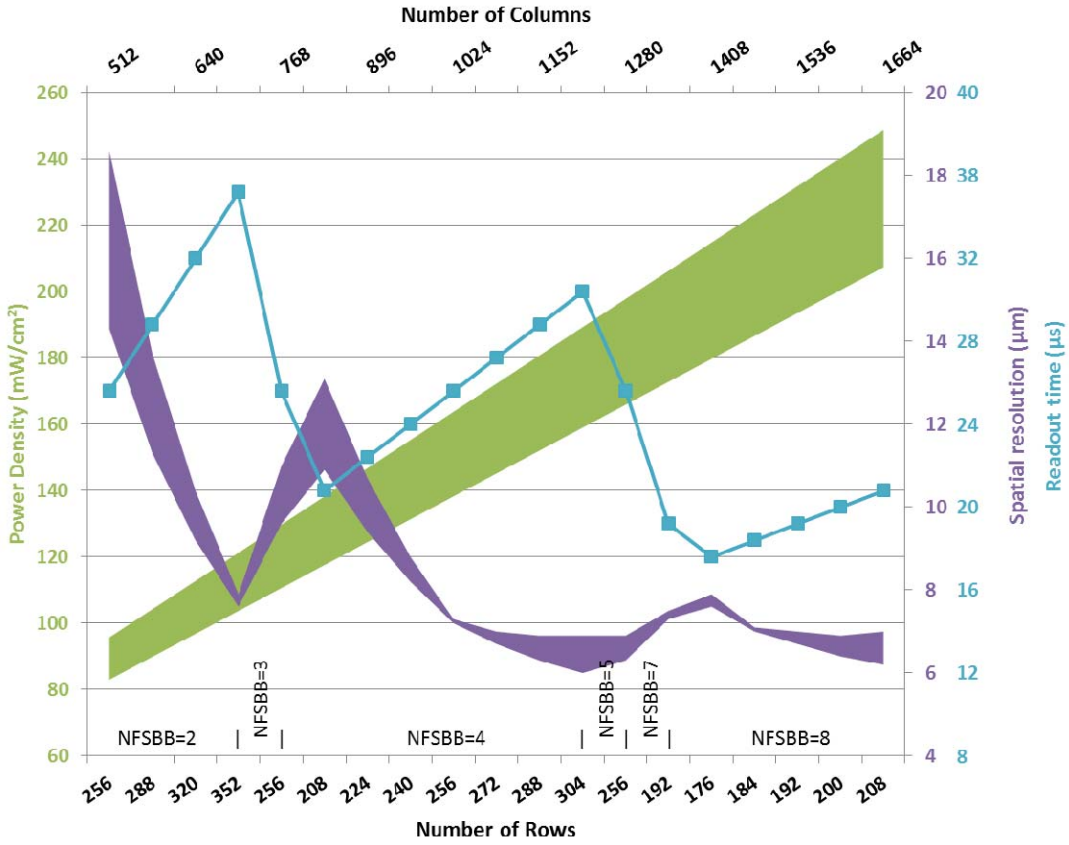


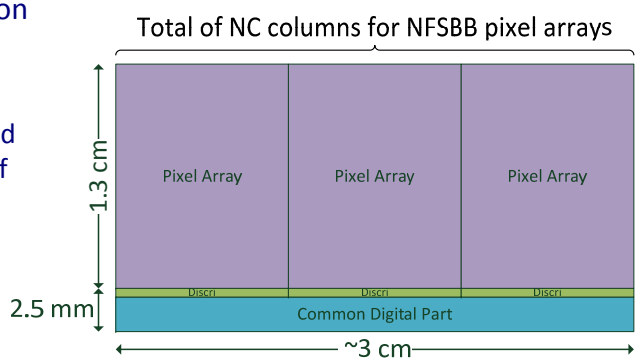
AROM-1e optimisation is validated
Some residual coupling effects are investigated

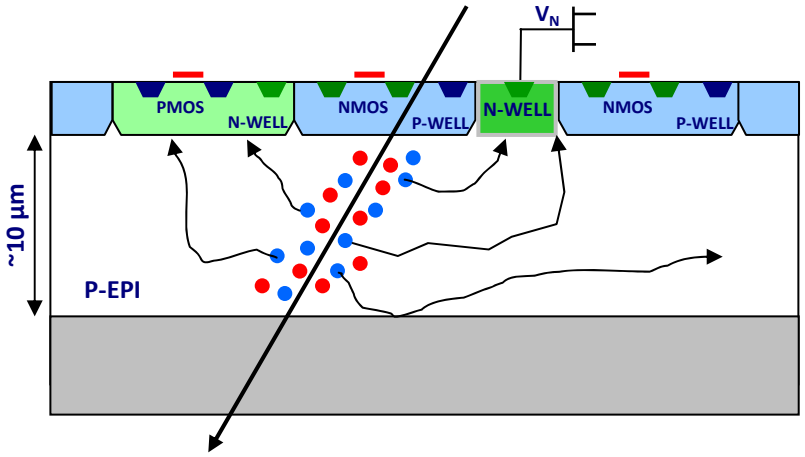


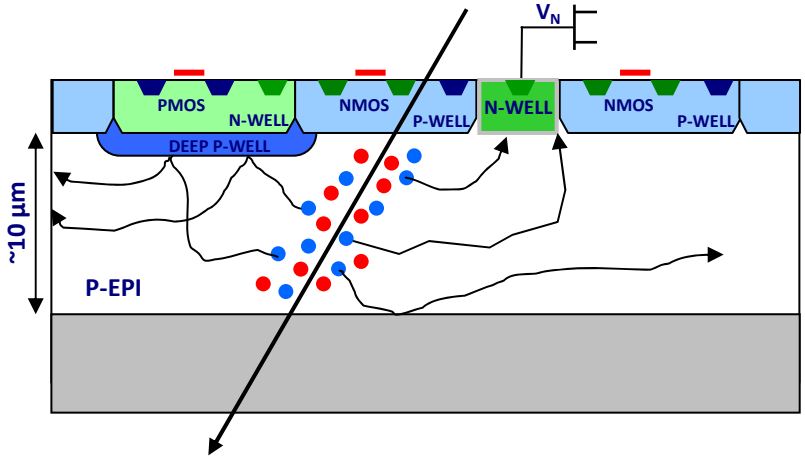
Power density, Integration time and Spatial resolution

- Effect of pixel pitches on these 3 factors:
  - Assumptions
    - MISTRAL for outer layers
    - Same sensitive area (1.3x3 cm²)
    - 1 SUZE per final sensor
    - Constant power consumption for digital
    - NC=Number of Columns (modulo 32)
    - NFSBB= Number of FSBBs per final sensor
    - NC/NFSBB = Number of rows
  - Row pitch (RP) has an effect on Readout time (RT
    - RP = 30000 µm / NC
    - **RT = (NC / NFSBB) / 2 x 200 ns**
  - Column pitch (CP) has an effect on Power densit (PD)
    - CP = 13000 µm / (NC / NFSBB)
    - **PD = (60 mA + 0,117 mA x NC x 2) x 1.8 V**
    - **PDopt = (60 mA + 0,09 mA x NC x 2) x 1.8 V**
  - Both pitches have an effect on Spatial resolution (SR)
    - **SR = 7µm (RP x CP / (22 x 66 µm²))$^{1/2 \text{ or } 1}$**
    - Empirical formula for a specific technology and architecture based on the spatial resolution of tested chip with an area of 22 x 66 µm²






V_N
PMOS
N-WELL
NMOS
P-WELL
N-WELL
NMOS
P-WELL
~10 µm
P-EPI


V_N
PMOS
N-WELL
NMOS
P-WELL
N-WELL
NMOS
P-WELL
DEEP P-WELL
~10 µm
P-EPI