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SI LAB Silizium Labor Bonn

DEPFET Active Pixel Detector

The DEPFET Vertex Detector

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DEPFET Collaboration

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The DEPFET Collaboration

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- Charles University, Prague
- DESY, Hamburg
- IFCA, Santander
- IFIC, Valencia
- IFJ PAN, Krakow
- IHEP, Beijing
- LMU Munich
- MPI, Munich
- HLL, Munich
- TU, Munich
- University of Barcelona
- University of Bonn
- University of Heidelberg
- University of Giessen
- University of Göttingen
- University of Tabuk

depfet.org

Outline

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- DEPFET for future colliders
  - SuperKEKB and ILC
- DEPFET system
  - Sensor
  - ASICs
- Latest results
  - Lab and beam tests

Future Vertex Detectors

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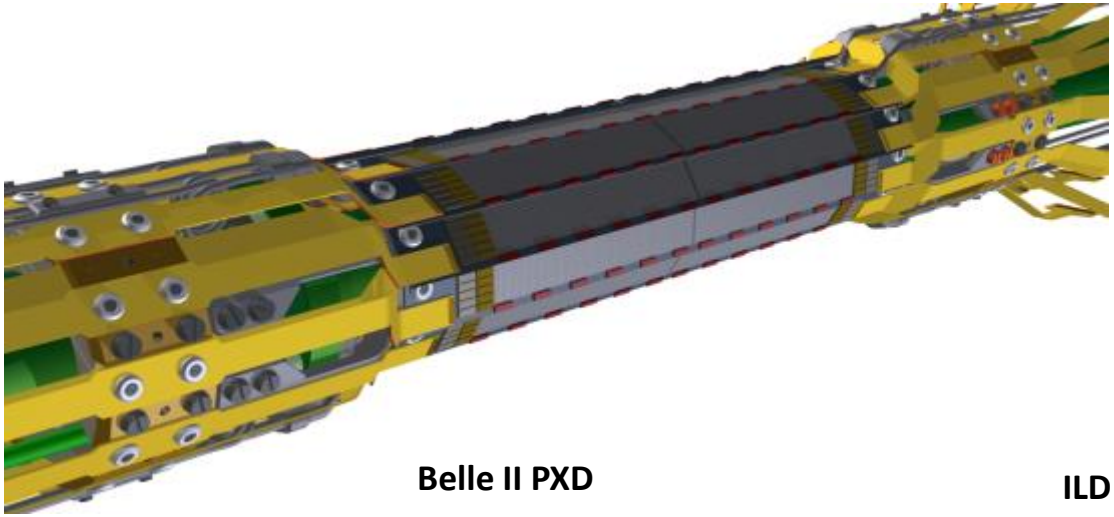
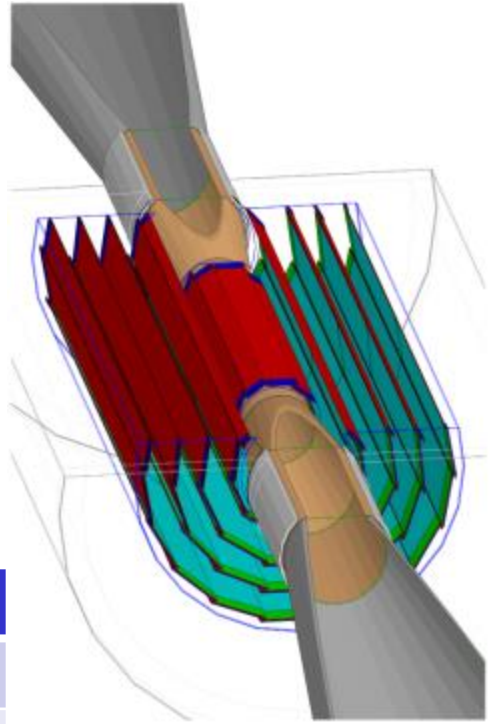
The Belle II Collaboration decided on DEPFET as baseline for the pixel detector



Belle II PXD



ILD 5-layer VXD

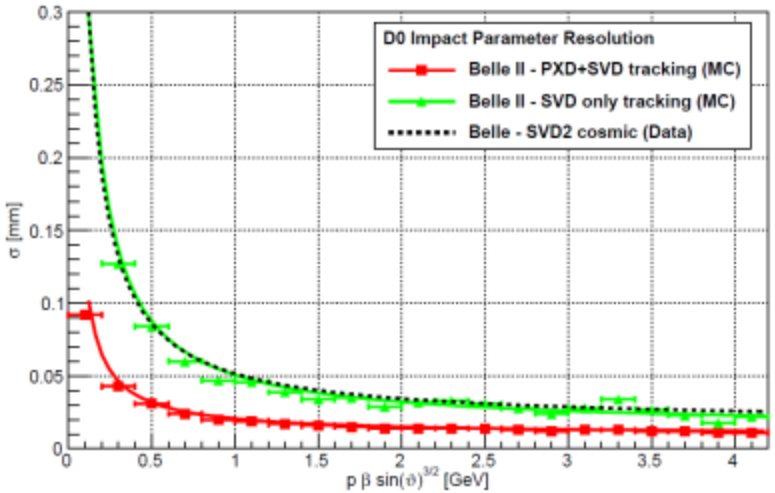
	Belle II	ILD LOI 5-layer layout	
Radii	14, 22	15, 26, 38, 49, 60	mm
Ladder length	90 (L1), 122 (L2)	123 (L1), 250 (L2-L5)	mm
Sensitive width	12.5 (L1-L2)	13 (L1), 22 (L2-L5)	mm
Number of ladders	8, 12	8, 8, 12, 16, 20	
Pixel size	50x50 (L1), 50x75 (L2)	25x25 (L1-L5)	μm^2
Frame rate	50	20 (L1), 4 (L2-L5)	kHz

The Belle II PXD DEPFET ladders: *almost* prototypes for L1 and L2 of ILD

↘ **Positive impact on DEPFETs for ILC**

Belle II Vertex Detector Requirements

	Belle II
Occupancy	0.4 hits/μm^2/s
Radiation	2 Mrad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year
Duty cycle	1
Frame time	20 μs
Momentum range	Low momentum (< 1 GeV)
Acceptance	17º-155º
Material budget	0.21% X_0 per layer
Resolution	15 μm (50x75 μm^2)



- Modest resolution (15 μm), dominated by multiple scattering → Pixel size (50 x 75 μm²)
- Lowest possible material budget (0.2% X_0/layer)
  - Ultra-transparent detectors
  - Lightweight mechanics and minimal services

ILC Detector Concepts and Belle II

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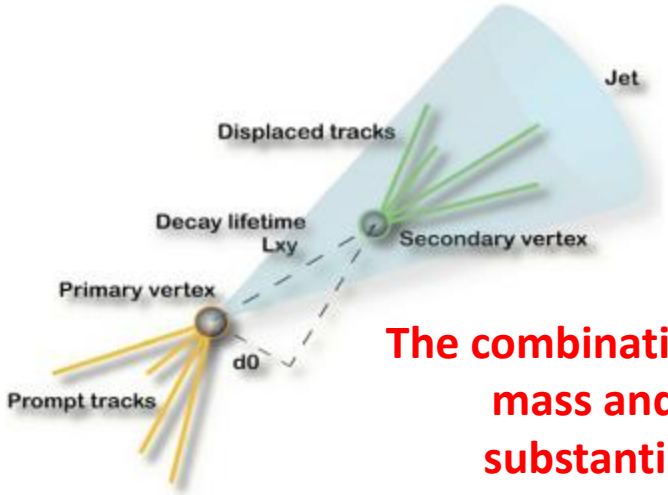
	Belle II	ILC
Occupancy	0.4 hits/μm^2/s	0.13 hits/μm^2/s
Radiation	2 Mrad/year	< 100 krad/year
	$2 \cdot 10^{12}$ 1 MeV n_{eq} per year	10^{11} 1 MeV n_{eq} per year
Duty cycle	1	1/200
Frame time	20 μs	25-100 μs
Momentum range	Low momentum (< 1 GeV)	All momenta
Acceptance	17º-155º	6º-174º
Material budget	0.21% X_0 per layer	0.12% X_0 per layer
Resolution	15 μm (50x75 μm^2)	5 μm (20x20 μm^2)

- Excellent resolution (5 μm) → Pixel size (20 x 20 μm²)
- Lowest possible material budget (0.1% X_0/layer)
  - Ultra-transparent detectors
  - Lightweight mechanics and minimal services

→ Both detectors have very similar requirements

Vertexing Requirements HEP



$$\sigma_{d0} \approx \sqrt{\frac{r_2^2\sigma_1^2 + r_1^2\sigma_2^2}{(r_2 - r_1)^2}} \oplus \frac{r}{p \sin^{\frac{3}{2}} \theta} 13.6MeV \sqrt{\frac{x}{X_0}}$$

$$\sigma_{d0} \approx a \oplus \frac{b}{p \sin^{\frac{3}{2}} \theta}$$

The combination of resolution, mass and power is a substantial challenge

- Common vertex detector requirements
  - First layer close to the IP
  - Low material budget
    - Reduced services
    - Low power dissipation
  - High granularity
    - Good spatial resolution
  - Fast readout
  - Radiation hardness

	a (μm)	b (μm GeV)
LHC	12	70
STAR	12	19
Belle II	8.5	10
ILC	5	10

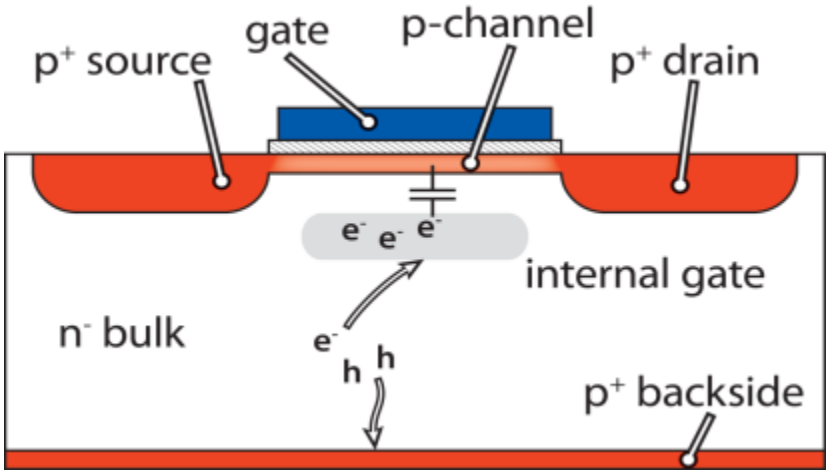
a: Governs high momentum
b: Dominates at low momentum

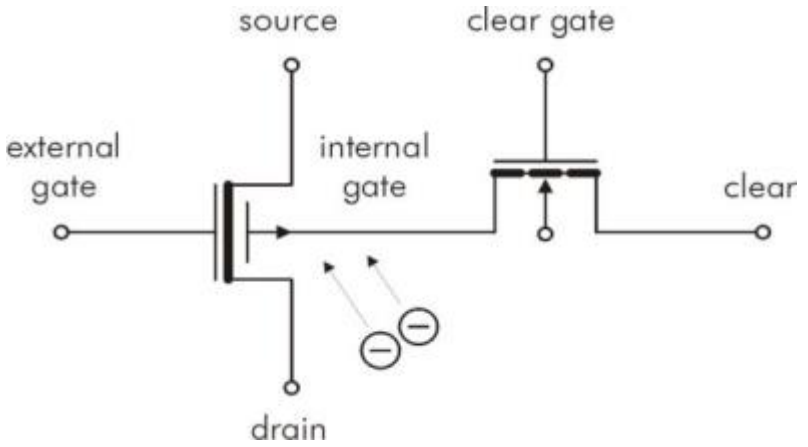
DEPFET – DEpleted P-channel FET

- Each pixel is a p-channel FET on a completely depleted bulk.
- A deep n-implant creates a potential minimum for electrons under the gate (internal gate)
- Signal electrons in the internal gate modulate the transistor current

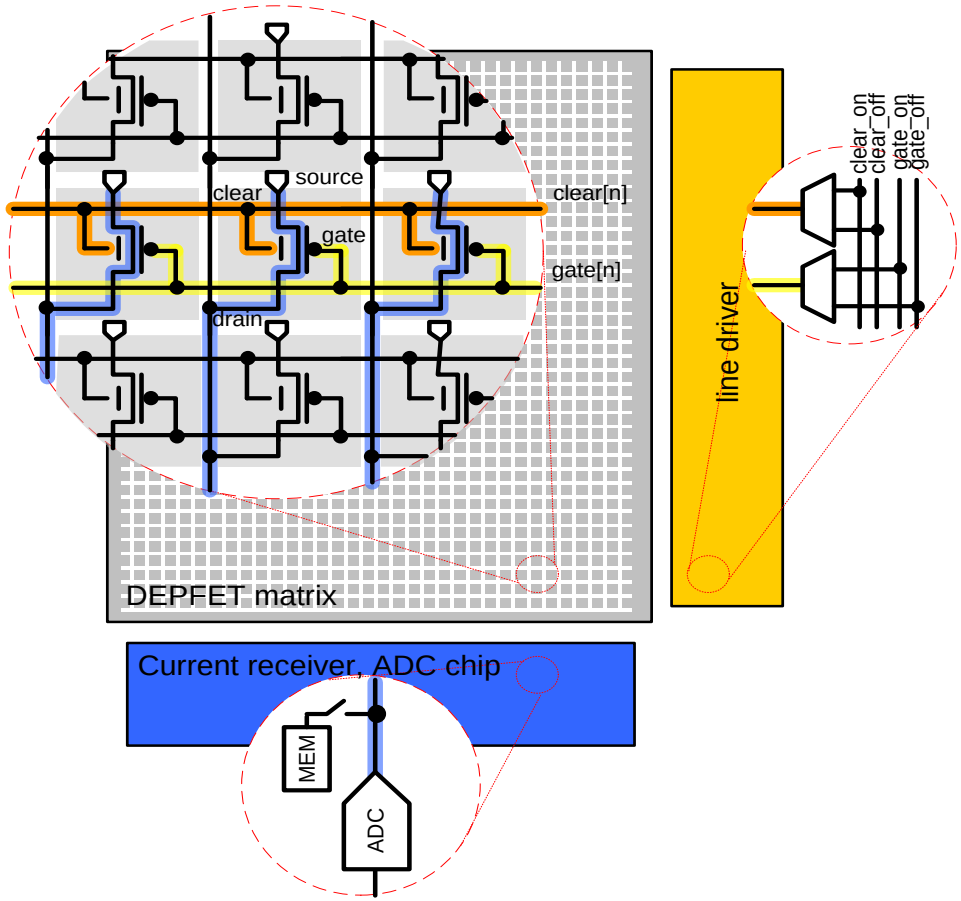
$$g_q = \frac{\partial I_d}{\partial q} \propto \left(\frac{I_d}{L^3 W C_{ox}} \right)^{1/2} \sim 500 pA/e^-$$

- Detection and internal amplification
- Small intrinsic noise
- Low power consumption



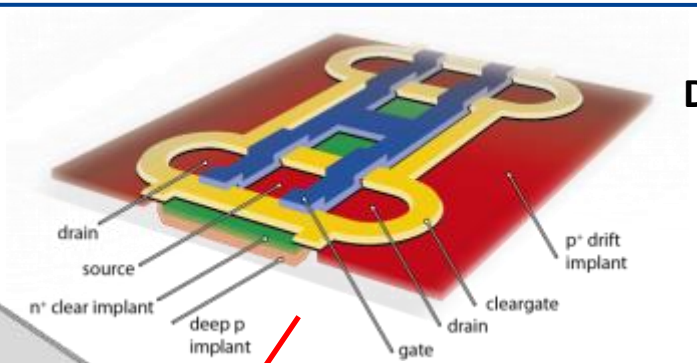


DEPFET Pixel Array

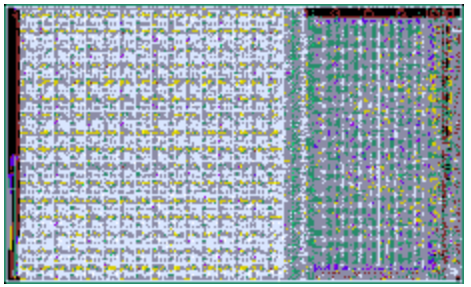


- Pixels are arranged in a matrix
- Row wise readout (4 rows at a time)
- Gate, clear lines need Switcher steering chip
- Long drain readout lines to keep material out of the acceptance region
- Only ‘activated’ rows consume power
  - The others are still sensitive to charge
  - Low power consumption

The DEPFET Ladder

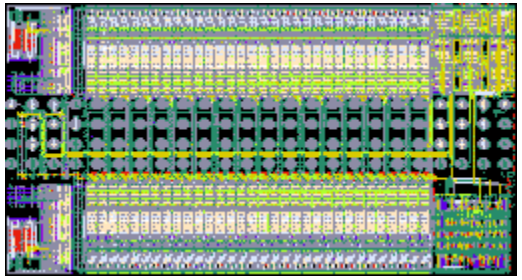


DCDB (Drain Current Digitizer)
Analog frontend

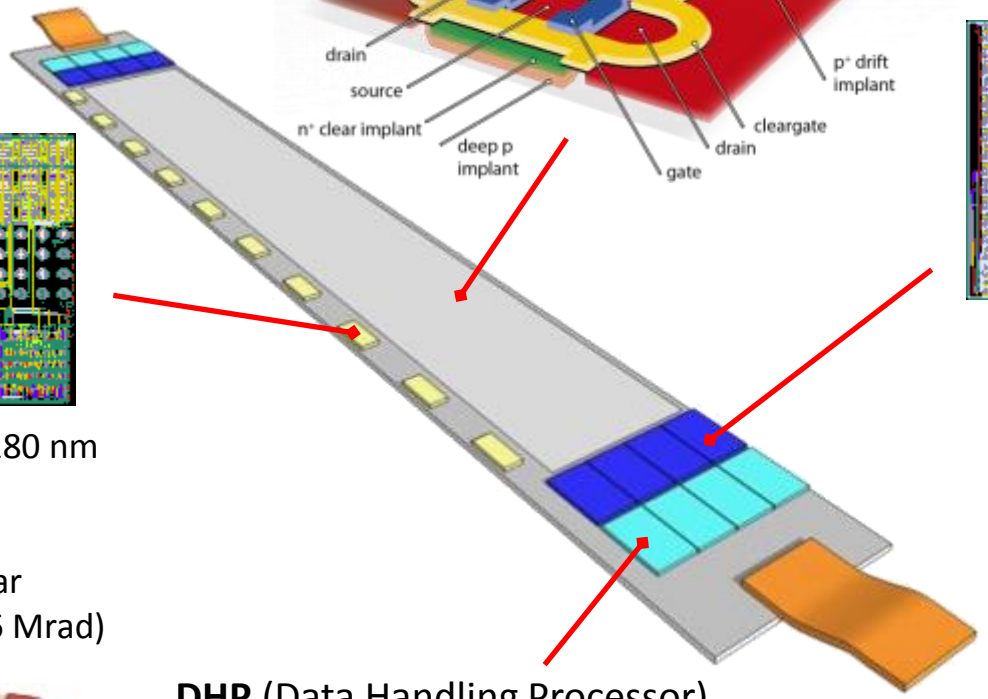


UMC 180 nm
Size 5.0×3.2 mm^2
TIA and ADC
Pedestal compensation
Rad. Hard proved (20 Mrad)

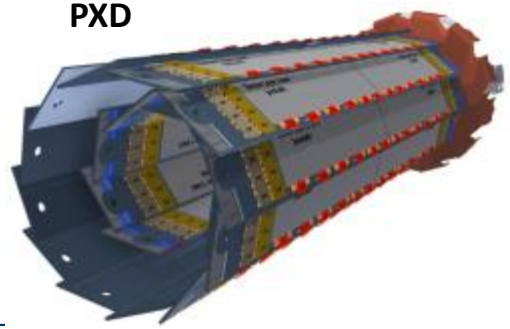
SwitcherB
Row control



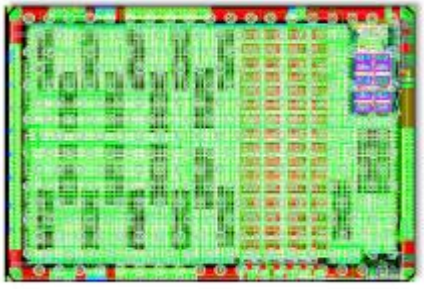
AMS/IBM HVCMOS 180 nm
Size 3.6×1.5 mm^2
Gate and Clear signal
Fast HV ramp for Clear
Rad. Hard proved (36 Mrad)



PXD

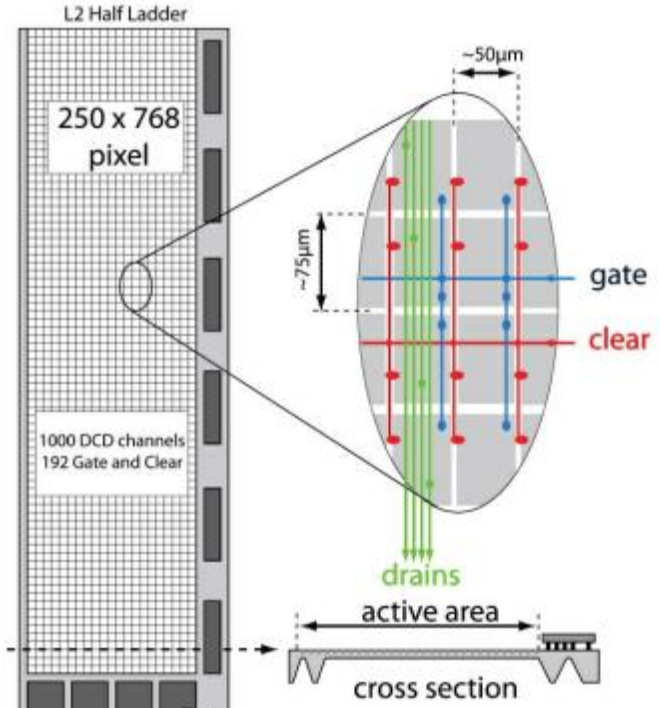


DHP (Data Handling Processor)
First data compression

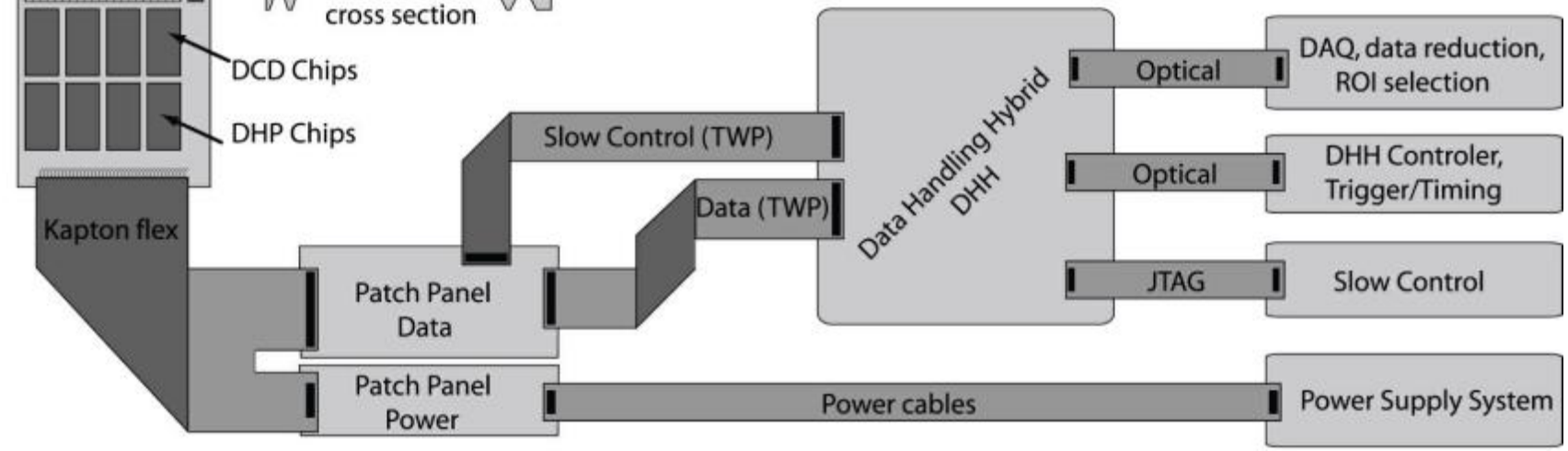


TSMC 65 nm
Size 4.0×3.2 mm^2
Stores raw data and pedestals
Common mode and pedestal correction
Data reduction (zero suppression)
Timing signal generation
Rad. Hard proved (100 Mrad)

Off-module Data Flow



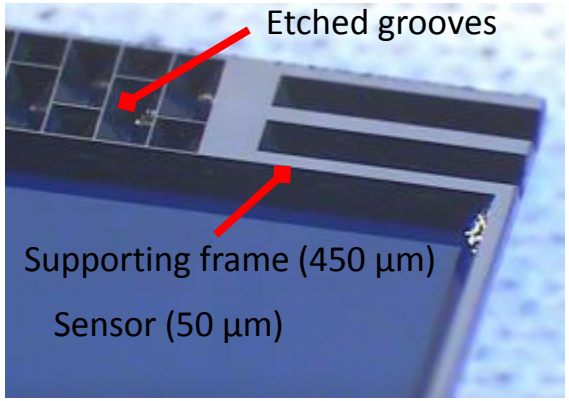
- **DHH** (Data Handling Hybrid)
  - Electrical - optical interface
  - Slow control master (JTAG)
  - Clustering
- **ONSEN**
  - Data buffer
  - Reduction via ROI selection (DATCON, HLT)

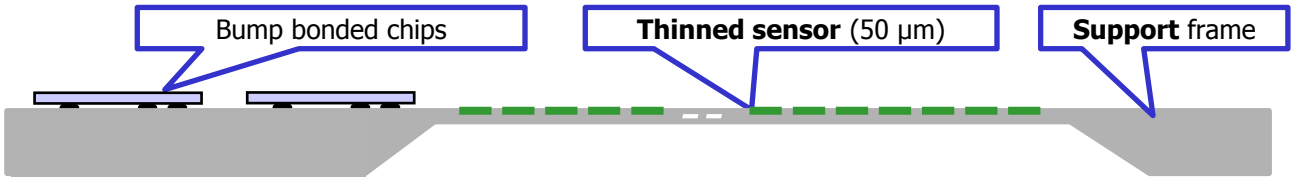


Thin DEPFET Sensors

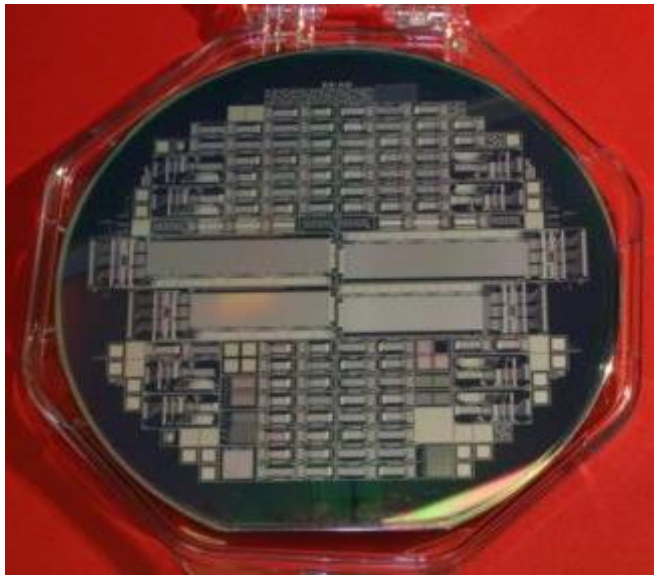
Use anisotropic etching on bonded wafers to create a thin, self-supporting sensor

- One material: uniform and small thermal expansion
- The DEPFET thickness is a free adjustable parameter

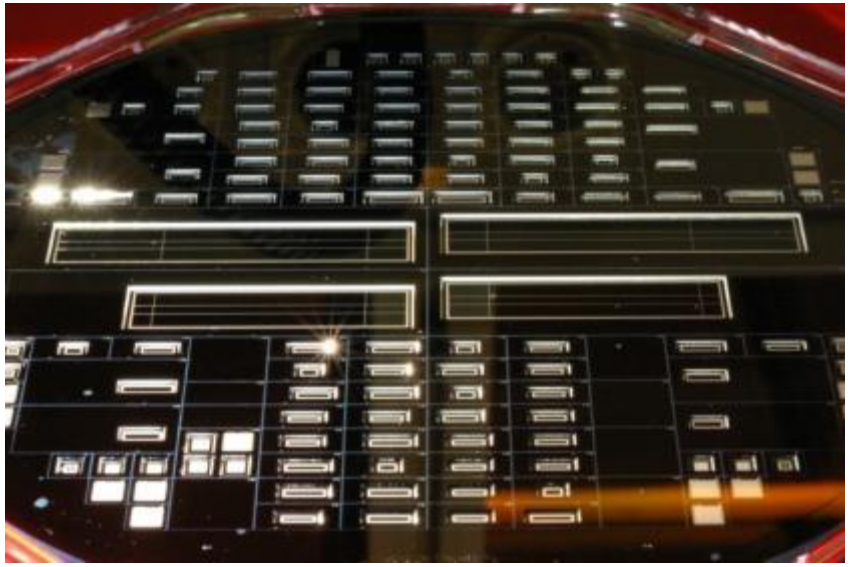


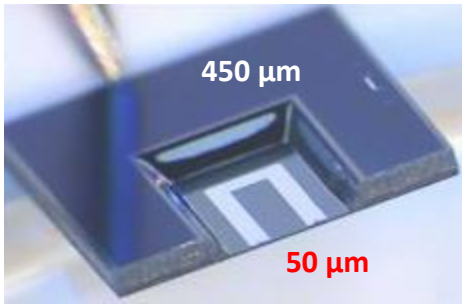


PXD6 Prototype Production



8 SOI wafers with 50 µm thin sensors (450 µm handle)
- Small test matrices with design variations
- Full size sensors for prototyping





90 steps fabrication process:
- 9 Implantations
- 19 Lithographies
- 2 Poly-layers
- 2 Alu-layers
- 1 Copper layer
- Back side processing

Hybrid 5.0 - Full System Test

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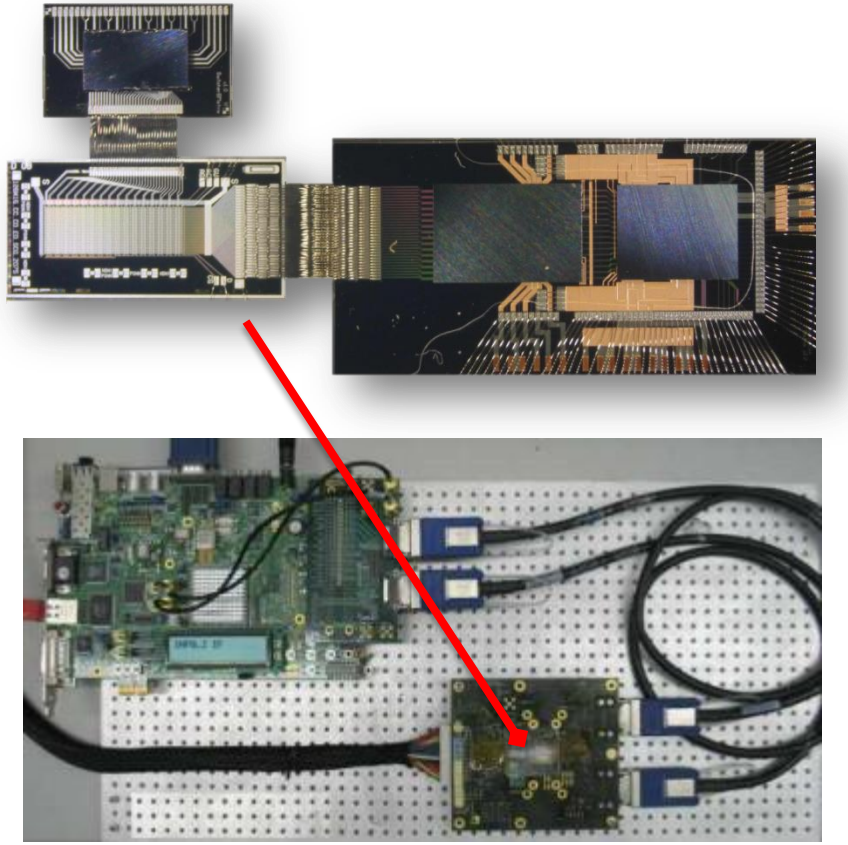
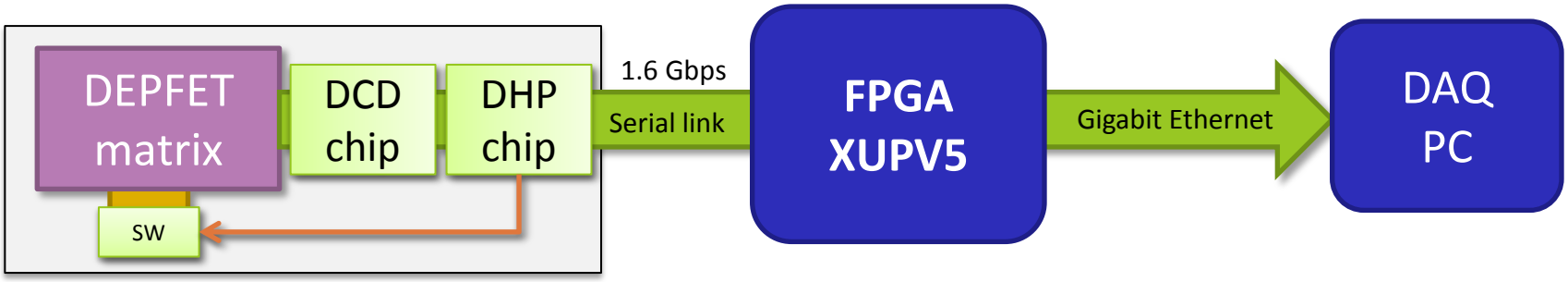
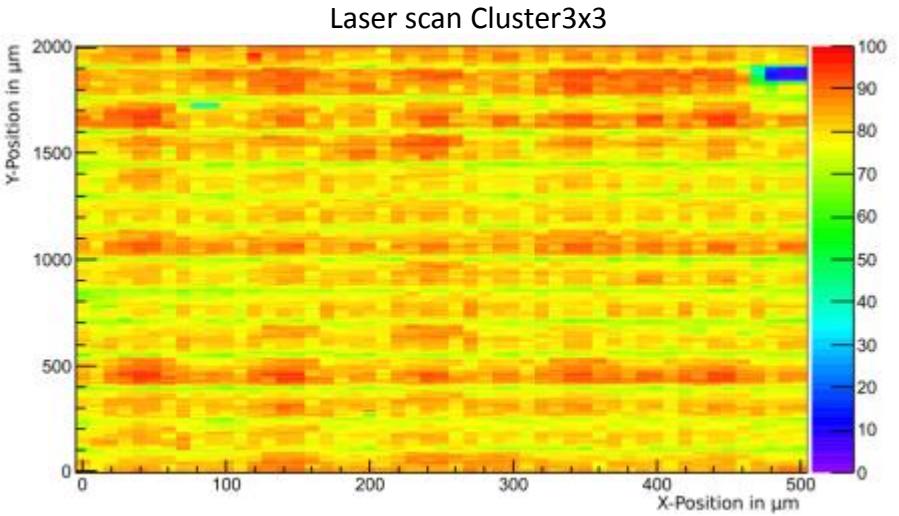
- Zero suppressed readout with the minimum necessary amount of components:
  - One Switcher-B
  - One DCDBv2
  - One DHP 0.2
  - Small thin matrix: Belle II SD PXD6 type, 16x128 pixels, 50x75 µm² pitch



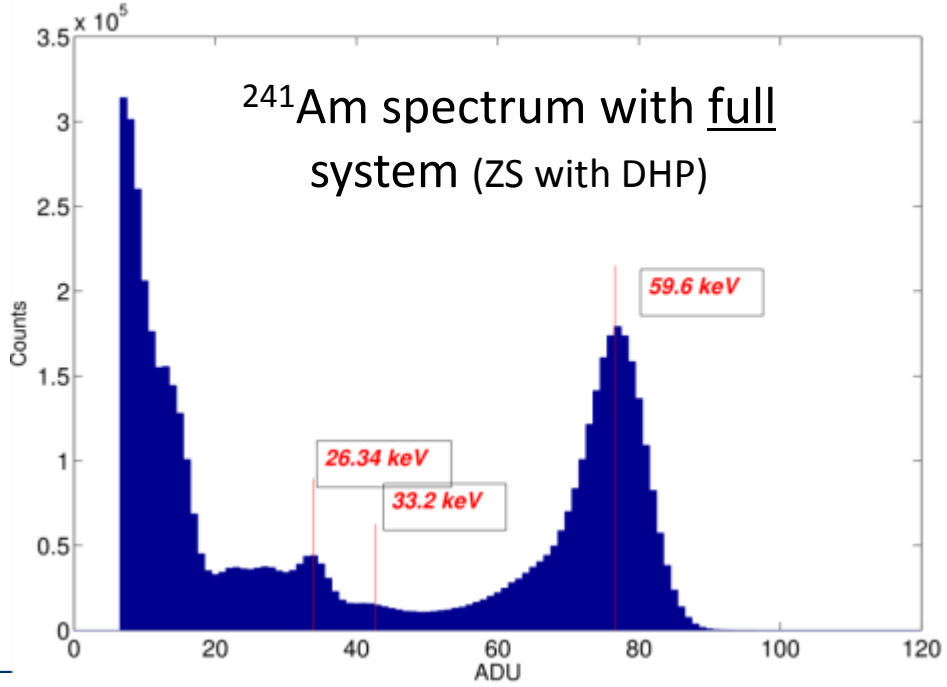


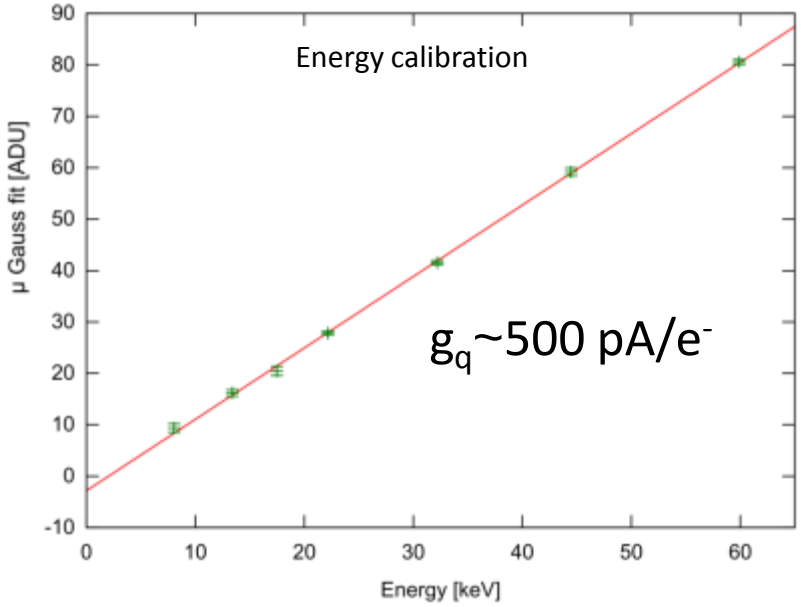
DEPFET Sensor Characterization

- Biasing optimization (HV, ClearGate, Drift)
- Laser scan
  Charge collection homogeneity
  In pixel studies
- Radioactive source
  System calibration



Homogeneous charge collection





Beam Tests

- DEPFET PXD6 extensively tested over the last campaigns
  120 GeV pions at CERN-SPS
  1-5 GeV electrons at DESY
  Magnetic field

- Sensor properties
  Charge collection homogeneity, operating points, efficiency, angular scans
  Various pixel sizes, gate lengths, clear structures, drift regions and pixel designs

- System related aspects
  Power supply prototypes
  DHH and ONSEN readout

Here, just an appetizer

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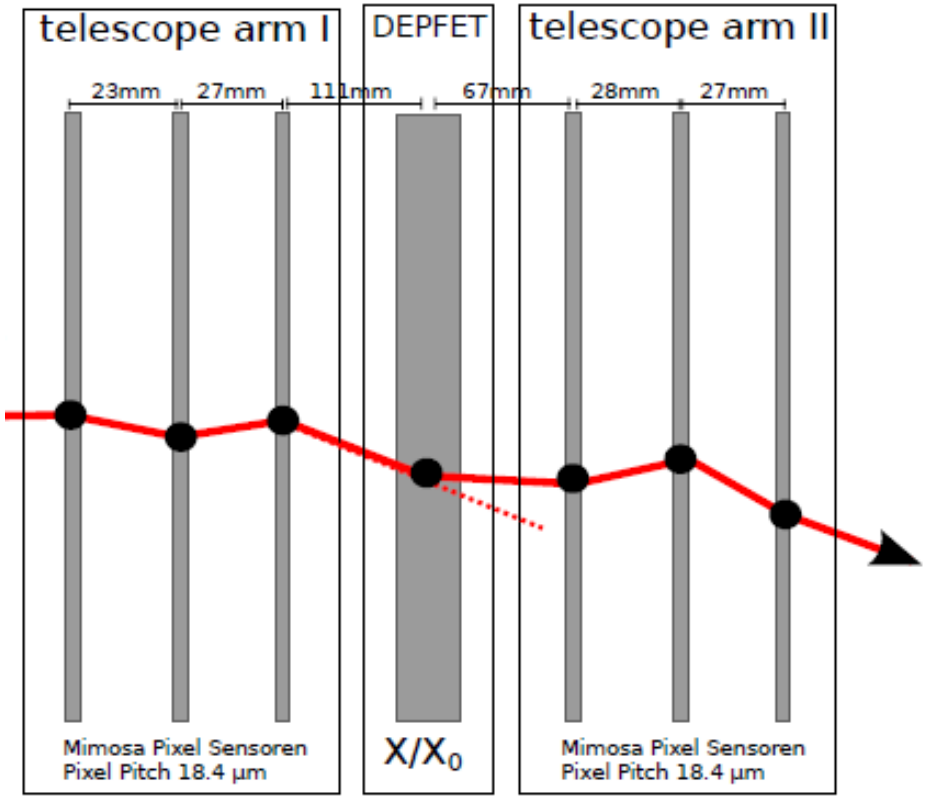
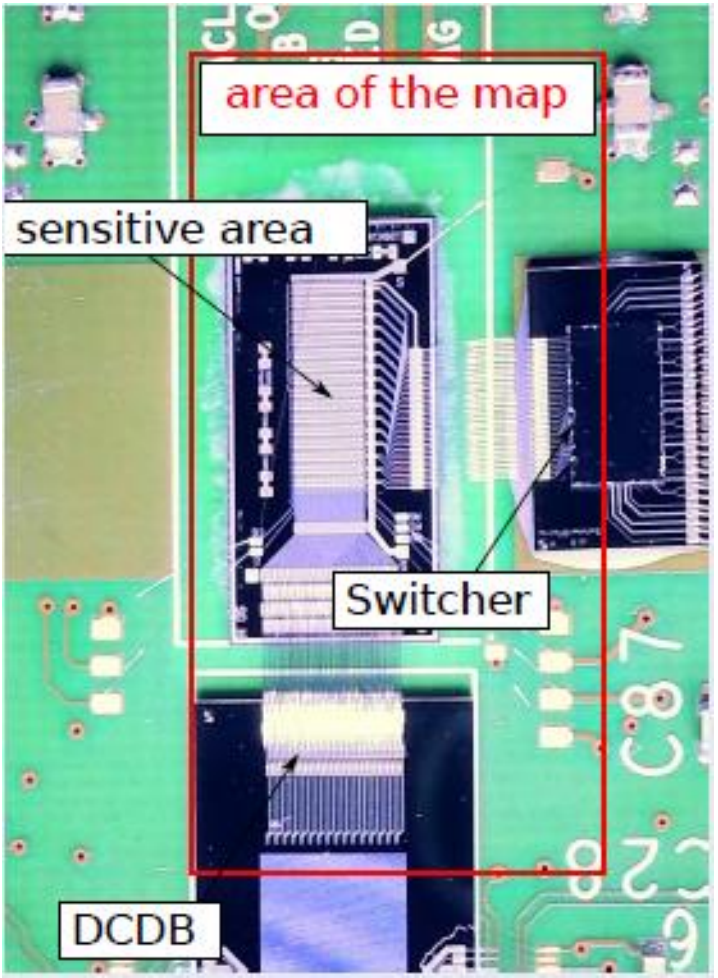
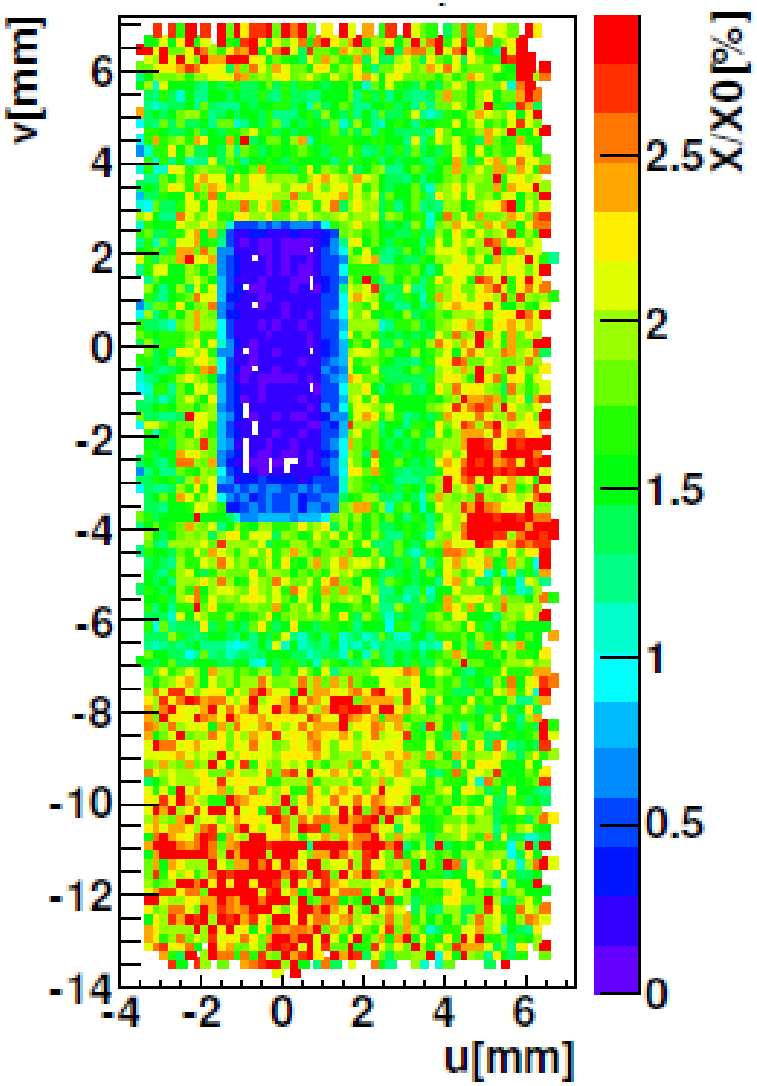
X/X0 Map Using Tracks

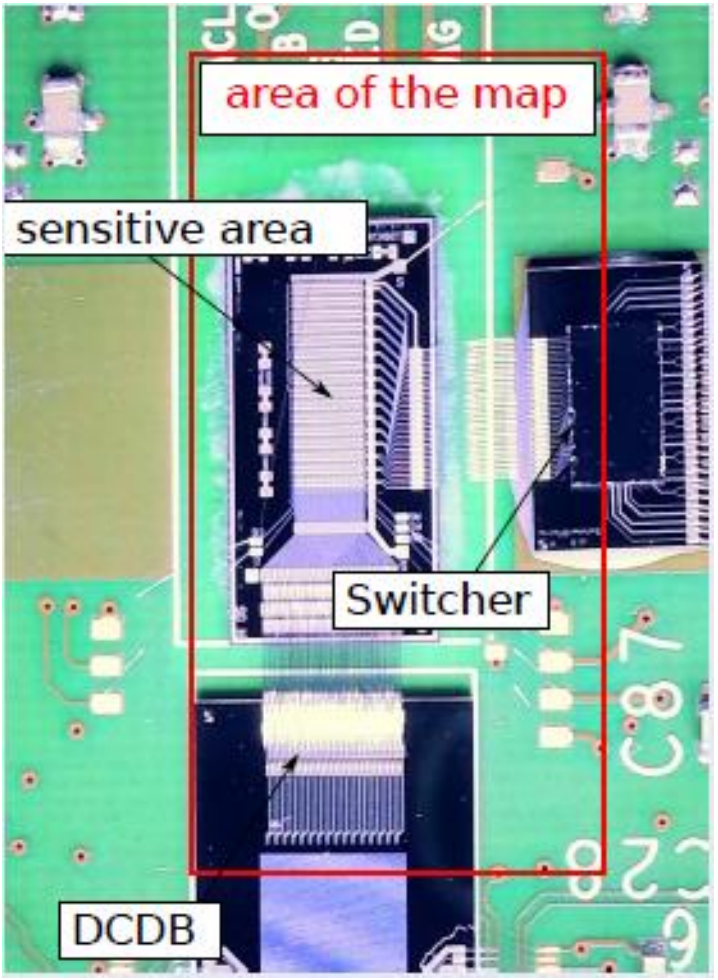




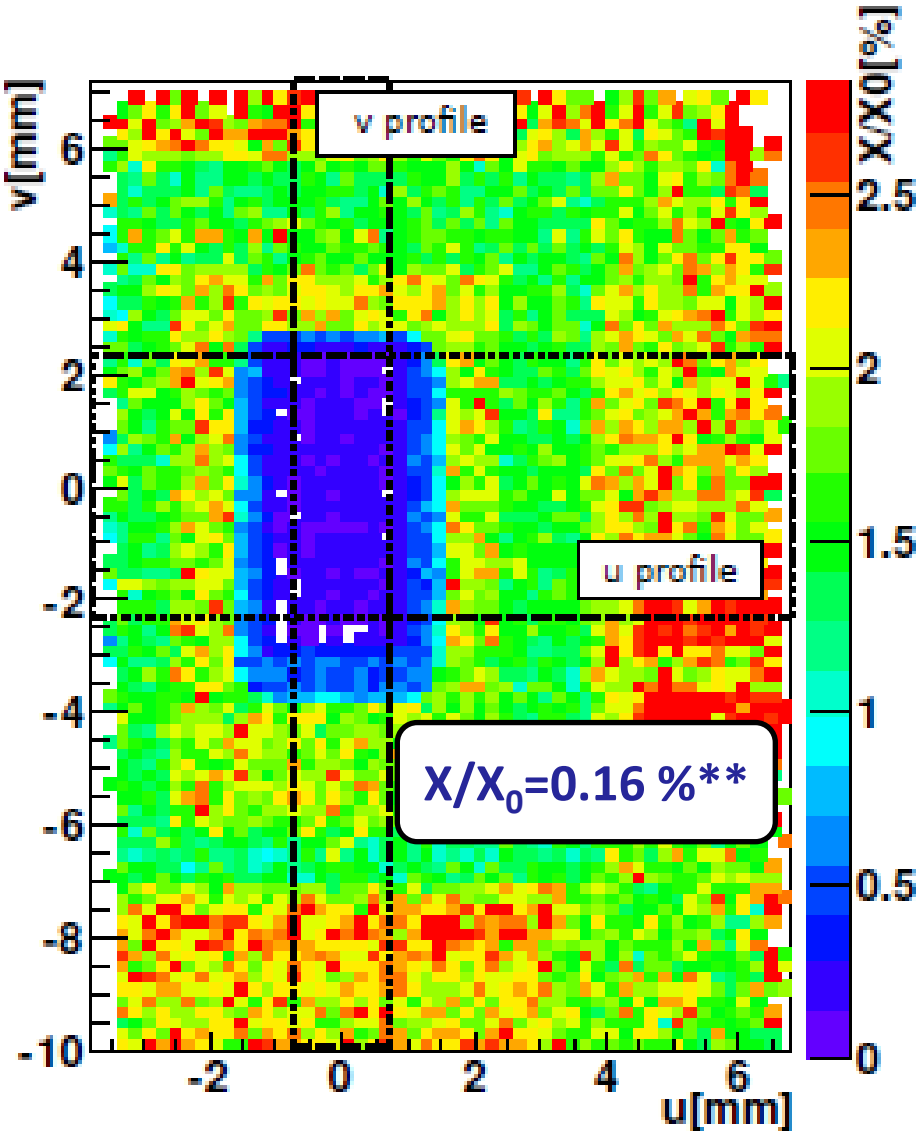
Use tracks from the telescope to reconstruct angle distributions from multiple Coulomb scattering on a central plane

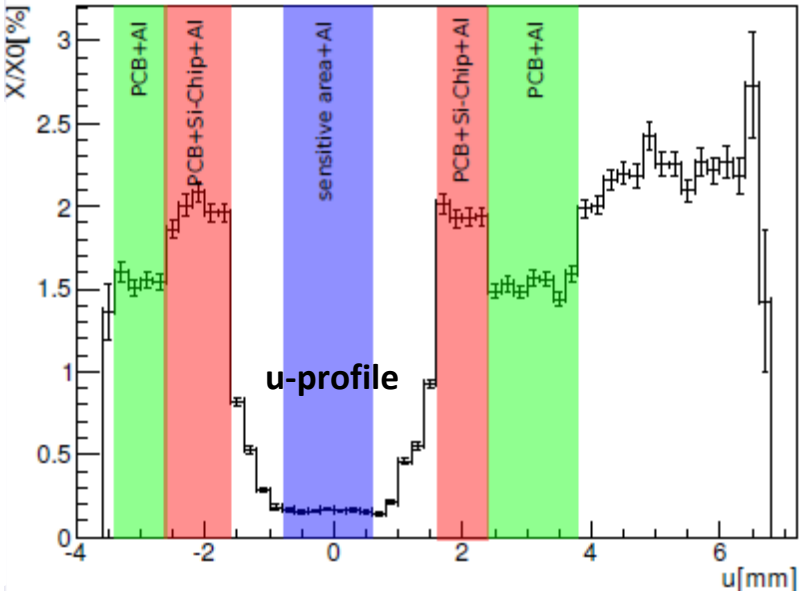
X/X0 Map Using Tracks

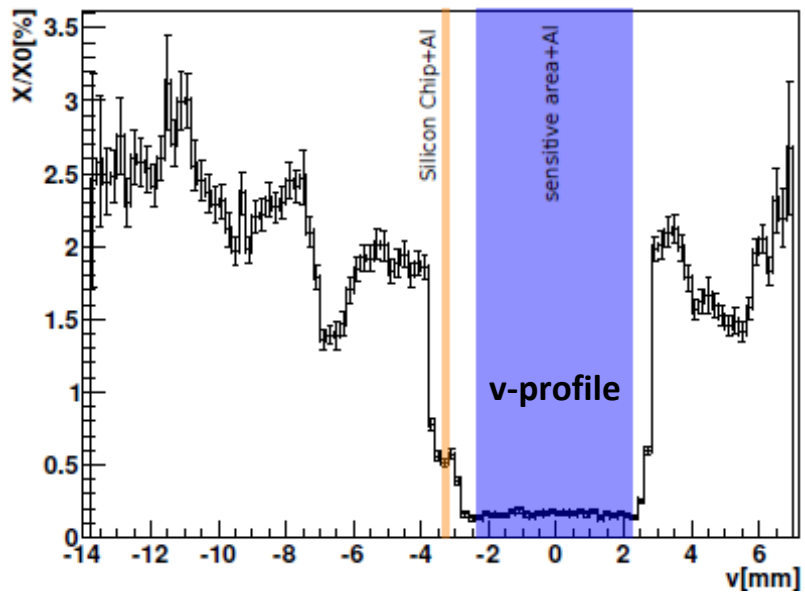




Material Budget Measurement



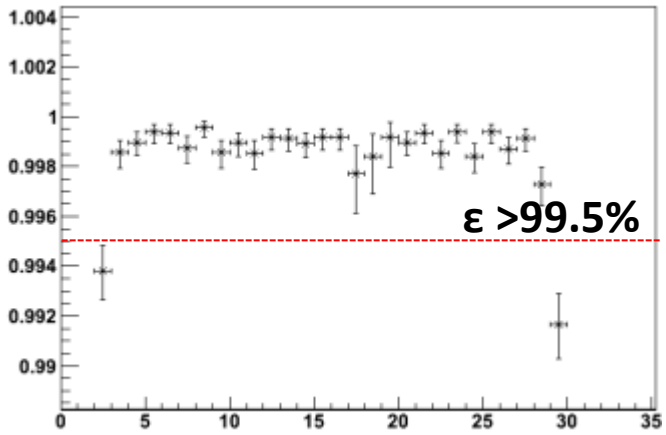


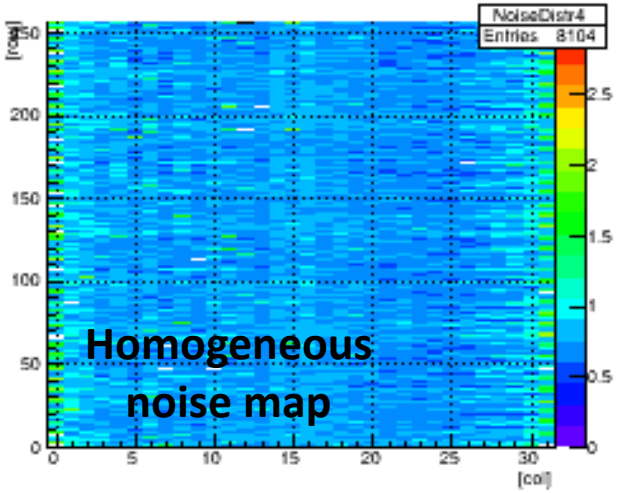


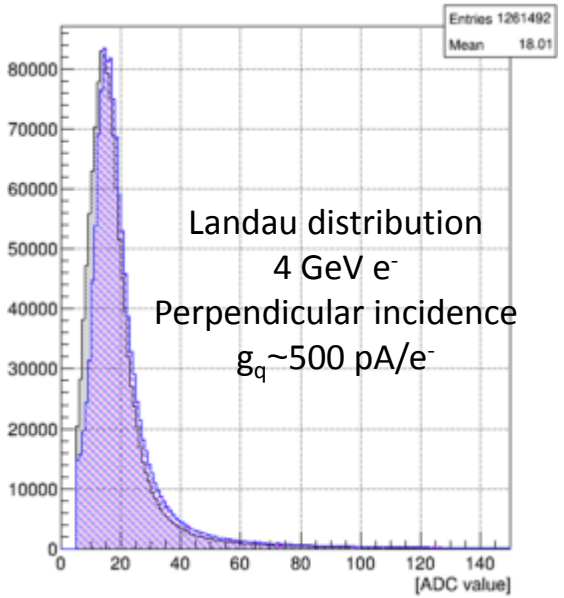
** Including (2x) Al windows

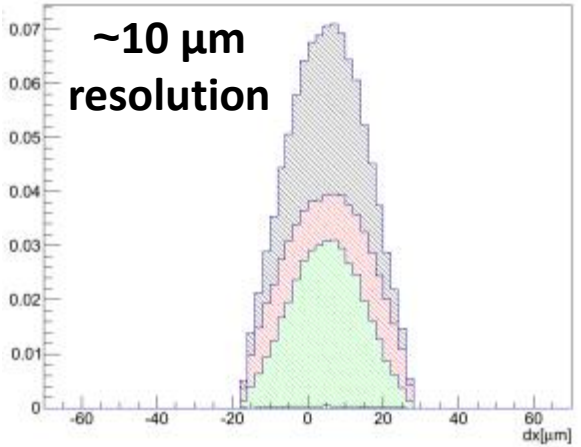
Summary Test Beam Campaigns

PXD6 Belle II design
Thin **50** µm sensor
Pitch 50x75 µm²
Targeted speed readout





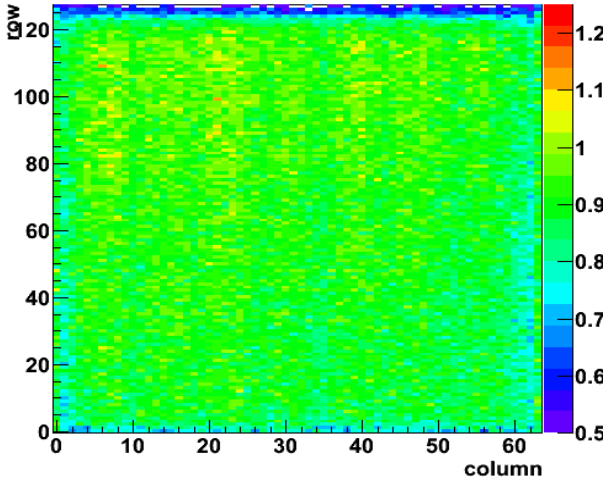


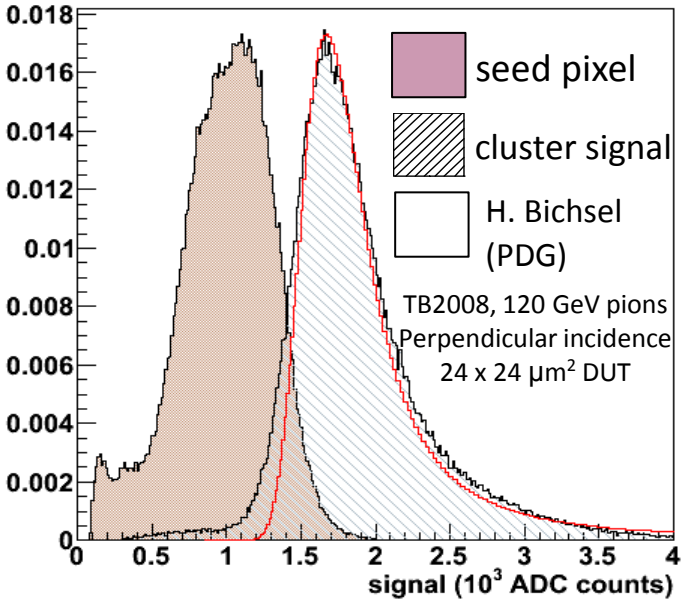


Prove of principle demonstrated in many test beam campaigns over the past years

PXD5 ILC Type DEPFET

Gain map: Deviation from average seed signal

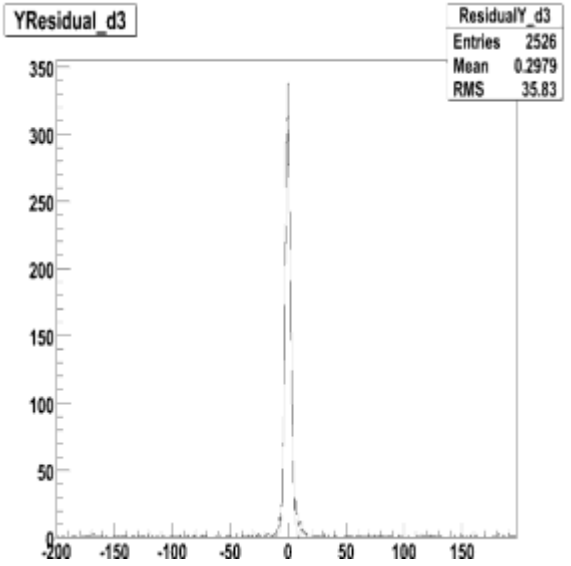




- 64x128, 24x24x450 µm^3 CCG, 6 µm (TB2008)
  g_q=363 pA/e$^-$

- 64x256, 20x20x**450** µm^3 CCG, 5 µm (TB2009)
  g_q~650 pA/e$^-$

- Resolution **σ~1 µm**, 20x20x**450** µm^3, analog readout with charge interpolation



ILC Design

→ Extensively tested

Latest Test Beam Campaign – Jan2014

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- PXD+SVD common test beam in January 2014
- Small sector of the close to final prototype detectors and ASICs
  PXD half ladder + 4 SVD single module layers
- Readout using the complete DAQ chain
- CO_2 cooling, slow control, environmental sensors
- Alignment, tracking algorithms, ROI with B=1 Tesla

- **Goal**: **System integration test**

The Belle II Vertex Detector

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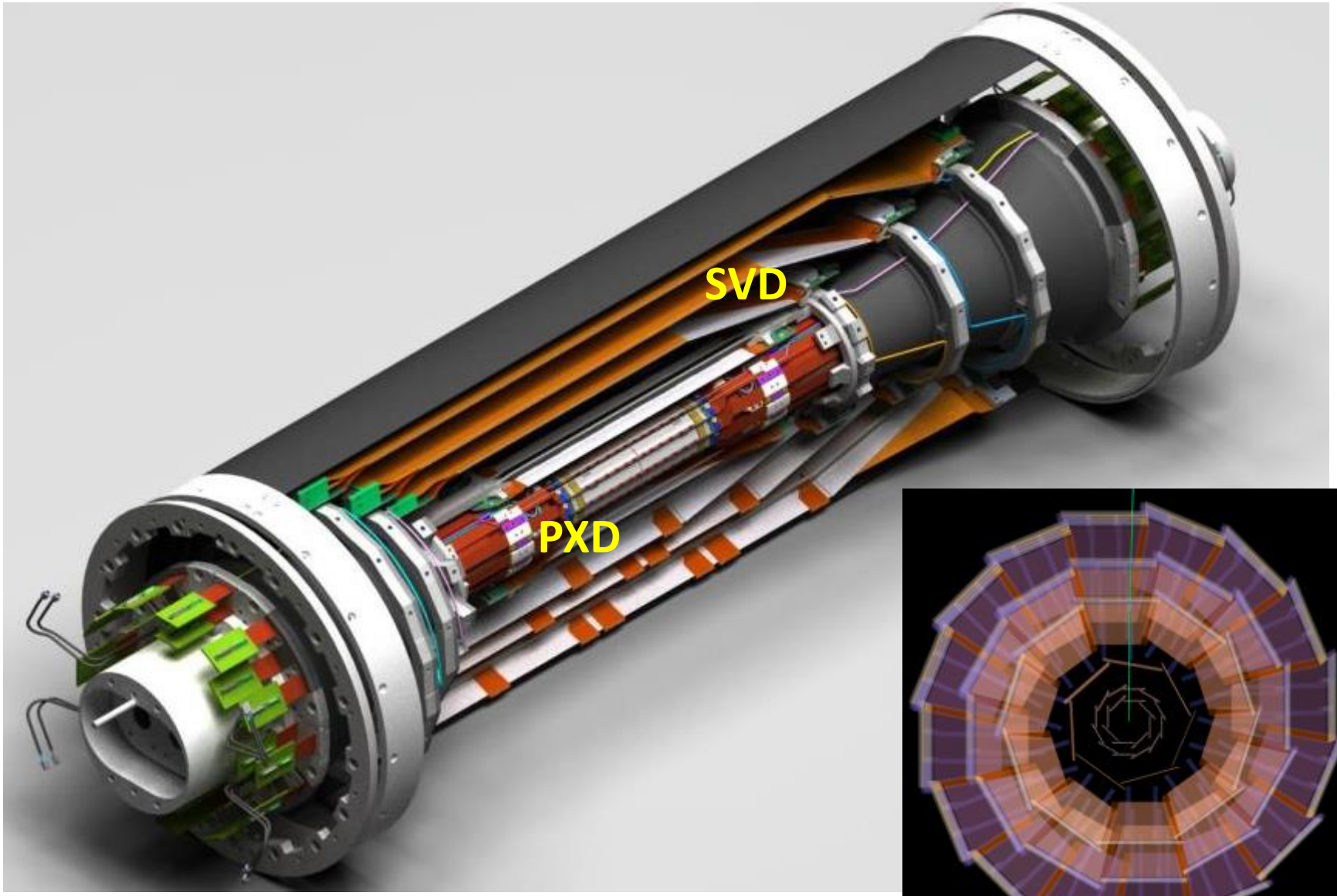

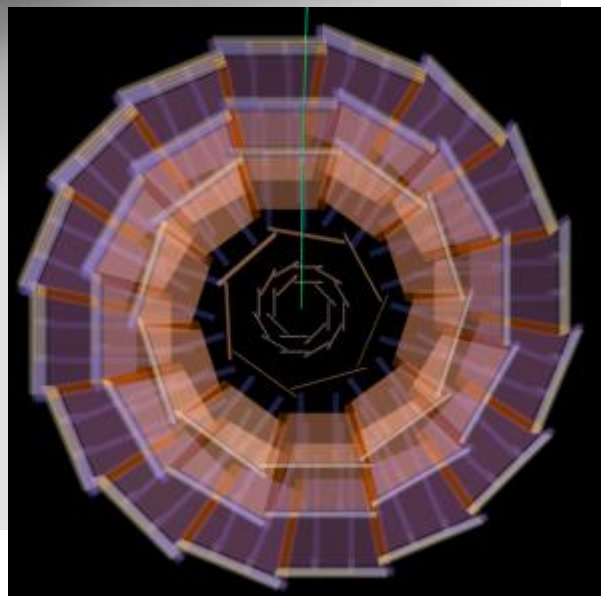

Test Beam Setup

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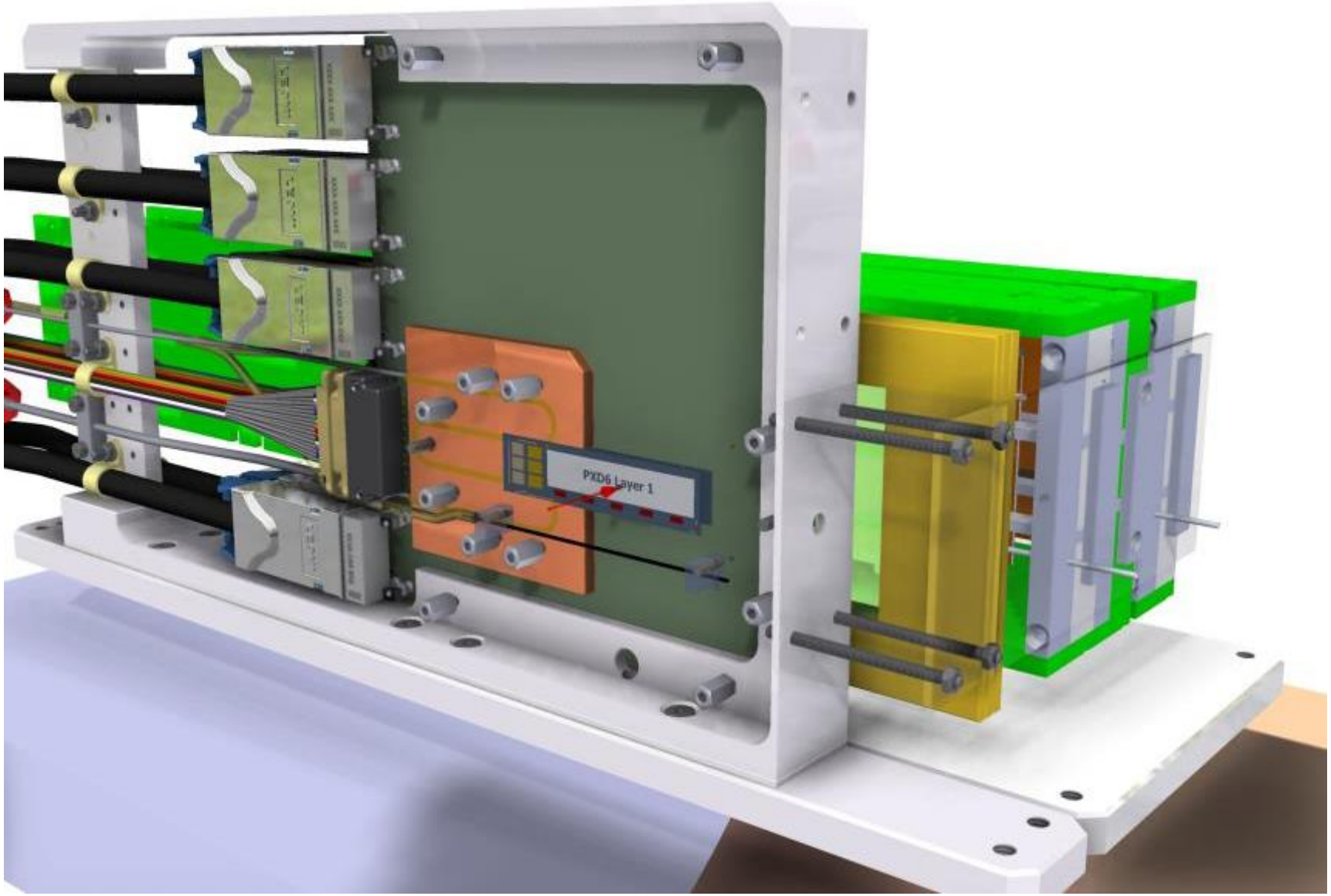
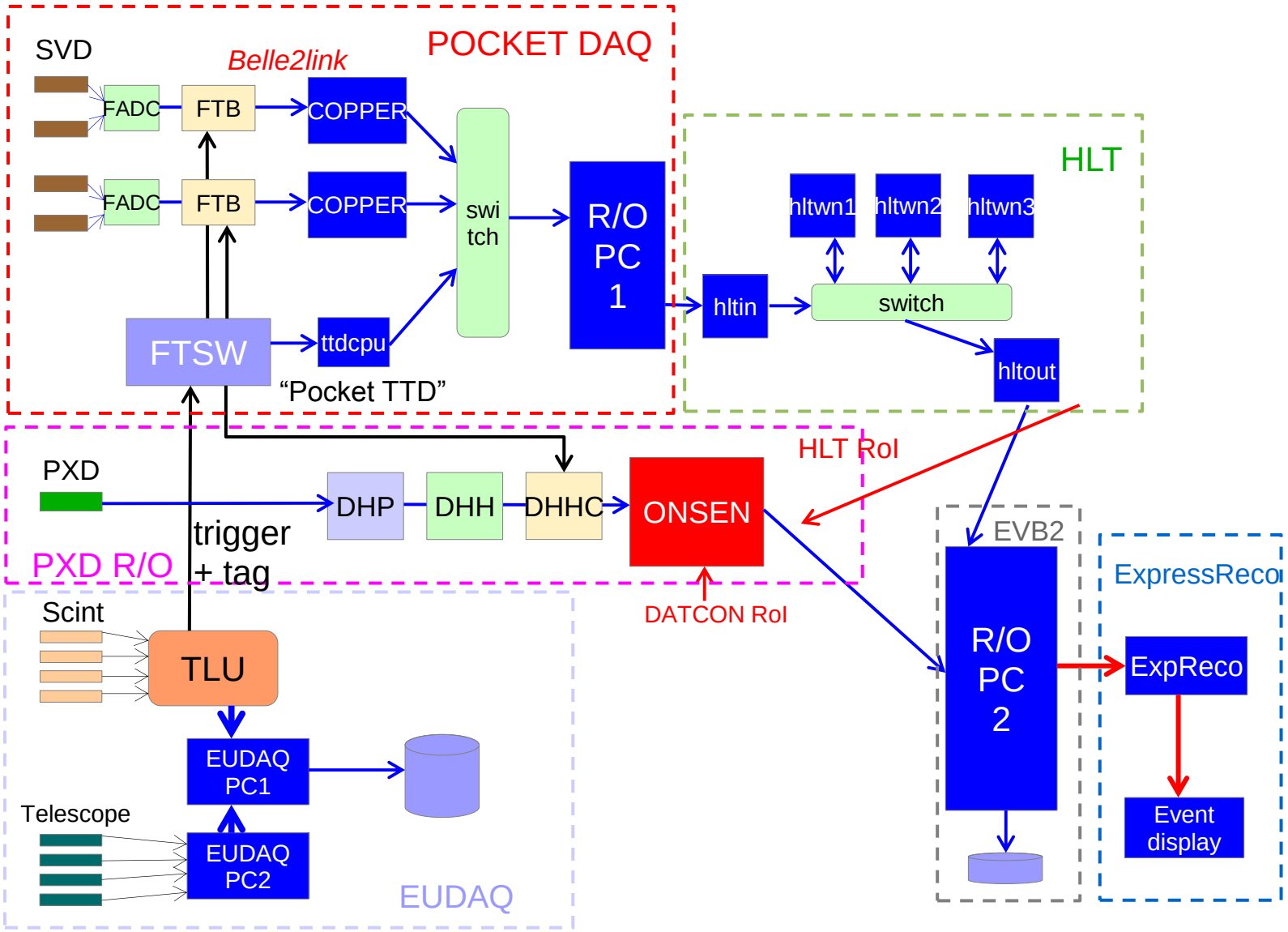
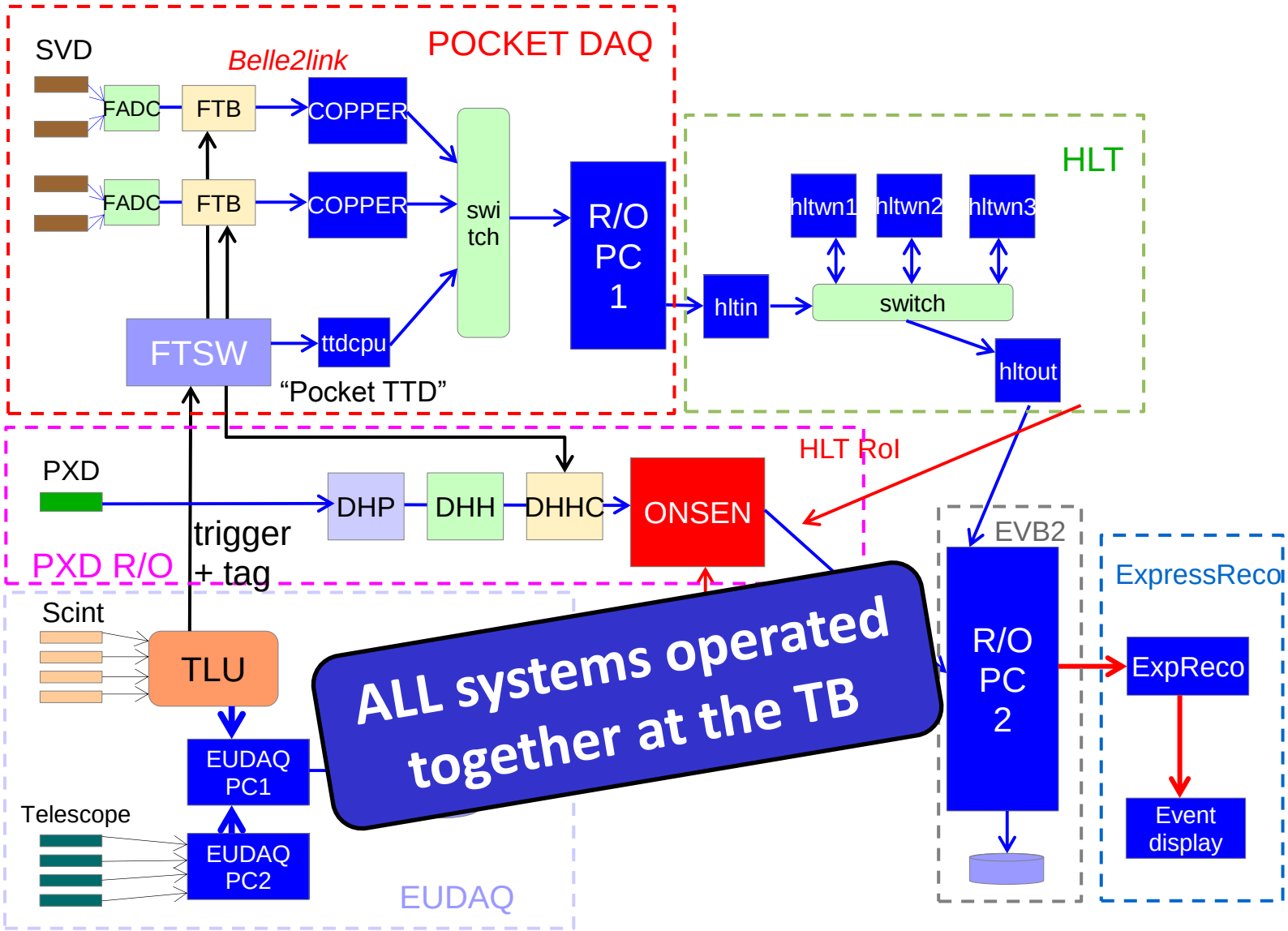


Test Beam DAQ Structure



Test Beam DAQ Structure



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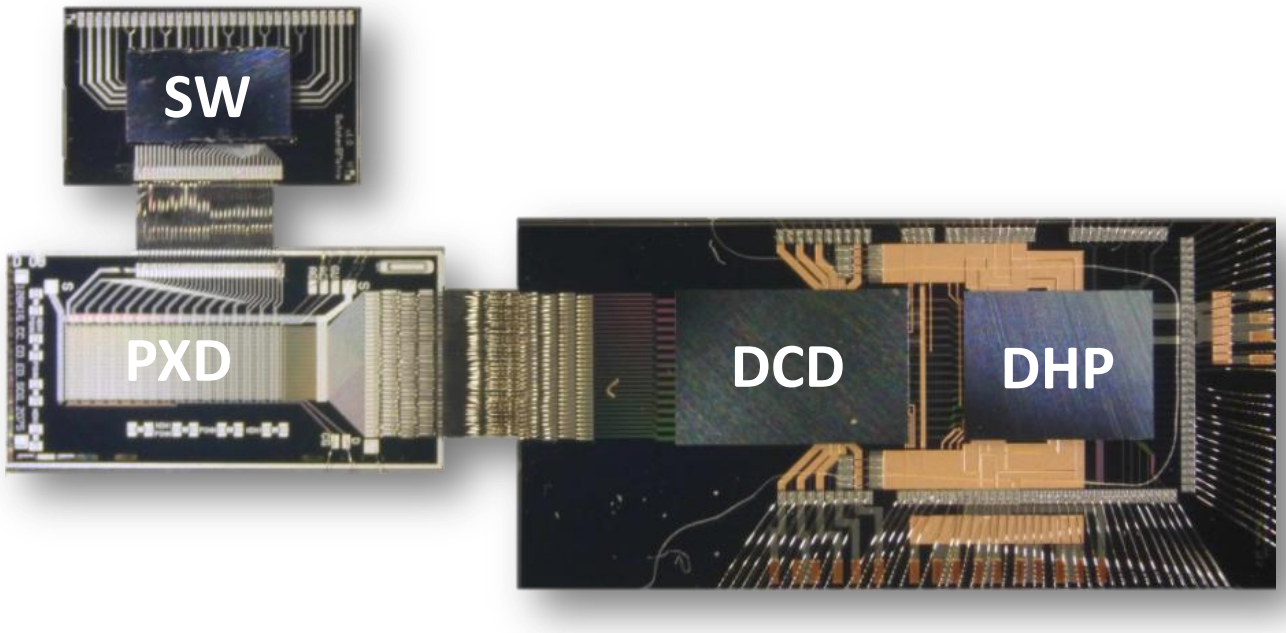
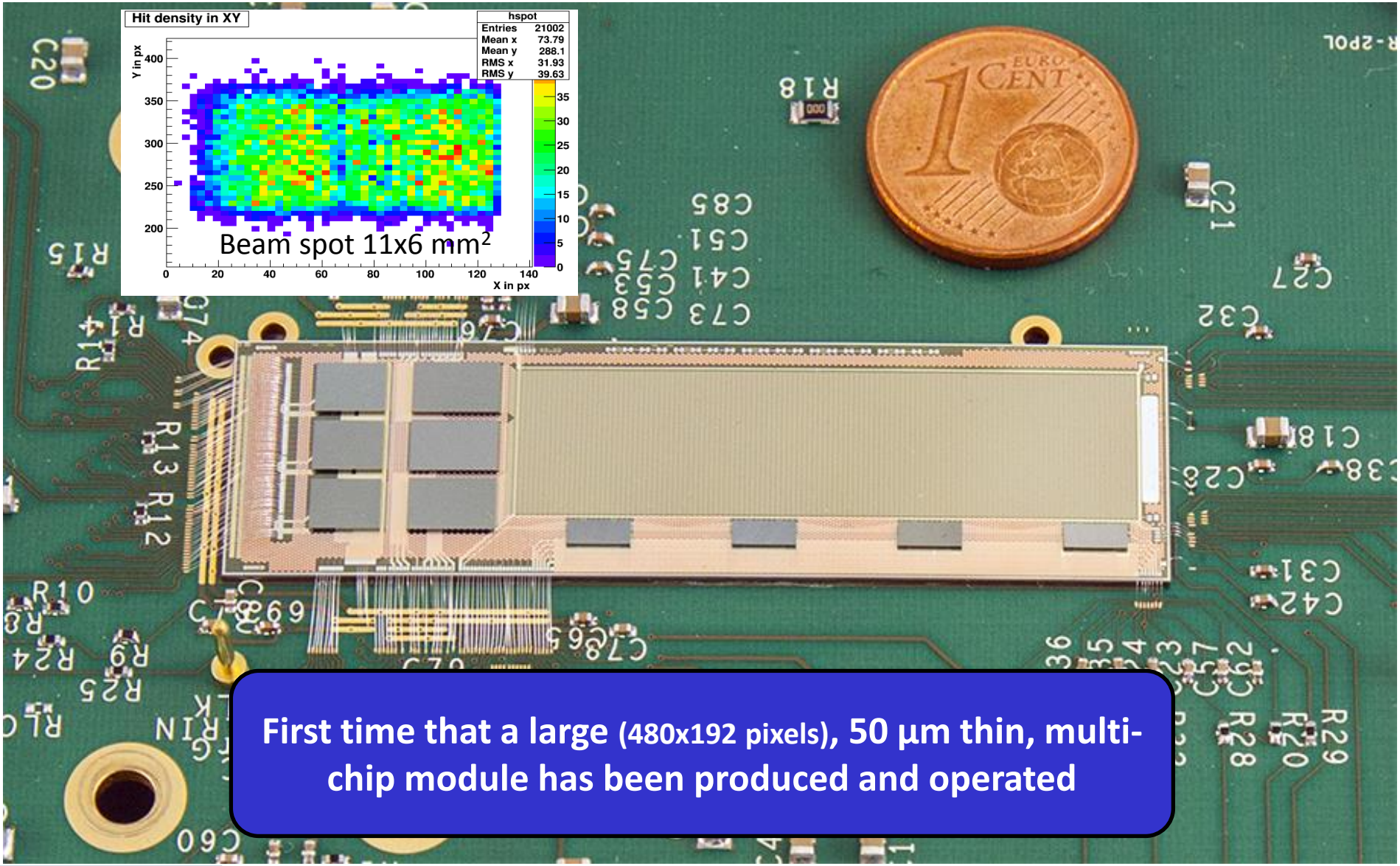
From this…



… to this



First time that a large (480x192 pixels), 50 µm thin, multi-chip module has been produced and operated

Test Beam Setup

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PXD DAQ

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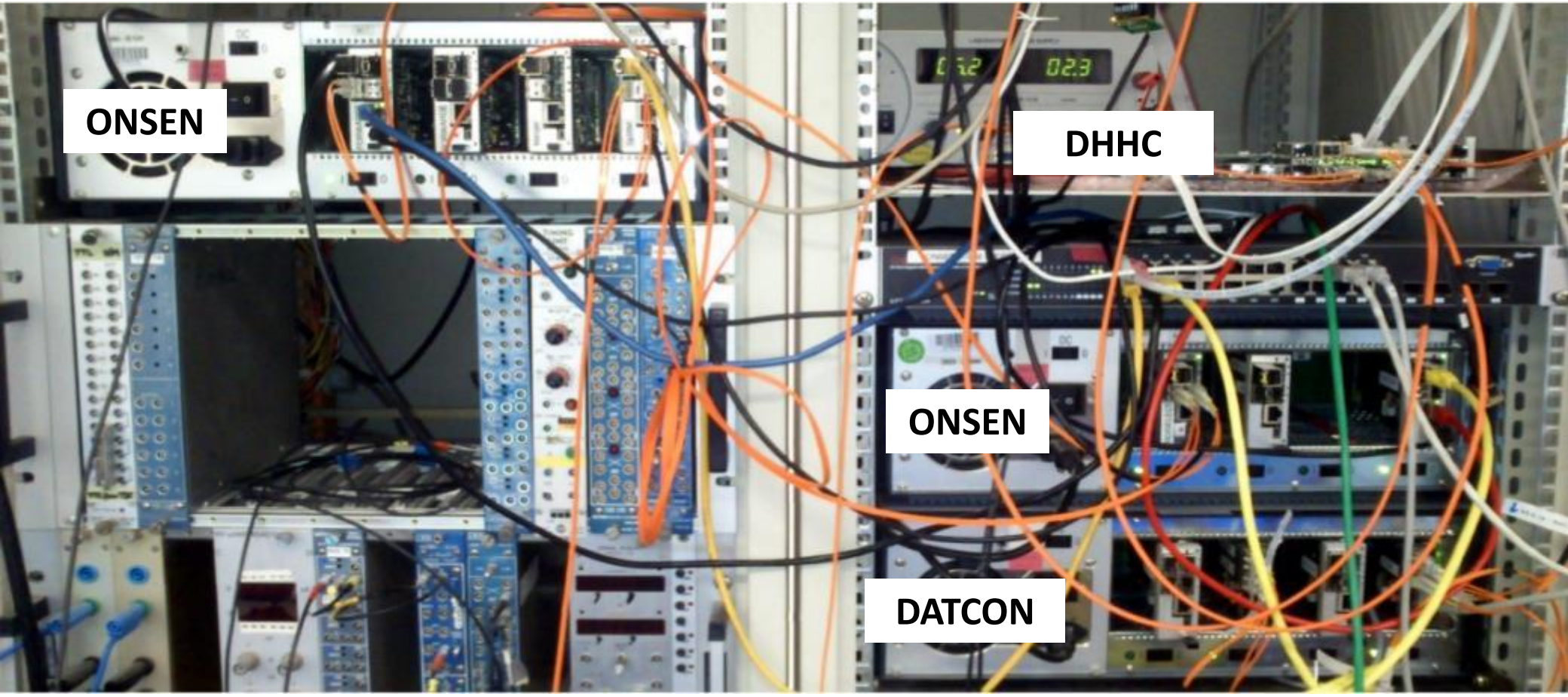
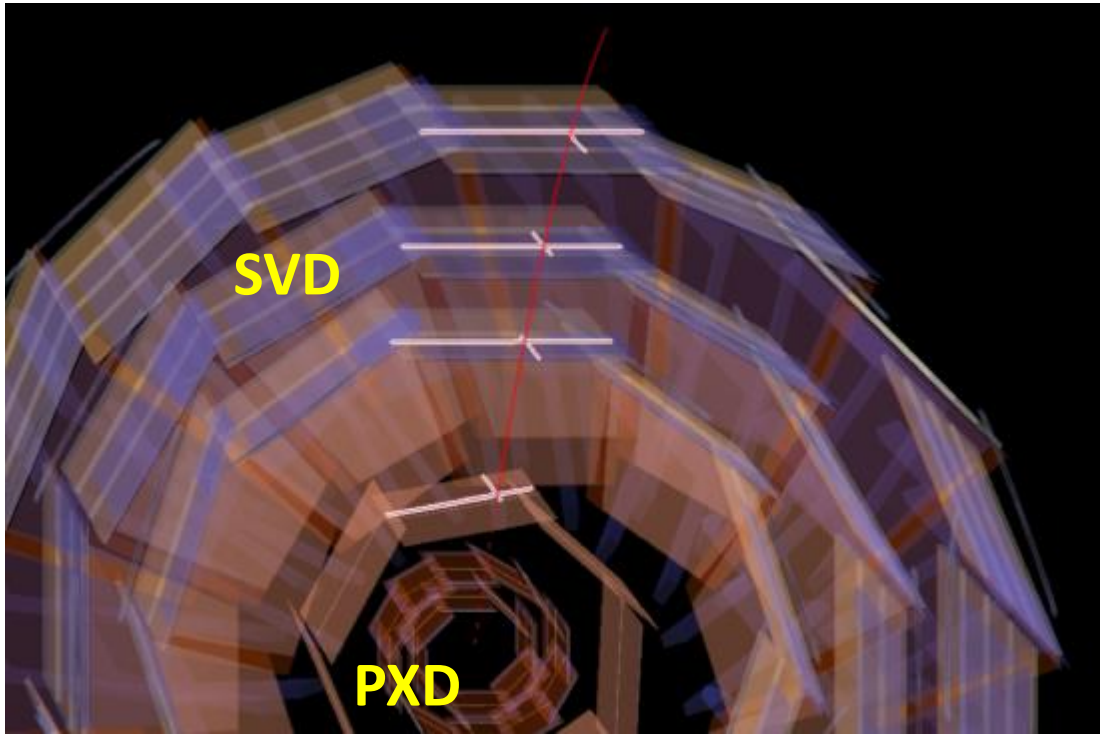
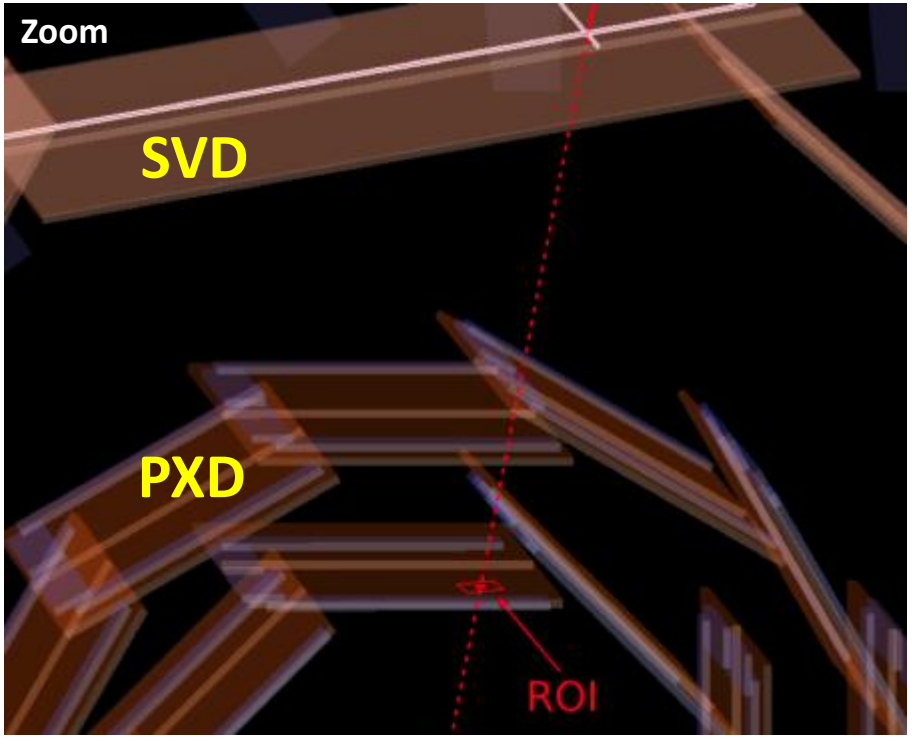


60 Million events recorded

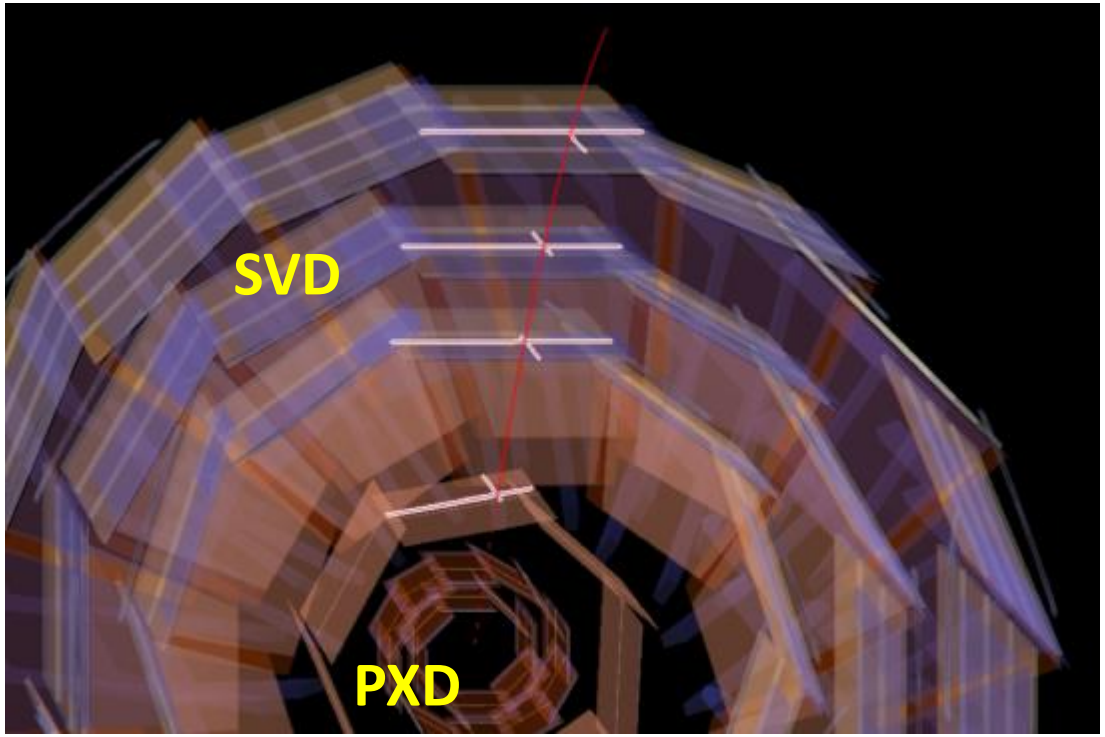
PXD Data Reduction

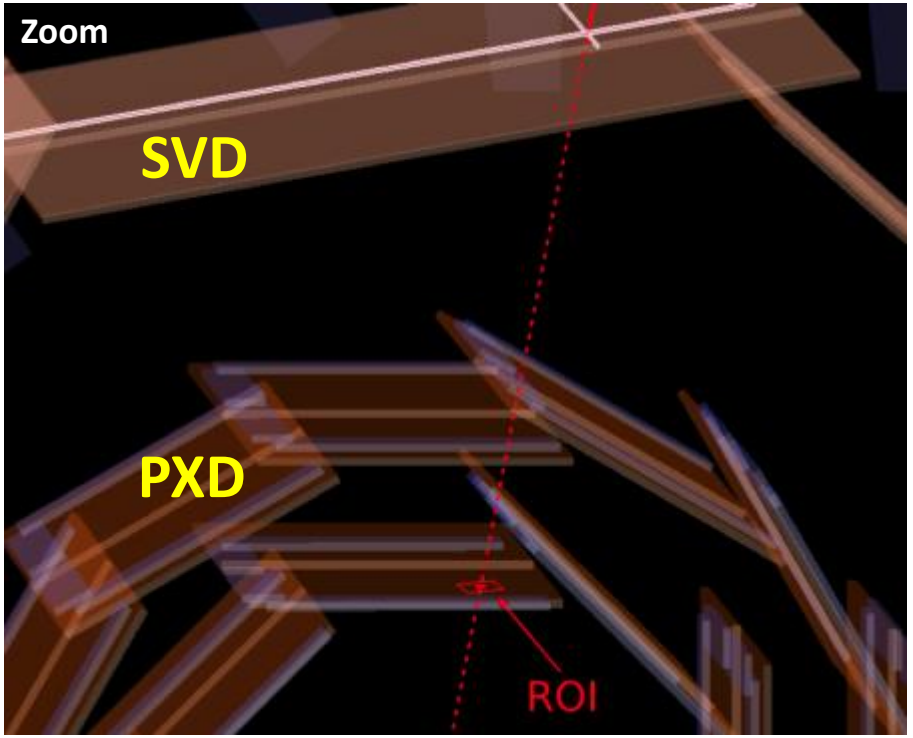




- Expected maximum occupancy 3%
- Total data rate >20 GB/s after zero suppression
- Data reduction (factor ≥10) needed for data storage
- Solution: region of interest (ROI) by track extrapolation from the outer detectors

PXD Data Reduction





- Expected maximum occupancy 3%
- Total data rate >20 GB/s after zero suppression
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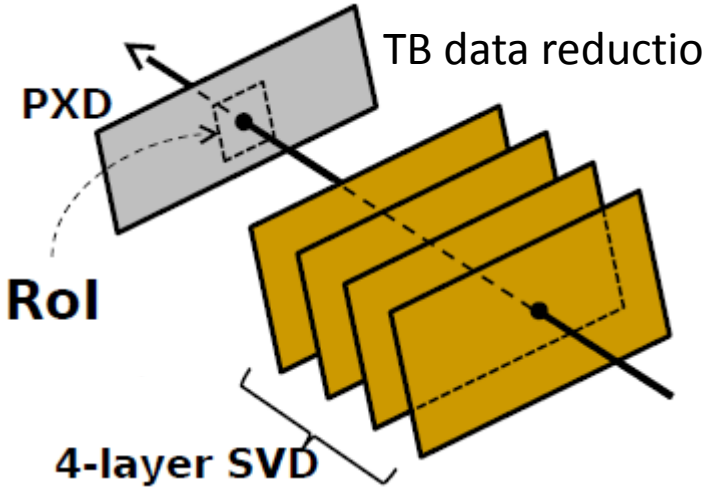
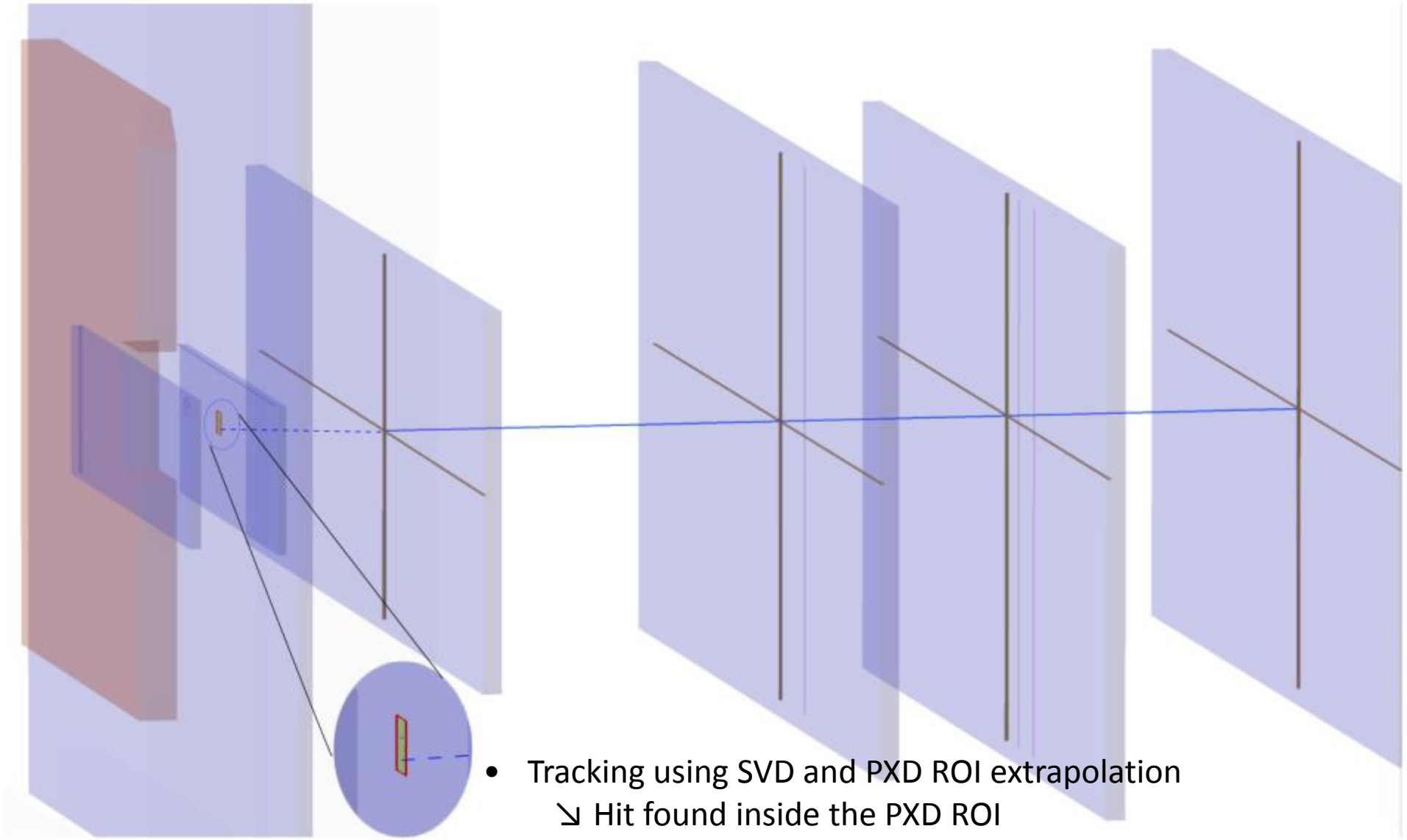
- Solution: region of interest (ROI) by track extrapolation from the outer detectors

TB data reduction scheme

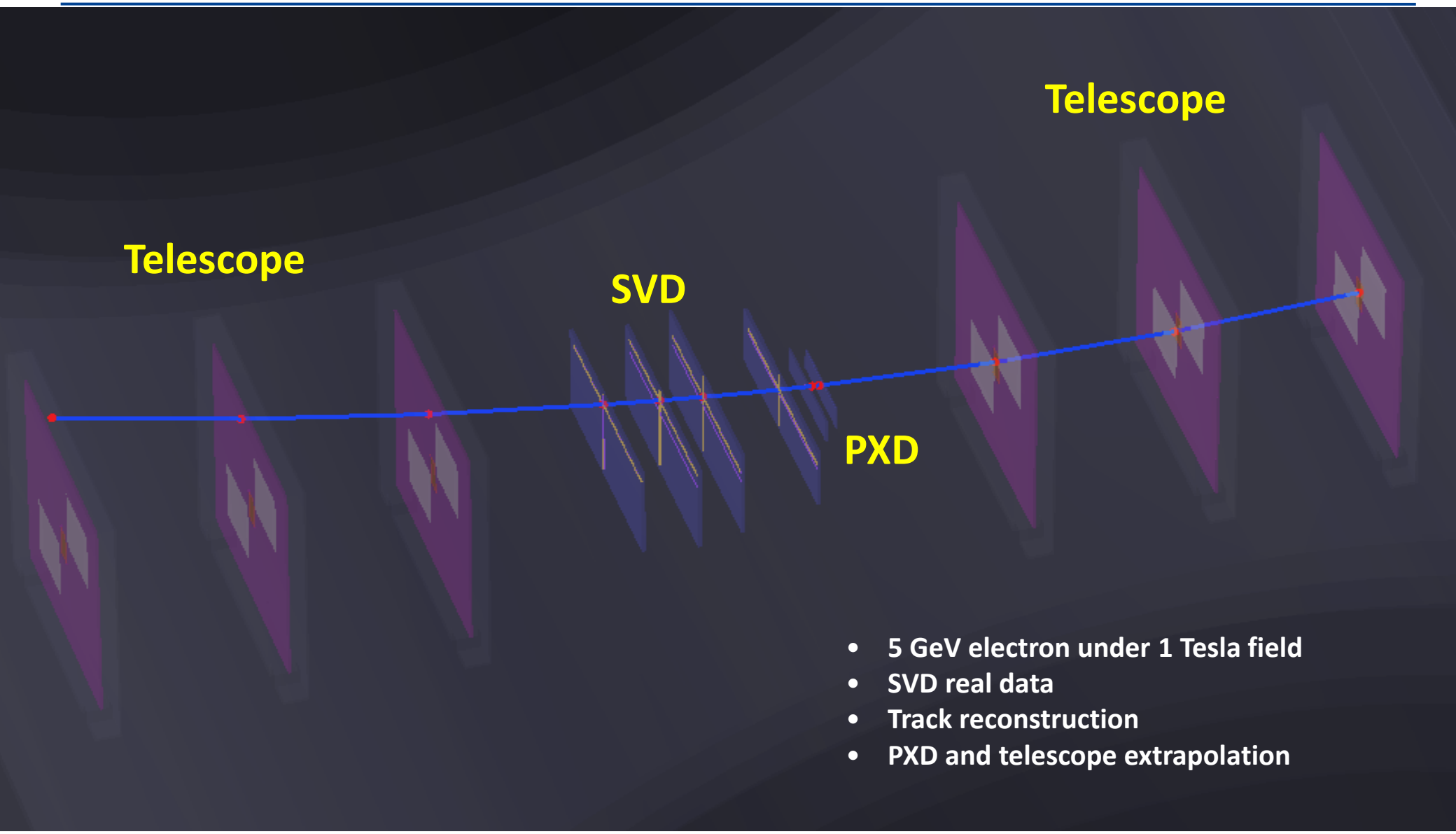


Region of Interest



- Tracking using SVD and PXD ROI extrapolation
  ↘ Hit found inside the PXD ROI
- Factor 6 data reduction → Further investigations ongoing

Event Display



- 5 GeV electron under 1 Tesla field
- SVD real data
- Track reconstruction
- PXD and telescope extrapolation

DESY News

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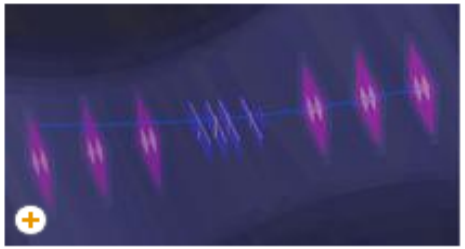
03.02.2014

Milestone for Belle II: Test beam measurements at the vertex detector successfully completed

Last Friday, a sophisticated test beam campaign has been completed at DESY, which provided important data for the operation of the vertex detector in the Belle II experiment. Over a period of four weeks, an international group of more than 30 scientists for the first time submitted prototypes of all components of the detector simultaneously to an integrated system test and checked the functions of the detector together with its entire intricate infrastructure. "The result is more than encouraging," said DESY project leader Carsten Niebuhr. "We were able to thoroughly test all aspects, including cooling with carbon dioxide, complex data taking and even the alignment of the detector layers – all this in a strong magnetic field, just as it will later take place in the real experiment." As the test is extremely important for the Belle II Collaboration, spokesman Tom Browder (University of Hawaii) came to Europe to observe the experiments first-hand. He too was very pleased with the result: "This 'mother of all beam tests' was really a big success. The conditions, support and infrastructure here at DESY perfectly matched our requirements for such a complex test."



The Belle II experiment at the SuperKEKB accelerator in Japan, which will start operating in 2016, aims to solve one of the great mysteries of particle physics; that is, why the universe today is filled almost only with matter,although in the big bang, matter and antimatter should have been created in equal amounts.

Summary

- The DEPFET Collaboration is developing utra-transparent pixel sensors with integrated amplification

- The good performance of the DEPFET detector system in terms of SNR, spatial resolution, readout speed is demonstrated

- The Belle II PXD boosted the development of DEPFET detectors
  → Direct benefit towards the ILC-VXD project (ILD-VXD layer concept '*engineered*')

- Building a real system: Every detail (although not covered here) is being considered
  → Cooling, mechanics, DAQ, …

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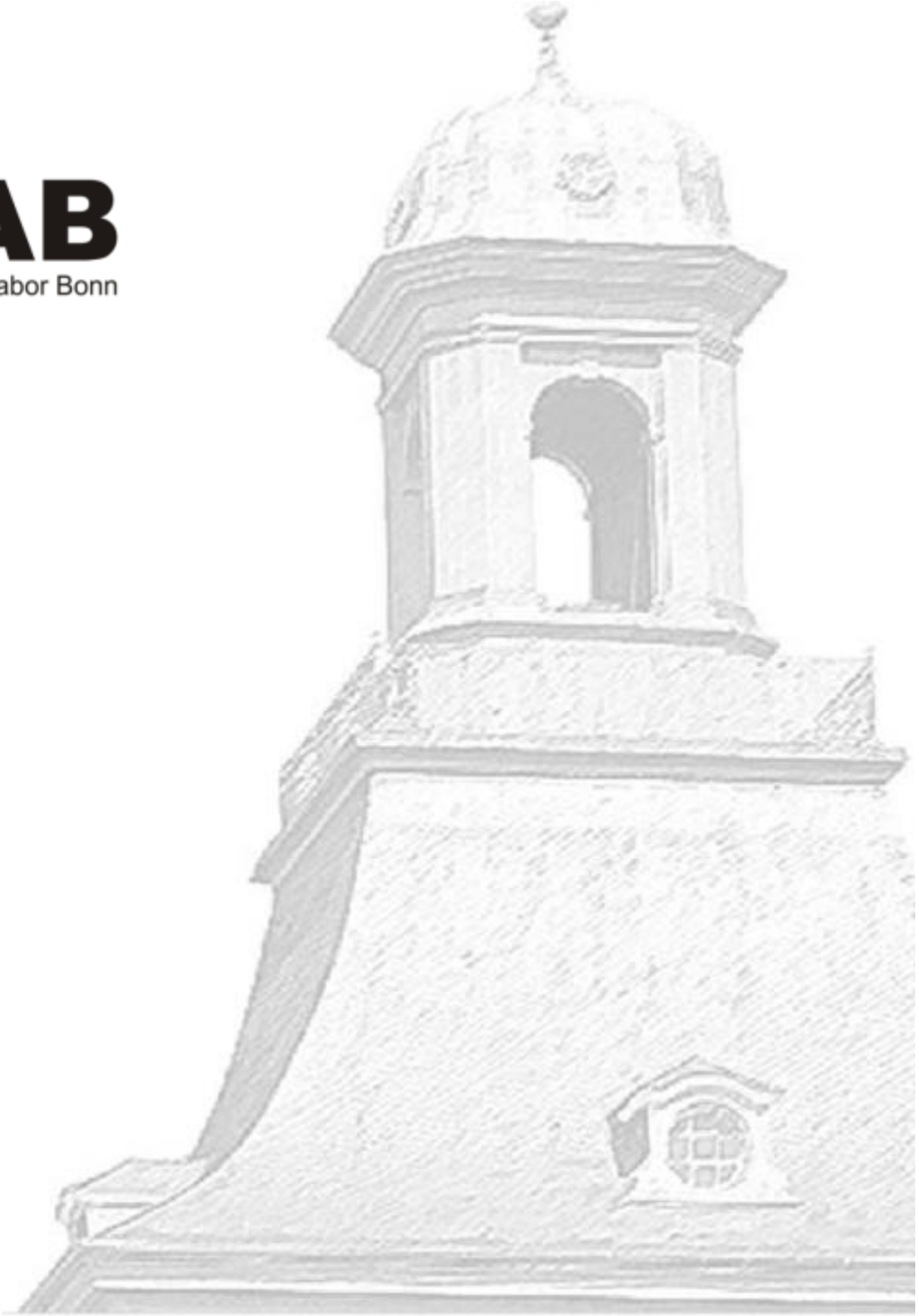
SI LAB
Silizium Labor Bonn



Thank you

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PXD Power Supply

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Powersupply
P03 Overview

ERROR

$(DEVICE) Disconnecte
Disconnecte

ENABLED CONNECTED **INITIAL** OVP THERMAL UPS Emergency Shutdown

	Set Current	Set Voltage	Regulator Status	Voltage at Regulator	Voltage at Load	Current
NOT_USED_1	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_2	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_3	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_4	0 mA	0 mV	1	0 mV	0 mV	0 mA
NOT_USED_7	0 mA	0 mV	0	3 mV	16 mV	1 mA
NOT_USED_8	0 mA	0 mV	0	9 mV	1 mV	6 mA
buffer	20 mA	2200 mV	1	2215 mV	2206 mV	8 mA
bulk	10 mA	17000 mV	1	17027 mV	16998 mV	0 mA
ccg	10 mA	5000 mV	1	5234 mV	5009 mV	0 mA
clear-off	20 mA	10000 mV	1	10225 mV	9990 mV	-10 mA
clear-on	50 mA	19000 mV	1	19304 mV	19029 mV	12 mA
dcd-amplow	400 mA	350 mV	1	414 mV	348 mV	-322 mA
dcd-avdd	900 mA	1900 mV	1	2768 mV	1907 mV	874 mA
dcd-dvdd	600 mA	1800 mV	1	2516 mV	1803 mV	509 mA
dcd-refin	100 mA	1050 mV	1	1447 mV	1052 mV	72 mA
dhp-core	200 mA	1200 mV	1	1622 mV	1196 mV	92 mA
dhp-io	150 mA	1800 mV	1	2199 mV	1795 mV	57 mA
drift	20 mA	4000 mV	1	4003 mV	4029 mV	0 mA
gate-off	20 mA	10000 mV	0	9003 mV	9003 mV	13 mA
gate-on	20 mA	2550 mV	1	2782 mV	2552 mV	-8 mA
hv	10 mA	-12000 mV	1	-12046 mV	-54 mV	0 mA
polycover	20 mA	4900 mV	1	4902 mV	4919 mV	-2 mA
source	70 mA	7000 mV	1	7361 mV	7000 mV	40 mA
sw-dvdd	100 mA	1800 mV	1	2042 mV	1804 mV	12 mA

- EPICS interface
- Interlock to CO_2 cooling plant
- Similar performance as with bench PS

CO_2 Cooling Plant

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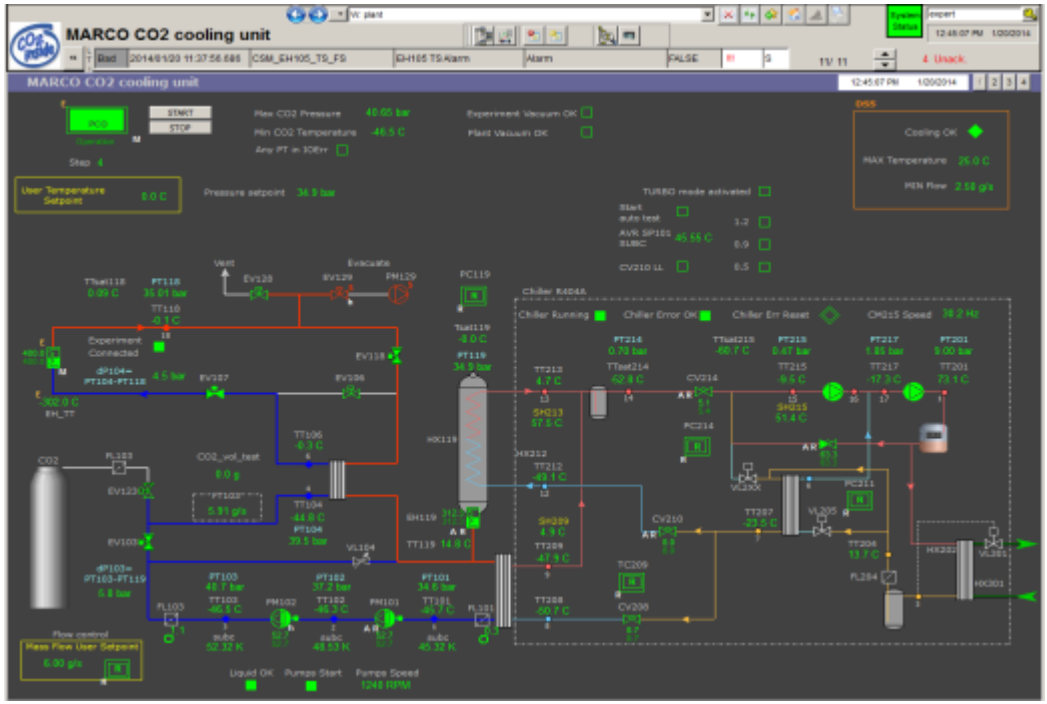

- Connected (only) to the SVD
- Additional close loops with heaters for tuning

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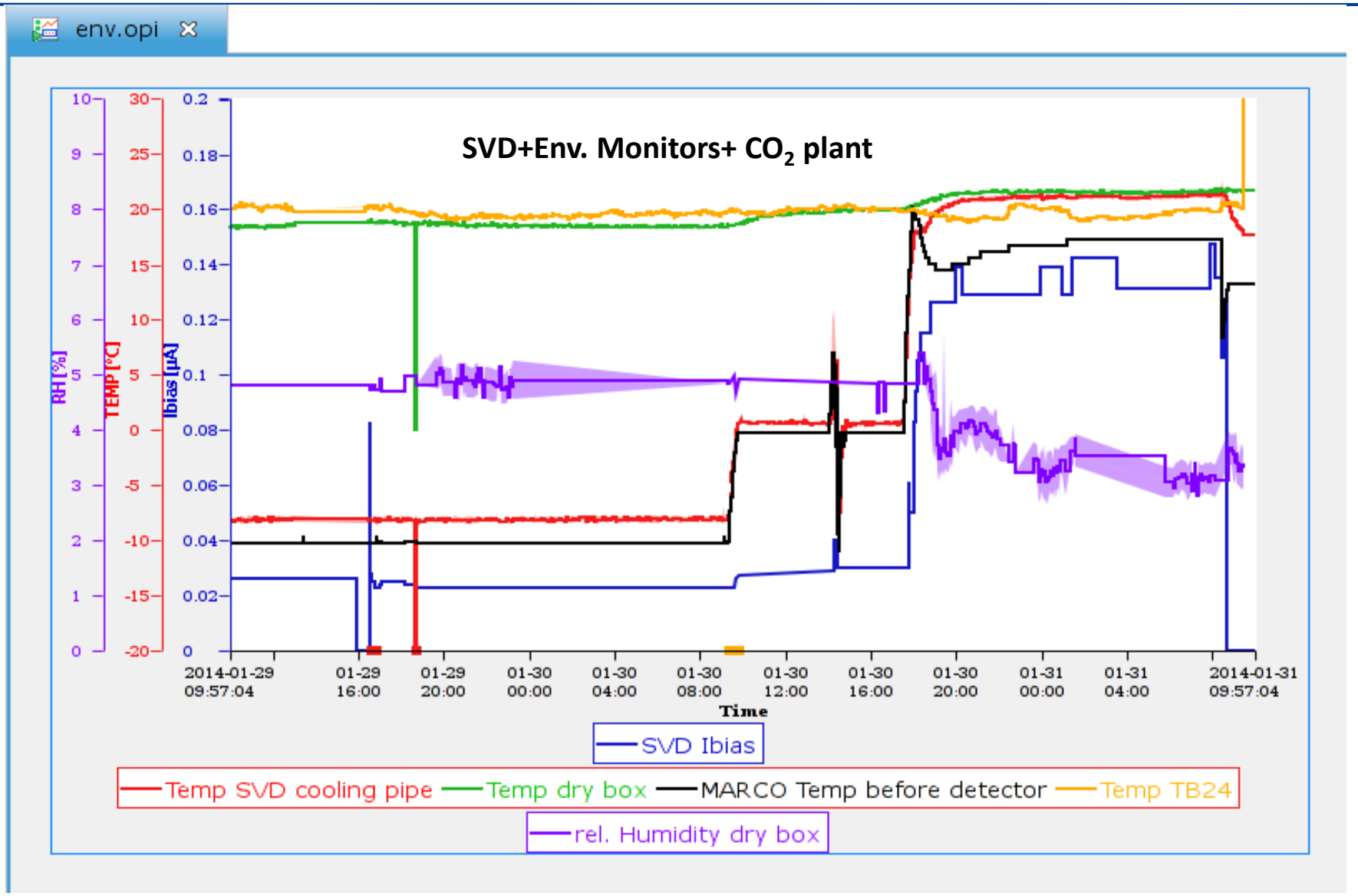
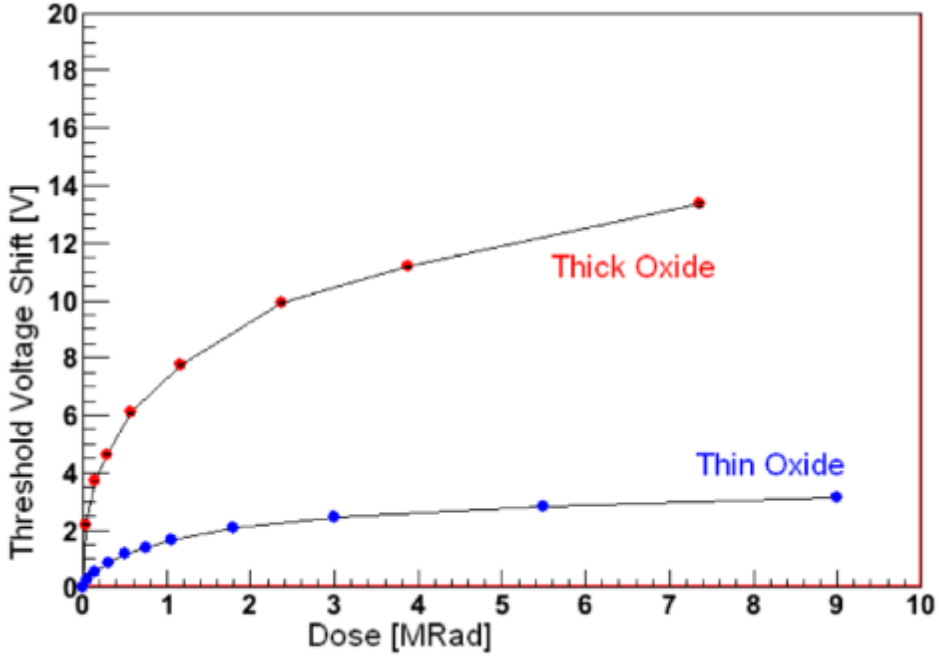
Global Slow Control Integration

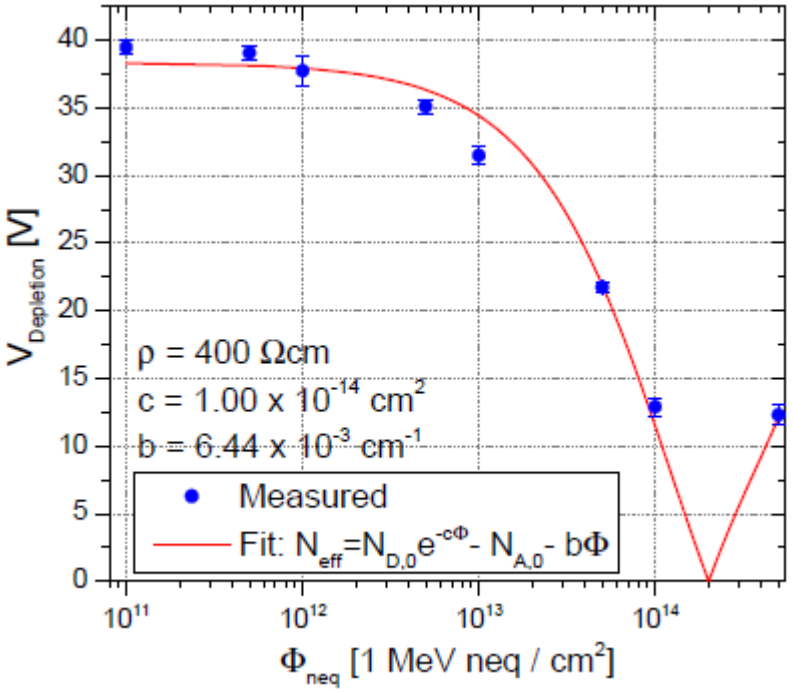


Radiation Damage in DEPFETs

- Surface damage



- Bulk damage



Sensor Deformation

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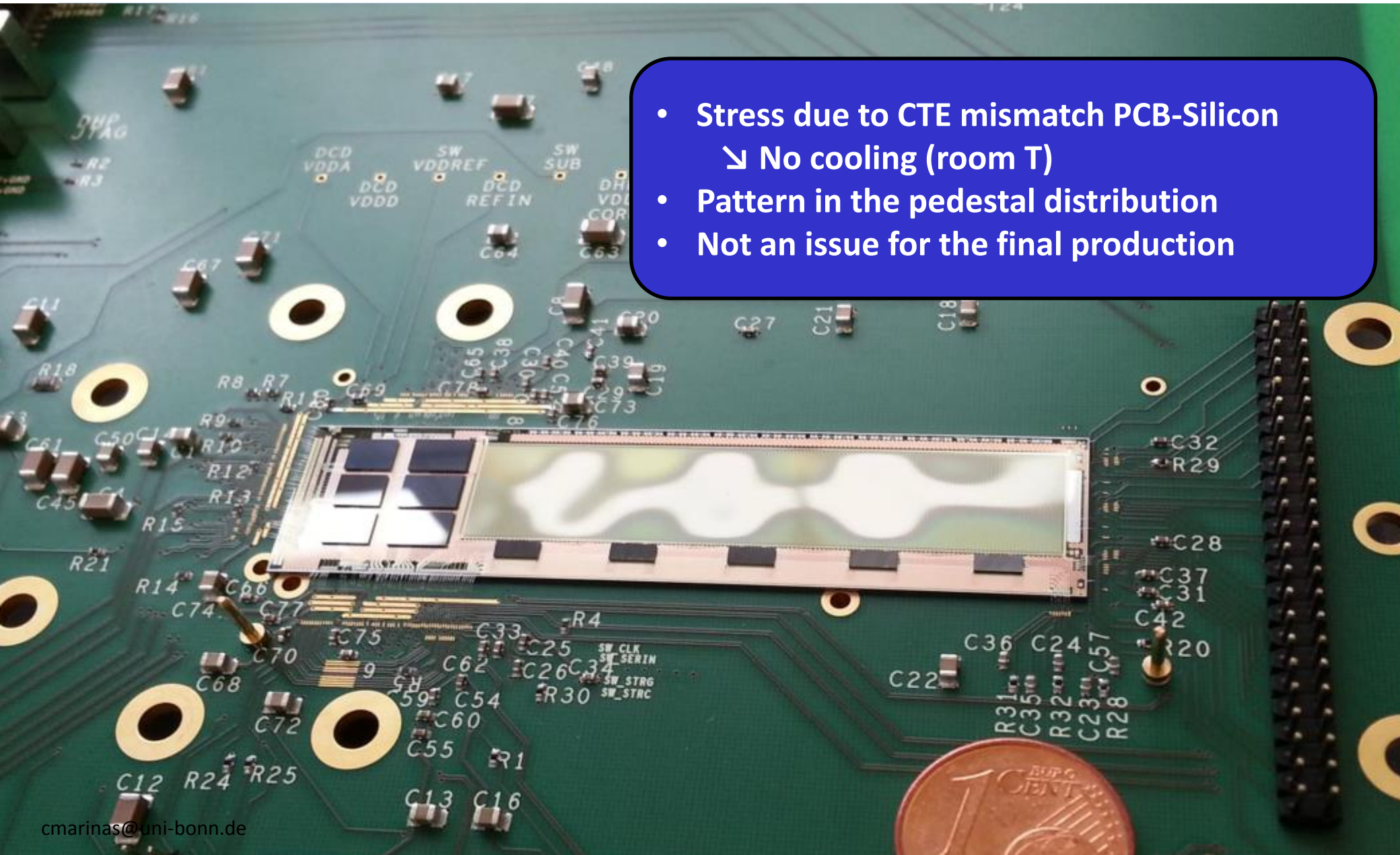

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SVD Layer 3

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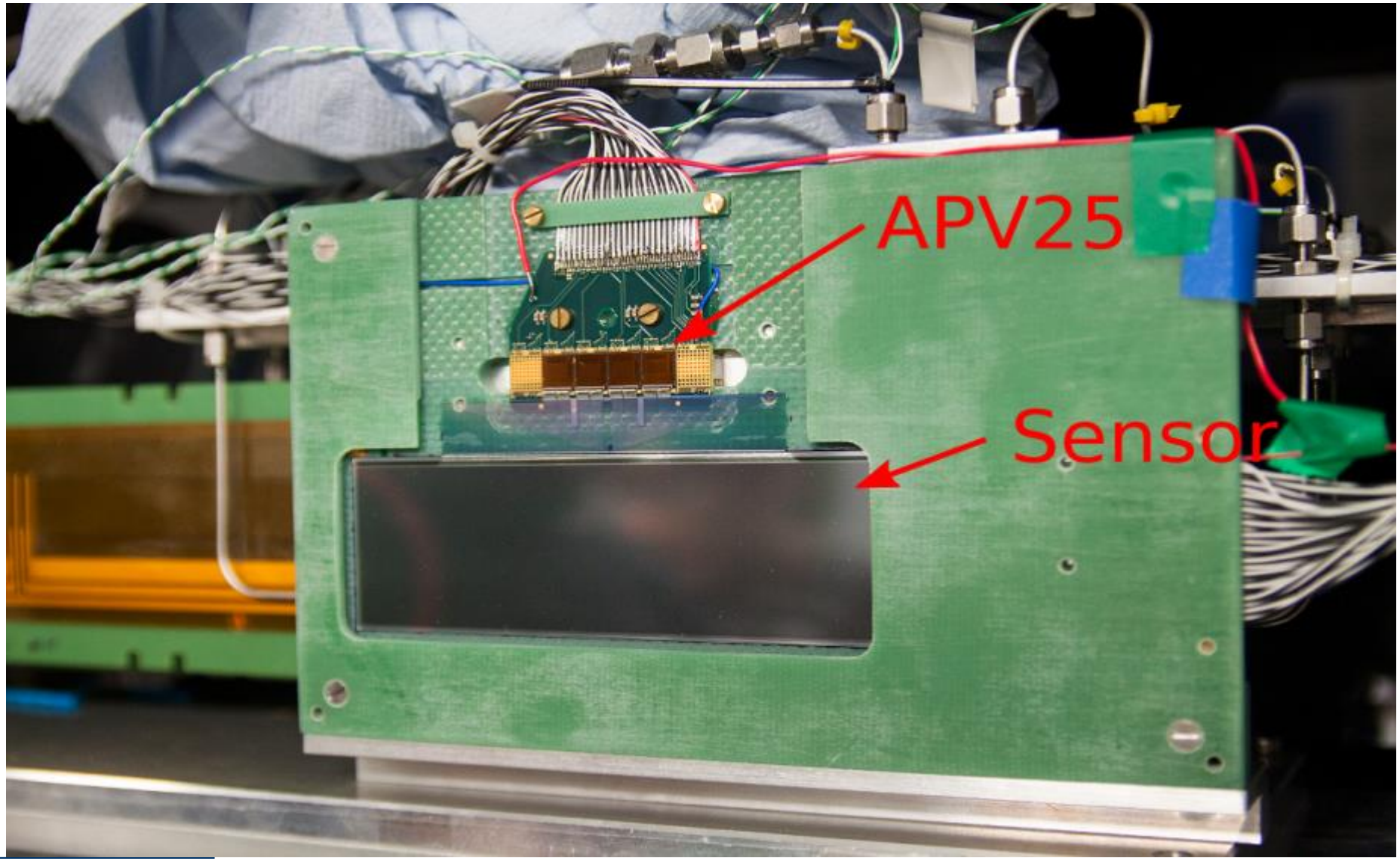

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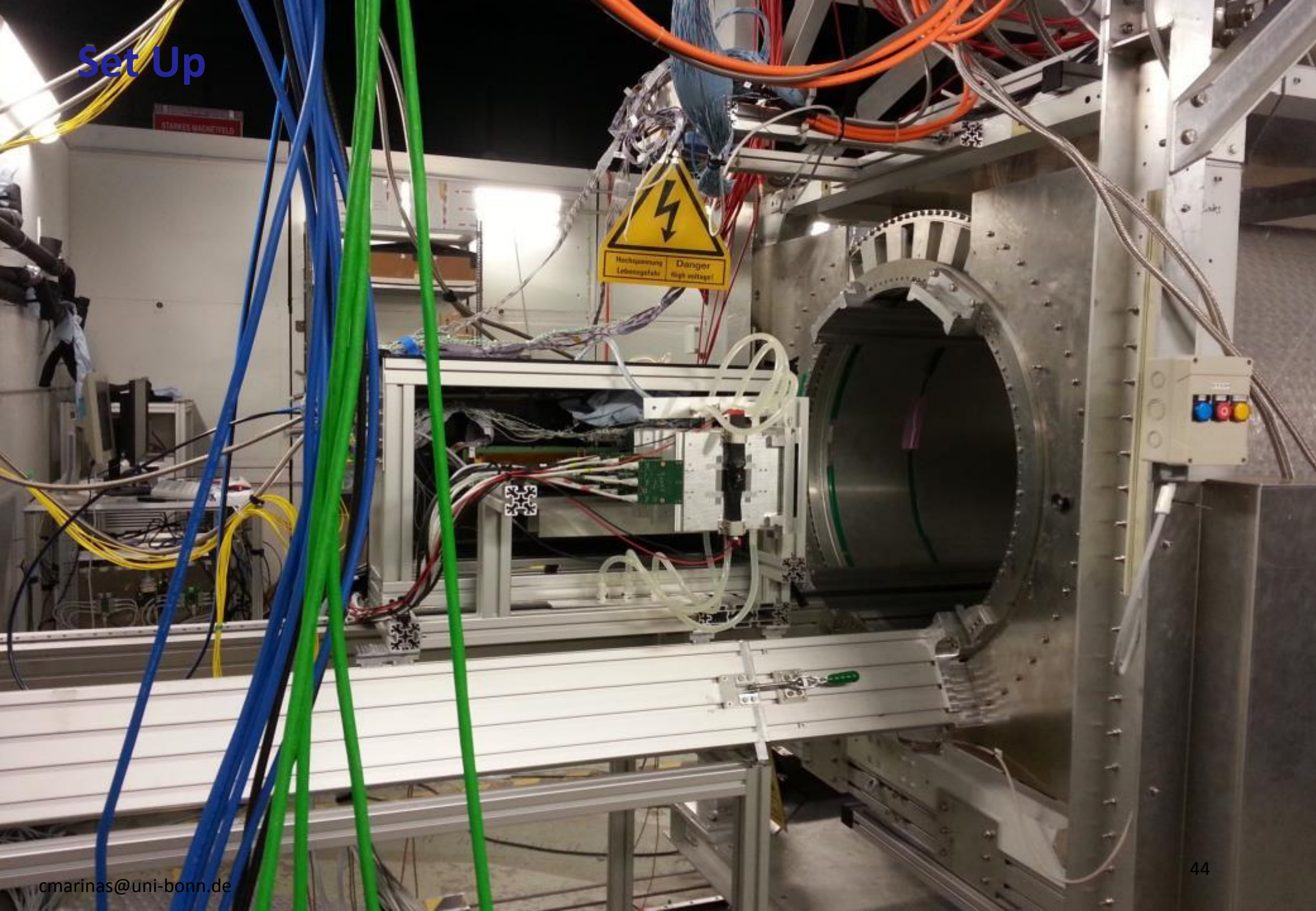
Set Up



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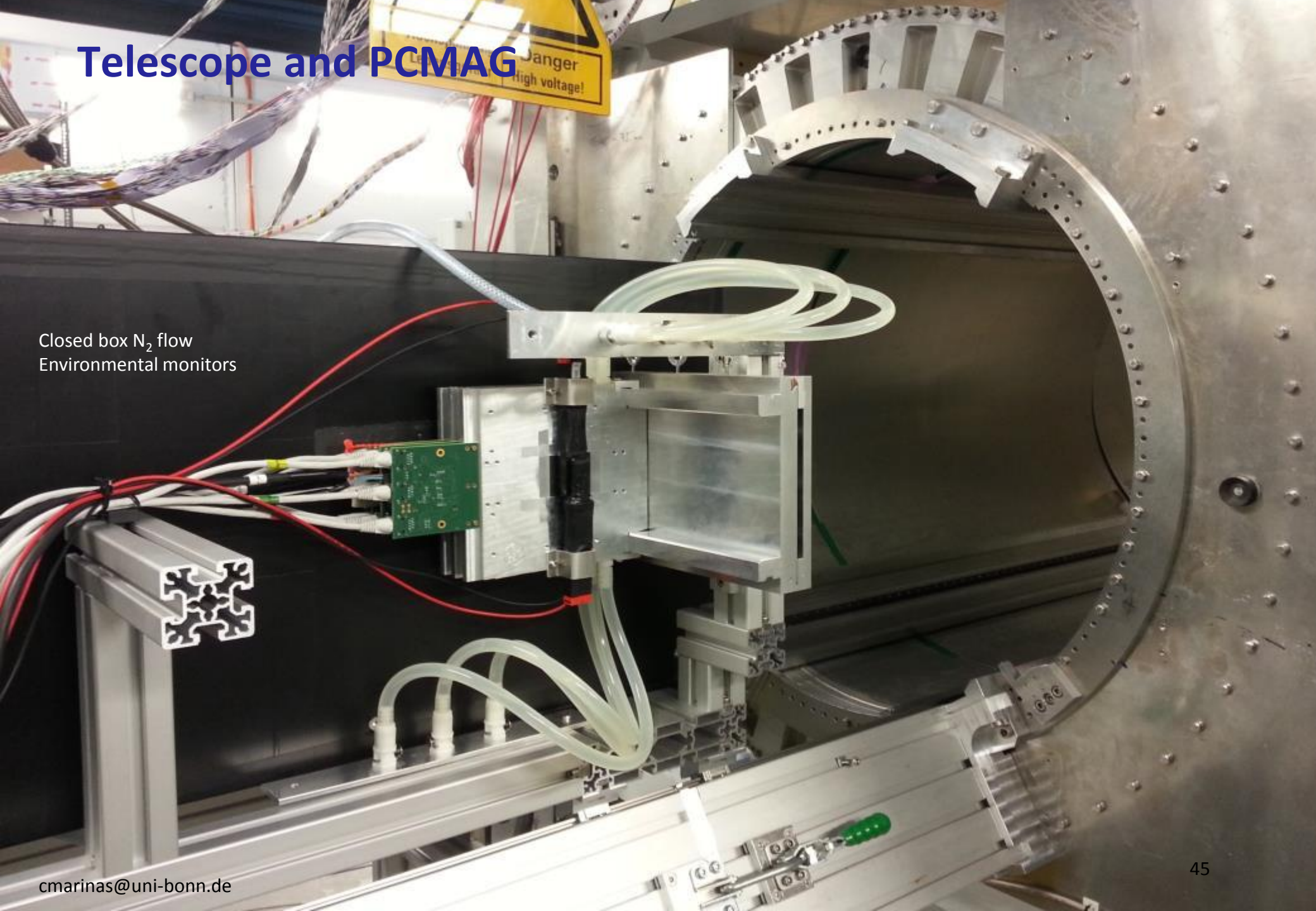
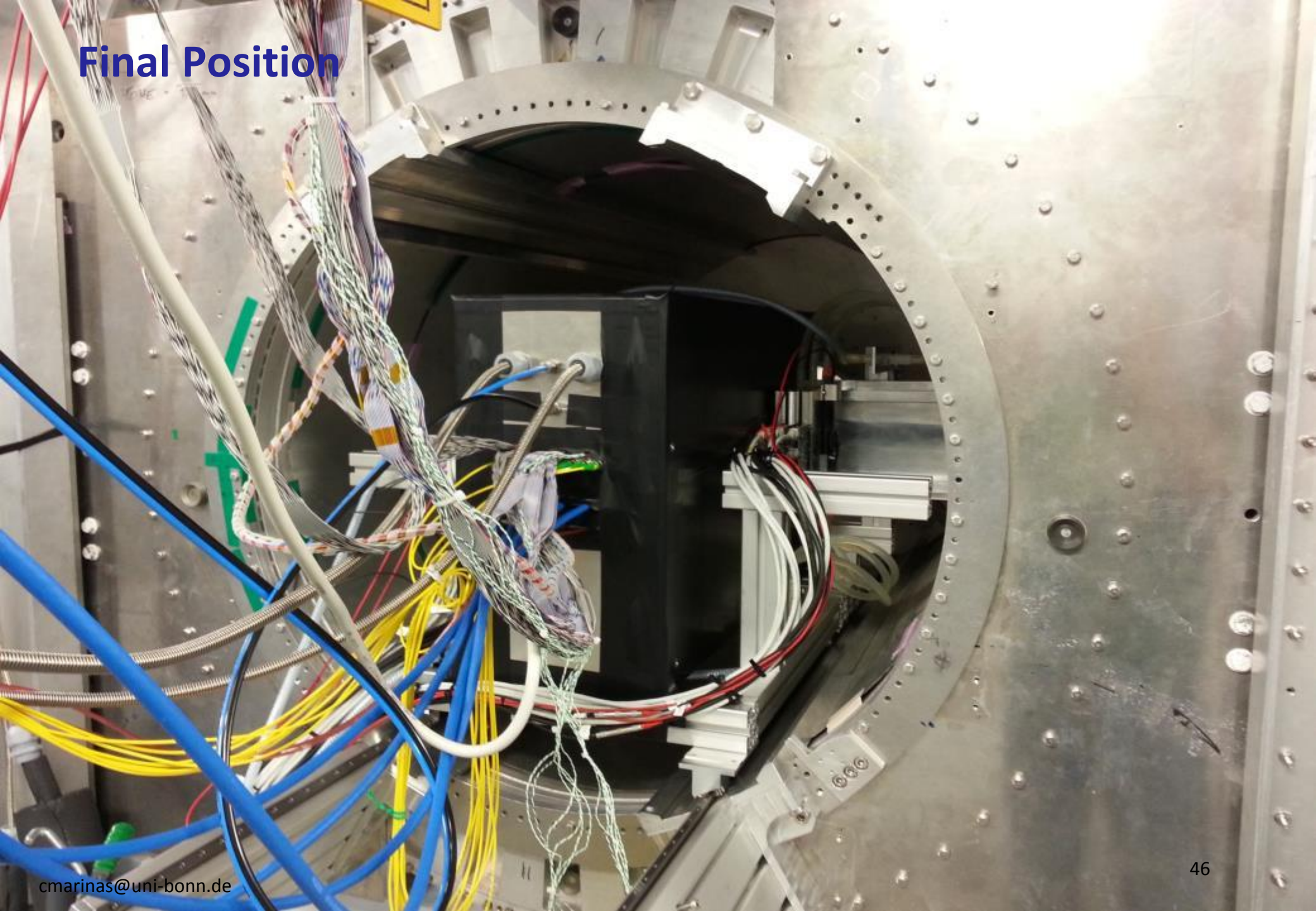
Telescope and PCMAG

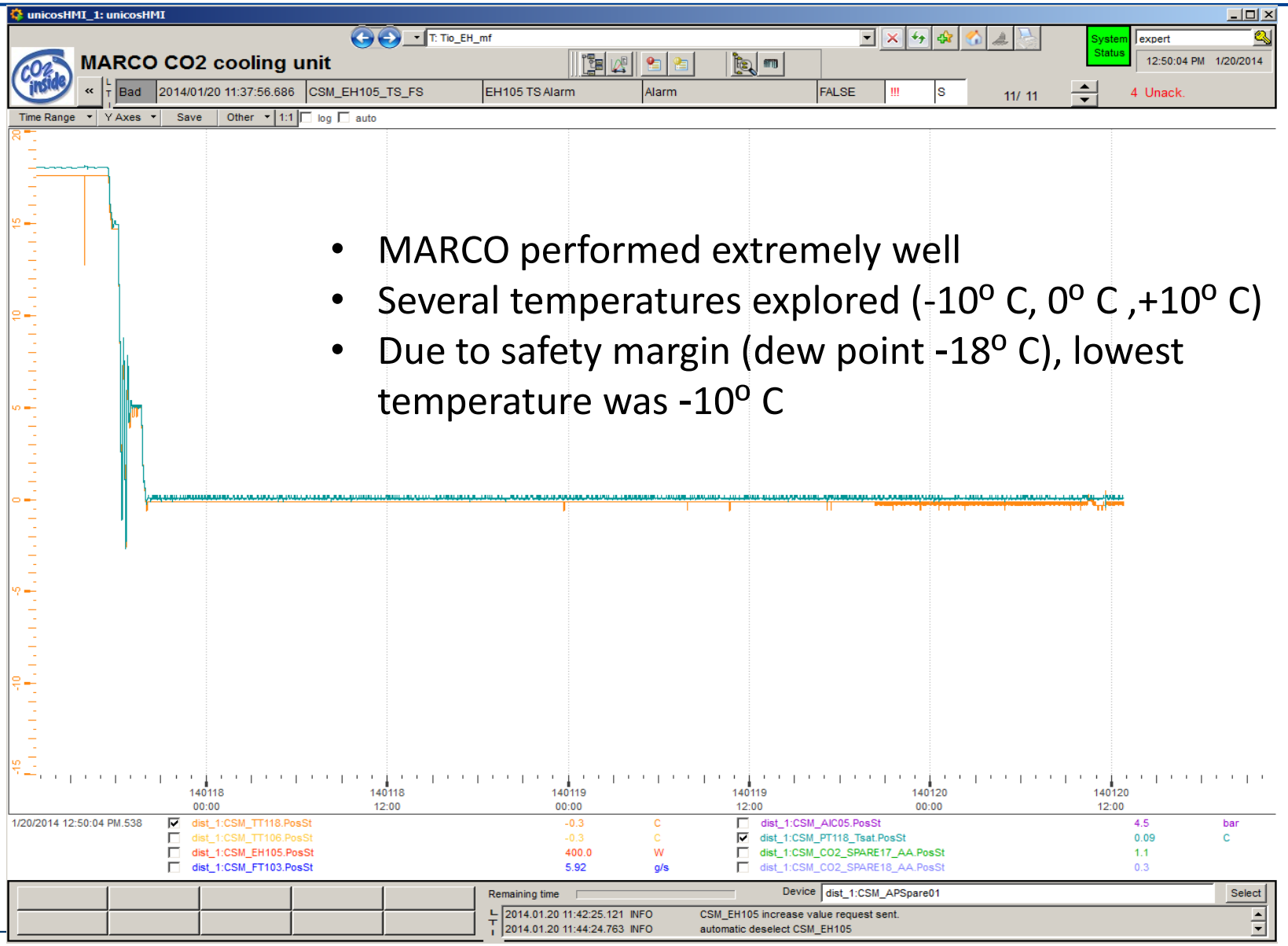


Closed box N_2 flow
Environmental monitors

Final Position



Temperature Stability



- MARCO performed extremely well
- Several temperatures explored (-10º C, 0º C ,+10º C)
- Due to safety margin (dew point -18º C), lowest temperature was -10º C

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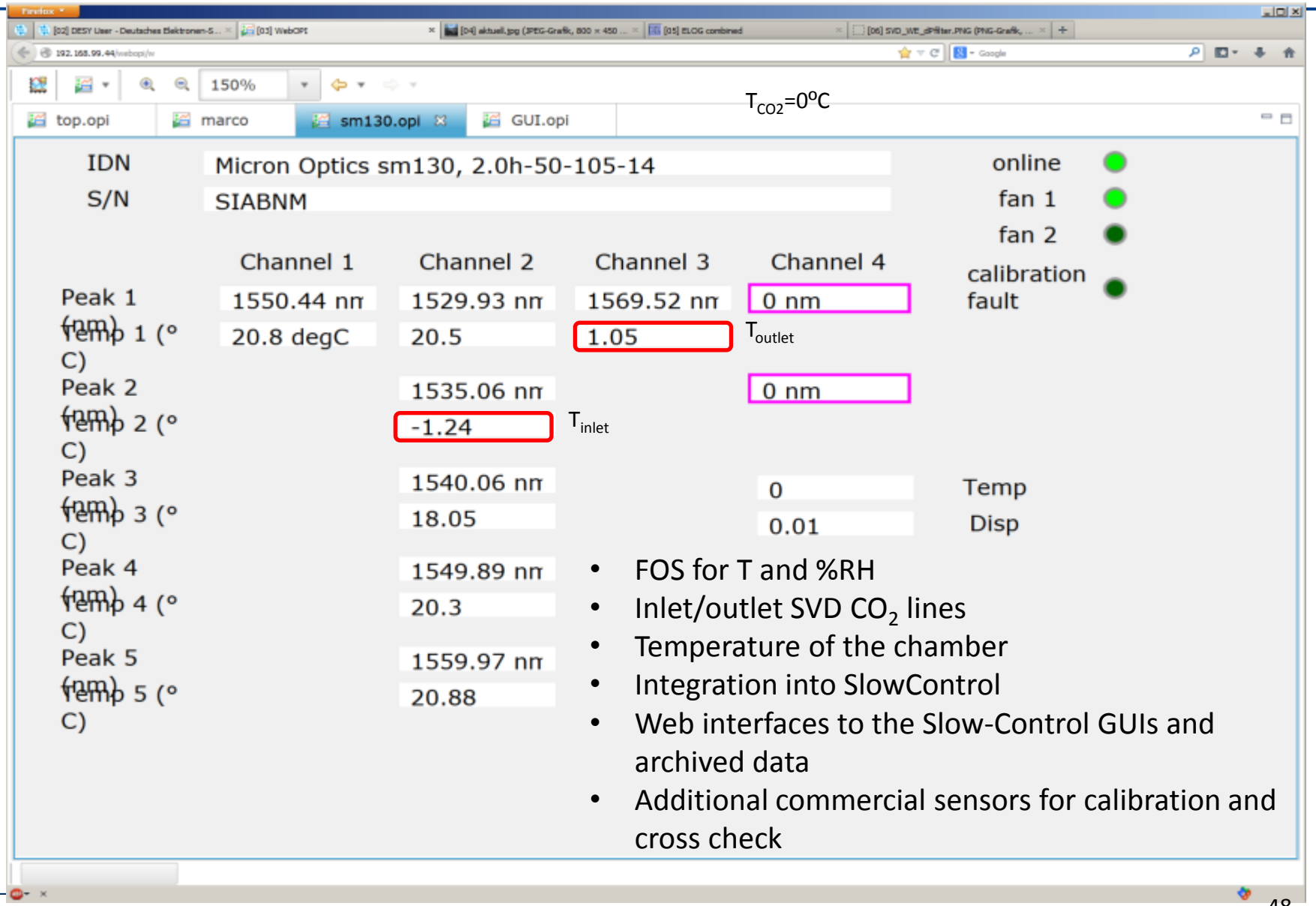
Environmental Monitors



- FOS for T and %RH
- Inlet/outlet SVD CO_2 lines
- Temperature of the chamber
- Integration into SlowControl
- Web interfaces to the Slow-Control GUIs and archived data
- Additional commercial sensors for calibration and cross check

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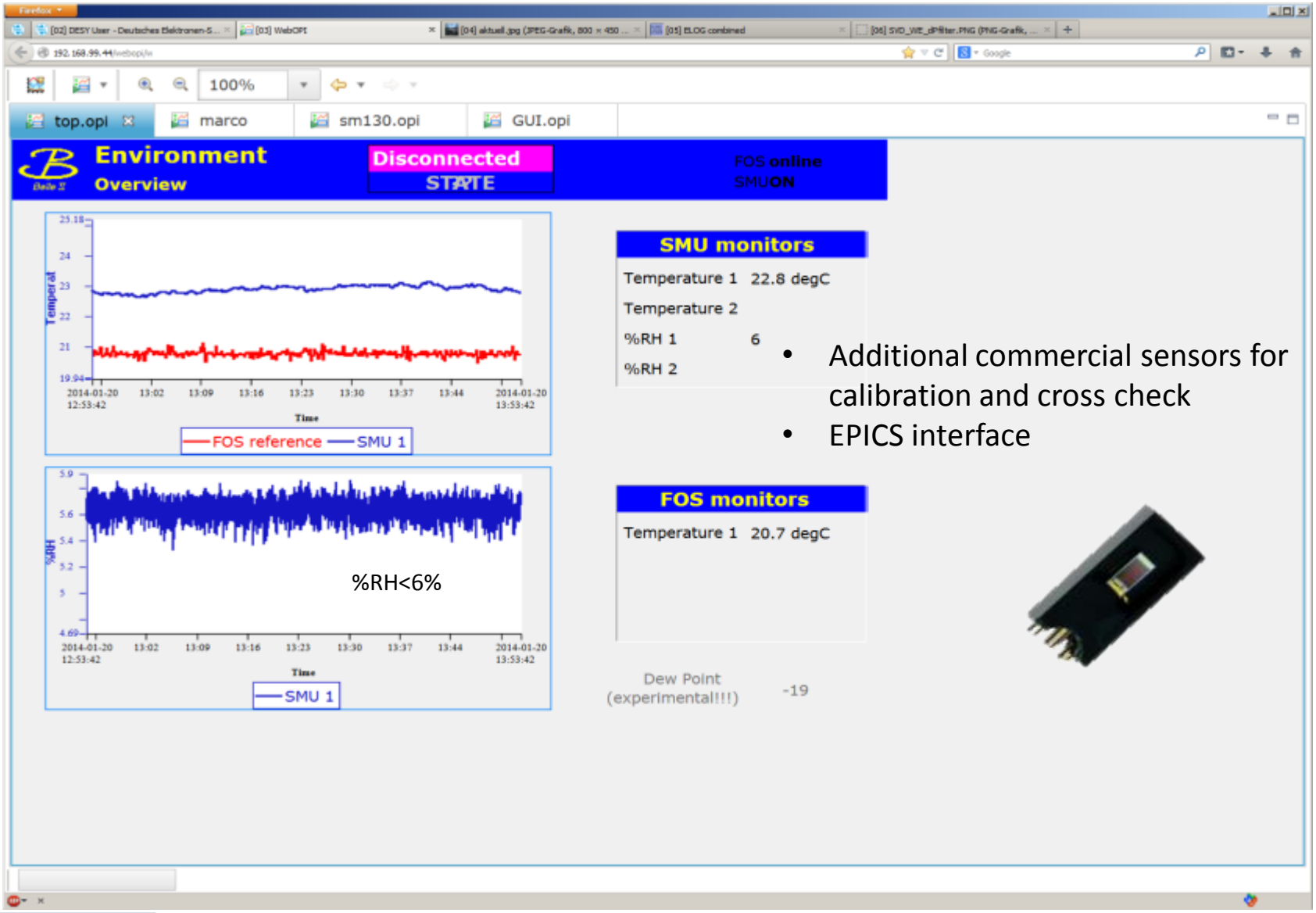
Environmental Monitors



- Additional commercial sensors for calibration and cross check
- EPICS interface

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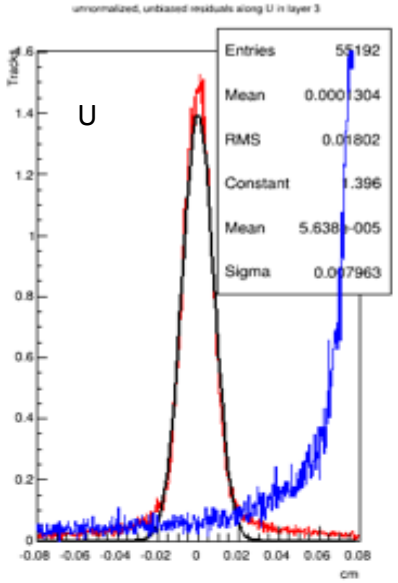
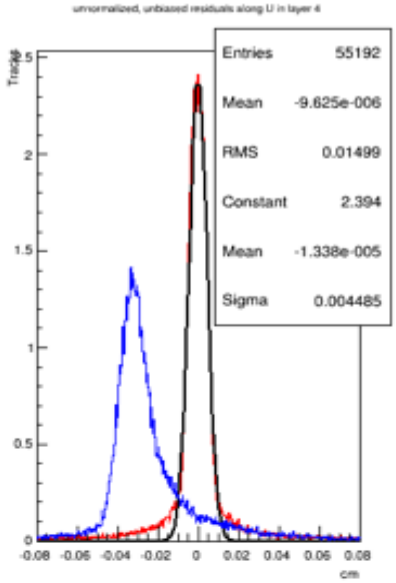
Alignment

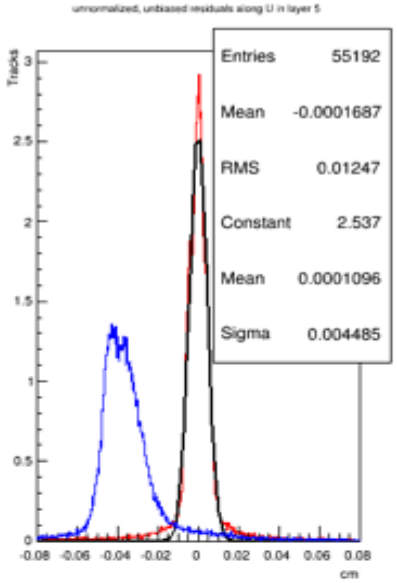
Before and After alignment



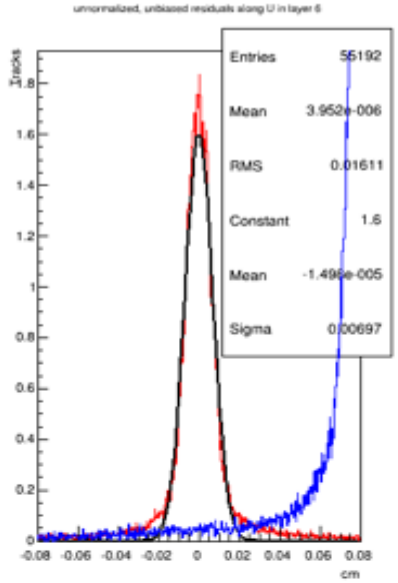
SVD3



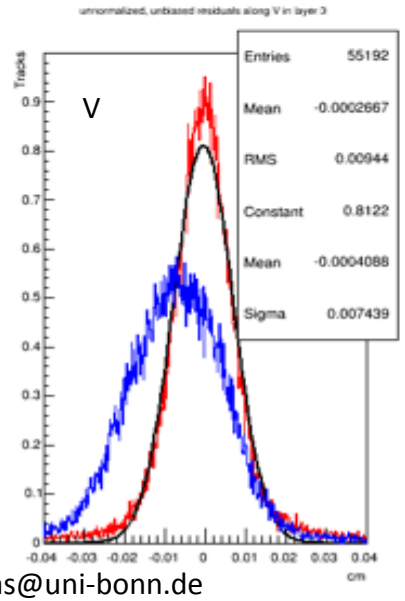
SVD4

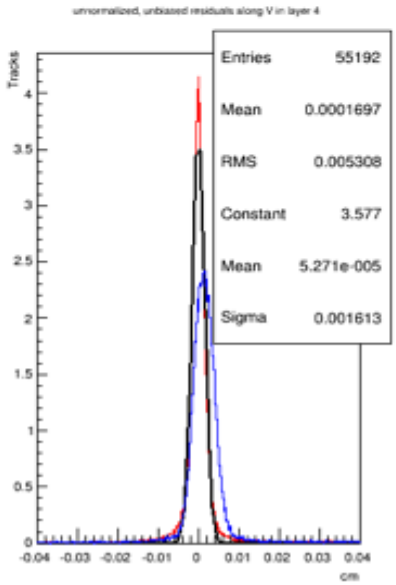


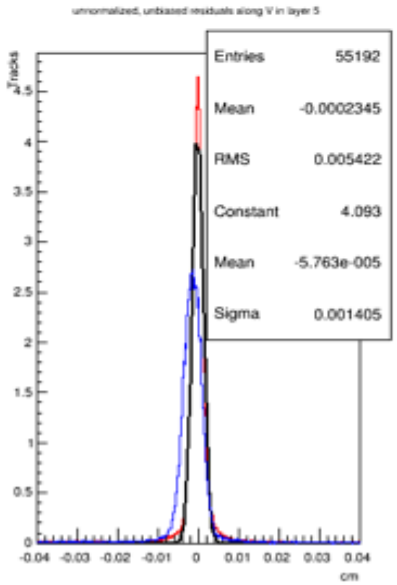
SVD5

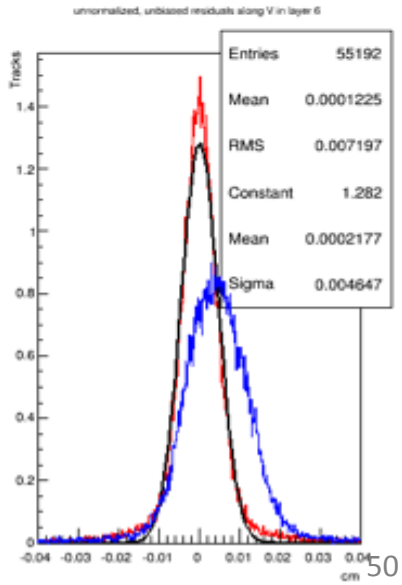


SVD6

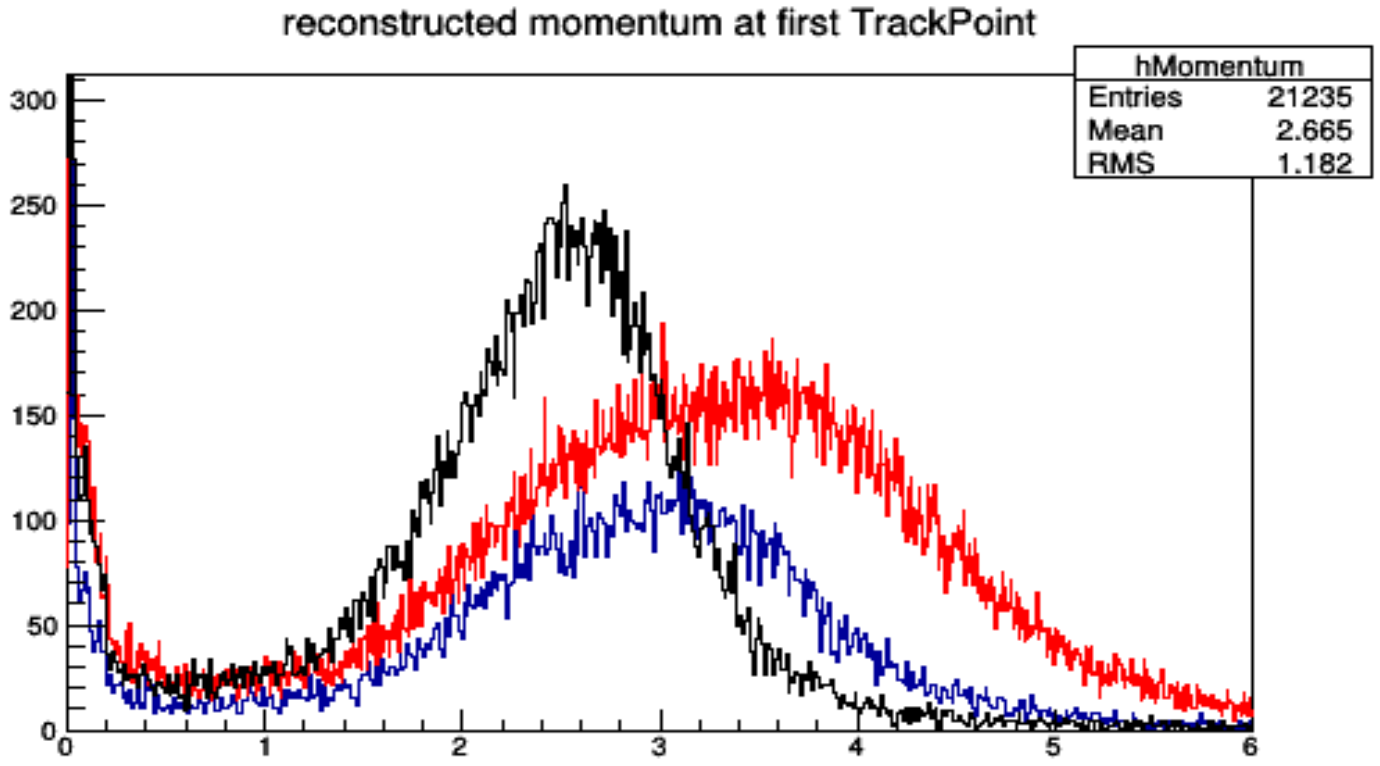








Having Fun with Tracks



Momentum spectra from three runs with different momenta (SVD only)

Resolution ILC DEPFETs

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Particle gun (single event)
EvtGen (physics event)
Mokka geometry

Ionization points
Signal points
Electronic noise
Digitization and clustering

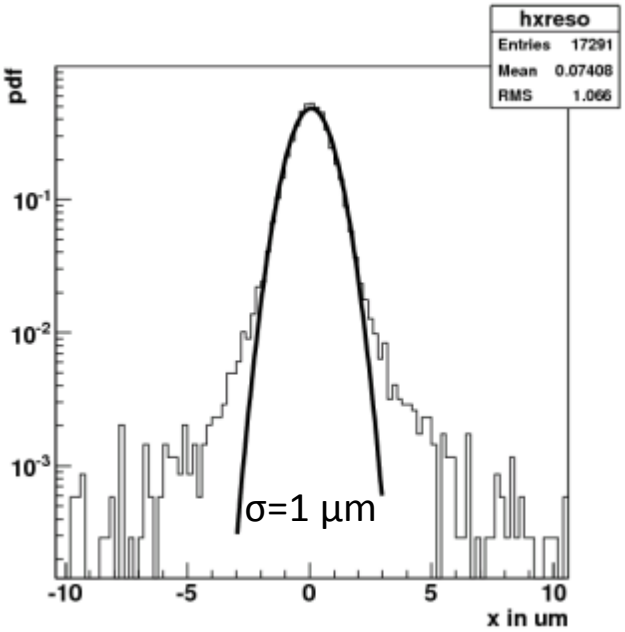
Marlin tracking
PXD+SVD+CDC

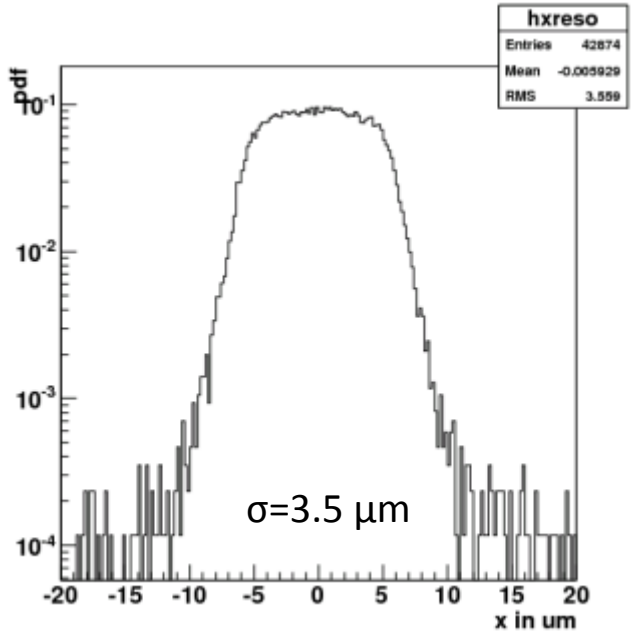
Physics channels

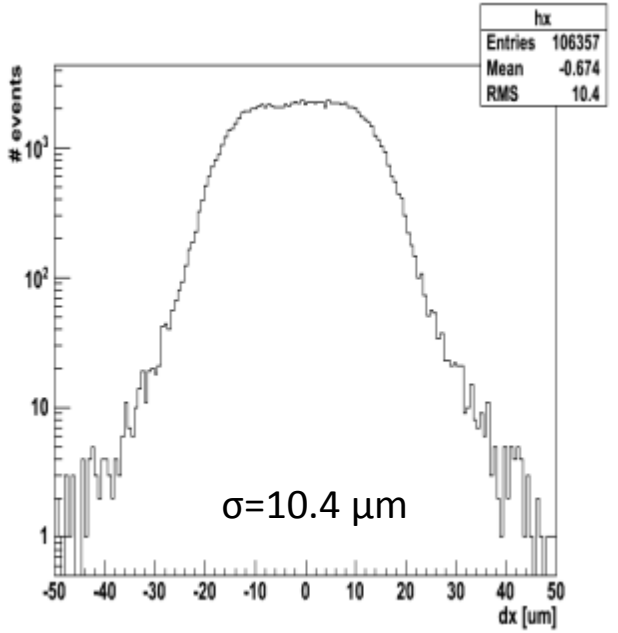
Test Beam Data
20x20x450 μm^3
Single point resolution: 1 µm

ILC (Simulation)
20x20x50 μm^3
Single point resolution: 3.5 µm

Test Beam Data
50x75x50 μm^3
Single point resolution: 10 µm







Spatial Resolution

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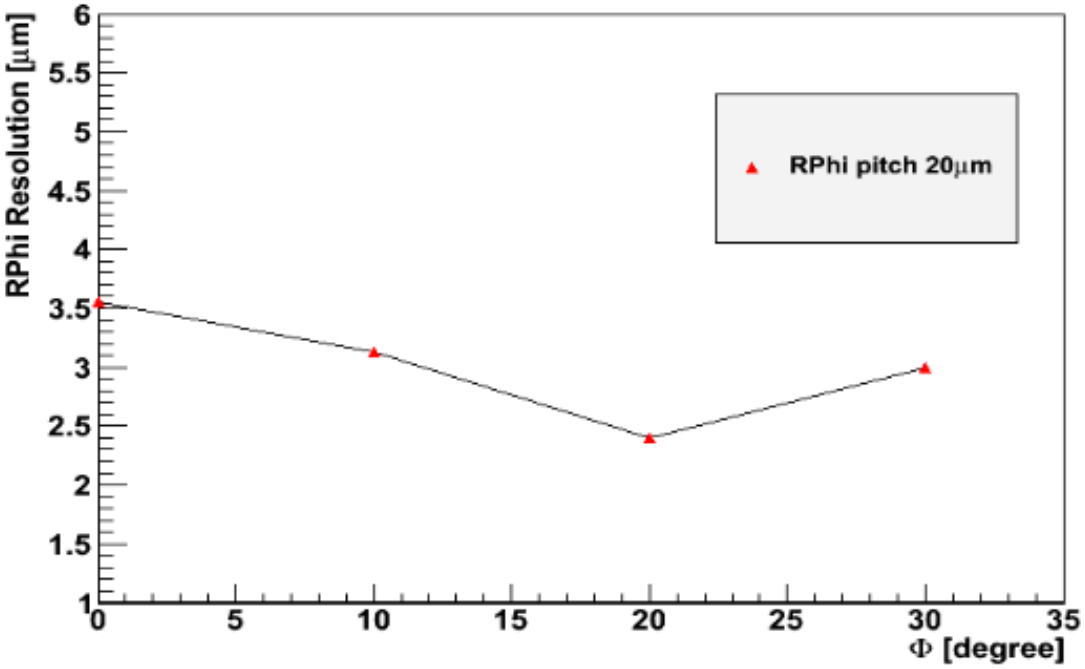
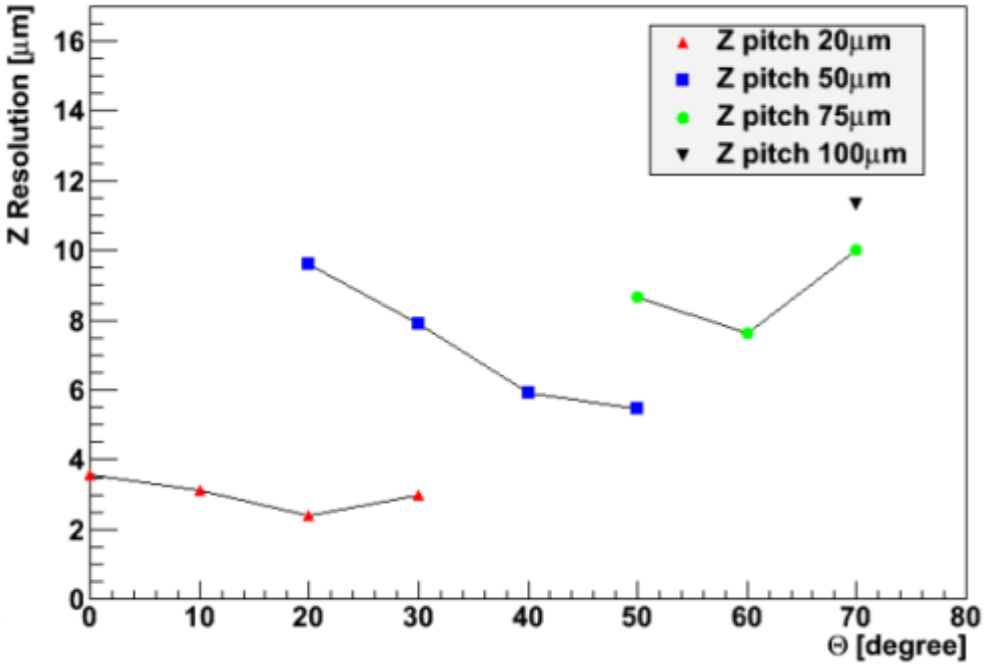
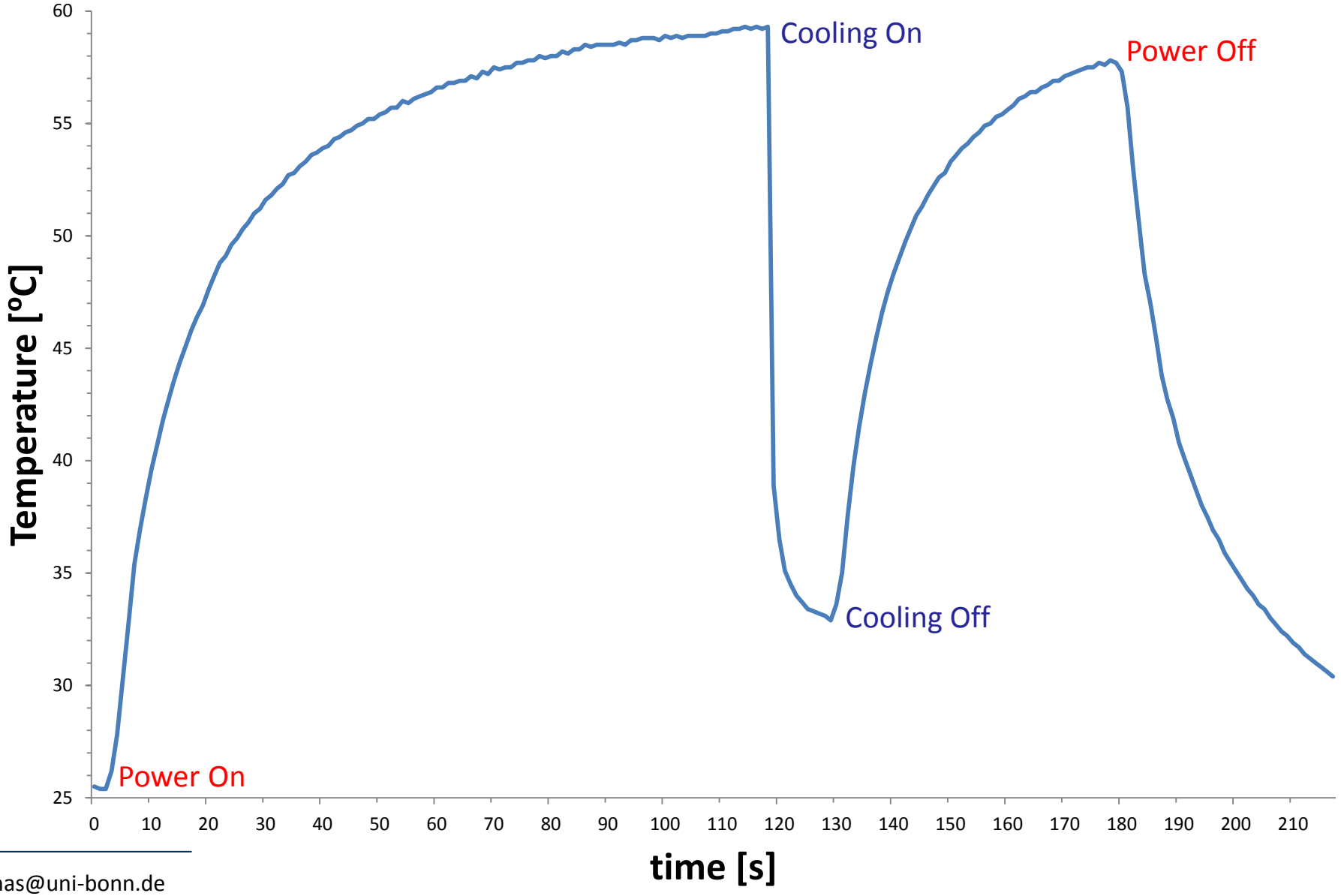
Digitizer predictions for a Linear Collider type DEPFET





Further details:

'Physical limitations to the spatial resolution of solid-state detectors'
arXiv:1404.3545

Micro-channel Cooling