



Electronics for a DEPFET vertex detector

**ECFA Detector R&D review
DESY, 11 June 2014**

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Halbleiterlabor der Max-Planck Gesellschaft

On behalf of the DEPFET collaboration

● Outline

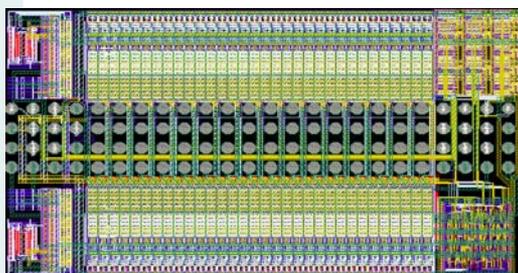


Electronics for a DEPFET vertex detector:

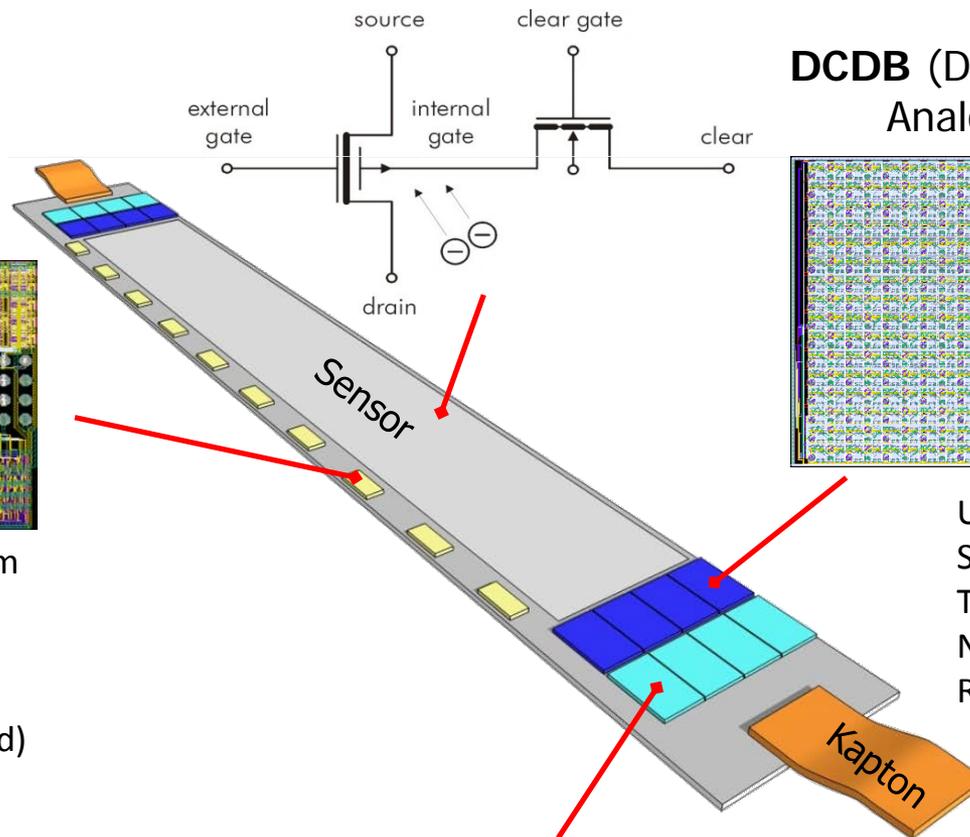
- ASICs (SwitcherB, DCD, DHP)
- Sensor Technology
- First Tests of assembled EMCs

● The DEPFET Ladder

SwitcherB Row control



AMS/IBM HVCMOS 180 nm
 Size $3.6 \times 1.5 \text{ mm}^2$
 Gate and Clear signal
 Fast HV ramp for Clear
 Rad. Hard proved (36 Mrad)

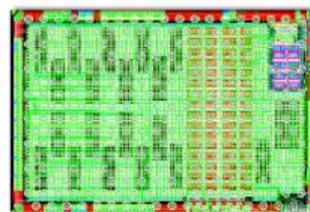


DCDB (Drain Current Digitizer) Analog frontend



UMC 180 nm
 Size $5.0 \times 3.2 \text{ mm}^2$
 TIA and ADC
 Noise 35 nA @ 100 ns/row
 Rad. Hard proved (20 Mrad)

DHP (Data Handling Processor) First data compression



IBM TSMC 65 nm
 Size $4.0 \times 3.2 \text{ mm}^2$
 Stores raw data and pedestals
 Common mode and pedestal correction
 Data reduction (zero suppression)
 Timing signal generation
 Rad. Hard proved (100 Mrad)

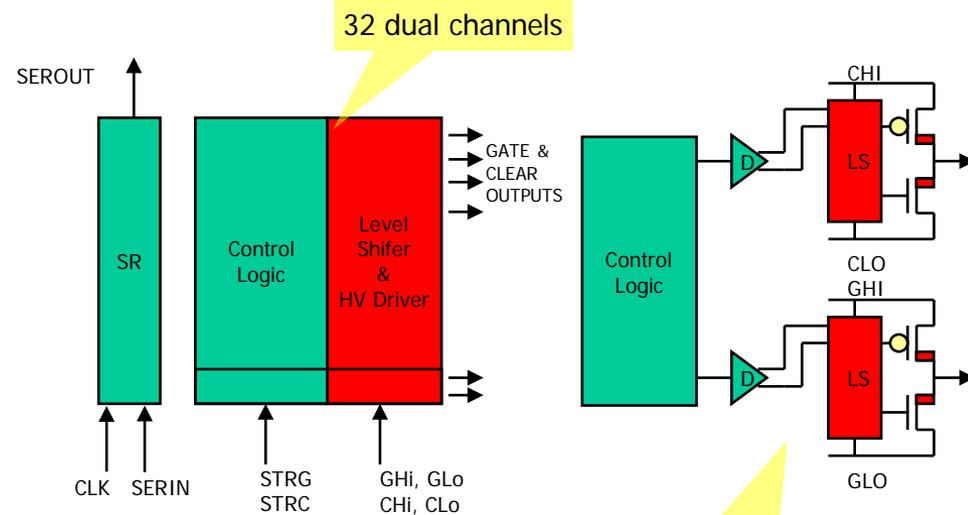
● Line Driver - SwitcherB

Requirements

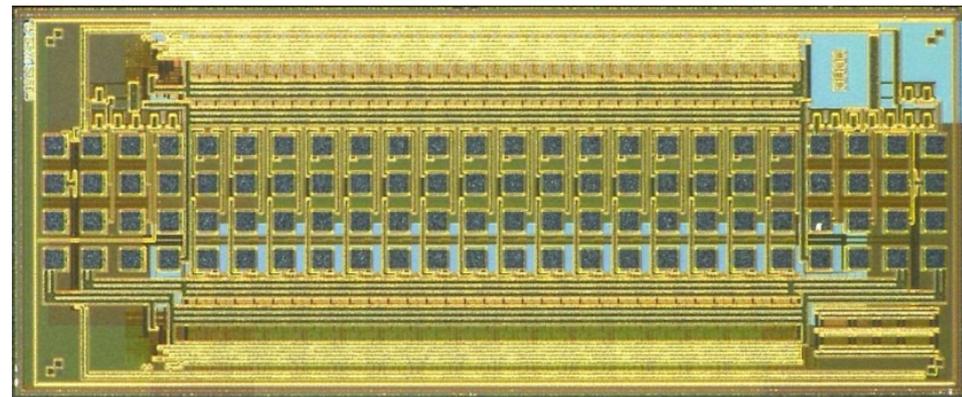
- high voltage (10-20V) pulses for clear and gate lines
- fast outputs
- radiation hard
- low power (chip inside acceptance volume)

Implementation (SWITCHERB18)

- 180nm HVCMOS AMS/IBM technology
- 1.8V supply voltage
- 20V MOSFET for output stages
- 32 channels, bump bond I/O
- **Chips thinned down to 75μm can be ordered**

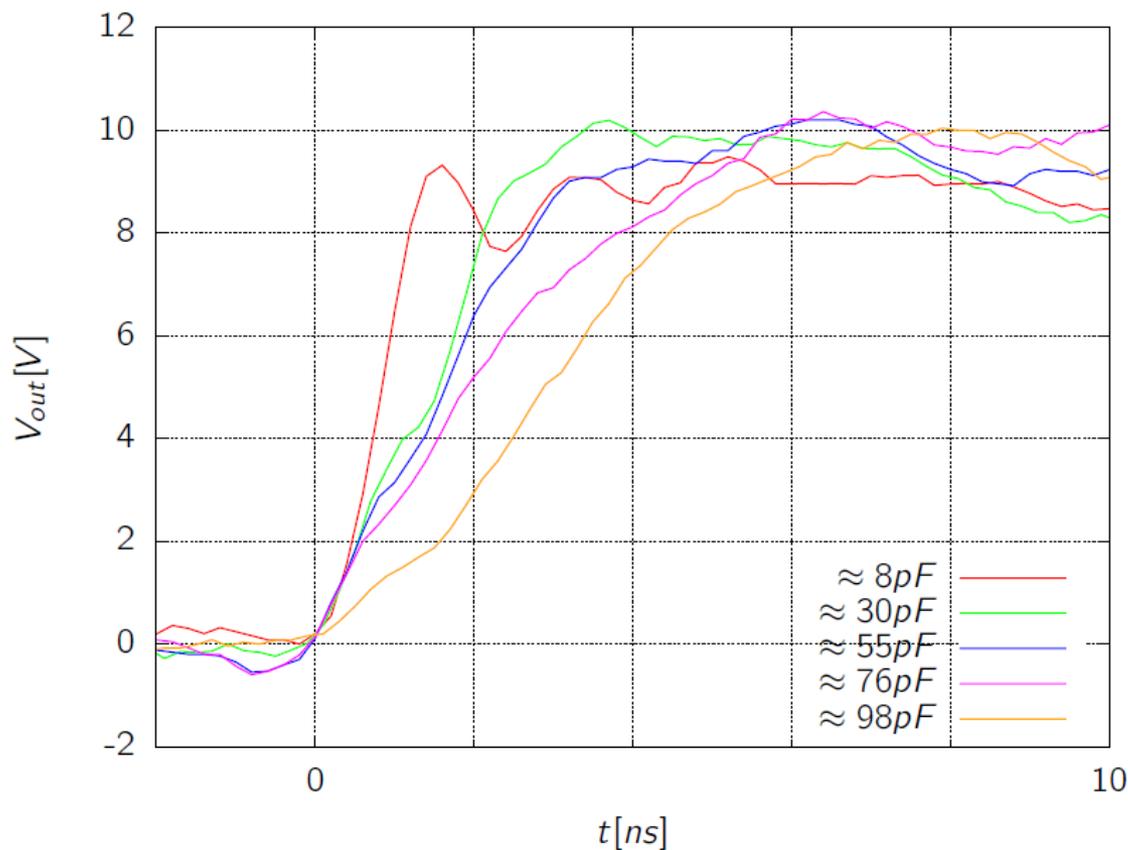


implementation detail of one channel



● Line Driver - SWITCHER

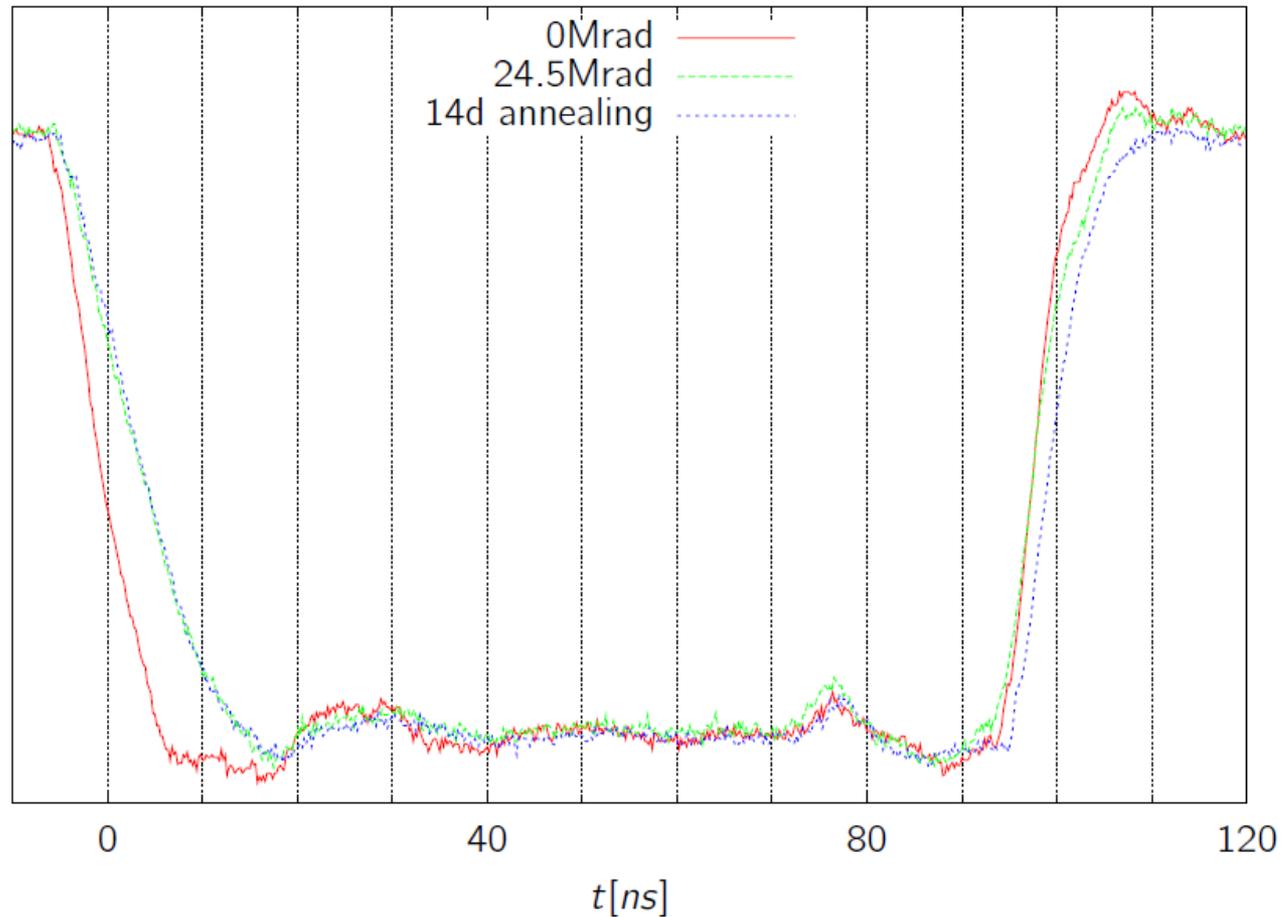
Output driver characteristic for different load capacitances:



capacitance	rising	falling
8pF	0.8ns	0.9ns
30pF	1.8ns	2.0ns
55pF	2.8ns	3.3ns
76pF	3.6ns	4.0ns
98pF	4.2ns	4.8ns

10%-90% rise and fall time of the signal

● Line Driver - SWITCHER

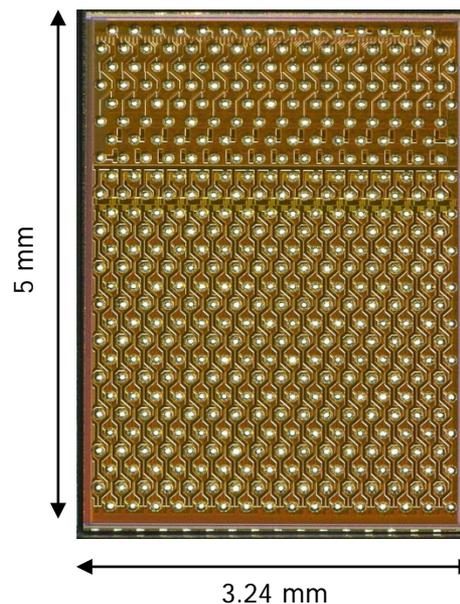
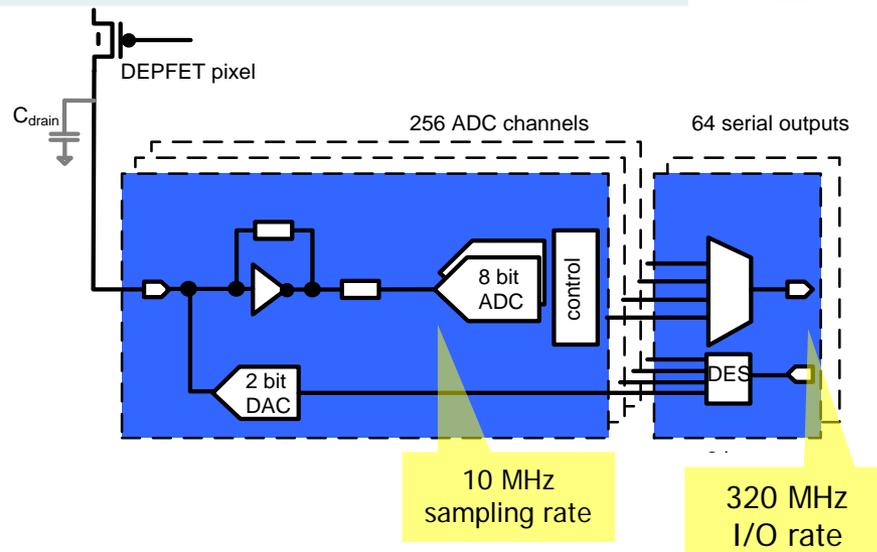


SwitcherB35 (fabricated in AMS 350nm technology)
- Gate Output channel before and after irradiation

● Drain Current Digitizer - DCD

- Receive and digitize drain current
 - transimpedance amplifier input
 - low impedance input for fast settling ($C_{\text{drain}} \sim 50\text{pF}$)
 - 8 bit ADC, 10 Msps
 - 2 bit DAC for range adjustment (individual pedestal current subtraction per pixel)

- Implementation (DCDB)
 - 180nm CMOS, 1.8V supply voltage
 - 256 channels
 - bump bond I/O
 - 320 MHz interface (64 + 8 lines) to DHP chip

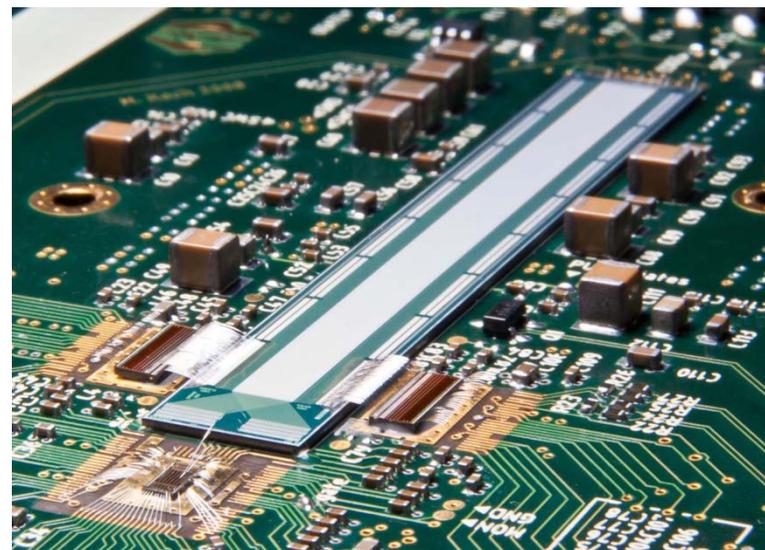


● DCD – Drain Current Digitizer

DCD dynamic measurements
Readout speed with single sampling

Belle II PXD frame readout: 20 μ s
(50 KHz frame rate)

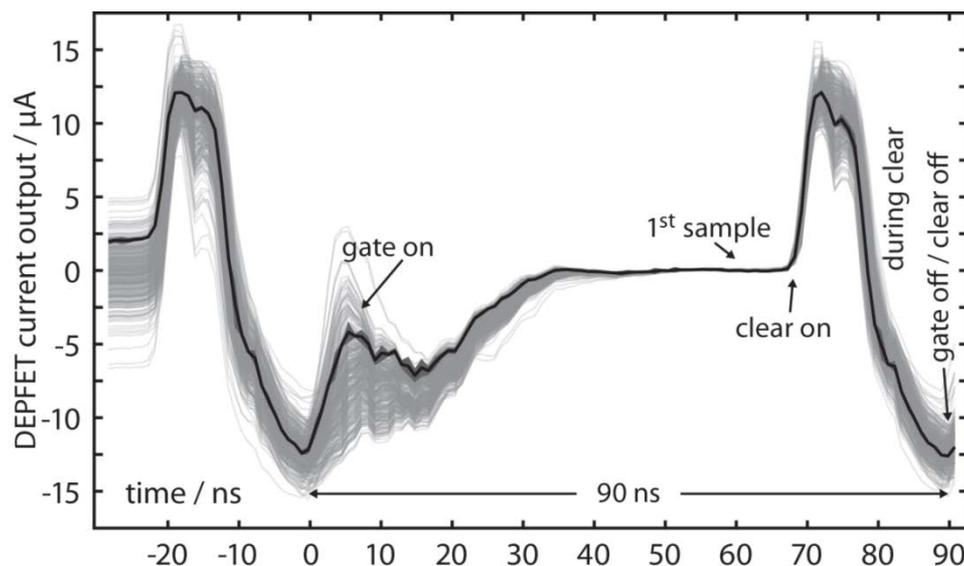
Read-clear cycle: 100 ns
(768 rows, 4 fold readout)



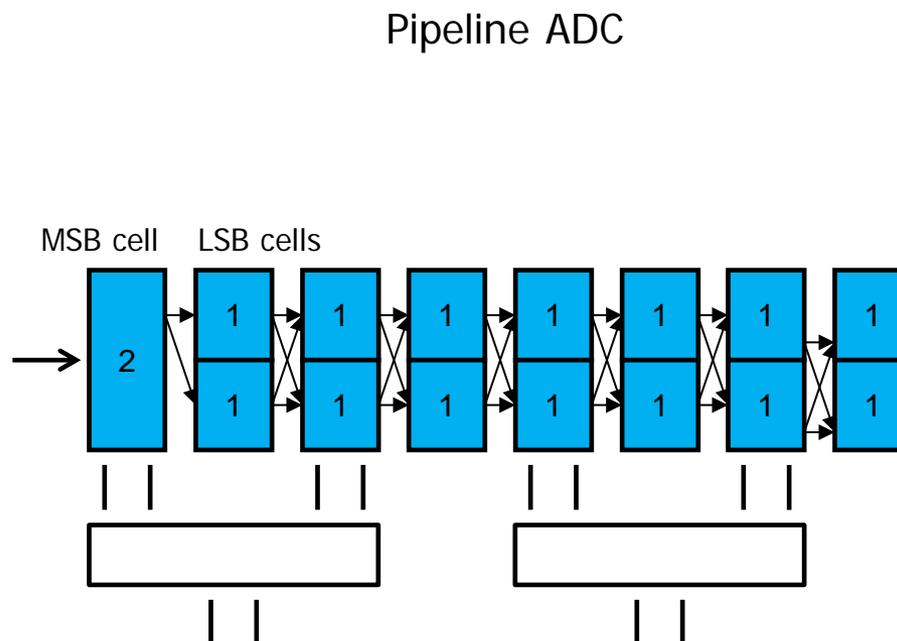
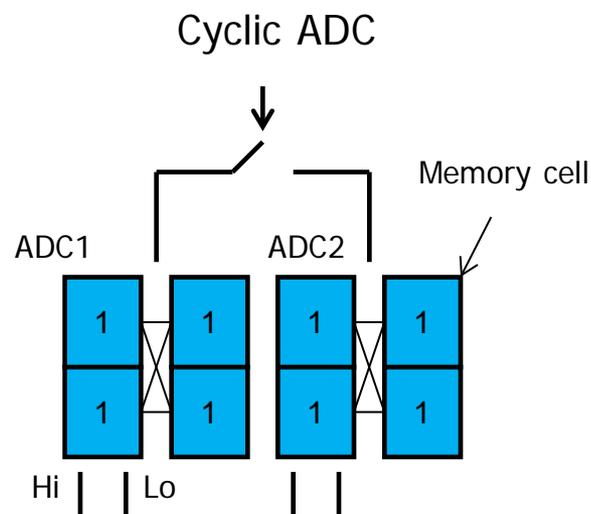
Long drain lines \sim 60 pF parasitic capacitance

Read-out speed: current state-of-the-art allows for a row rate of 1/100 ns.

→ Change from cyclic to pipeline ADC architecture will allow to reduce read-out time by factor 2



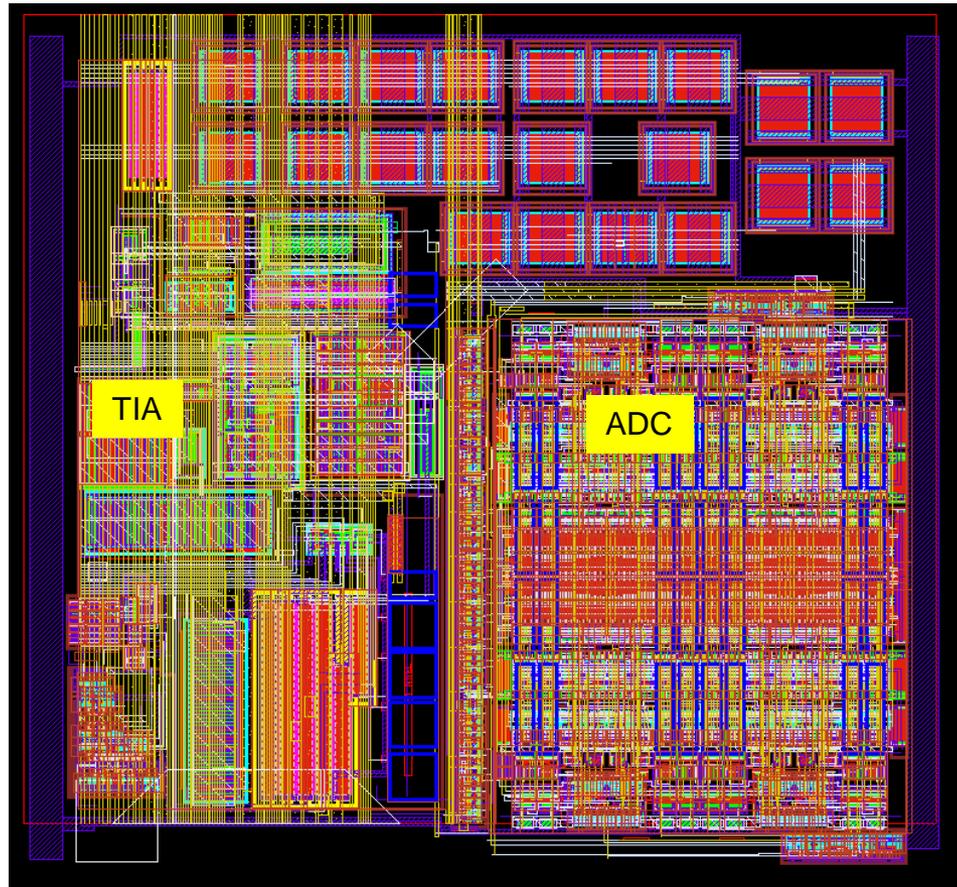
● Pipelined vs. Cyclic ADC



- Cyclic ADC approach
- Algorithm performed cyclically (ping pong wise)
- by two memory cell pairs
- Two ADCs per channel
- 200ns sampling rate/ADC

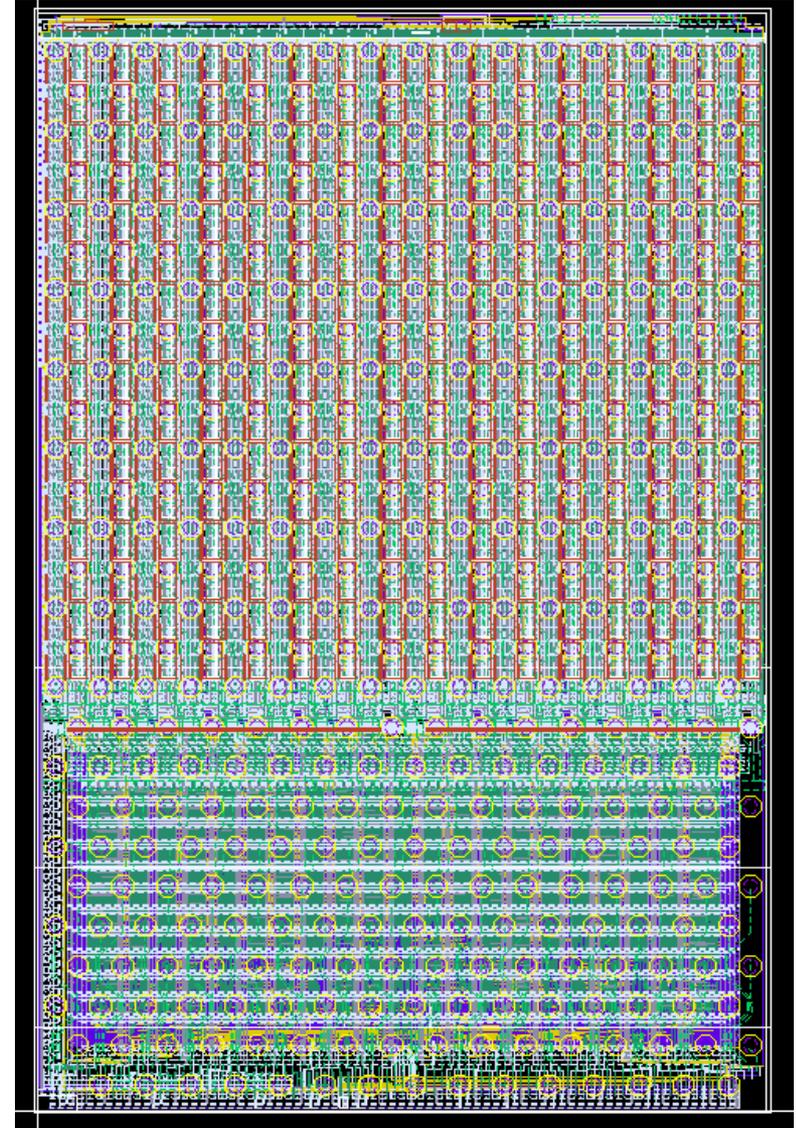
- Pipeline ADC approach
- Algorithm performed as in production line by 8 memory cell pairs
- One ADC per channel
- 100ns sampling rate
- Designed for 50 ns sampling rate

- DCD with Pipeline ADC Architecture

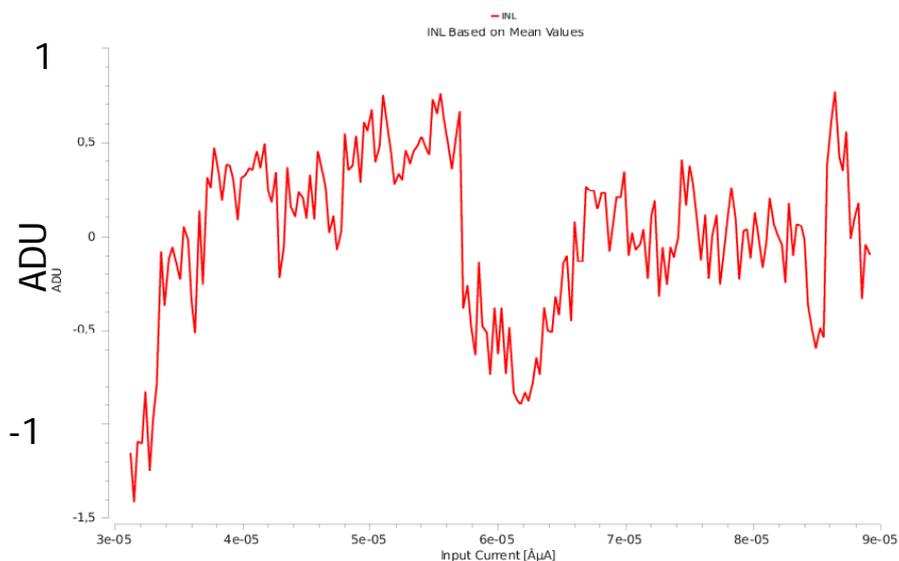
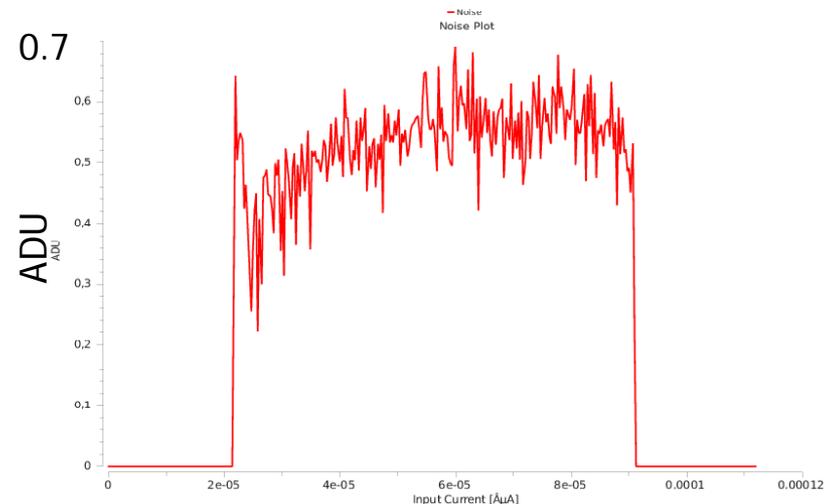
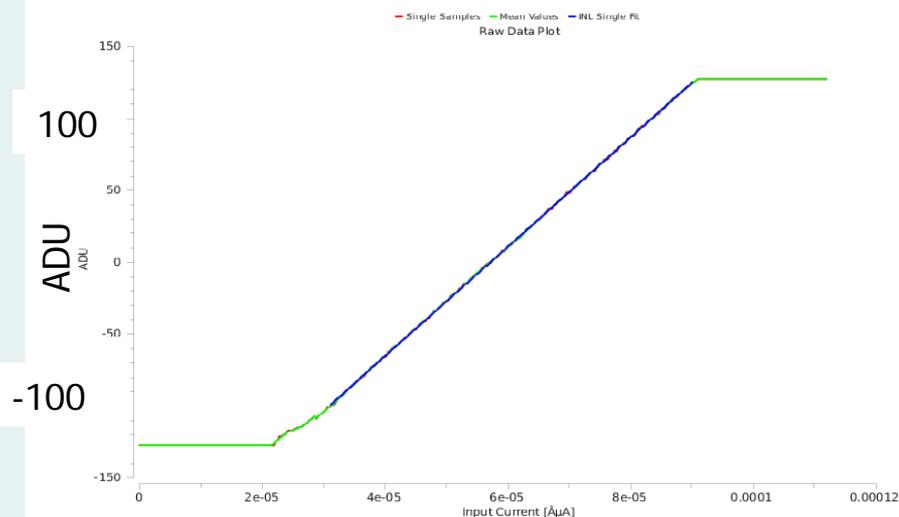


200 μm

5 mm



DCD with Pipeline ADC Architecture

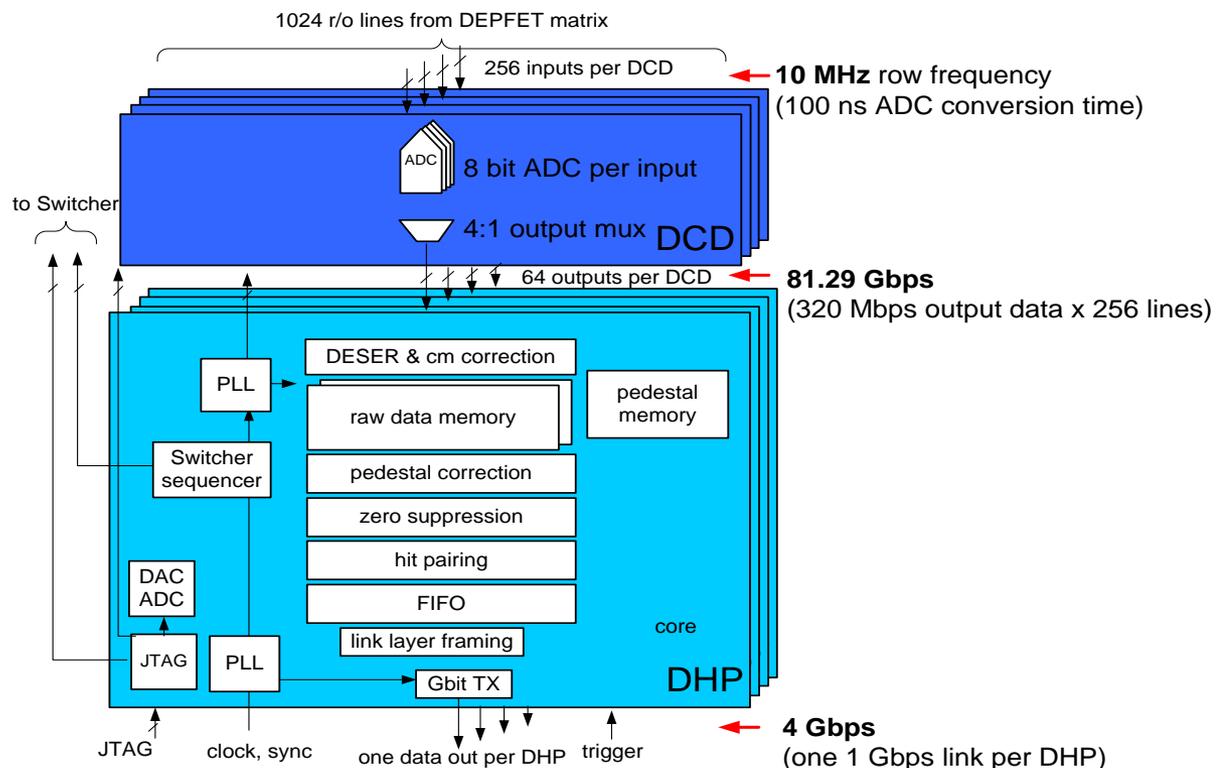


- Measurements done at 320MHz (100ns row sampling)
- Noise $\sim 40\text{nA}@320\text{MHz}$
- Power consumption $\sim 1.33\text{W}$
- First functionality tests at 500MHz clock rate (64ns row sampling)

● Data Handling Processor (DHP)

Functionality

- Module controller
 - JTAG bus to DCDB and SWITCHER chips
 - Clock & timing generation & distribution
- Data reduction (1/20): 0-suppression, triggered r/o



Data processing details

- Raw data buffer (two frames, 40 μ s)
- Common mode (two pass)
- Fixed pattern noise correction (static pedestals)
- Hit finder (FIFO1 + FIFO2)
- Framing (AURORA)
- SER \rightarrow CML link driver

● Data Handling Processor (DHP) - Performance

Data processing

SWITCHER sequencing

Inter-chip communication

Serial link

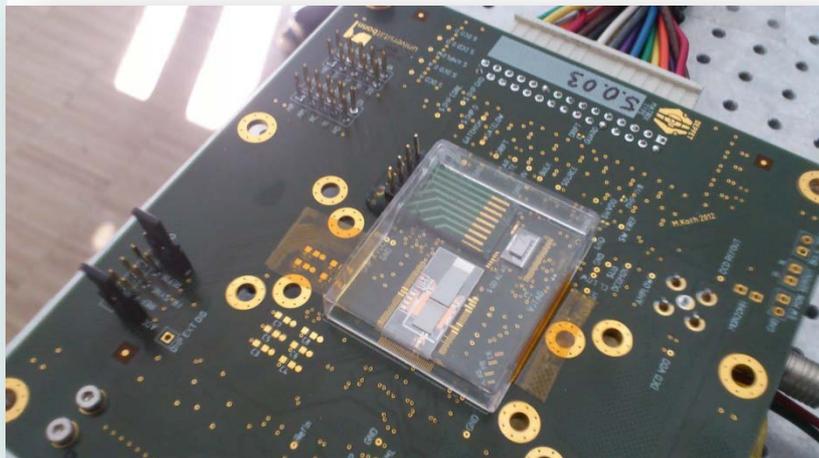
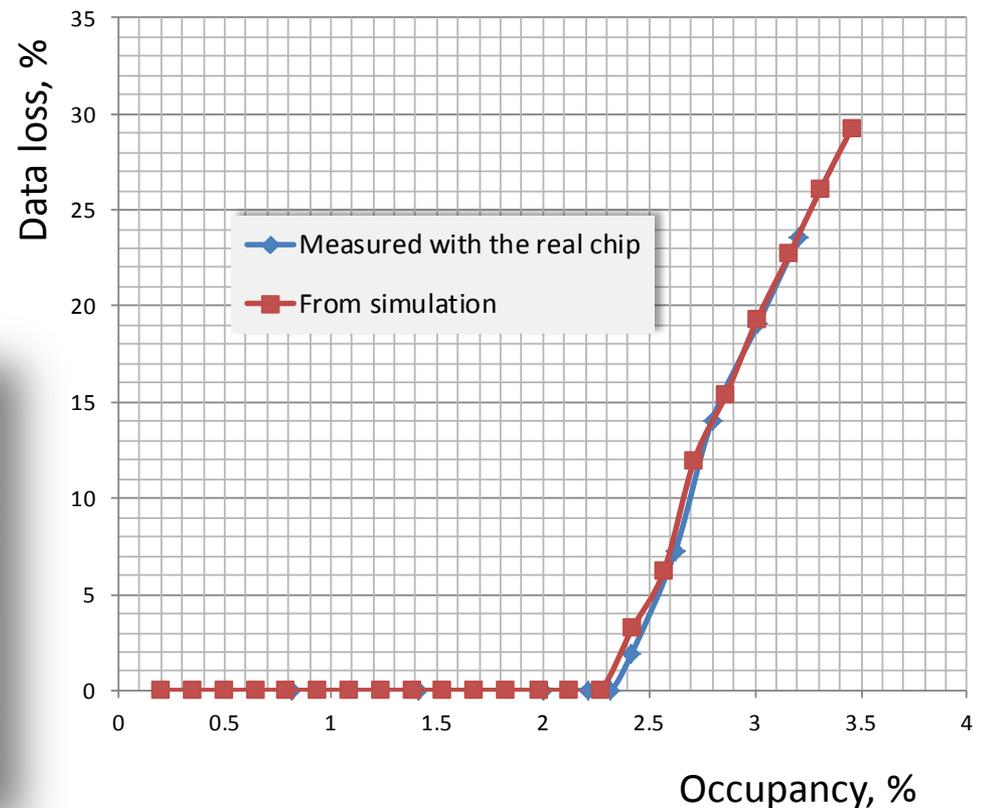


Photo of the hybrid 5 (without DEPFET matrix)

Un-triggered acquisition, DHP0.2 data loss characteristic as a function of the input data occupancy (C++ and real chip)



No data loss for the expected occupancy

● Data Handling Processor (DHP) - Performance

Data processing

SWITCHER sequencing

Inter-chip communication

Serial link

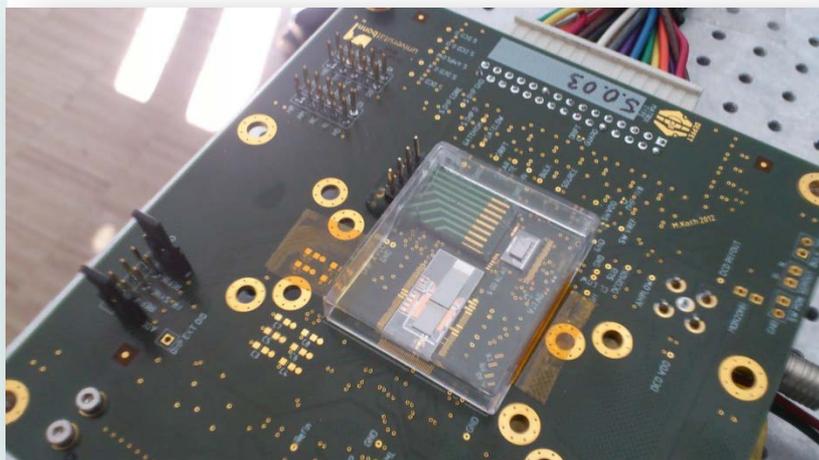
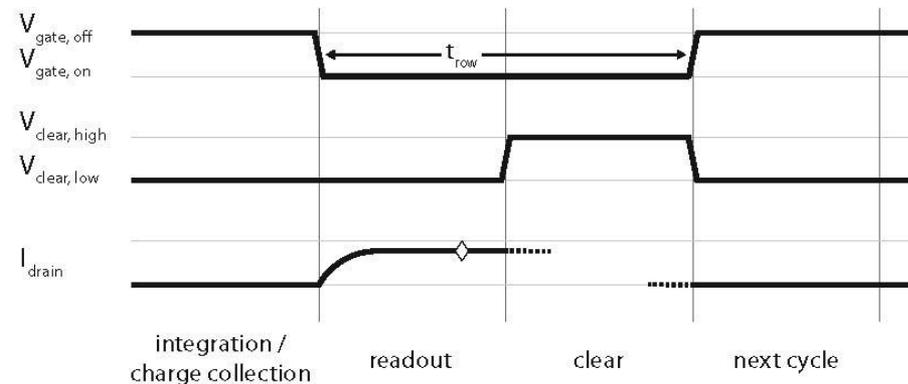
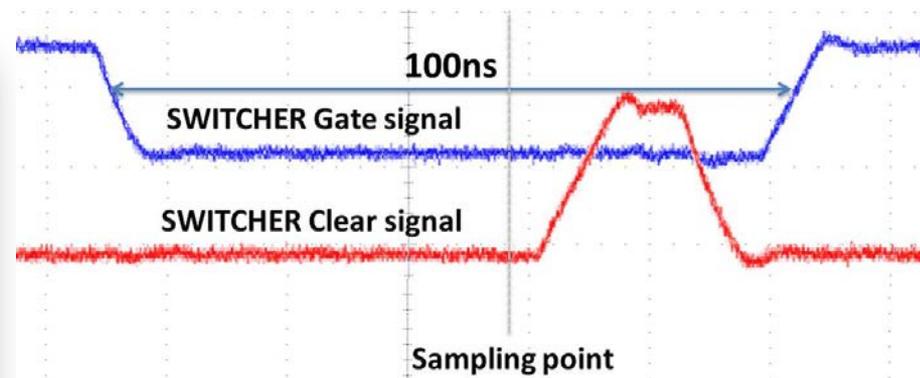


Photo of the hybrid 5 (without DEPFET matrix)



DHP can control the SwitcherB sequence

● Data Handling Processor (DHP) - Performance

Data processing
SWITCHER sequencing
Inter-chip communication
Serial link

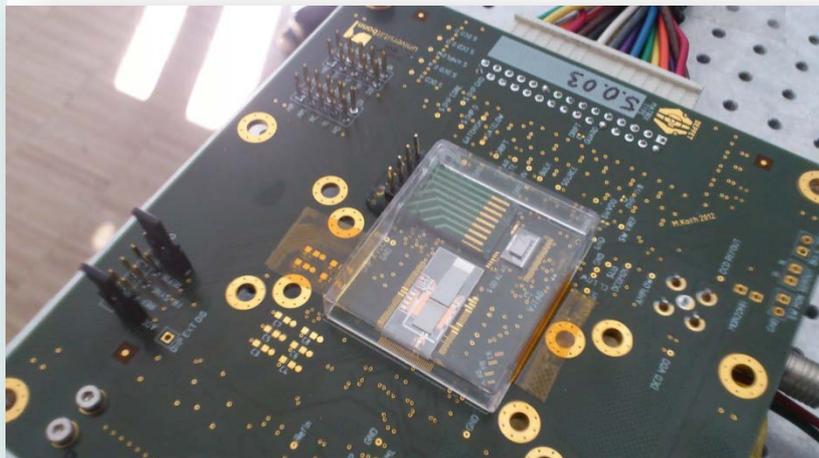
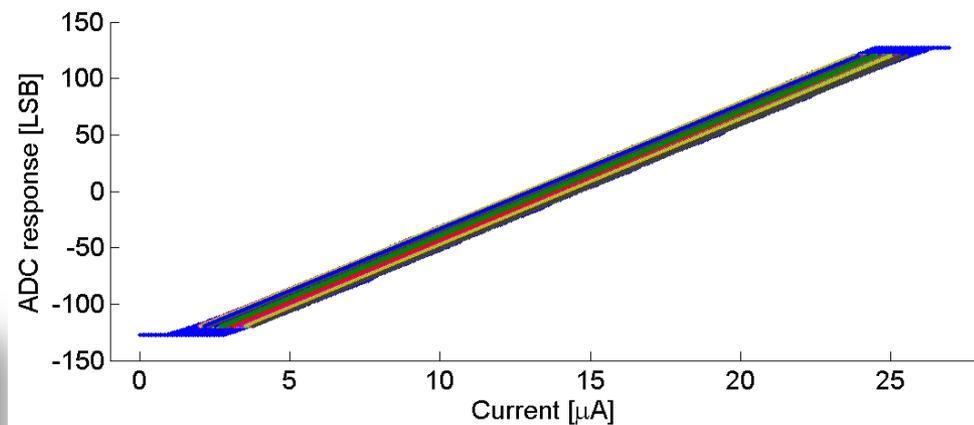


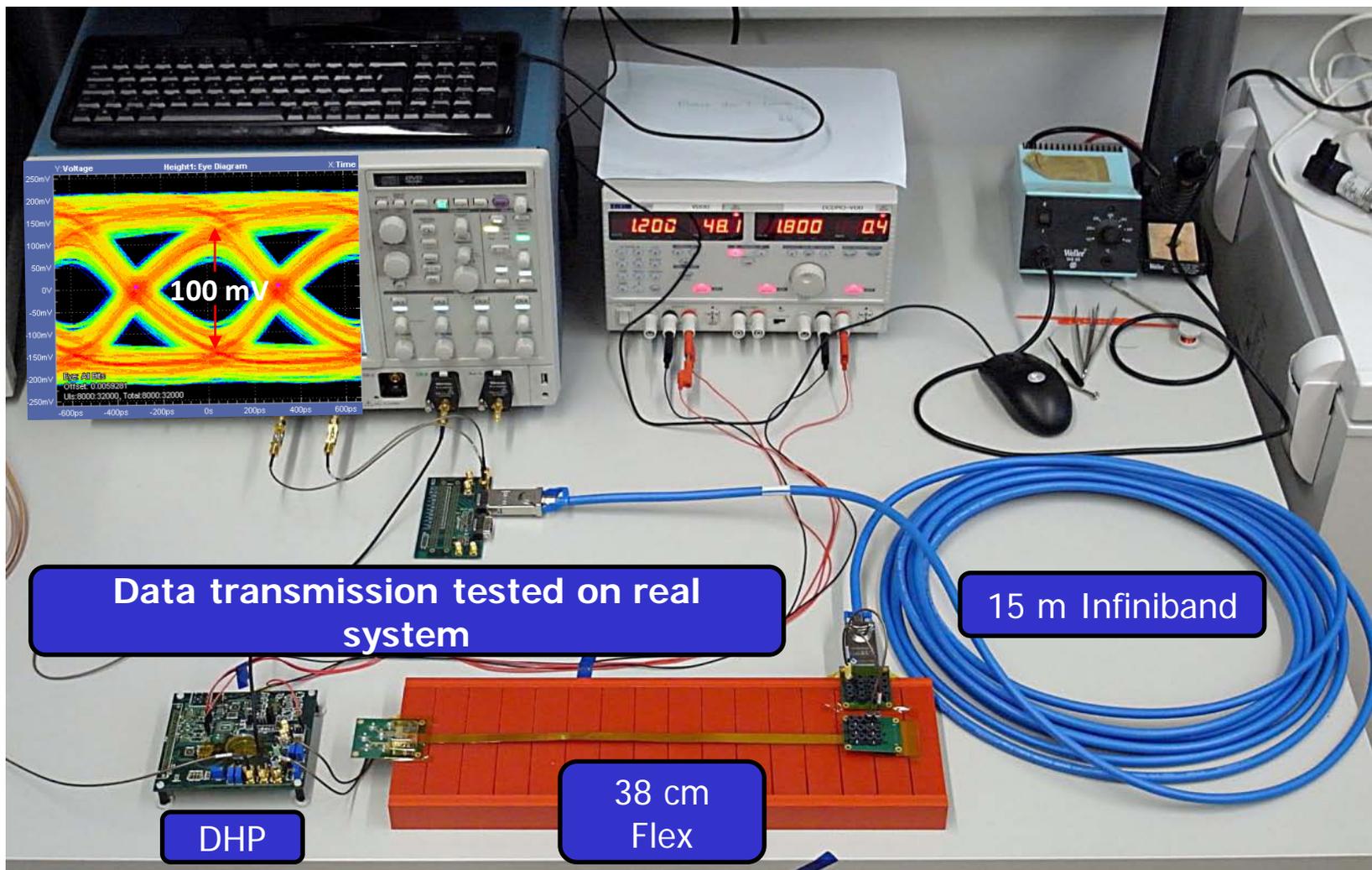
Photo of the hybrid 5 (without DEPFET matrix)

ADC vs Input current, all channels



DCDB and DHP can communicate at full speed

● Data Handling Processor (DHP) - Performance

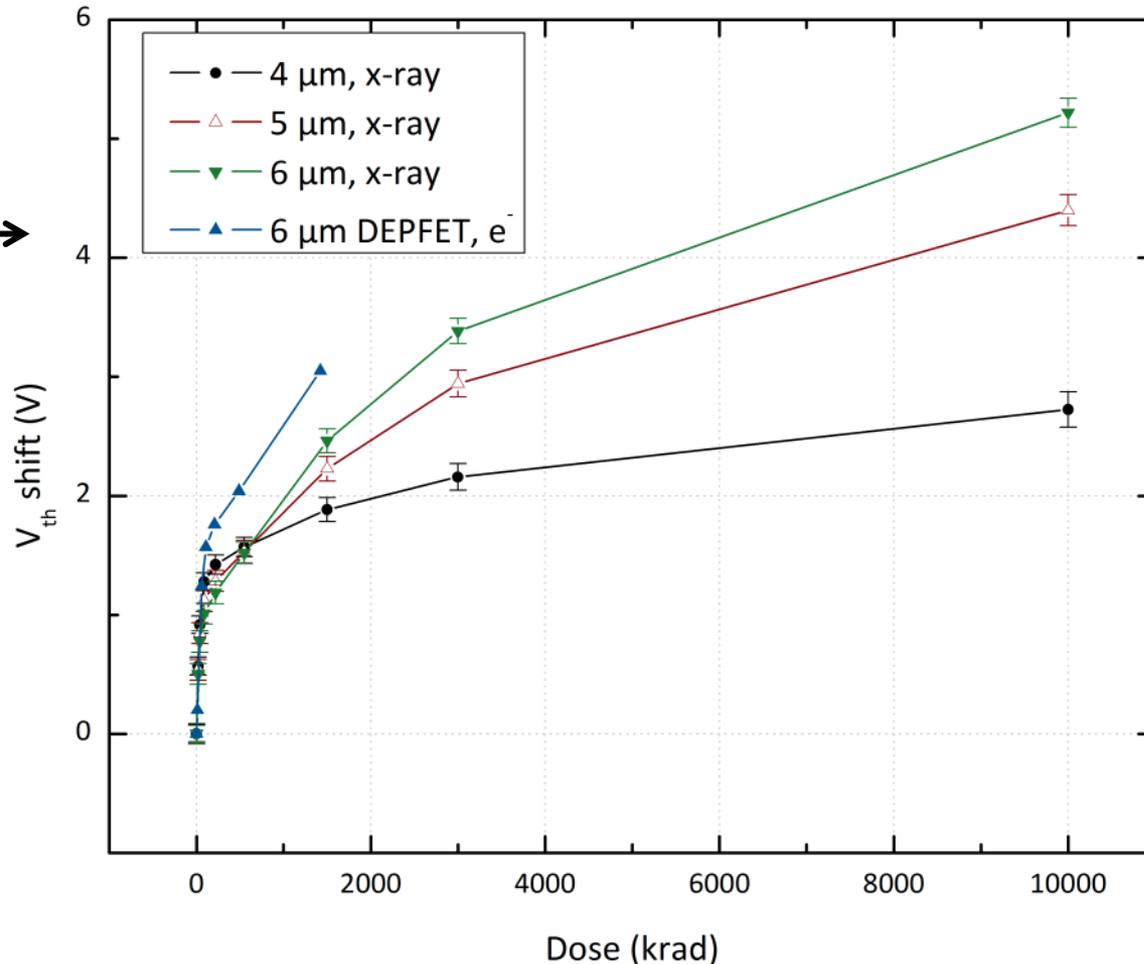


+ pre-emphasis

Irradiated (100 Mrad) DHPT 0.1, can drive 15 m of Infiniband cable

DEPFET Sensor Radiation Hardness

Small enough to be compensated by the system →

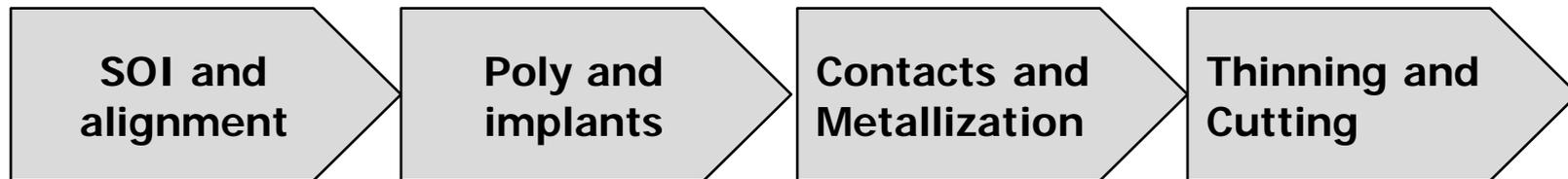


Optimal oxide thickness. Trade of between:

- Threshold voltage shift
- Internal amplification

A. Ritter, et al.
DOI:10.1016/j.nima.2013.04.069

● DEPFET Production for Belle II



>20 mask steps

Done:

- SOI wafer sandwich
- Top side production
 - 2 polysilicon layer
 - 14 masks steps
 - 10 implantations

To be done:

- 2 Al layer
- 1 Cu Layer
- backside thinning
- passivation
- 7 mask steps remaining

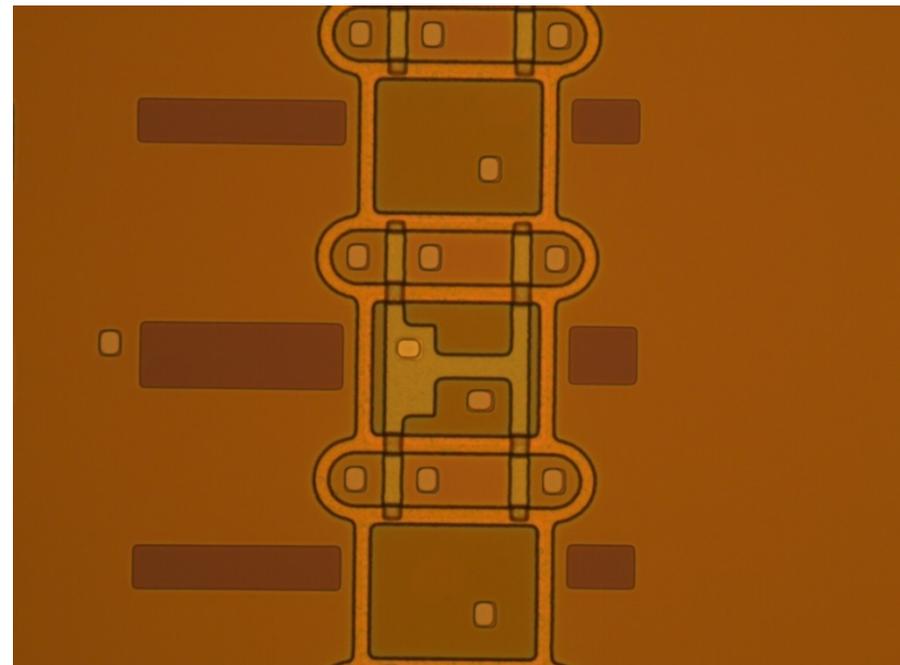
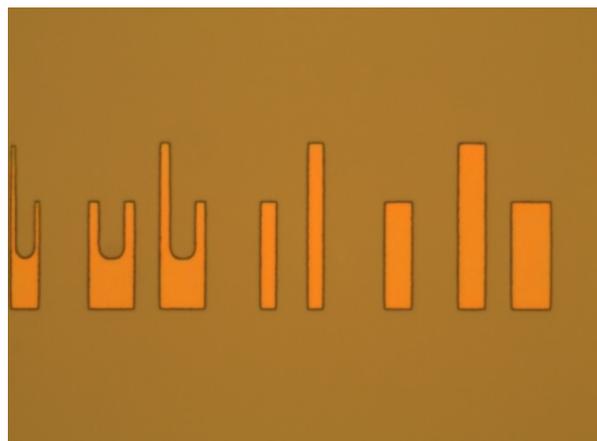
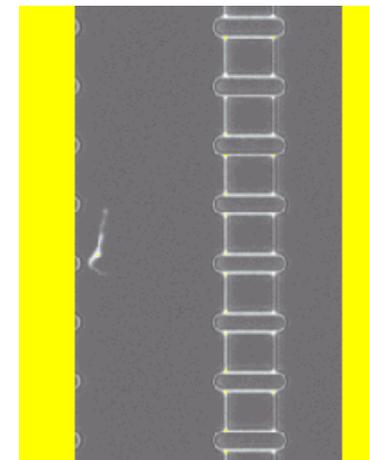
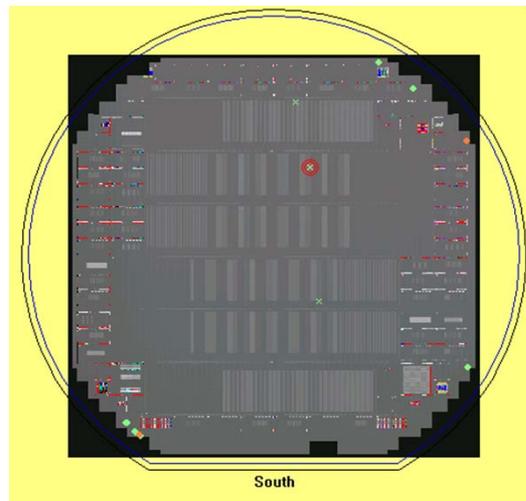


Photo shows the 2 poly silicon layers and the contacts to the silicon bulk and poly silicon

● Metrology and Inline Inspection

Muetec Optical Inspection Tool



- Contamination monitoring
- Layer thickness control & Line width control
- During the fabrication process:
all wafers are scanned by Muetec for each mask step
- Yield Estimate: defects are counted, classified and assigned to chips

● Yield Estimation

Modules	Mark						Needed
	0	1	2	3	4	5	
Inner fwd	14	4	2	2	1	6	8
Inner bwd	10	8	2	2	1	6	8
Outer fwd	31	10	4	2	0	11	12
Outer bwd	22	7	9	5	3	12	12

Giving marks (lowest is best)

0 – no severe defects

1 – single pixel

2 – single rows and columns

3 – whole module affected?

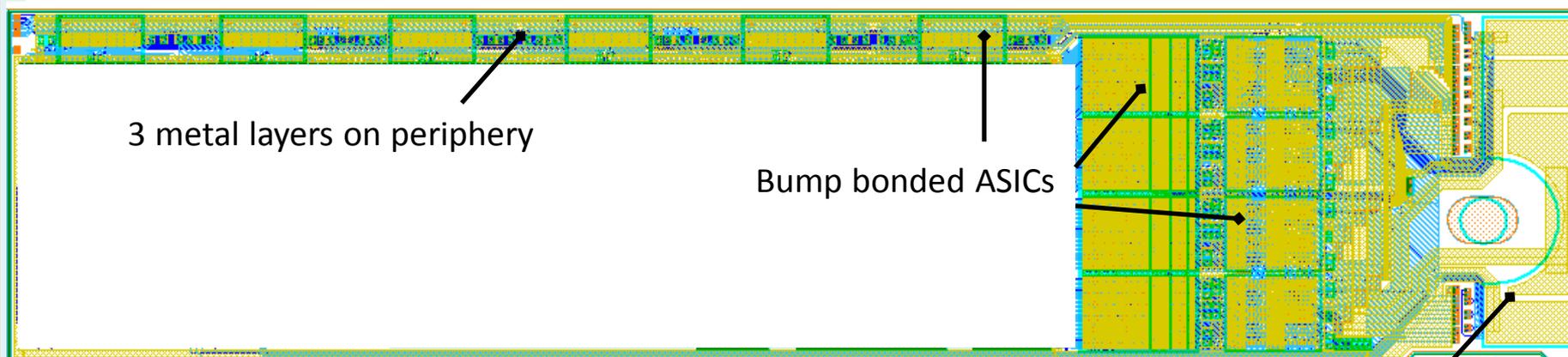
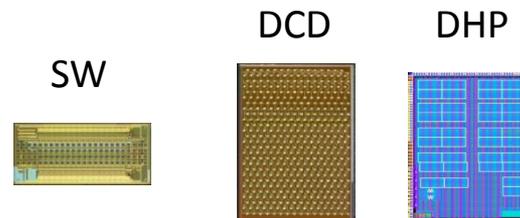
4 – whole module killed

5 – to be clarified

- **PXD9 production is well on track**
- Numbers are based on optical inspections and best knowledge but still they are an estimate only
- Next processing steps are the deposition and structuring of the metal system (aluminum and copper)
- EMCM to prove technology and to operate the control and readout ASICs already now on the All-Silicon-Module

● Electric Multi Chip Module (EMCM)

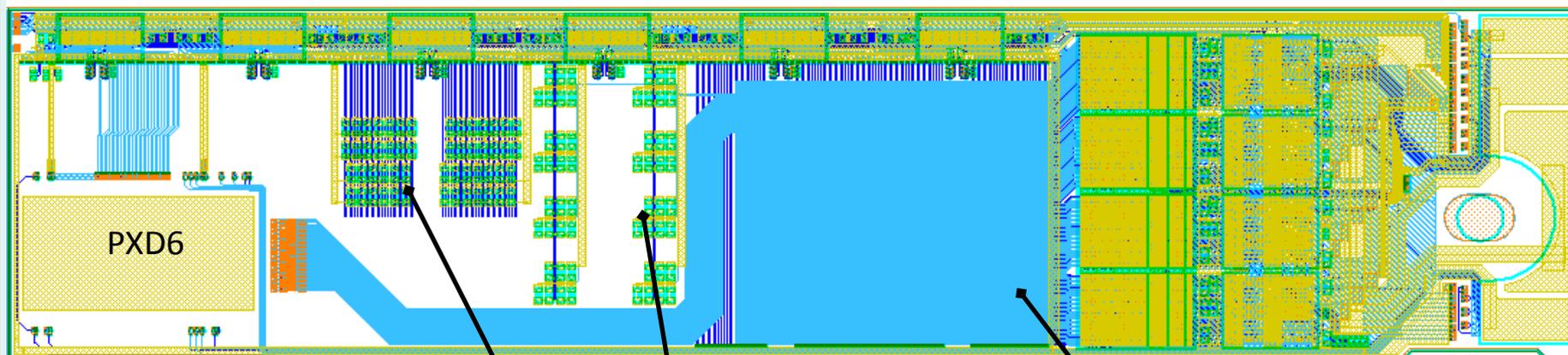
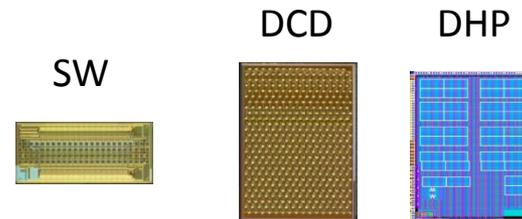
EMCM: Everything but the DEPFET
 Electrically active prototype of a half ladder



4 layer kapton cable attached and wire bonded to Si-Module for I/O and power

● Electric Multi Chip Module (EMCM)

E-MCM: Everything but the DEPFET
 Electrically active prototype of a half ladder



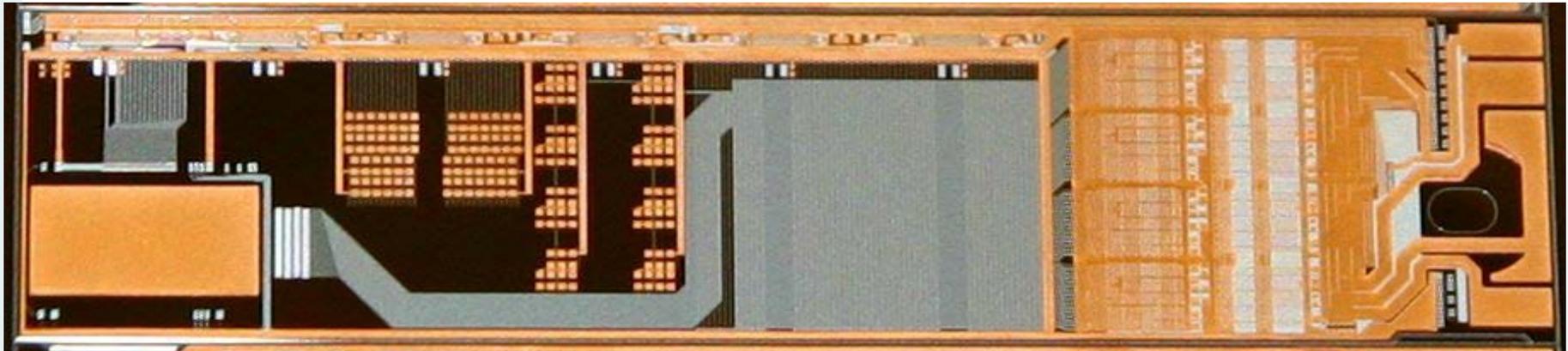
Capacitors for SW tests
 Circuitry for DEPFET emulation
 Long drain lines to DCD

- Metal system as close as possible to final → Electrical information
- Commissioning: Flip chip, discrete components and kapton attachment

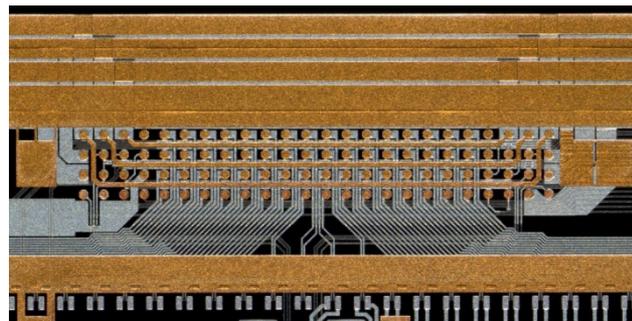
- Electric Multi Chip Module (EMCM)

EMCM in reality

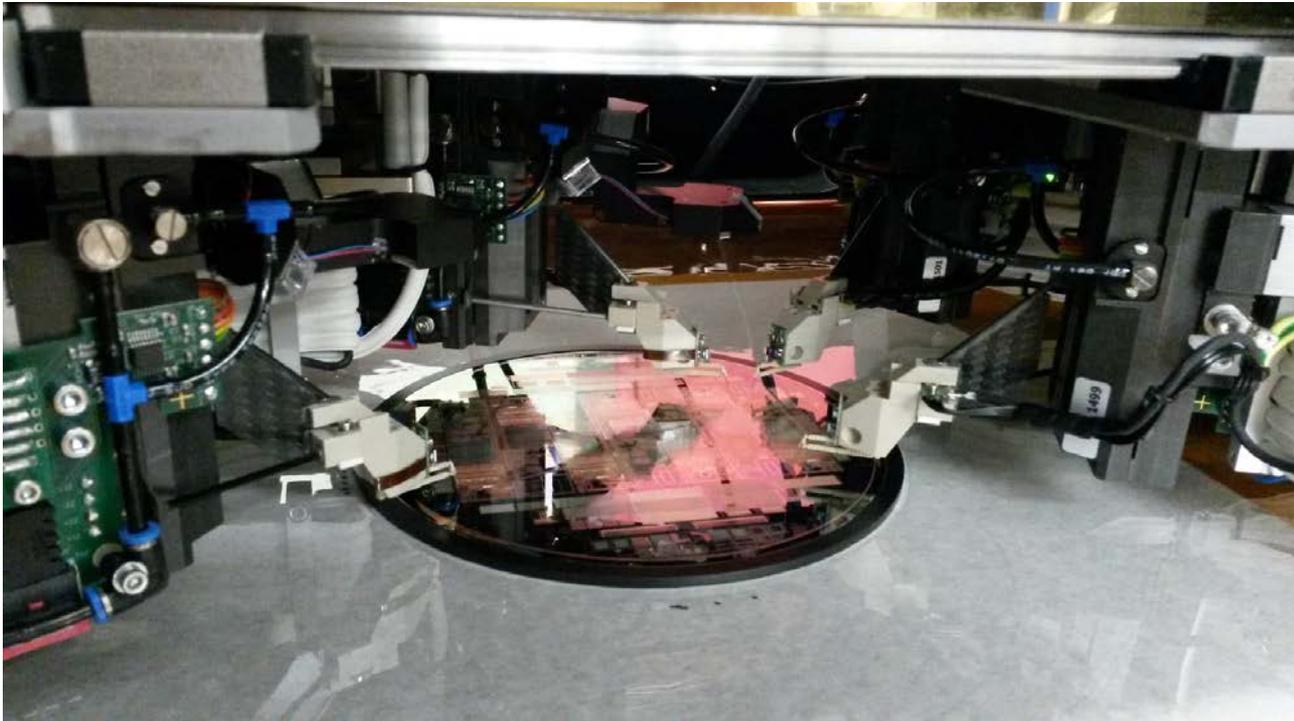
→ Modules produced, tested and flip chipped



Detail of the
Switcher landing
area



● EMCM Substrate Testing

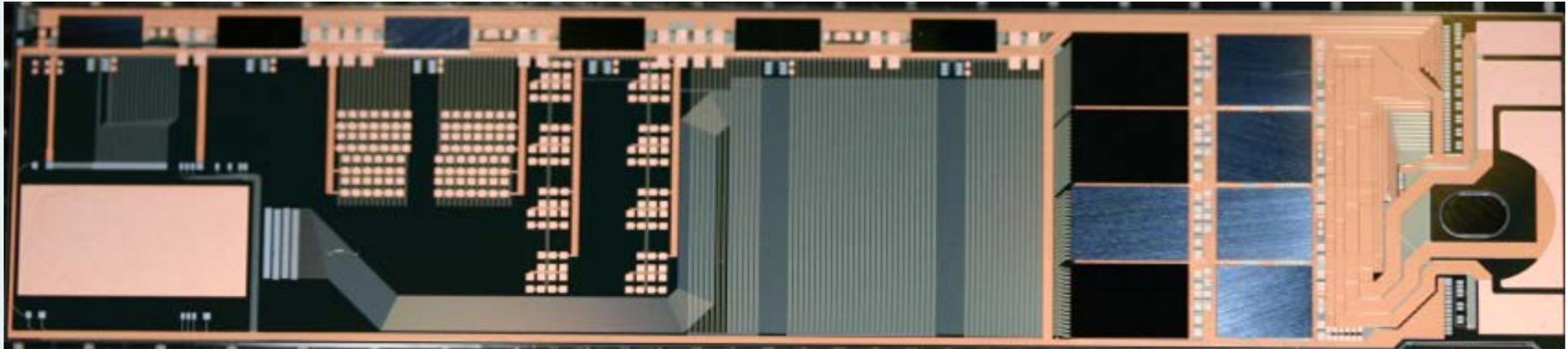


- Test of the EMCM substrate is done with flying probe system
 - one EMCM test contains 2406 Open Tests, >110k test of neighboring lines for shorts
- The chosen technology for the DEPFET production passed the open and short test for more than 20k open and 900k short test

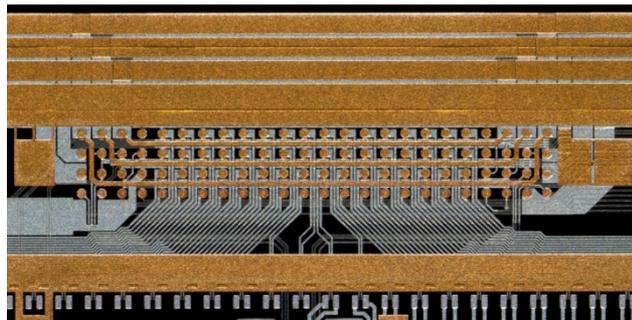
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EMCM in reality

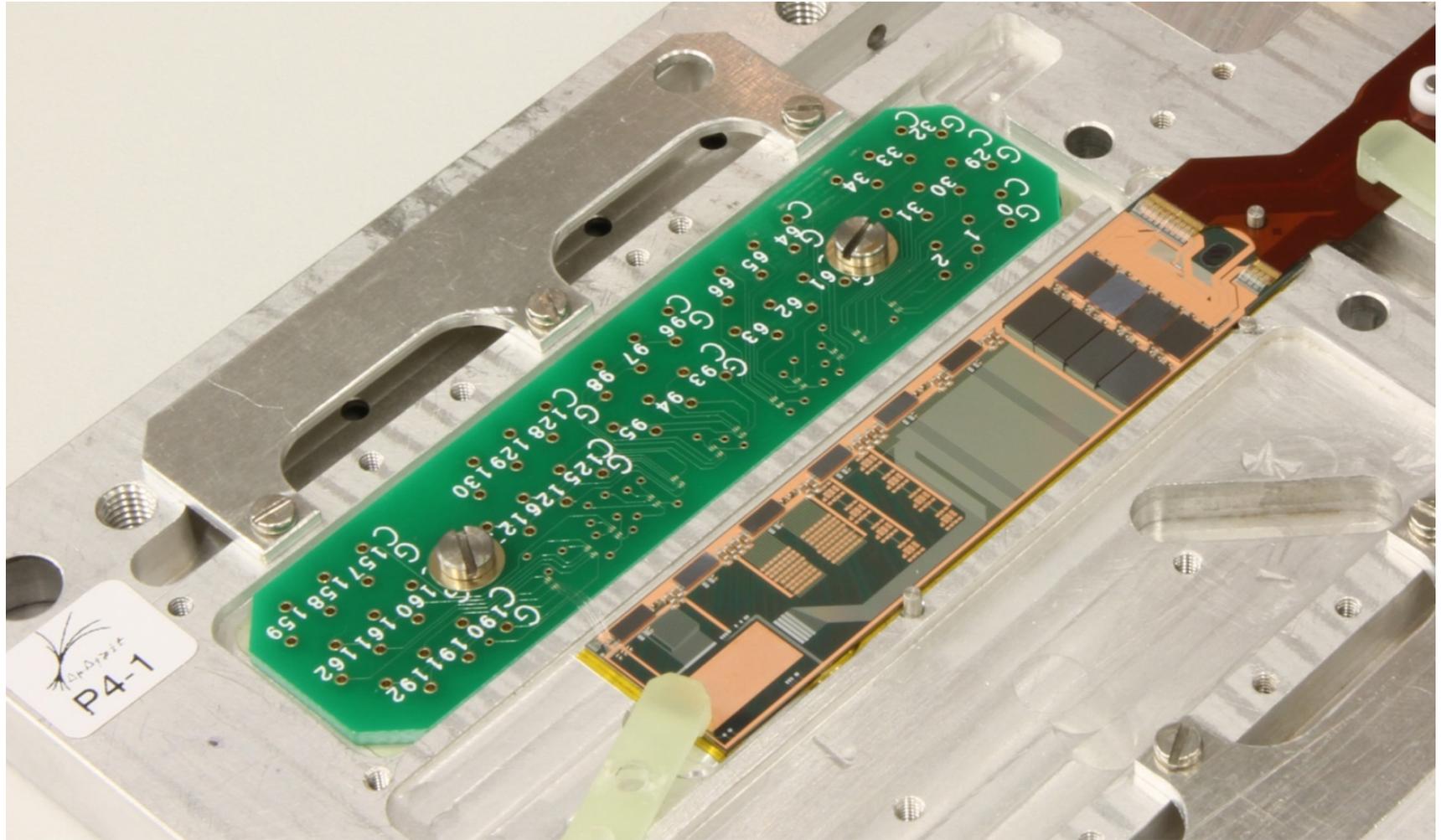
→ **Modules produced, tested and flip chipped**



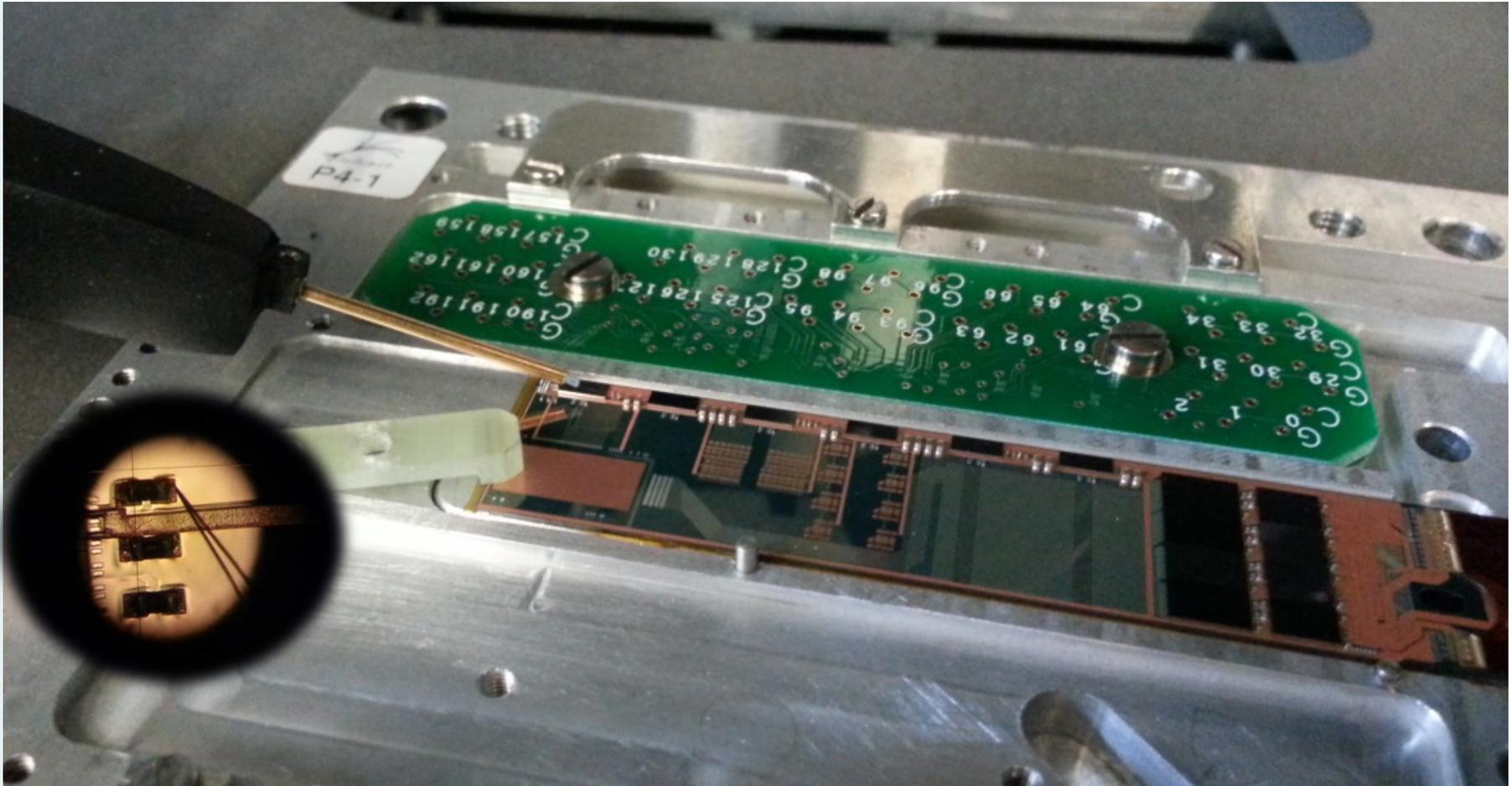
Detail of the
Switcher
landing area



- EMCM – Fully Assembled with Kapton



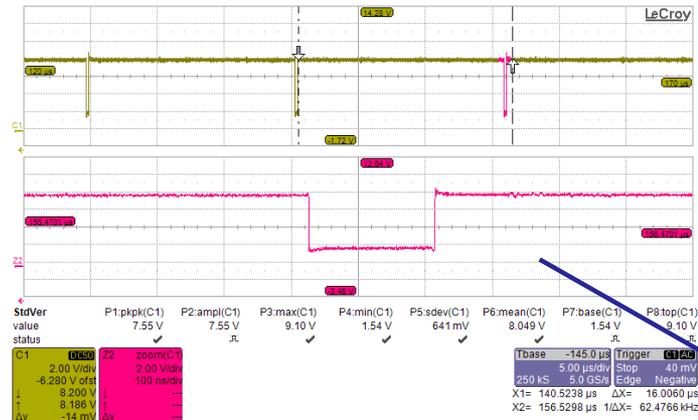
- Fully assembled EMCM



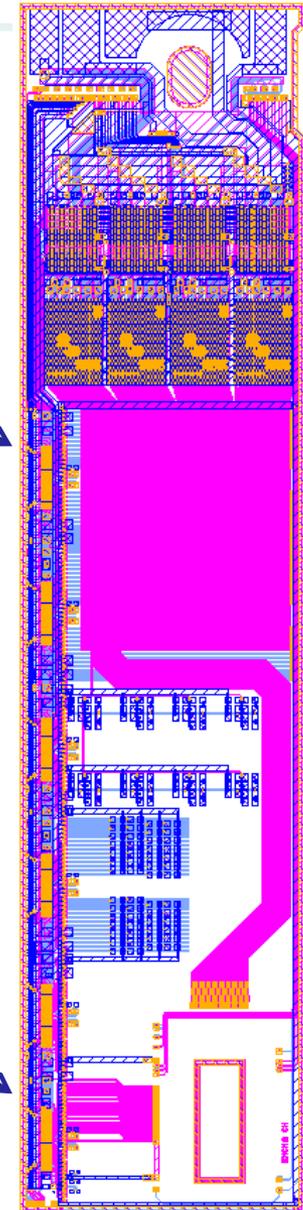
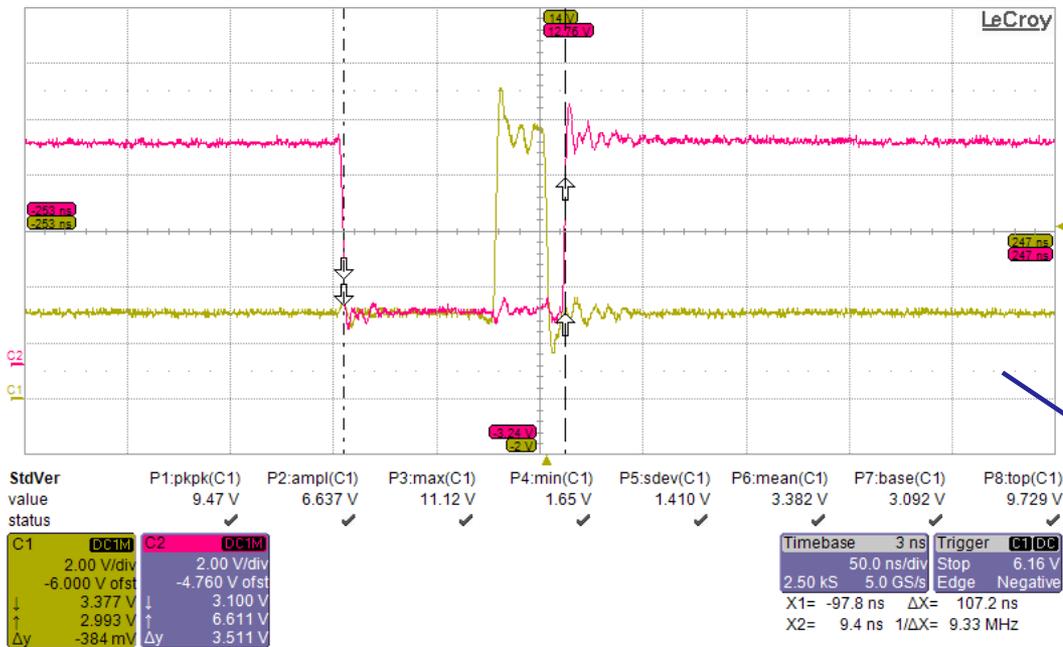
Probing SwitcherB control signals and outputs

● Switcher #1 - #3 Gate Outputs

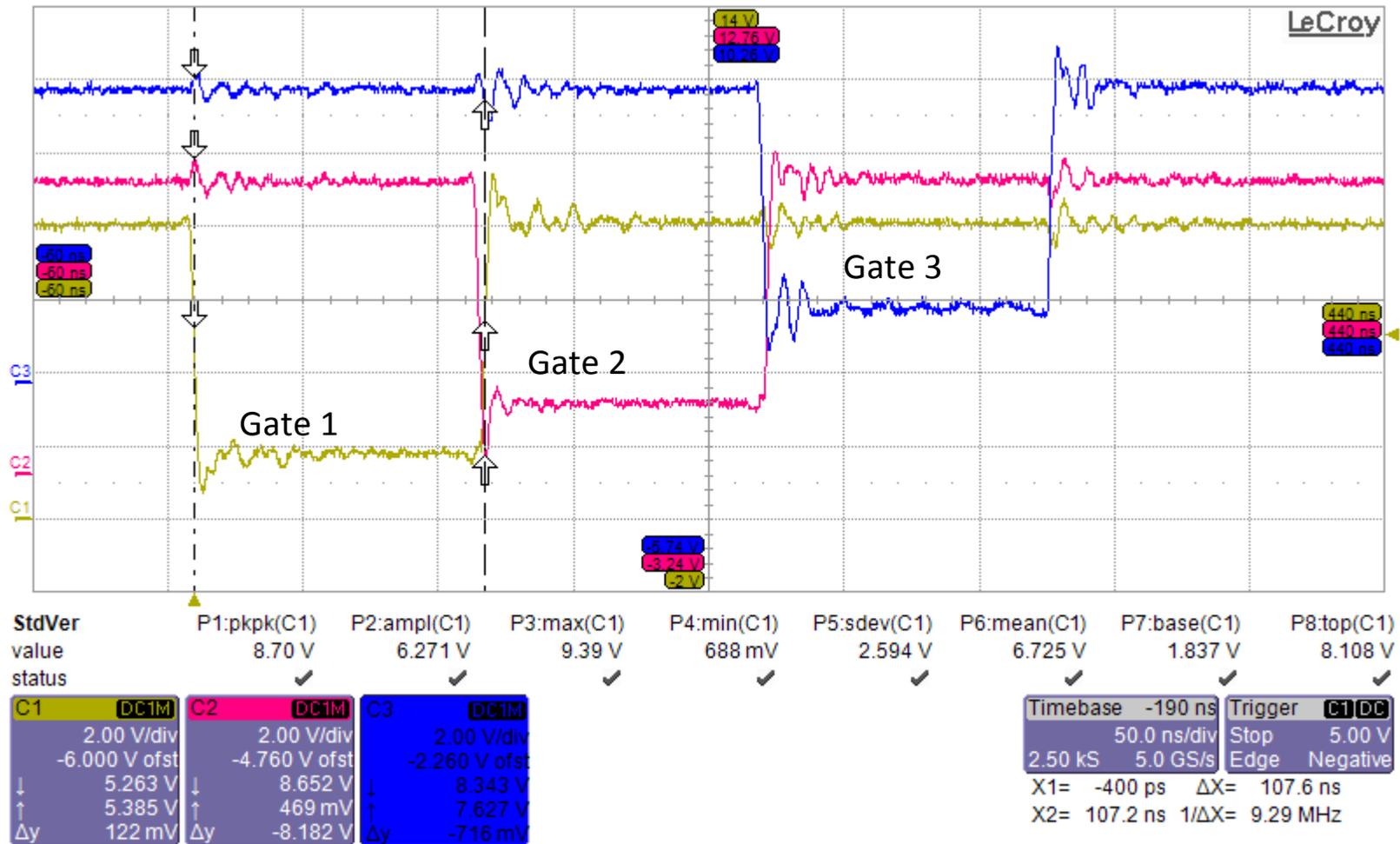
SWB #1



SWB #6

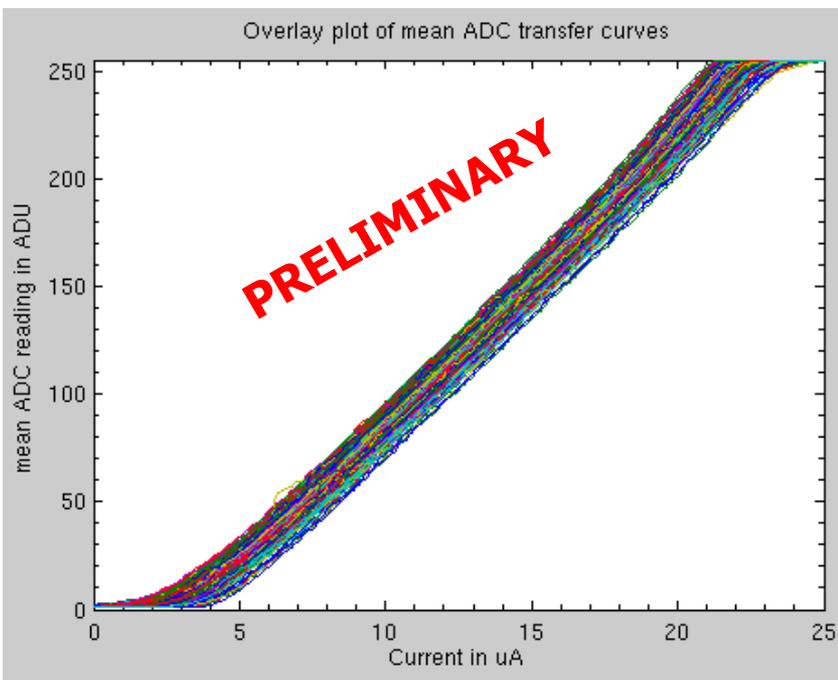


Three consecutive Gates – SWB #6

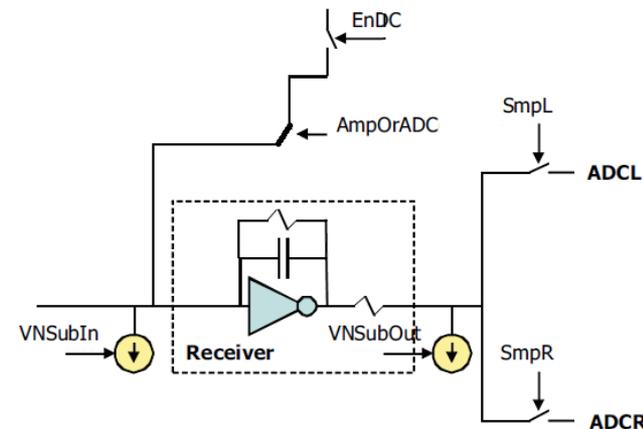


GateOn Time 108ns (DHP clock 76.2MHz)

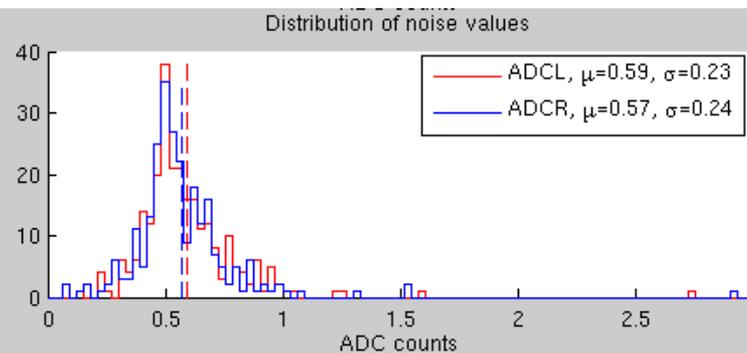
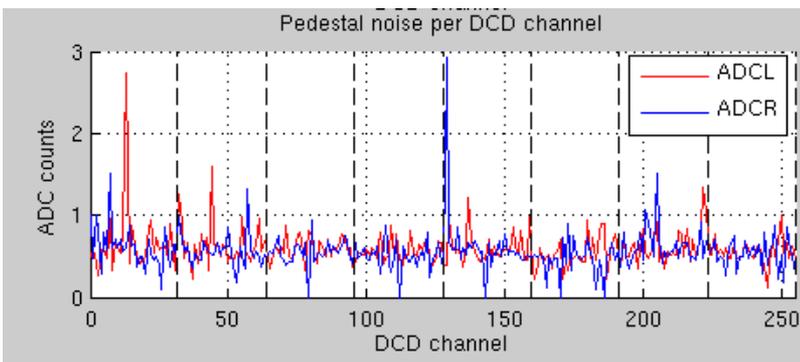
DCD-B Operation on EMCM



Keithley 2400 SMU 0 ... 25 μA , 0.1 μA steps

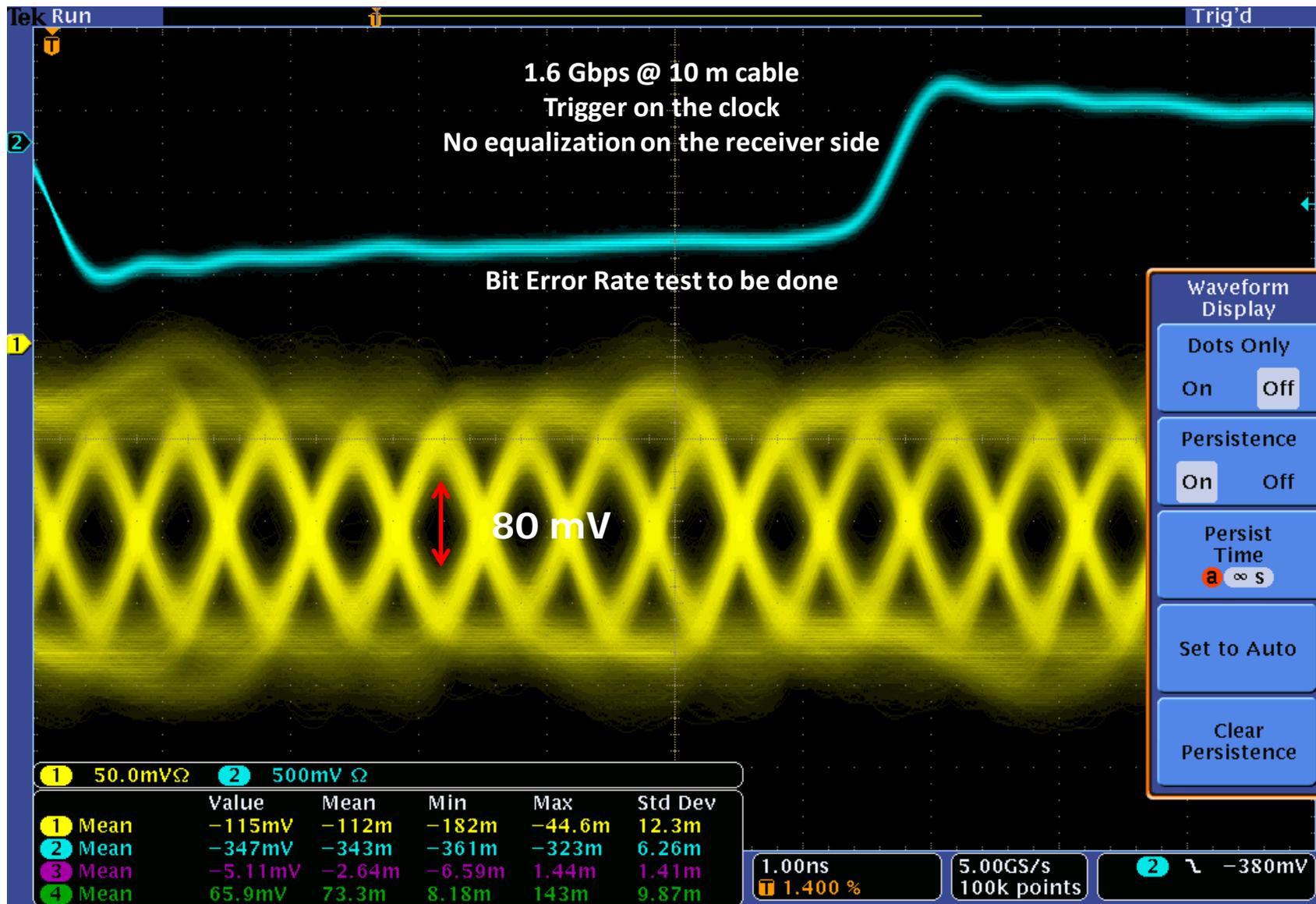


- DCD-B operated with 250MHz on EMCM
- Not optimized DAC settings and bias voltages**



Noise of DCDB ≈ 0.6 ADU $\triangleq 46\text{nA}$

- DHP Serial Link: EMCM – Kapton – 10m cables



● Summary: Electronics for a DEPFET Vertex Detector



- Control- and Readout ASICs are designed, fabricated and tested
 - Functionality, Speed, Radiation hardness are validated

- DEPFET Ladder production for Belle II is well on track
- EMCM proofs the metal system and interconnection technology
- Fully populated EMCM assembled and tested
 - All ASICs functional
 - Timing for Belle II can be achieved

- ASICs are designed for Belle II but fulfil most of the ILC requirements
- Belle II sensor production paves the way for the ILC sensor production

Thank you!