# The Electronics of the CMS Outer Tracker Upgrade

CMS Upgrade School

17-21 Nov 2014

Francois Vasey

Thanks to many CMS Tracker collaborators, too numerous to acknowledge individually.

ACES-2014: https://indico.cern.ch/event/287628/

TWEPP-2014: https://indico.cern.ch/event/299180/

ECFA-2014: https://indico.cern.ch/event/315626/

# I) The Electronics of the CMS Outer Tracker Upgrade

PH-ESE Seminar

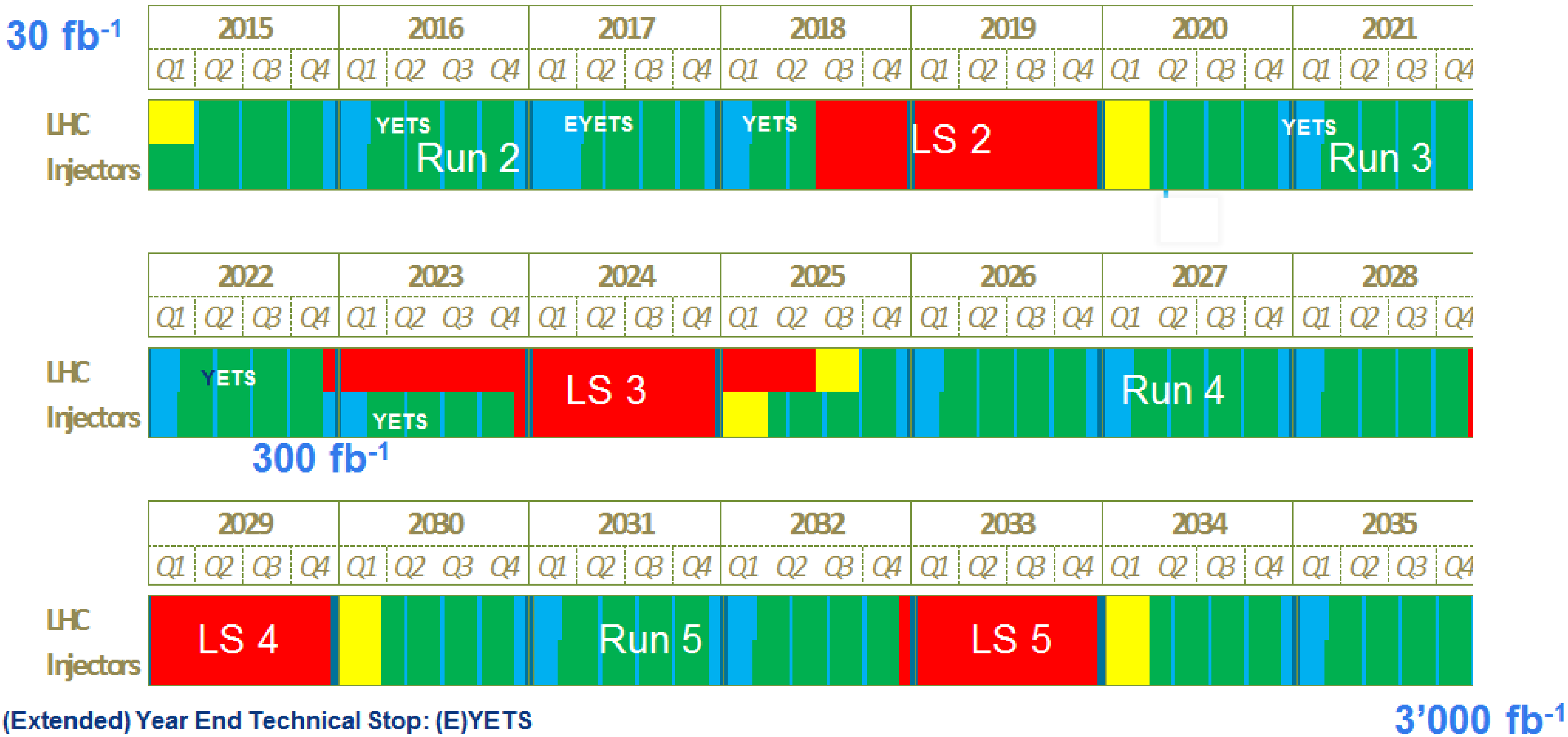
Francois Vasey

Slide material from: F. Bordry, D. Contardo,
G. Hall, S. Mersi, and many others

# LHC Roadmap: Schedule beyond LS1

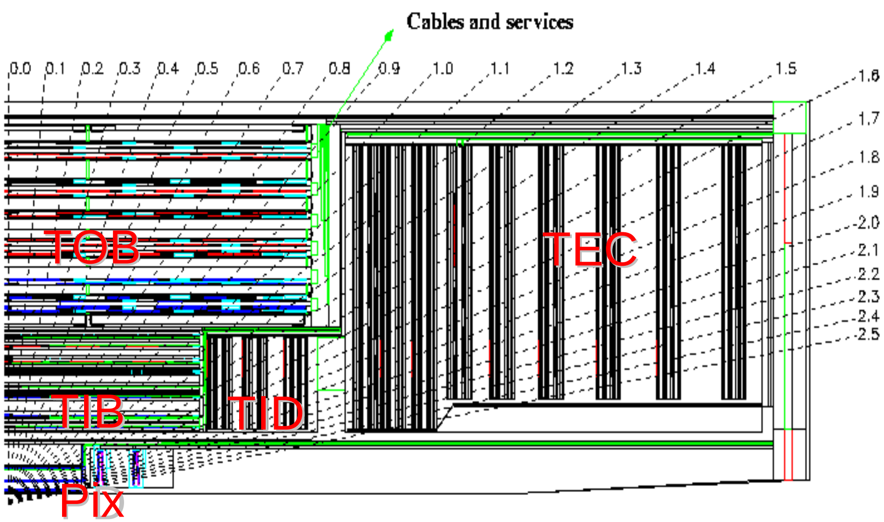
LS2 starting in 2018 (July) => 18 months + 3 months BC
LS3 LHC: starting in 2023 => 30 months + 3 months BC
Injectors: in 2024 => 13 months + 3 months BC

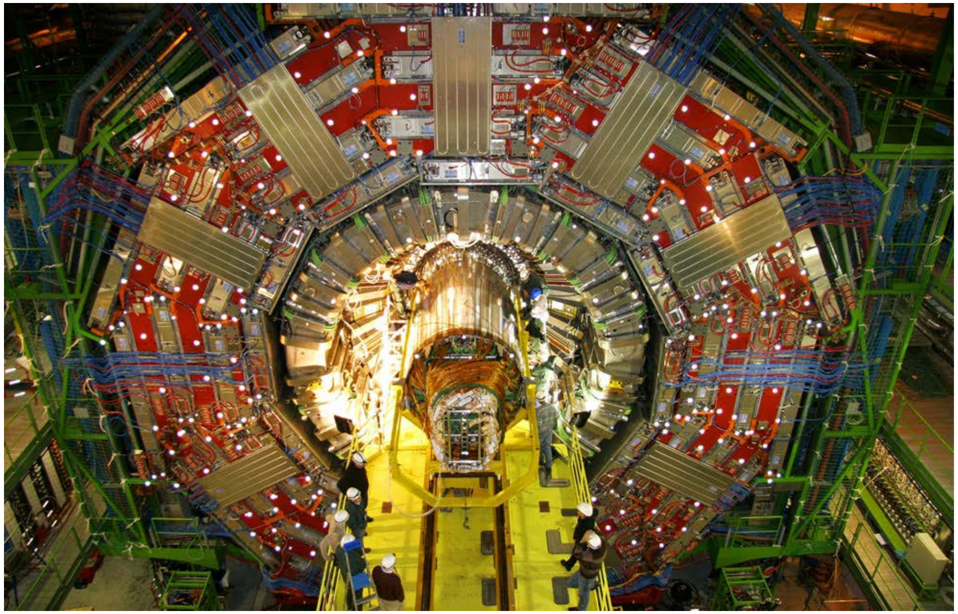
Physics
Shutdown
Beam commissioning
Technical stop




(Extended) Year End Technical Stop: (E)YETS

# The present CMS Tracker



| Microstrip tracker | Pixels |
|---|---|
| ~210 $m^2$ of silicon, 9.3M channels | ~1 $m^2$ of silicon, 66M channels |
| 73k APV25s, 38k optical links, 440 FEDs | 16k ROCs, 2k olinks, 40 FEDs |
| 27 module types | 8 module types |
| ~34kW | ~3.6kW (post-rad) |

# Requirements to Phase II Tracker

| | | |
|---|---|---|
| Survive **∫L.dt = 3000 $fb^{-1}$** | **Radiation hardness** **Operating cold** (-20°C) | O(1MGy, 1E15 n/$cm^2$) |
| Higher L1A rate → **> 500 kHz** | **Bandwidth!** | O(10 Tbps) |
| Resolve **<μ>=140** → 200 | **Higher granularity** | Short Strips & Macro Pixels |
| Latency → **> 10 μs** | Larger front-end **buffers** | O(0.5kb deep buffers per cell) |
| Ensure **experiment lifetime** | **Redundancy** for Outer Tracker Possible **extraction** for Pixels | O(10yrs) |
| **Improve tracking** at high pT | **Increase granularity** | O(250M channels) |
| **Improve tracking** at low pT Reduce **secondary interactions** | **Reduce material** | Low mass, New Layout |
| **Increase forward acceptance** | Mostly through **pixel layout** | |
| **Improve CMS trigger** | **Provide tracking to Level-1** 40 MHz output for L1 | Module-level Stub Finding |

# Requirements to Phase II Tracker

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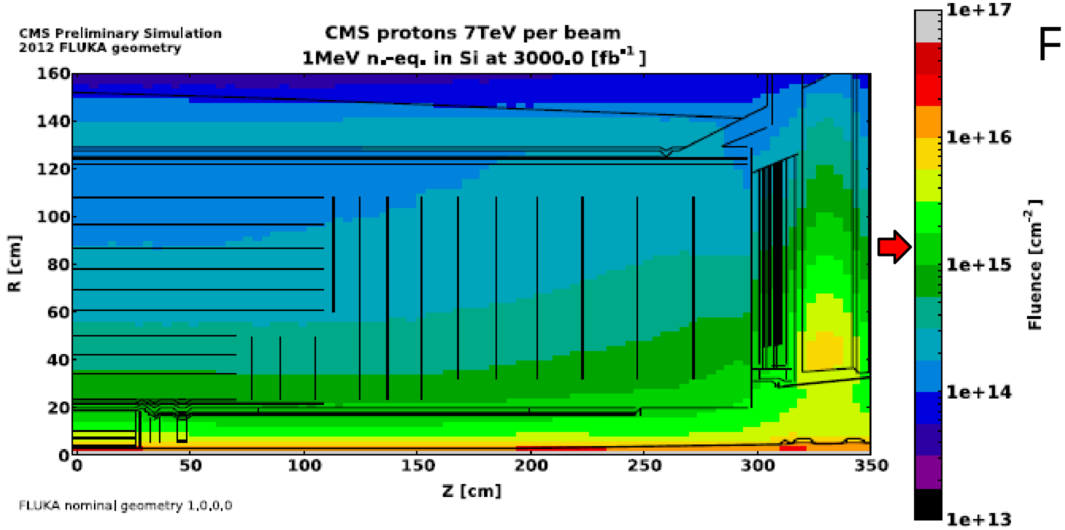
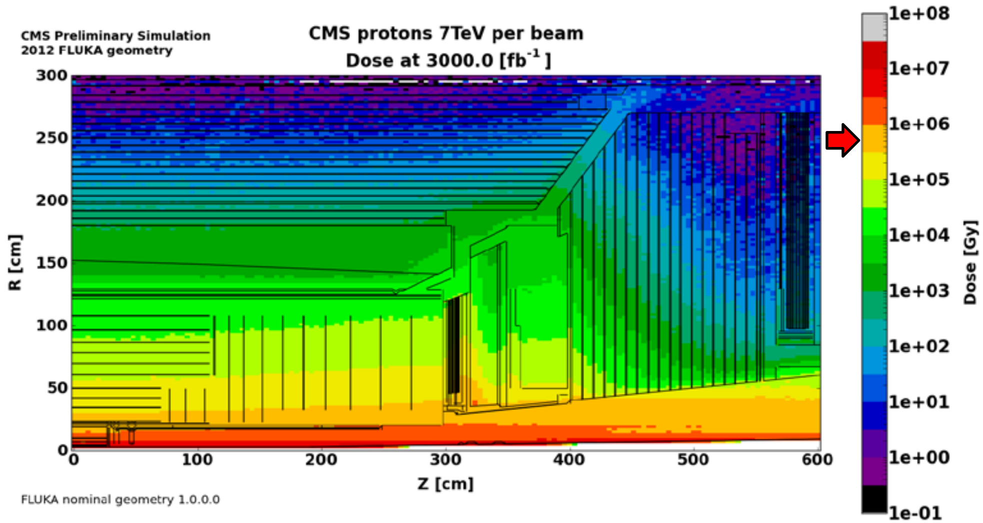
| **Improve CMS trigger** | **Provide tracking to Level-1**<br>40 MHz output for L1 | Module-level Stub Finding | c) |

# a) Radiation Fields at 3000 $fb^{-1}$

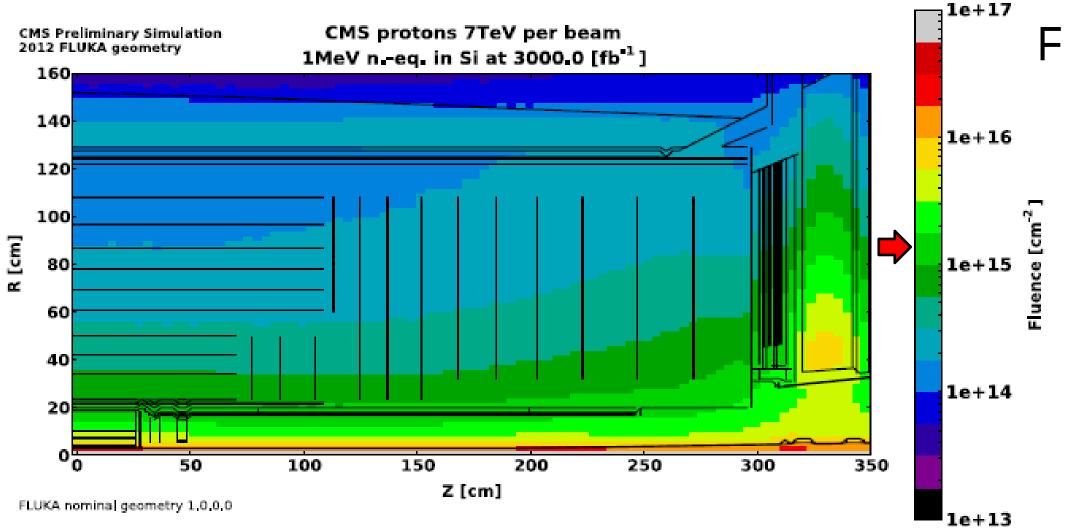



Fluence O(1E15 n/cm²)

Dose O(1MGy)

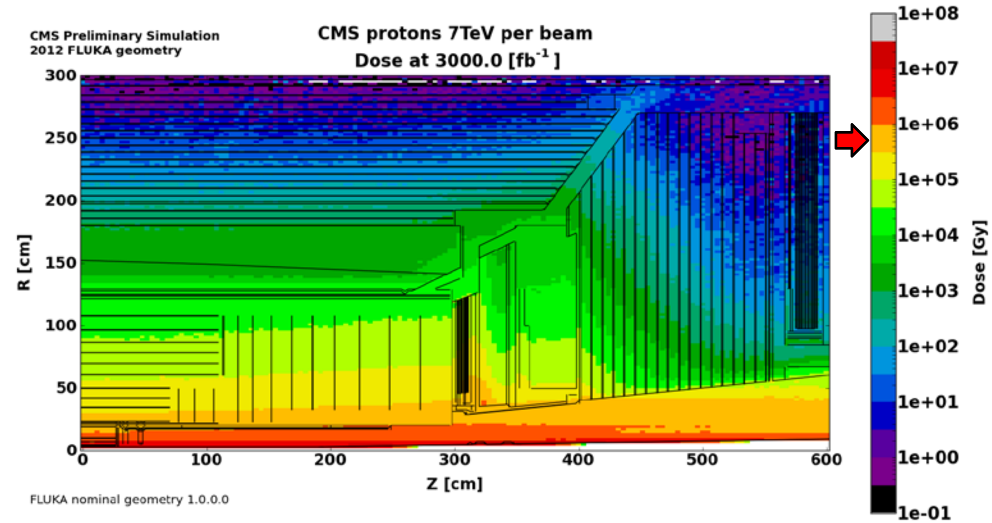


# a) Radiation Fields at 3000 fb$^{-1}$




Fluence O(1E15 n/cm$^2$)

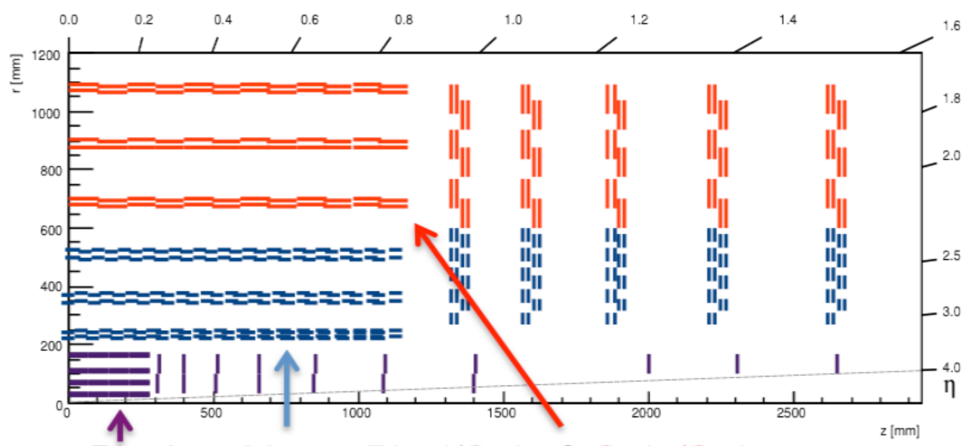
Dose O(1MGy)




Radiation testing and qualification
not part of this talk.

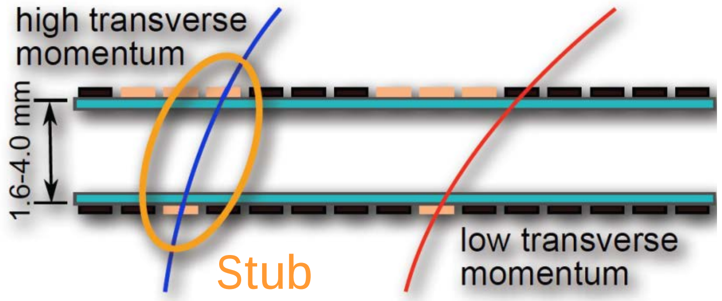
# b) CMS Phase II Tracker Layout

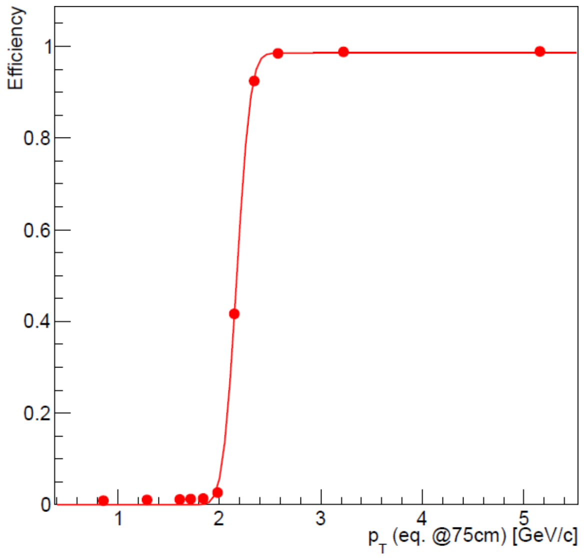
- High Granularity with short strips and small pixels
  - Strip pitch ~90-100µm & length ~ 2.5 to 5 cm
- Light detector with DC/DC powering, CO2 cooling, light module assembly
- Powerful concept to implement tracks in hardware trigger
  - 2 sensor modules to select track "stubs" of Pt≥2GeV for trigger readout (40MHz) Strip-Strip (SS) in outer layers and Macro Pixel-Strip (PS) in inner (z meas.)
- Extension of Pixel coverage up to |η| ~ 4
  - Reduce rate of fake jets due to PU for VBF/VBS physics

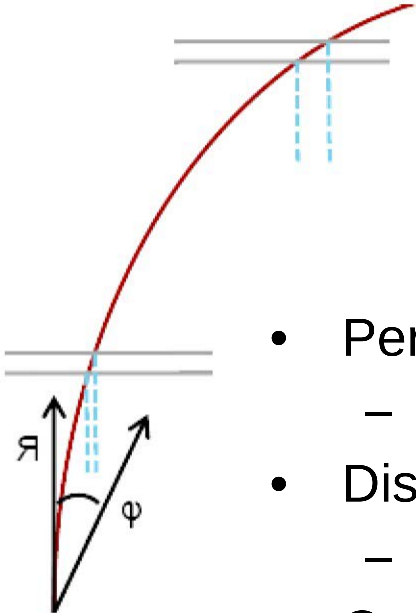



Pixels - Macro-Pixel/Strip & Strip/Strip
7100 Modules with z info
8400 Modules

# c) Pt Modules for Stub Finding



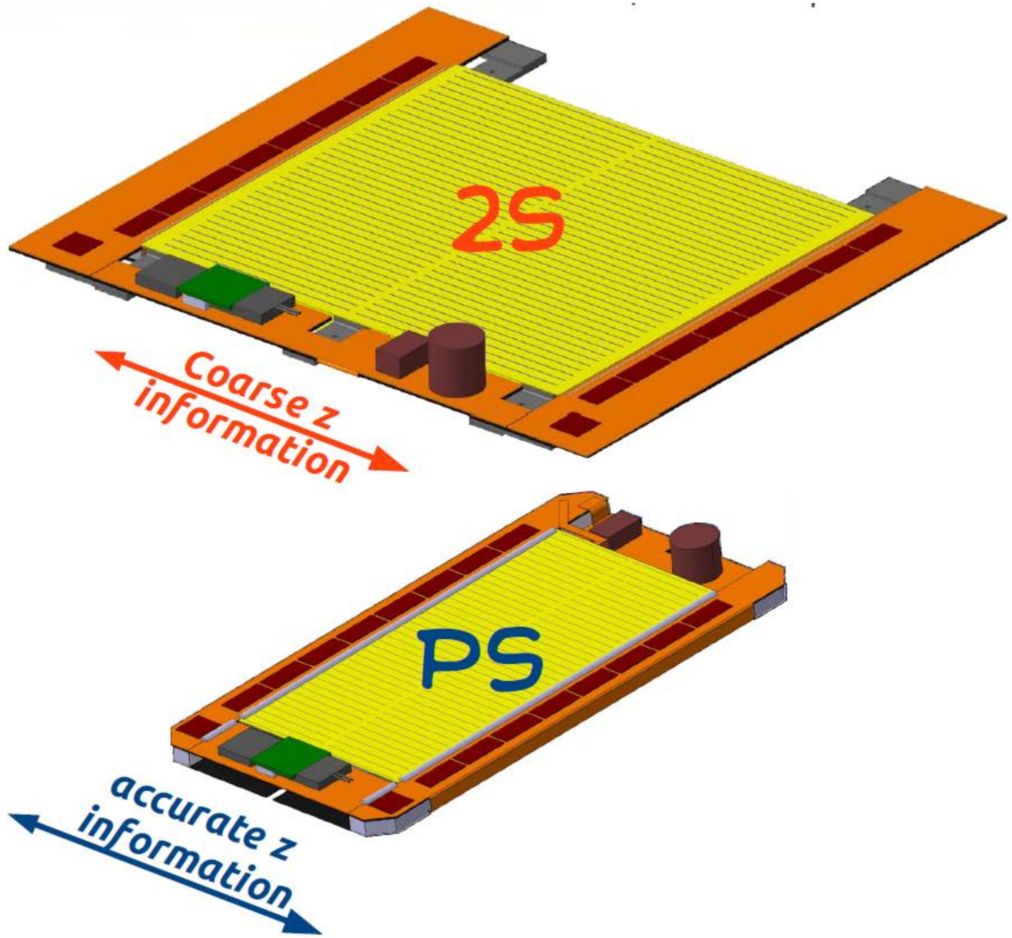

- Perform correlation locally
  - Adjust window according to R
- Discard tracks below ~2GeV
  - Keep threshold tunable
- One order of magnitude data reduction
- Possible thanks to strong CMS B-field

# Pt Modules for Outer Tracker

Each Module is an independent tile with its own services

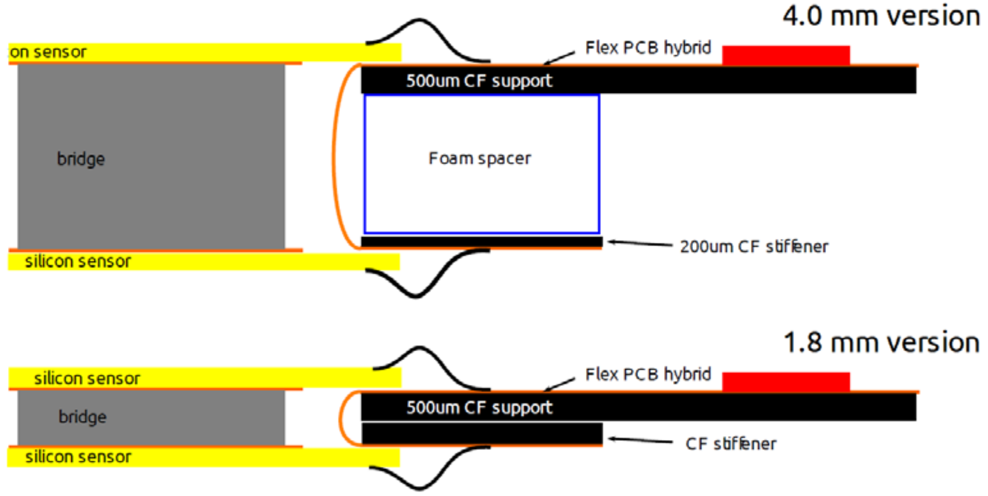
**2 Strip sensors**
**Strips**: 5 cm × 90 µm
**Strips**: 5 cm × 90 µm
P ~ 4W
~ 92 cm² active area
For r > 40 cm

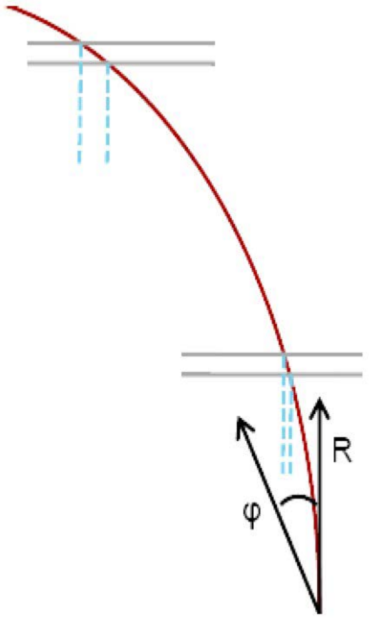
**Pixel + Strip sensors**
**Strips**: 2.5 cm × 100 µm
**Pixels**: 1.5 mm × 100 µm
P ~ 6-8W
~ 44 cm² active area
For r > 20 cm



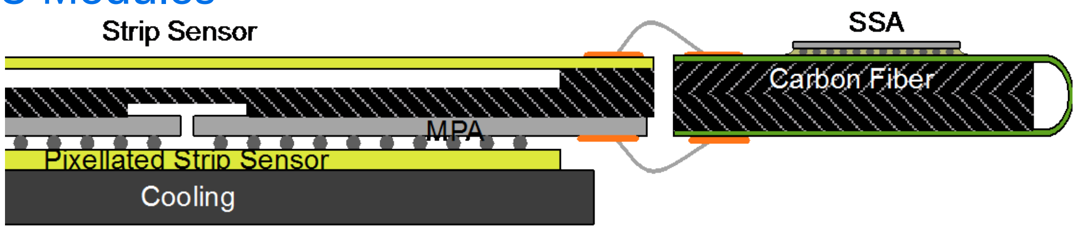
# Sensor Interface to FE Electronics

## 2S Modules

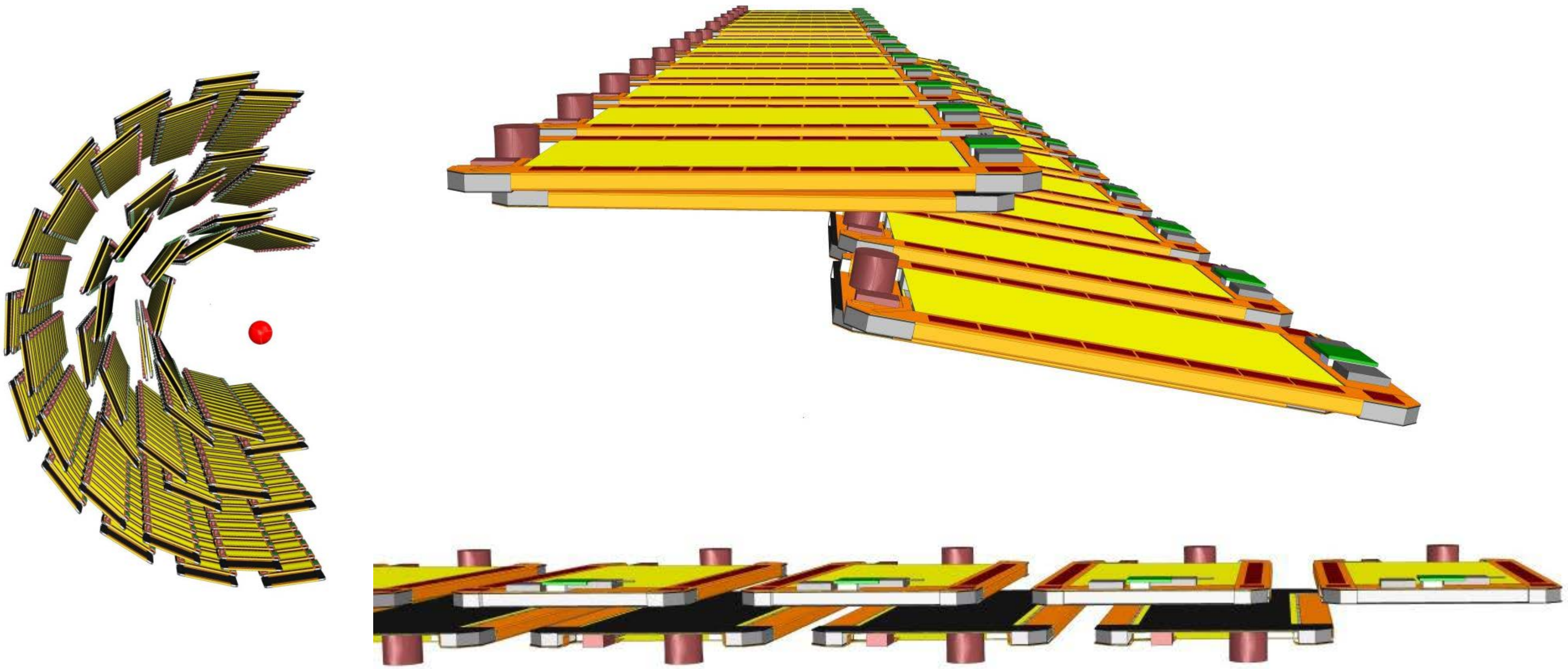


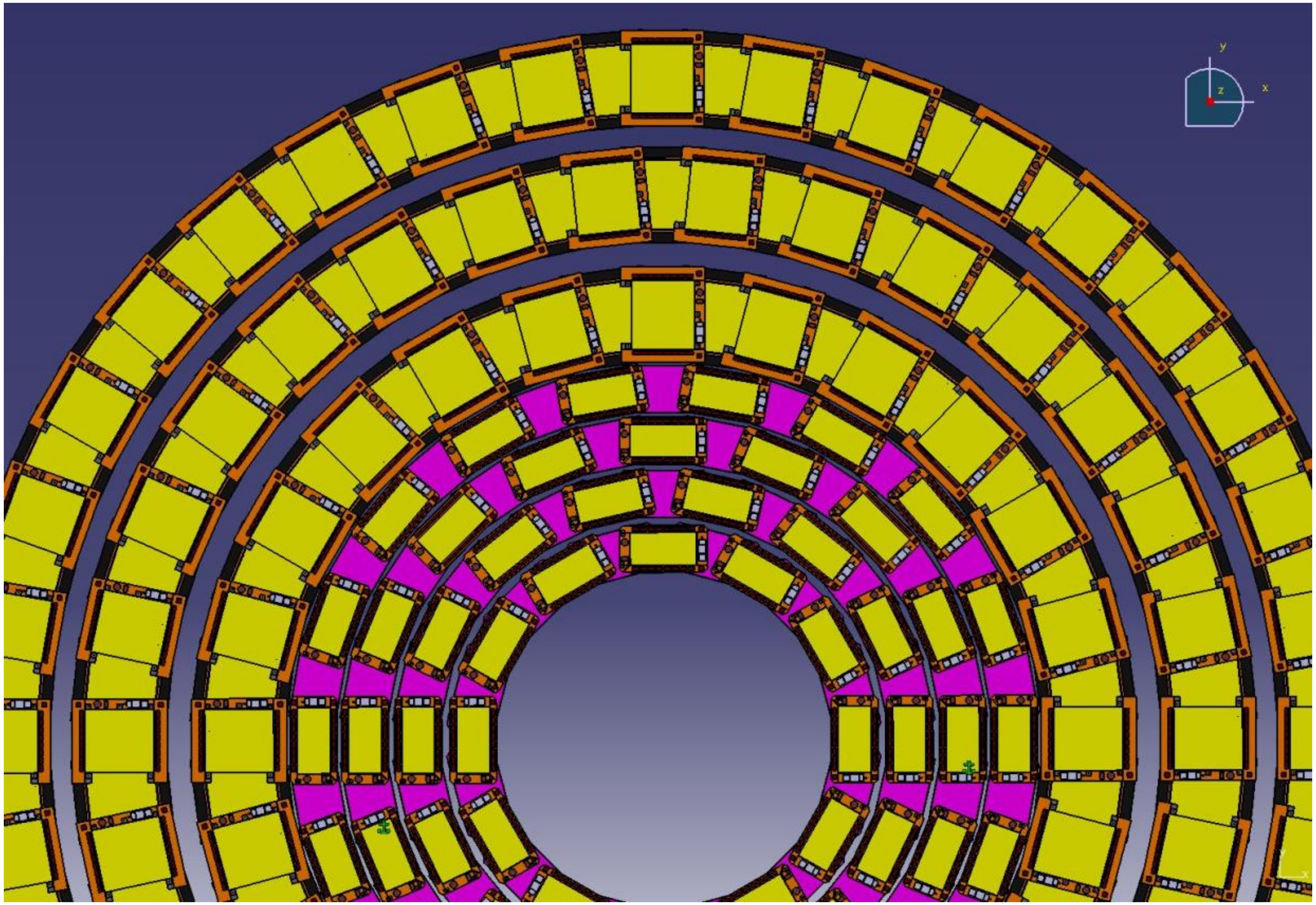

## PS Modules



# Building Tracker Barrel Rods



# Building Tracker Endcap Disks

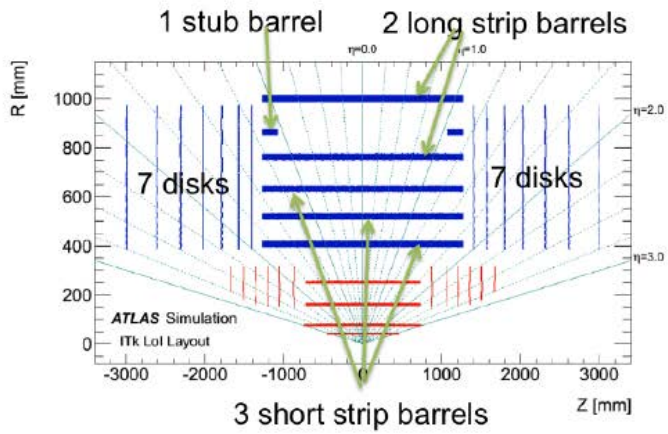


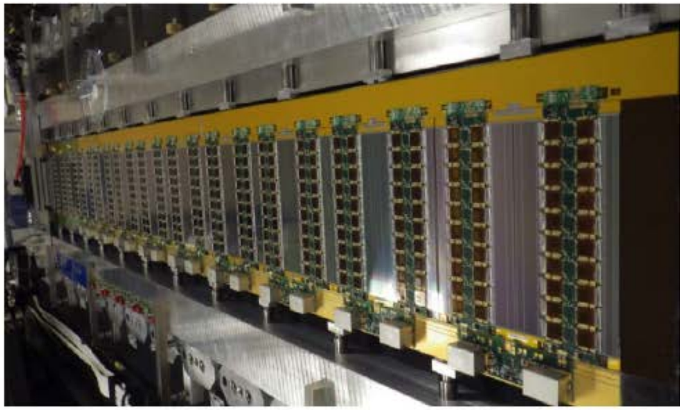
# A Side-Look to ATLAS

## ATLAS Outer Tracker

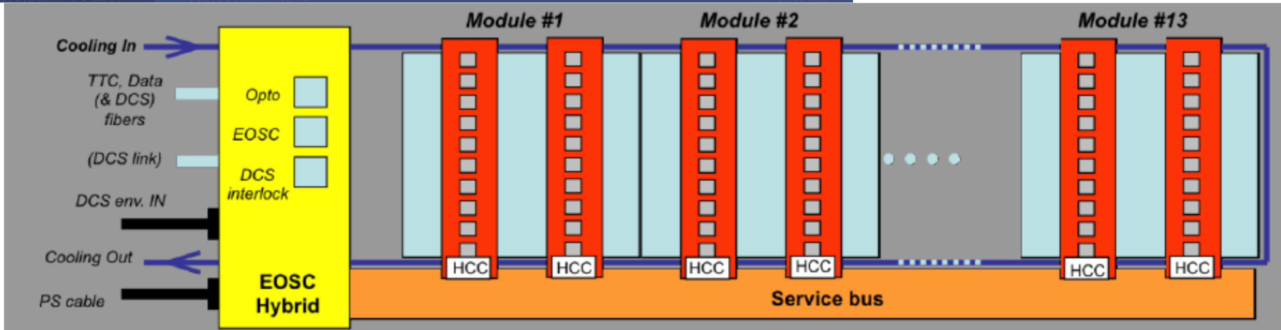
Two types of modules

- Short strip modules
- Long strip modules
- Organised in double-sided staves with stereo angle







# II) The Electronics of the CMS Outer Tracker Upgrade

## a) System

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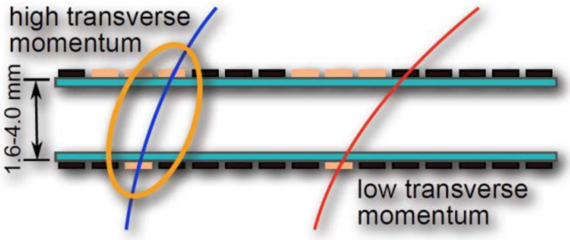
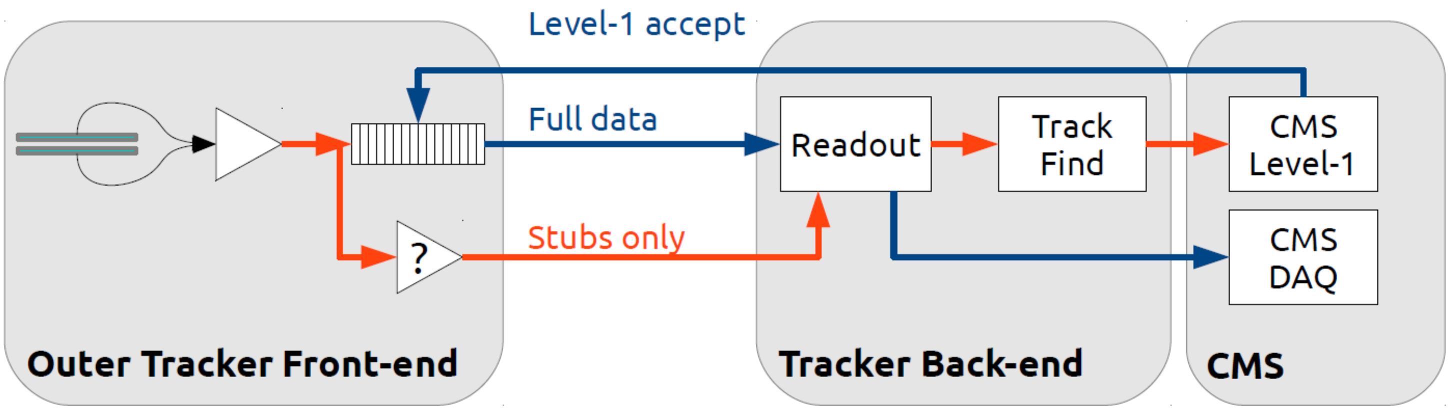
Slide material from: S. Mersi, S. Viret and many others

# Upstream Data Path

Level-1 "stubs" are processed in the back-end

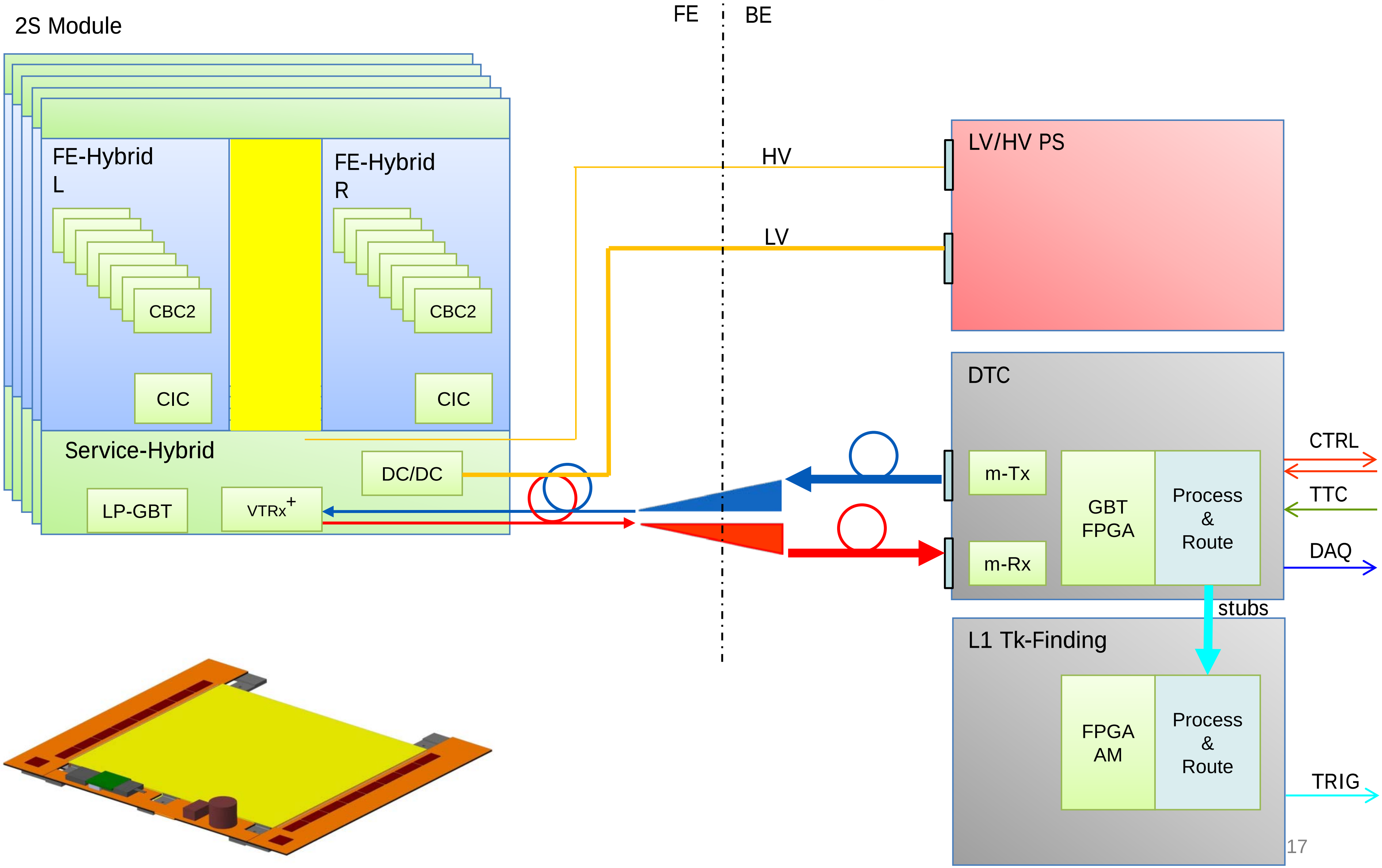
Form Level-1 tracks, pT above ~ 2 GeV, contributing to CMS Level-1 trigger



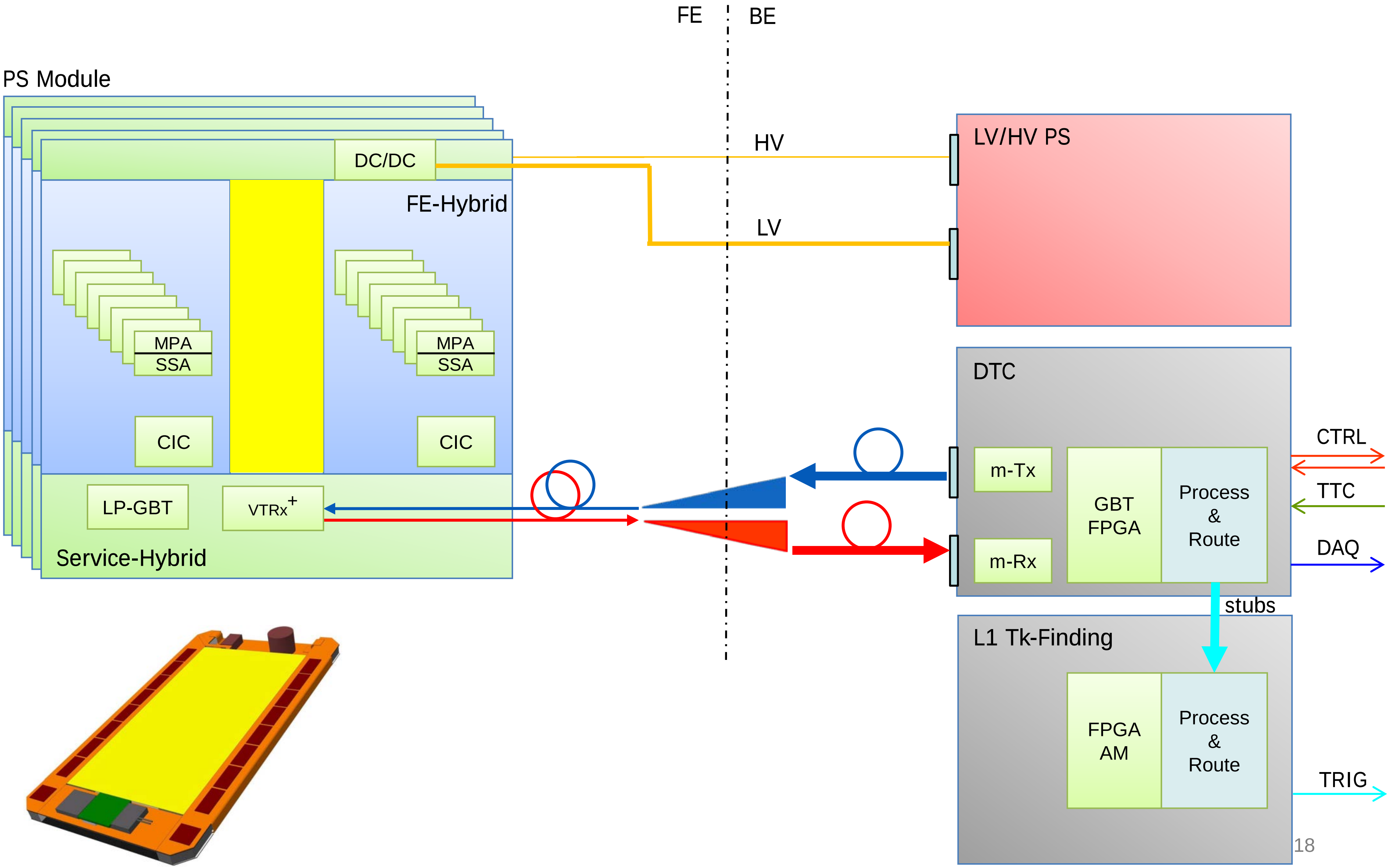




**@ 40 MHz** – Bunch crossing →Trigger Data
**@ ~ 500 kHz** – CMS Level-1 trigger →L1 Readout Data

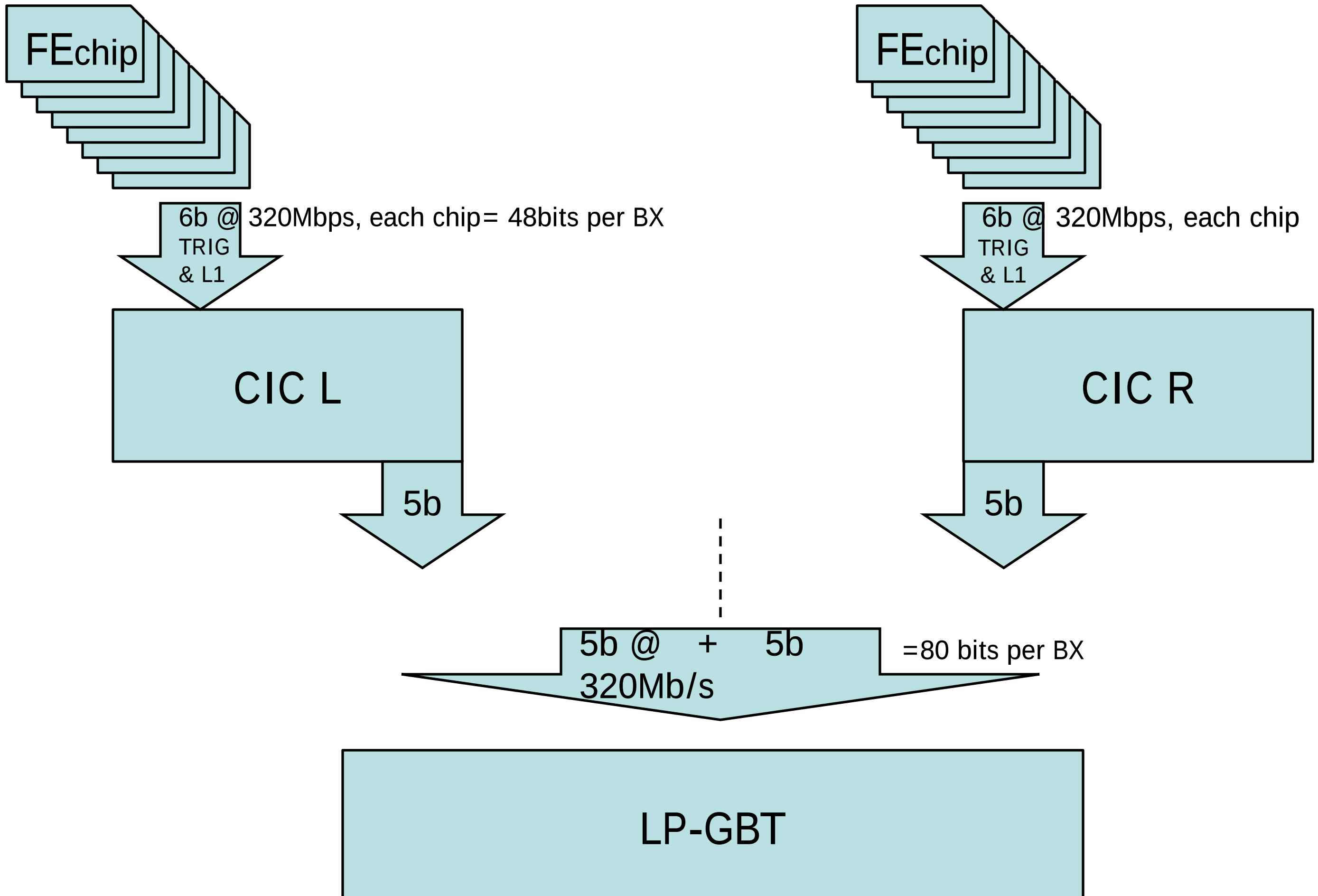
# Electrical System:
# Simple Block Diagram, 2S



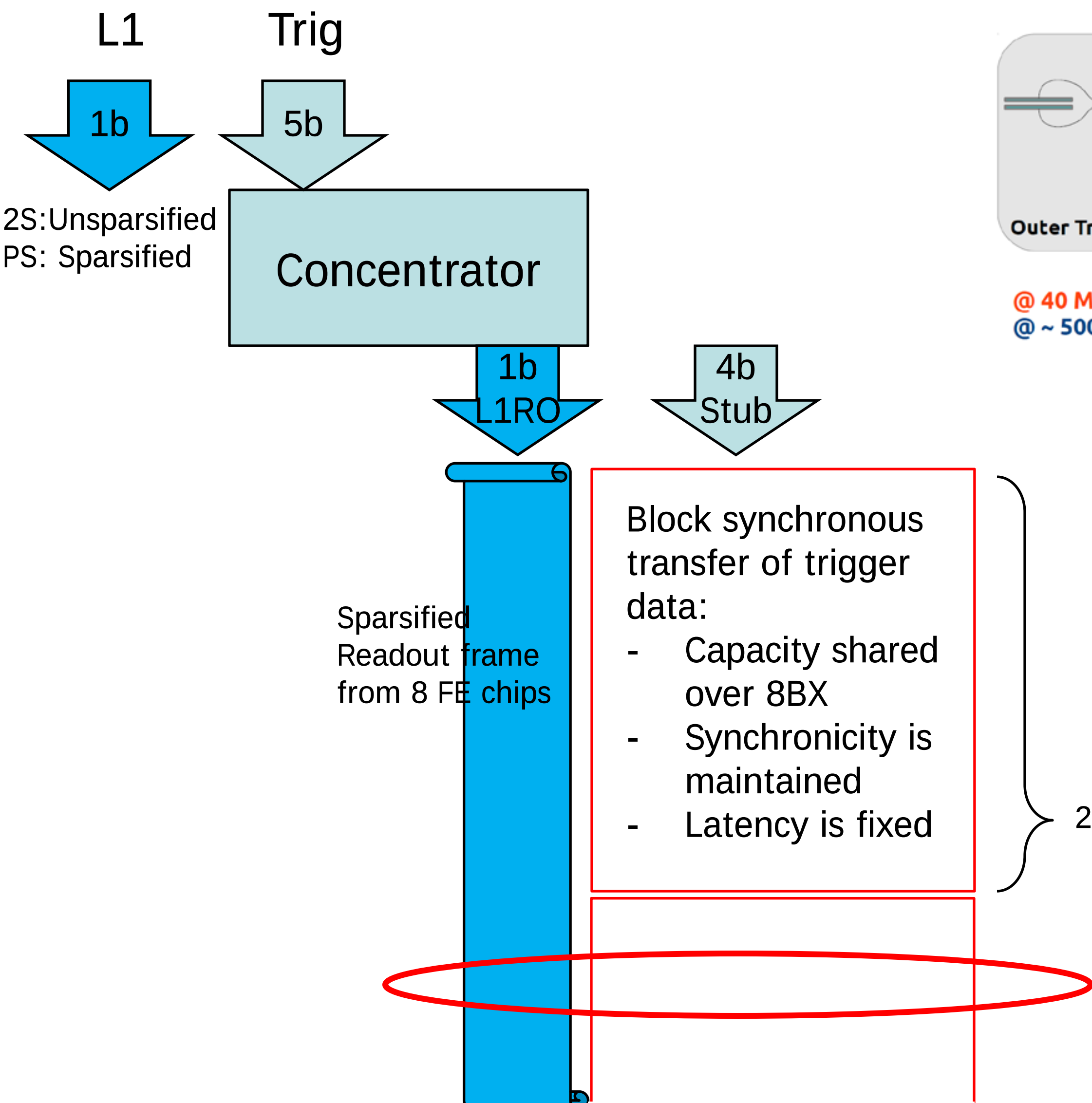
# Electrical System:
# Simple Block Diagram, PS

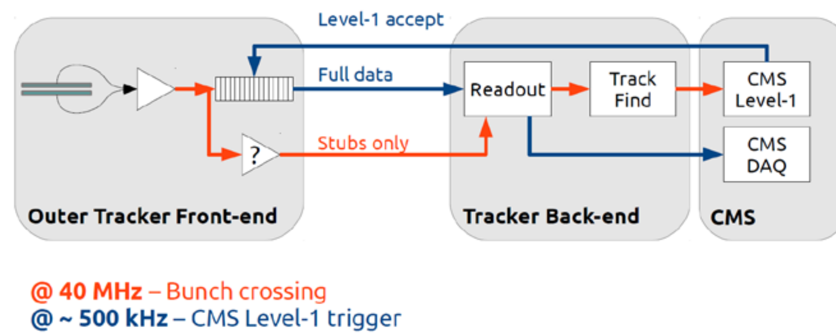


# Data Aggregation Chain @ 320Mbps



# Upstream Data Formats to/from Concentrator @ 320Mbps



# Capacity vs Stub Rates

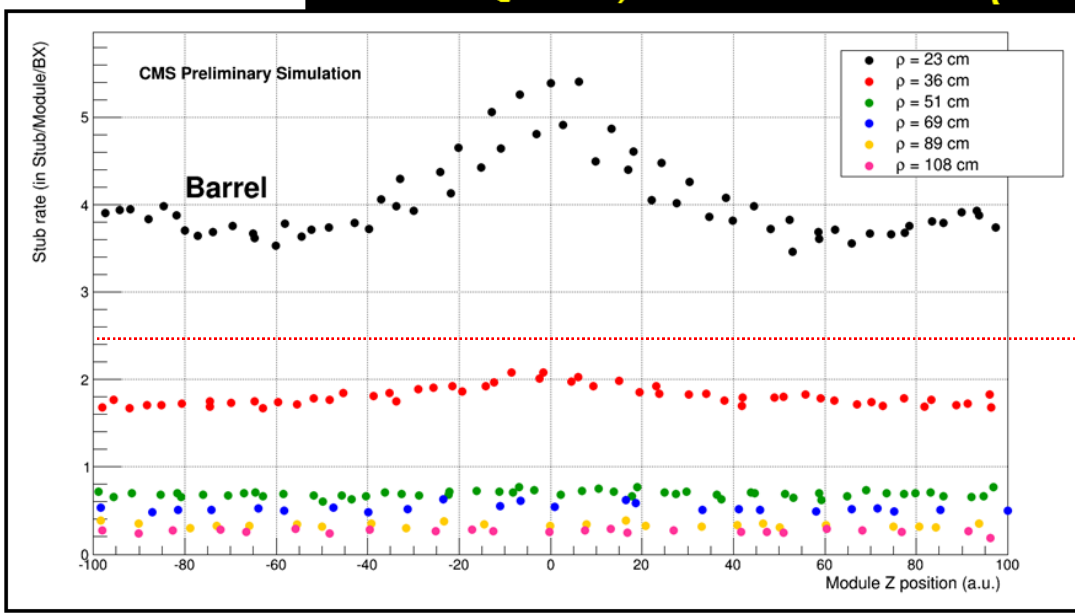
→ **Trigger losses estimation:**

→ Trigger Losses are estimated using a **mix of 90% PU140/200 events + 10% PU140/200+4tops events**. Other mix proportions are also tested (*0,20,…*).

→ Latest simulation available used (***SLHC15***), and latest minbias simulation to date (***UEP6S1***)

→ Only good stub losses (***pT>2Gev/c and d0<1cm***) are shown

***Stub rates @PU140, with loose T2 SW cuts (best turn-on)***




| | | Trigger |
|---|---|---|
| MPA output | Block sync | 4stub/2BX |
| Concentrator output | | |
| 80/20sparsified | Block sync | 10stubs/8BX 4x8bits x 8BX |
| Priority toTrig | Block sync | 12stubs/8BX 5x8bits x 8BX |

→ ***From the rate plots it's straightforward to predict where problems will occur…***

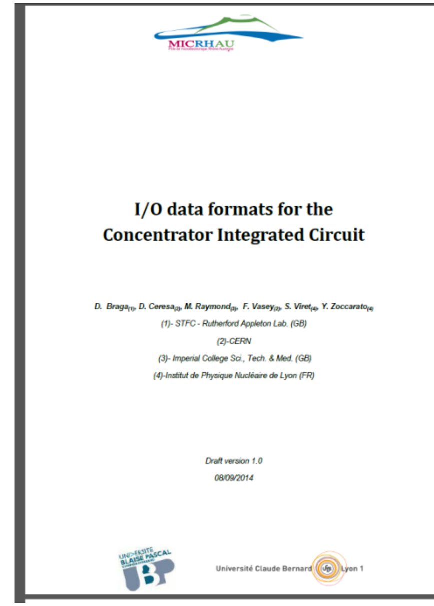
# System Features and Limits

→ **From FE to CIC:**

- **L1 data transmission @1MHz looks possible** for both FE chips.
- **Trigger data transmission @40MHz** is **OK for the CBC, OK also for the MPA** if one transmit data over 2BXs.

→ **From CIC to GBT:**

- **A common output data format for PS/2S modules was defined**
- **L1 data transmission @1MHz is possible with some safety margin for the 2S part, much tighter for the PS part. 500kHz looks feasible in all PU scenario**, need to evaluate the limit at PU140.
- **Trigger data transmission @40MHz is possible for the 2S part, but very challenging for the PS part.** With 64 bits for the L1 block, **the data loss in TIB1 is significant in ALL CASES**. Raising threshold and cutting the bends could significantly mitigate the problem, but not remove it.


MICRHAU

I/O data formats for the Concentrator Integrated Circuit

D. Braga(1), D. Ceresa(2), M. Raymond(3), F. Vasey(2), S. Viret(4), Y. Zoccarato(4)
(1)- STFC - Rutherford Appleton Lab. (GB)
(2)-CERN
(3)- Imperial College Sci., Tech. & Med. (GB)
(4)-Institut de Physique Nucléaire de Lyon (FR)

Draft version 1.0
08/09/2014

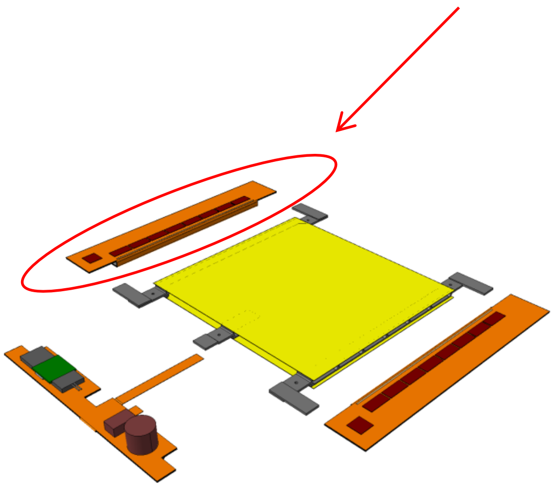
Université Claude Bernard Lyon 1

- Flexibility built into the FE chips to be able to tune bandwidth need and adapt to higher GBT capability in innermost layer
  - Decrease number of bend bits
  - Increase Pt threshold, sort stubs according to Pt
  - Use Lp-GBT in 10G mode
- See Technical Note
  - “I/O data formats for the Concentrator Integrated Circuit” by D. Braga(1), D. Ceresa(2), M. Raymond(3), F. Vasey(2), S. Viret(4), Y. Zoccarato(4)

# II) The Electronics of the CMS Outer Tracker Upgrade

## a) System

## b) FE Electronics for 2S modules



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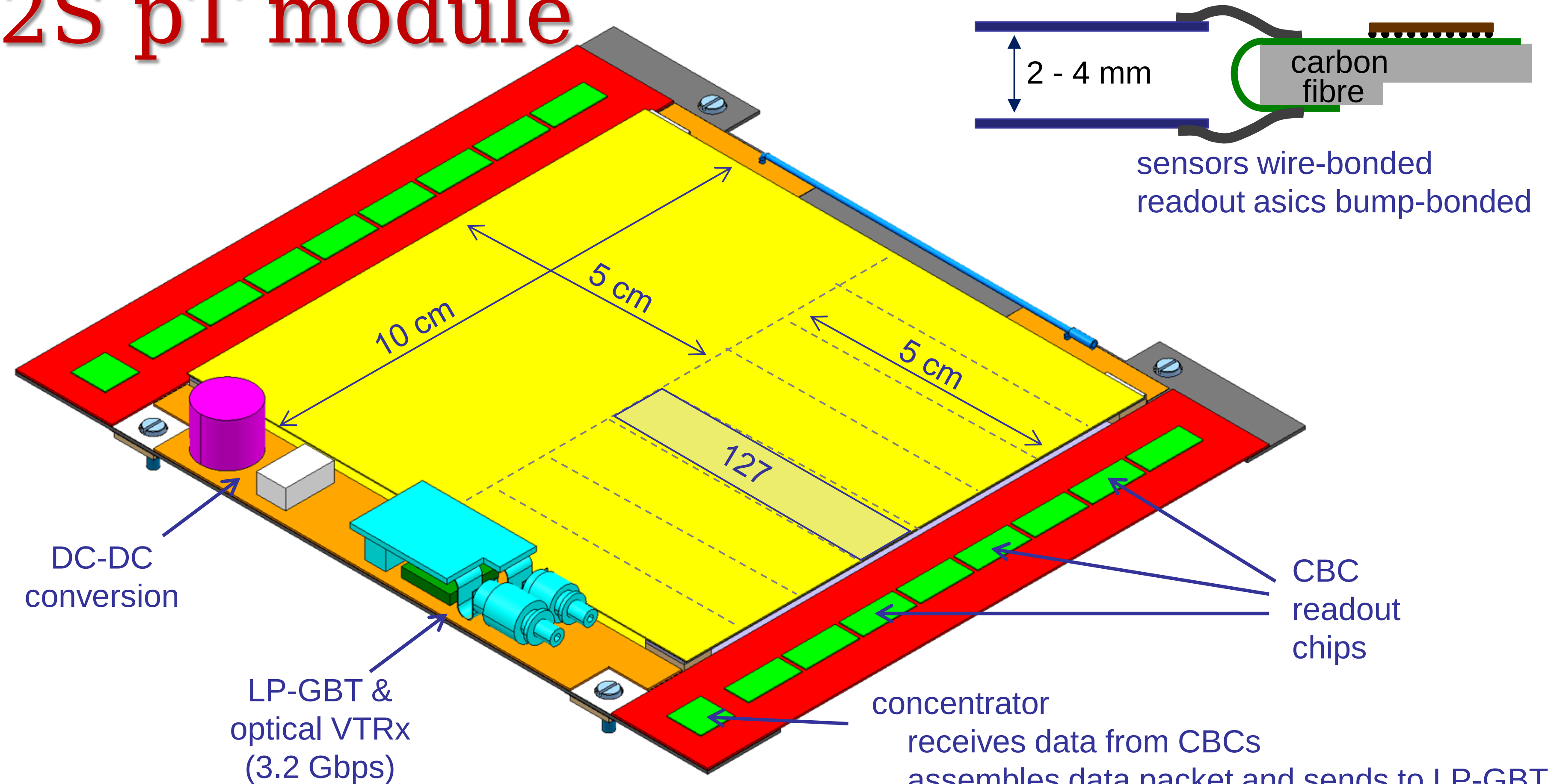
Slide material from: G. Blanchot, D. Braga, A. Honma, M. Kovacs, M. Raymond, Y. Zoccarato, and many others

# 2S pT module




1 module type, ~10 x 10 $cm^2$ active sensor area for whole of region beyond r = 50 cm (endcaps too)

self-contained single, testable object; only needs power and optical connection to function

2S => 2 silicon sensors, each read out at both ends, strips 5 cm x 90 $\mu$m pitch, ~4000 channels total

16 bump-bonded CBC readout asics, each reads 127 strips from top layer, 127 from bottom

# CBC readout chip history

2 versions have been produced - both in 130nm CMOS

**CBC1 (2011)**

128 wire-bond pads, 50 μm pitch
front end designed for short strips, up to 5 cm
DC coupled, up to 1μA leakage tolerant, both sensor polarities
binary unsparsified readout
pipeline length 6.4 μsec

chip worked well in lab and test beam (few workarounds)

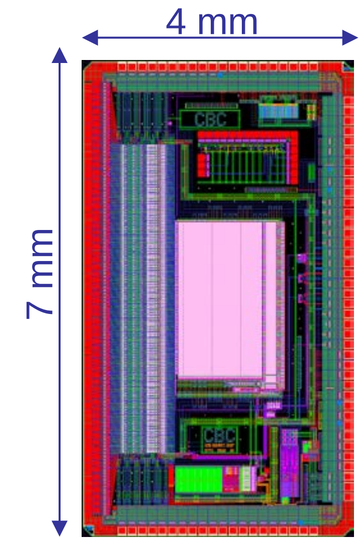
**no** triggering features

**CBC2 (January, 2013)**

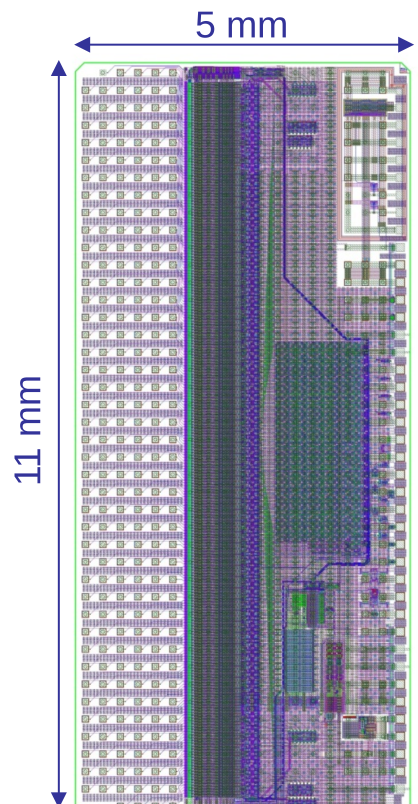
254 channels
~same front end, pipeline, readout approach as CBC1

**but**

bump-bond layout
- C4 bump-bond layout, 250 μm pitch, 19 columns x 43 rows
includes triggering features
- 30 interchip signals (15 in, 15 out), top and bottom

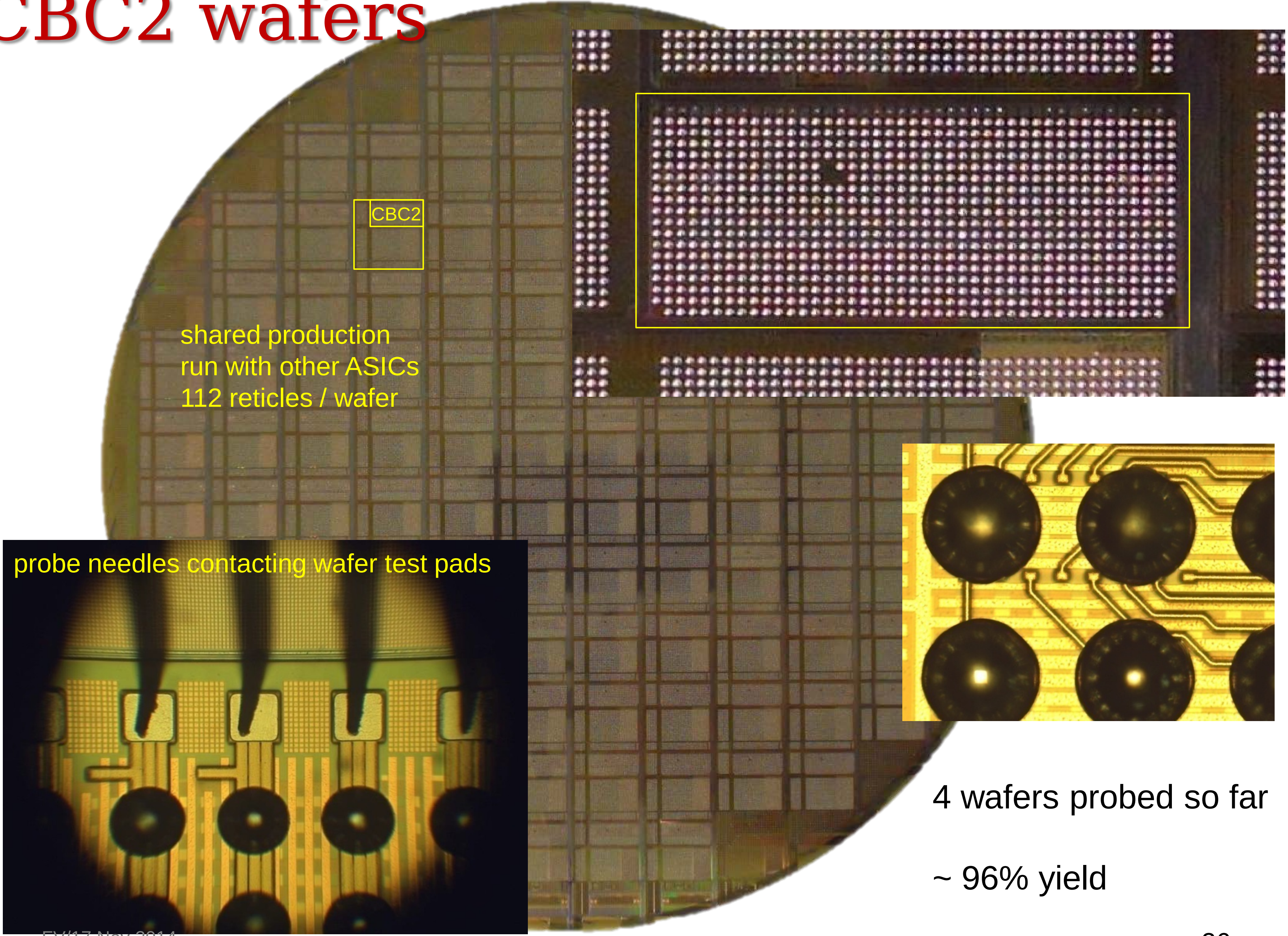



CBC1




CBC2

# CBC2 wafers




4 wafers probed so far

~ 96% yield

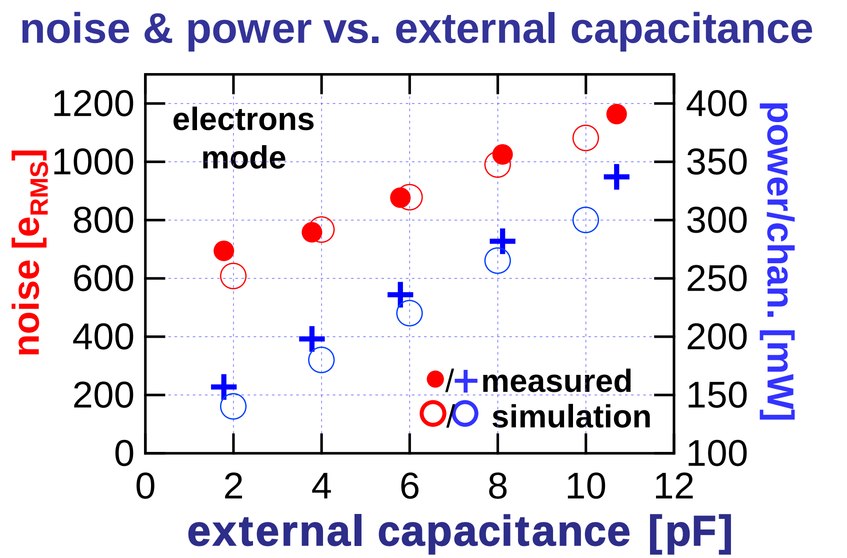
# CBC2 performance

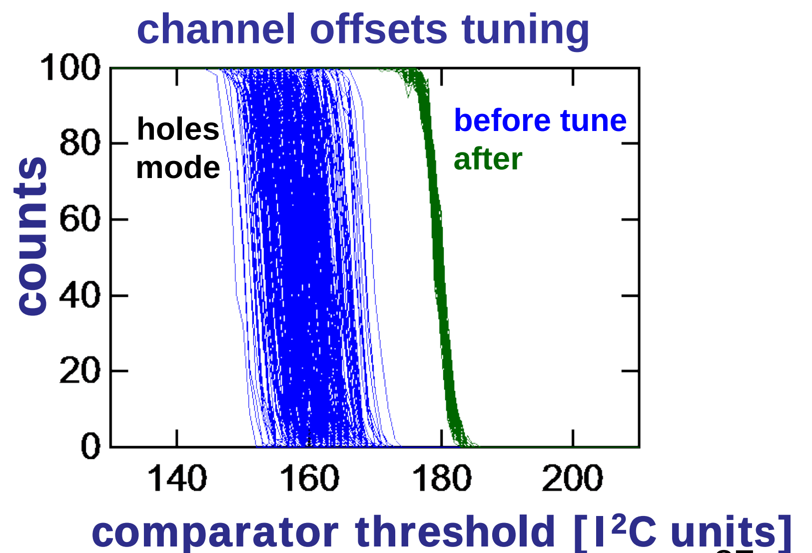
all core functionality meets requirements

- correlation functionality verified with test pulses, cosmics, and in test beam

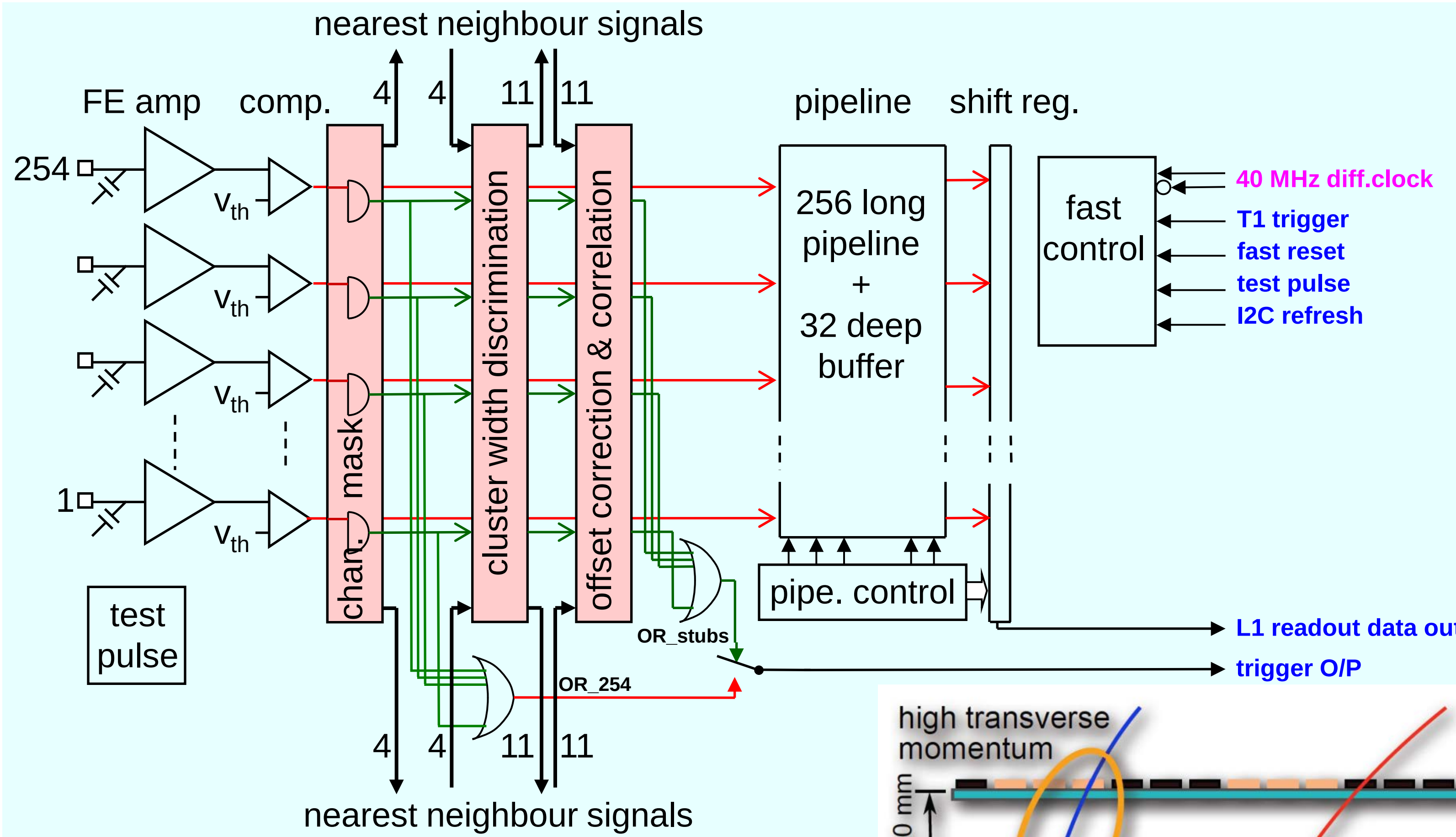
analogue performance close to simulation expectations and specifications

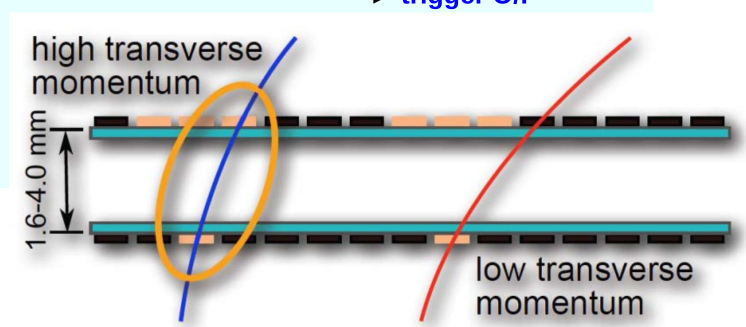
- e.g. 1000e noise for 5 cm strips (~8 pF)
- achievable for total channel power of 350 μW



# CBC2 triggering architecture

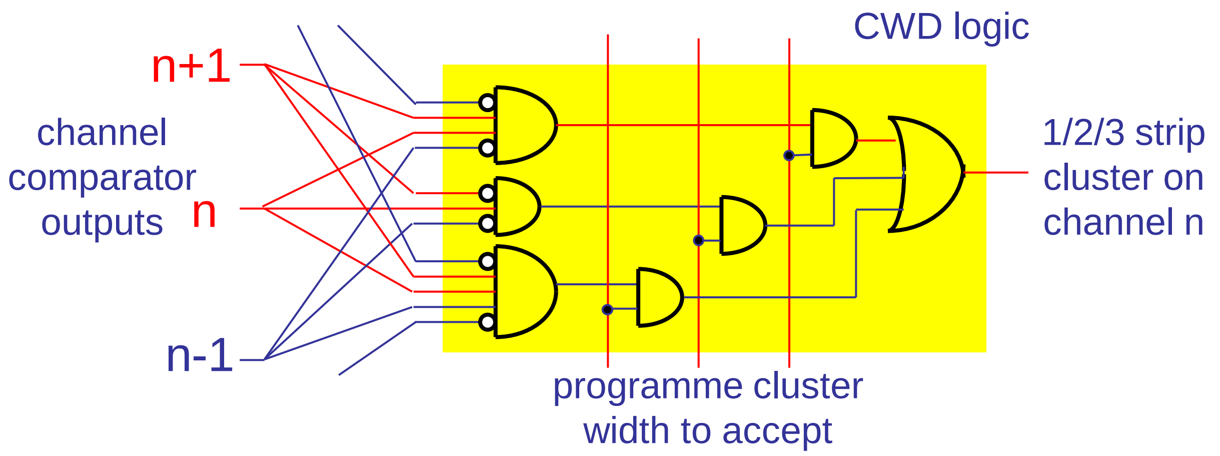



**254 channels**: 127 from each sensor layer
**channel mask**: block noisy channels from trigger logic
**CWD logic**: exclude wide clusters >3
**correlation logic**: for each cluster in lower layer look for cluster in upper layer window
**trigger output**: 1 bit per BX indicates correlation logic found one (or more) stubs
**L1 readout data out**: unsparsified binary data frame in response to L1 trigger

# CBC2 Triggering Implementation

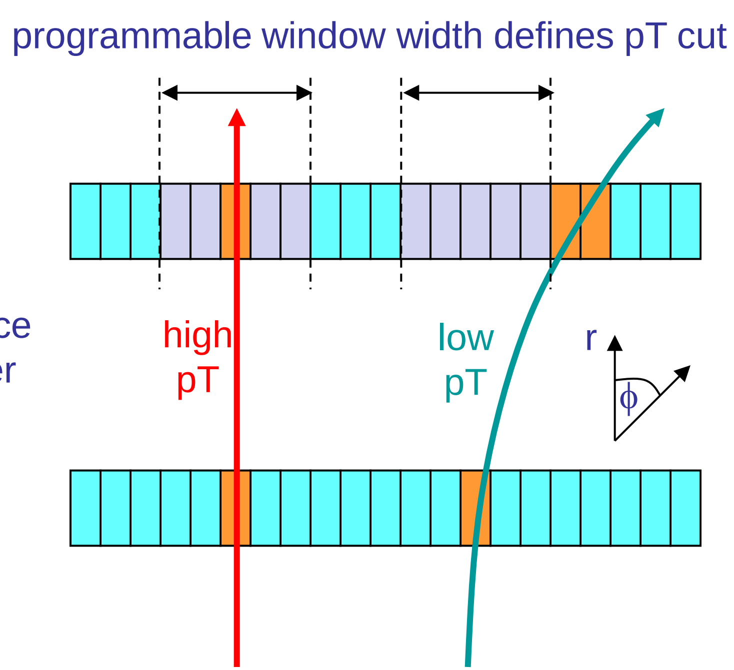
## cluster width discrimination




## correlation

seed cluster in lower layer in coincidence with cluster within window in upper layer

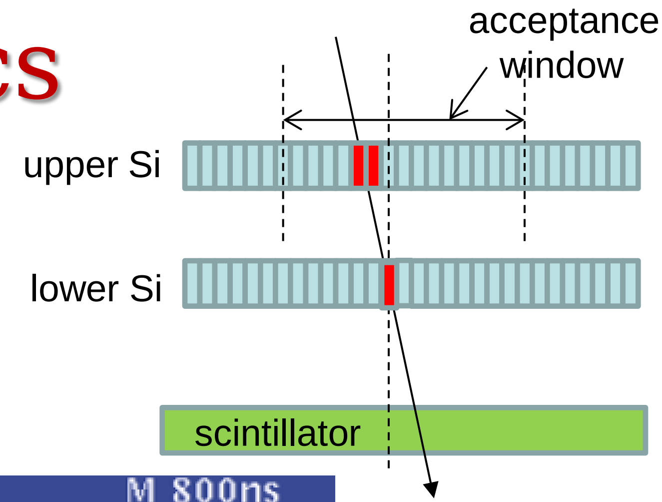
=> **pT stub**

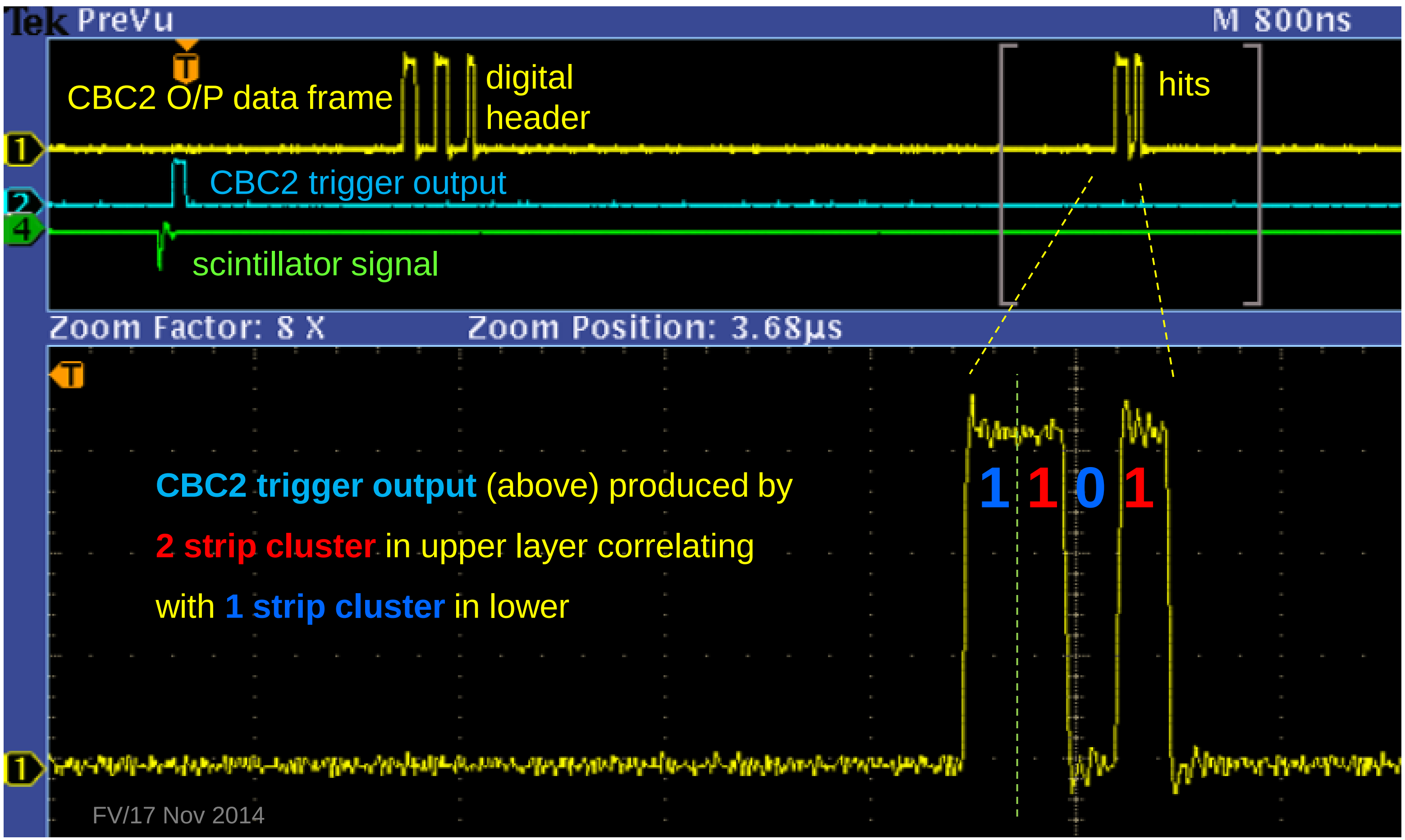


# Correlation using cosmics

data stream output bits alternate between upper and lower layers

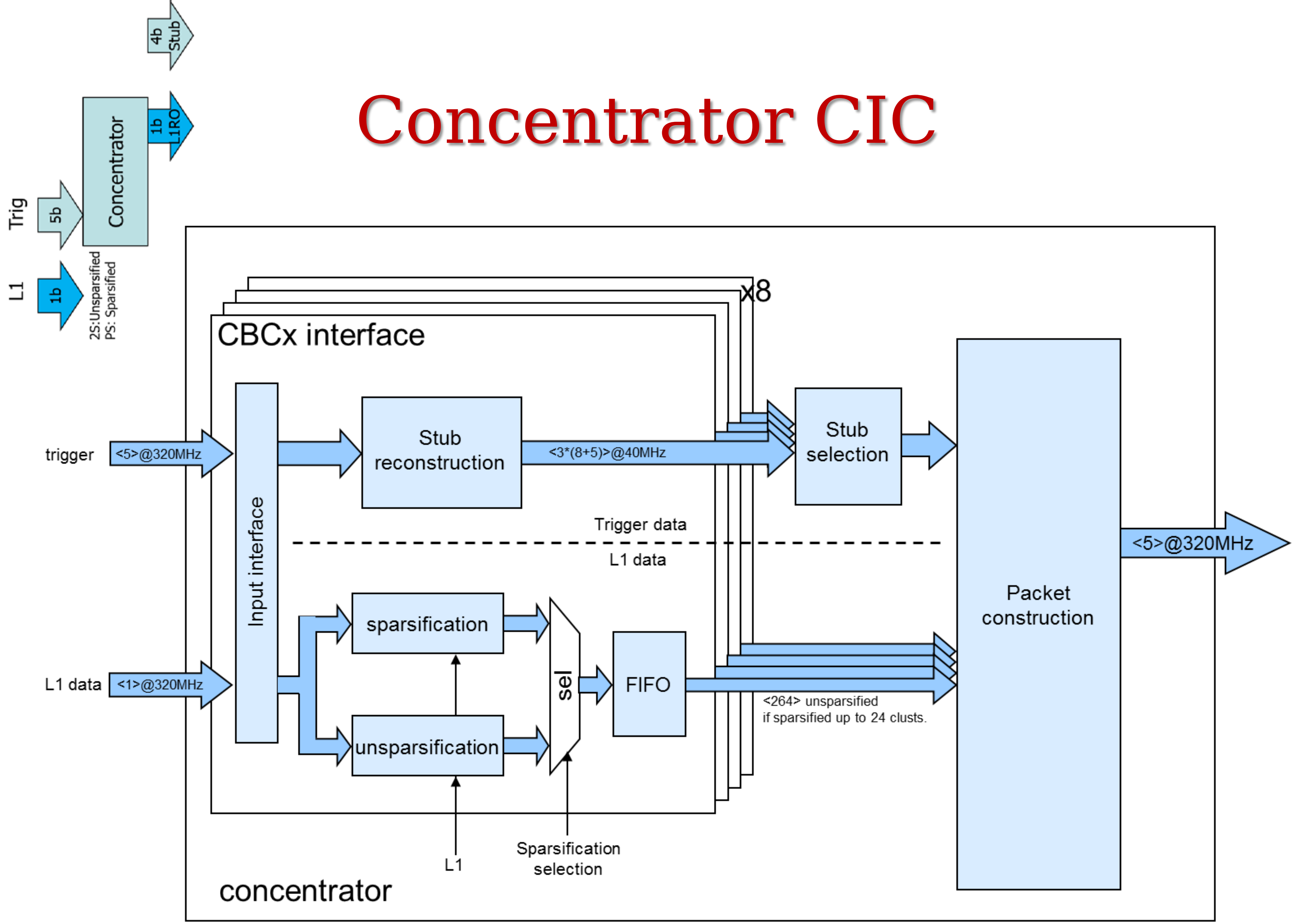
=> …0001101000…. bit pattern signifies
1 strip cluster in lower layer
and 2 strip cluster in upper layer



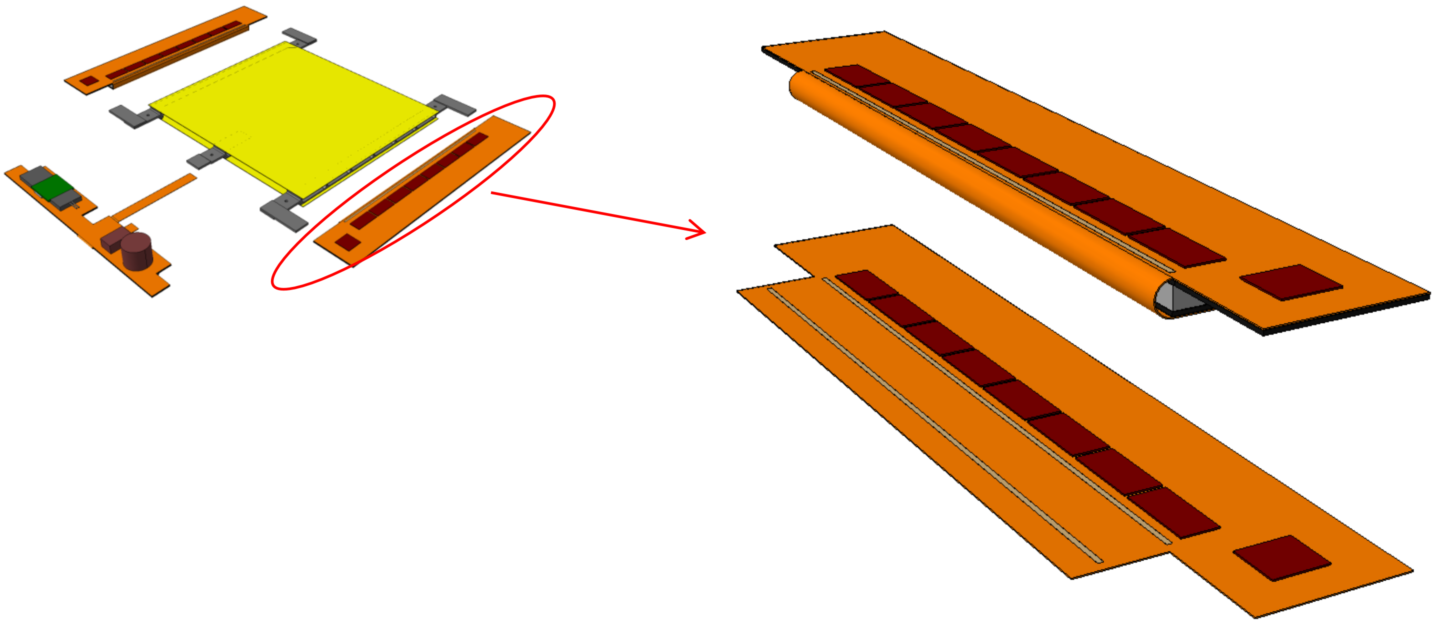




**=> correlation logic working as expected**

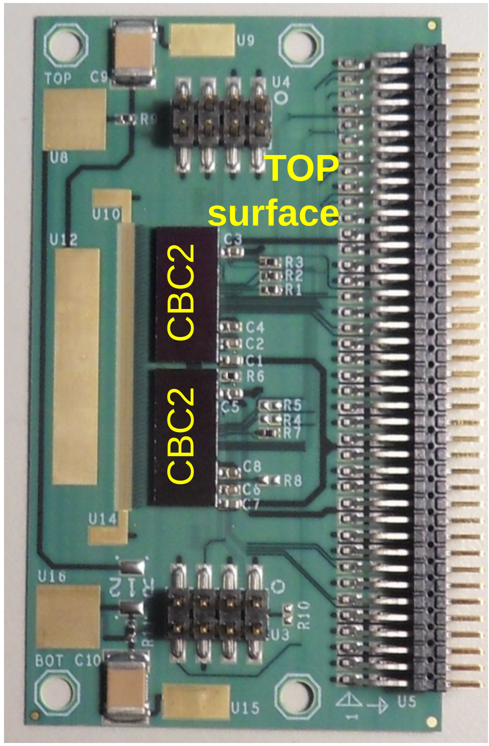
# Concentrator CIC



# 2S Hybrid Developments

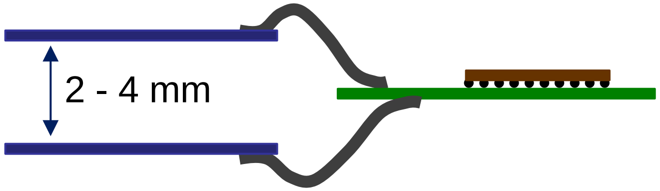


# Hybrid Developments: 2CBC2

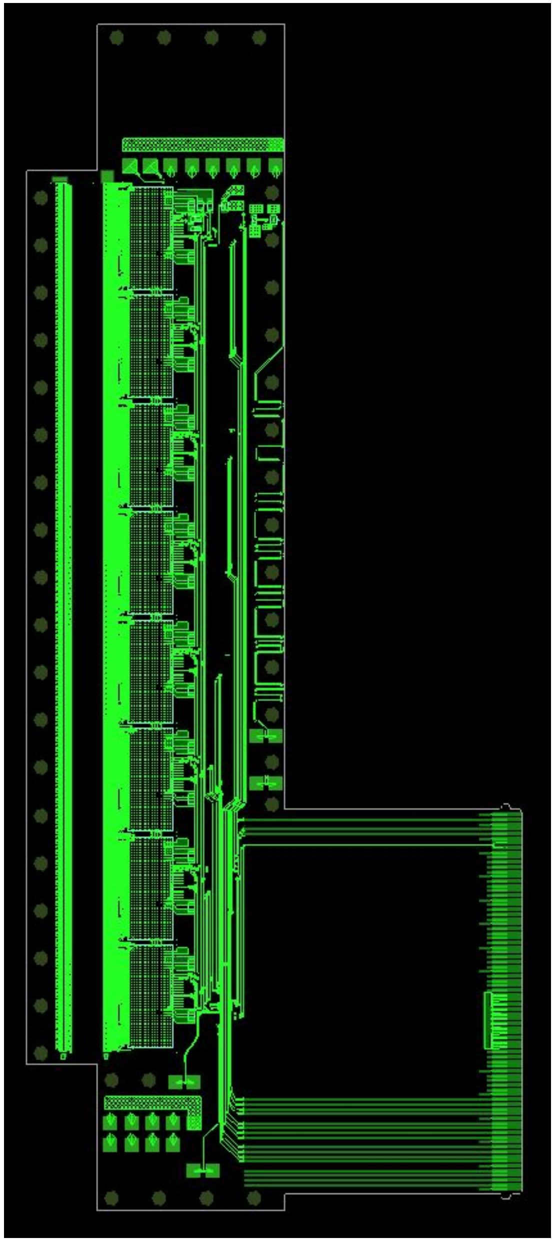


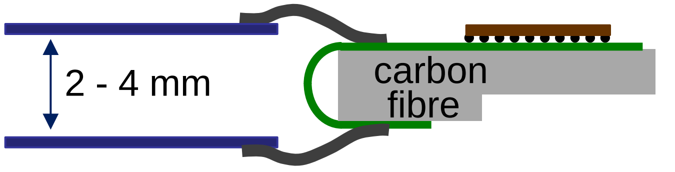

2 chips prototype - available since mid 2013

- 6 layer "rigid" technology - (actually quite flexible - 265 μm thick)
- For chip testing and mini-module assembly
- fully functional, but flexibility and thickness causes bonding problems when constructing modules



# Hybrid Developments: 8 CBC2

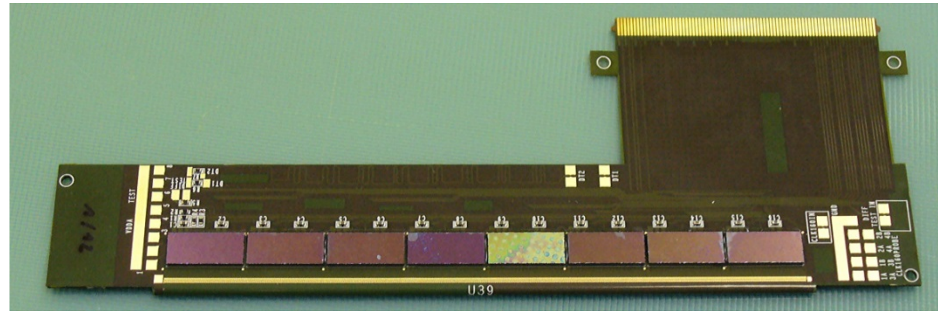


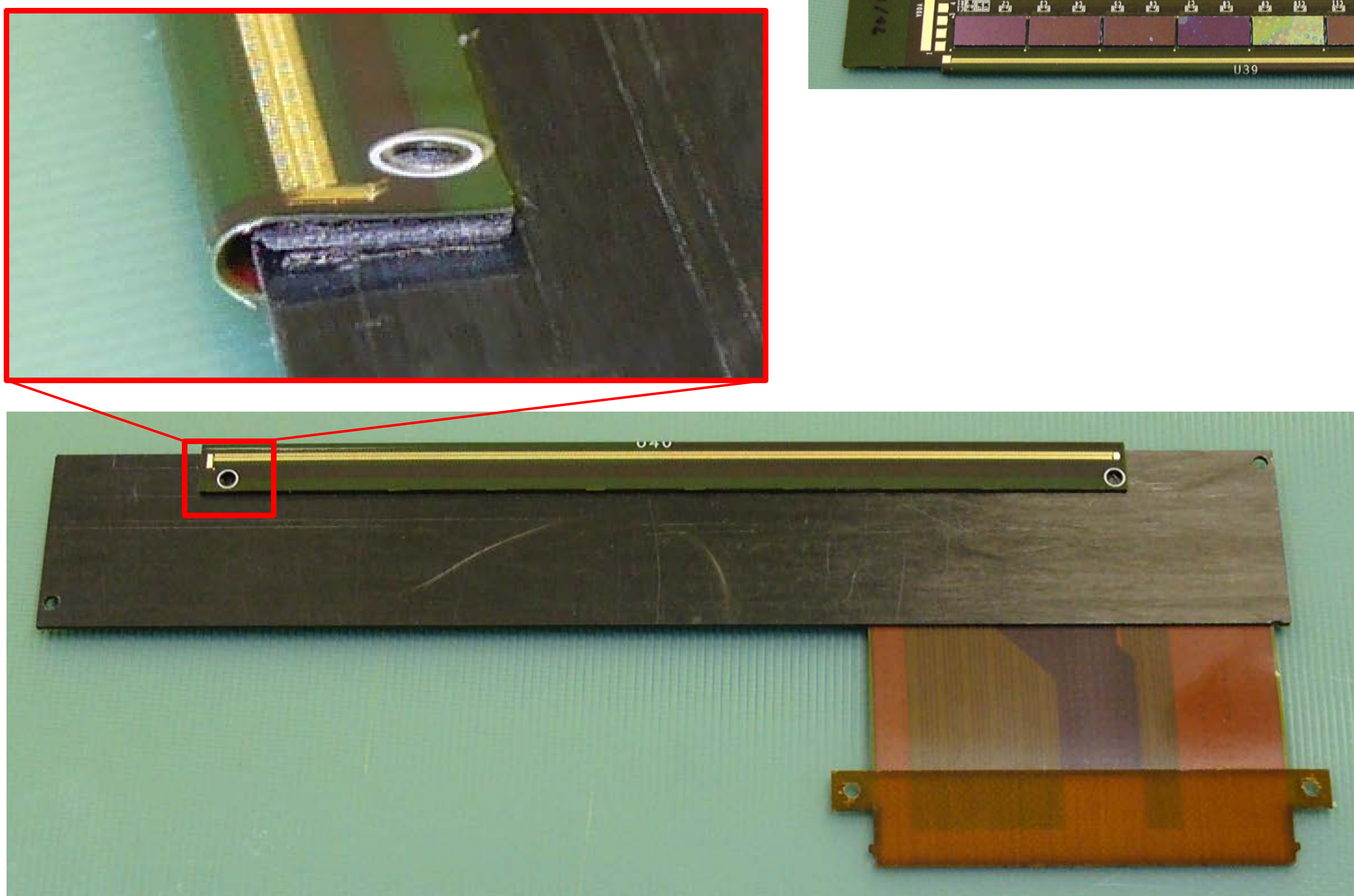



- **The 8CBC2Flex is a full 8 CBC2 readout system.**
  - 4 layer, 150µm thick
  - One 40 MHz clock input.
  - All chips configured separately through a common I2C bus.
  - All chips are powered at 1.25V.
- **Common back end signals to control the readout:**
  - Reset, Clock 40, I2C bus.
- **Paired control signals:**
  - Fast reset, I2C refresh, T1Trig, Test Pulse.
- **All readout signals are handled per chip:**
  - Trigger and Data lines.
- **All signals are brought to a FPC connector.**
  - No concentrator

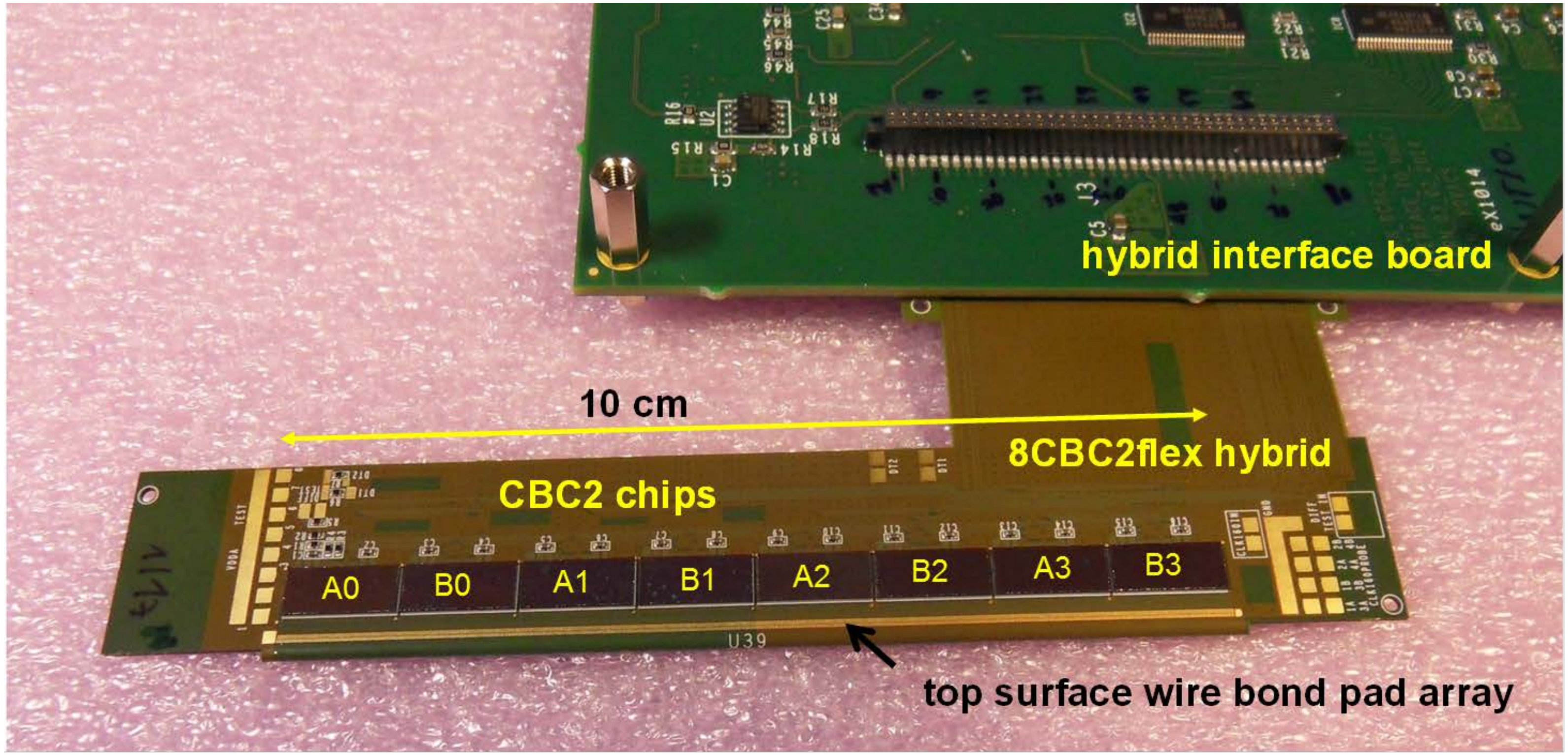
# 8 CBC2 Prototype Flex

Delivered Apr. 2014



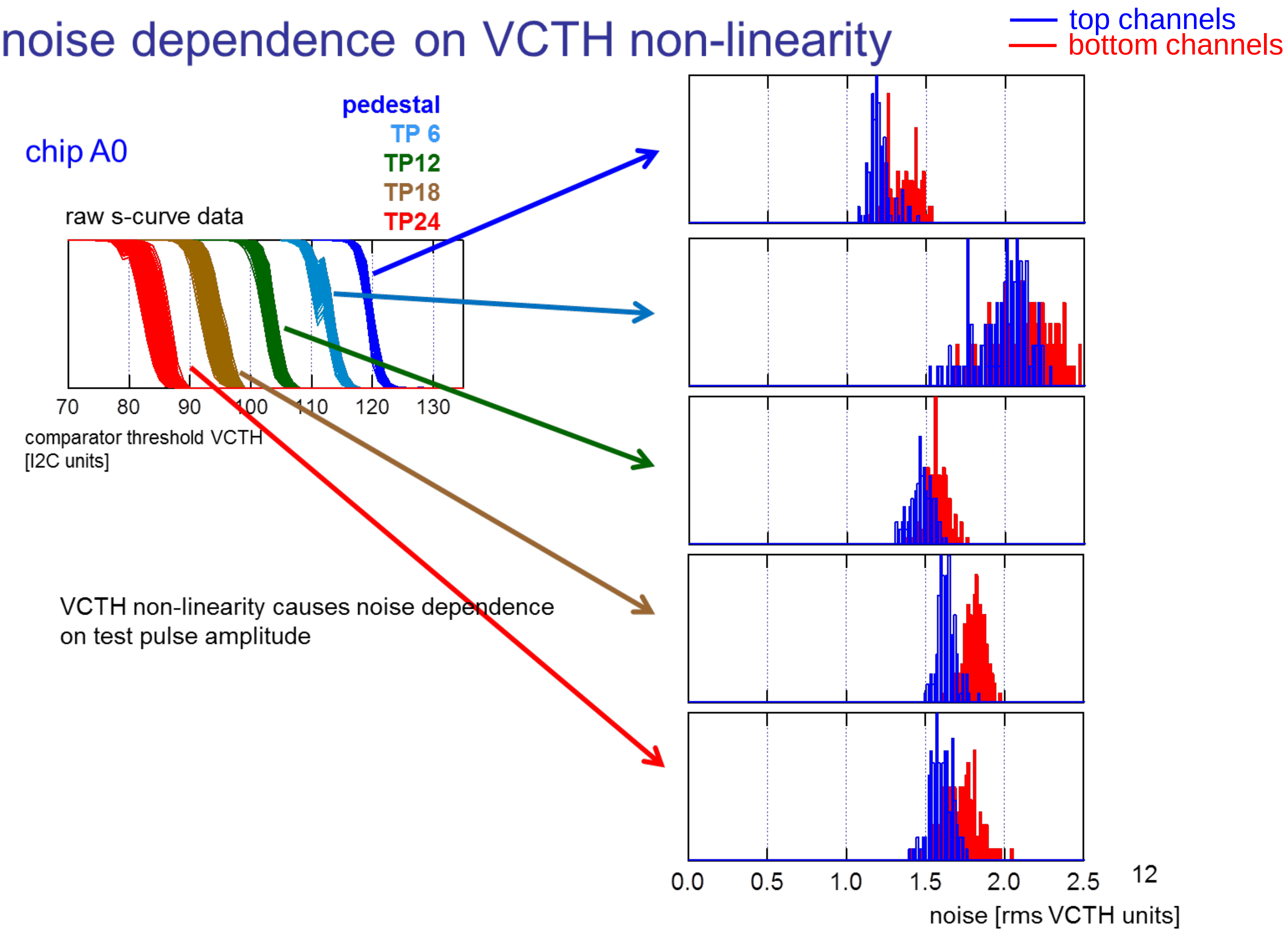



# 8 CBC2 Test Bench



# 8 CBC2 Test Results

## noise dependence on VCTH non-linearity

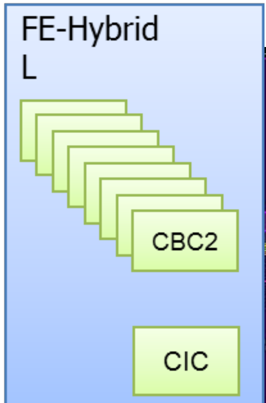


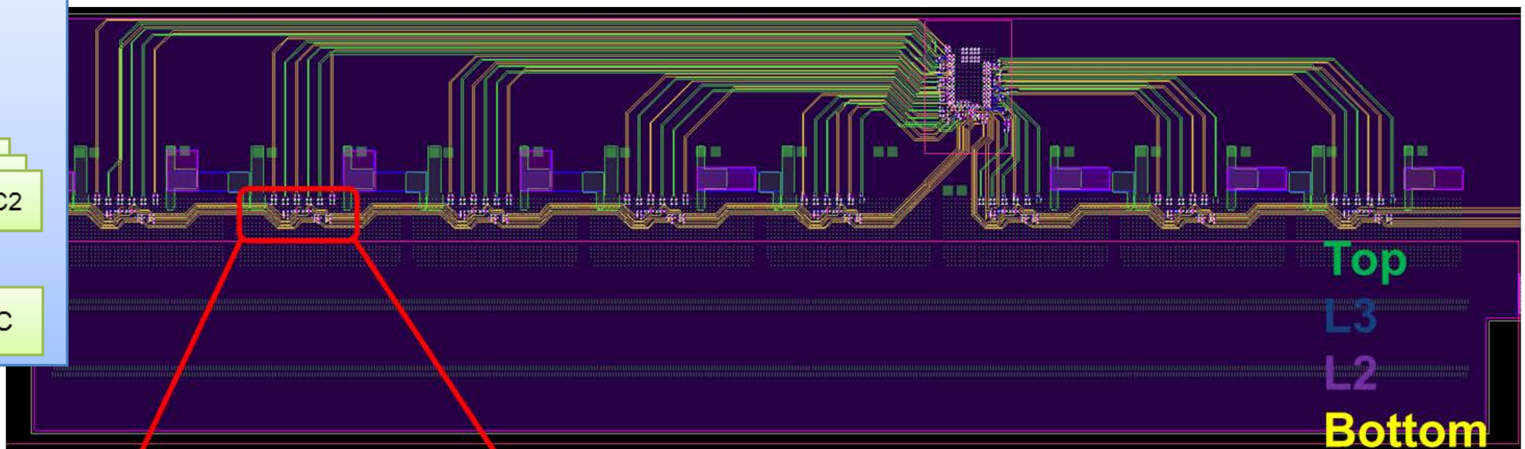

VCTH non-linearity causes noise dependence on test pulse amplitude

12

# How/Where to add the Concentrator

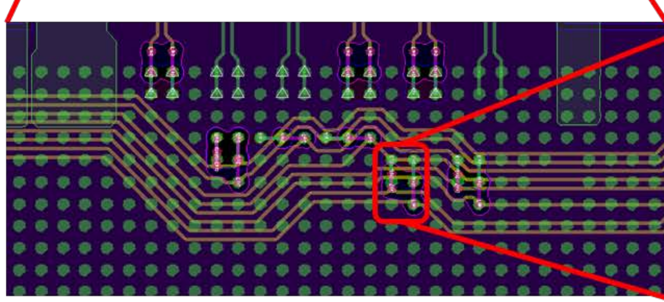
- A tradeoff between circuit width, Concentrator position and datarate

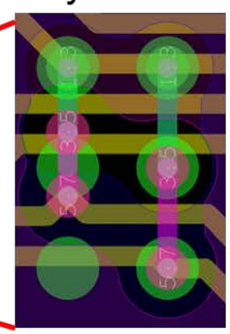


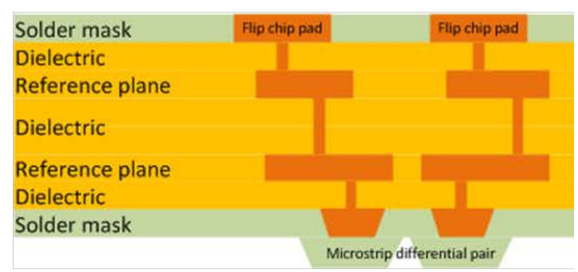




Differential pairs are using 50µm linewidth with 50µm gap. The spacing of differential pairs on the same layer is 250µm.

Clock signals and common control signals are routed on the bottom layer, under the surface mount components and connected by a via structure.







# II) The Electronics of the CMS Outer Tracker Upgrade

a) System

b) FE Electronics for 2S modules

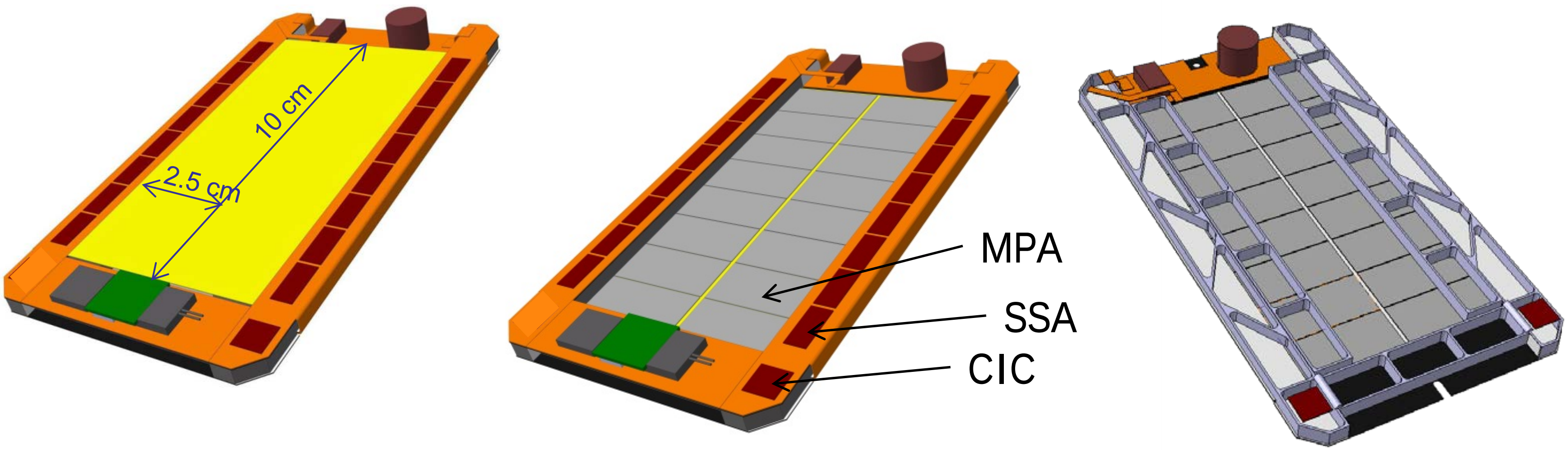
c) FE Electronics for PS modules

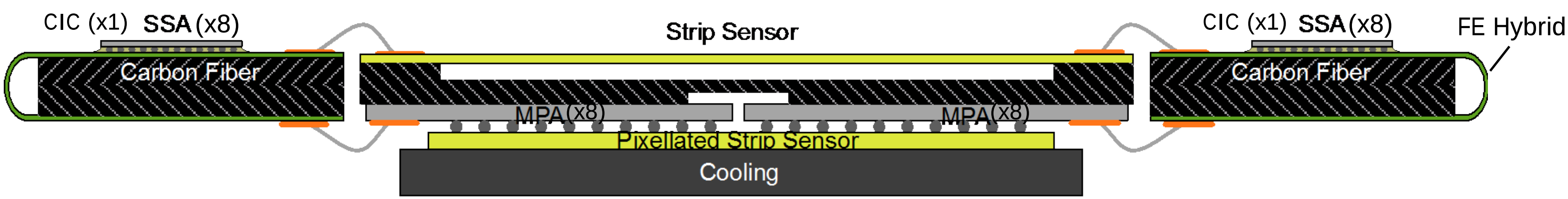
PH-ESE Seminar

Francois Vasey

Slide material from: G. Blanchot,
D. Ceresa, K. Kloukinas,
A. Marchioro, S. Mersi, and many others

# FE Electronics for PS Module

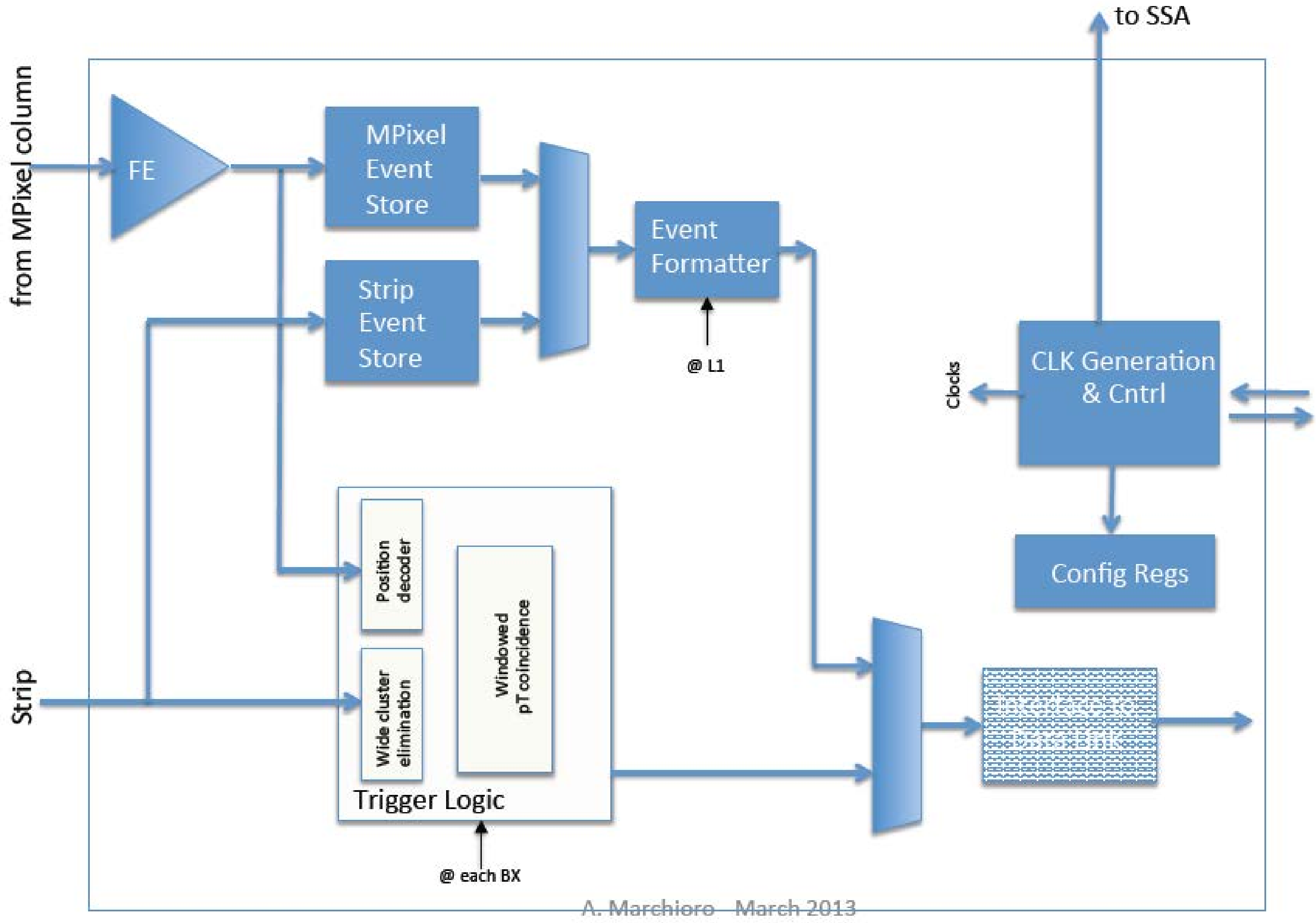


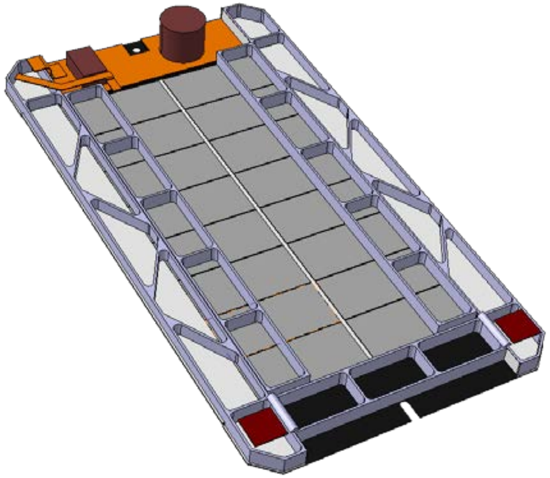

- ASIC in 65nm process
- Bump bonded on sensor/substrate

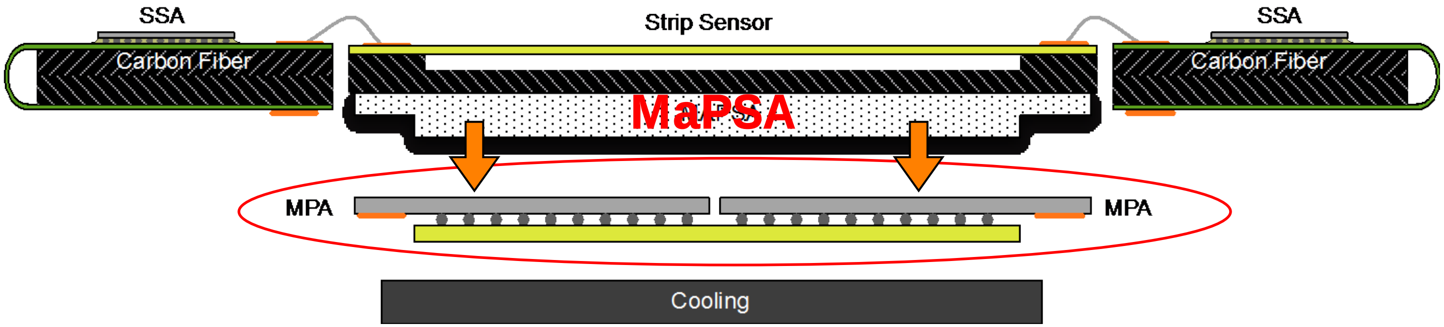
- 120 strips per SSA
  - 100 μm strip pitch
- 120 strips x 16 pixels per MPA
  - Pixel size: 100 x 1446 $\mu m^2$

# MPA Simple Block Diagram



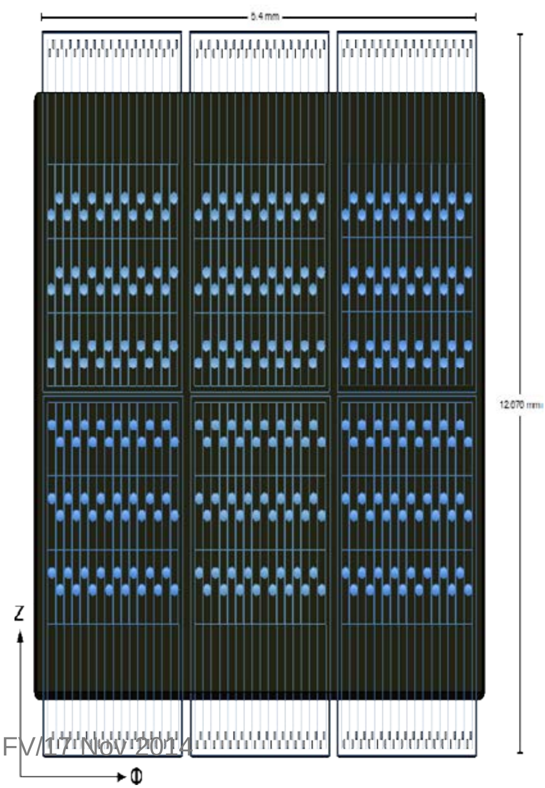
# Macro Pixel SubAssembly (MaPSA)

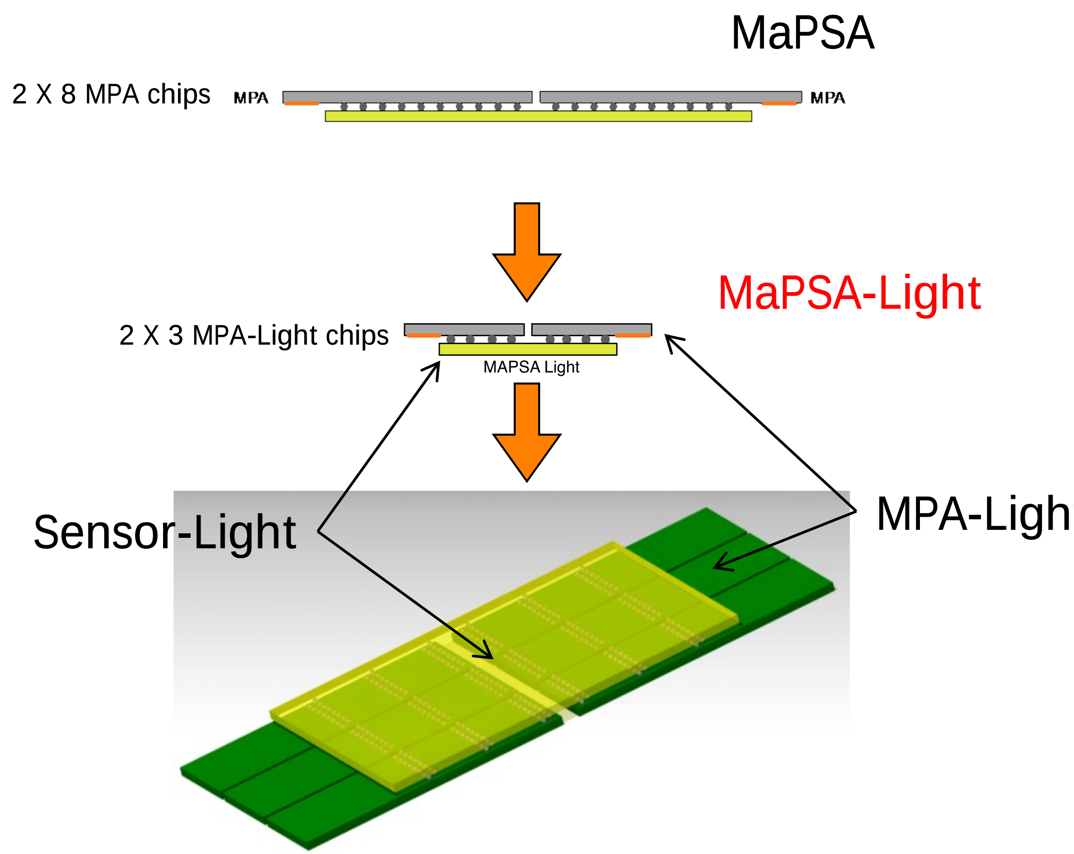




# MaPSA-Light Development

- Assembly of 3 x 2 MPA-light chips for a total of 288 pixels
  - Bump-bondable to detector
  - Wire-bondable to hybrid
  - 5.4mm x 12.7mm



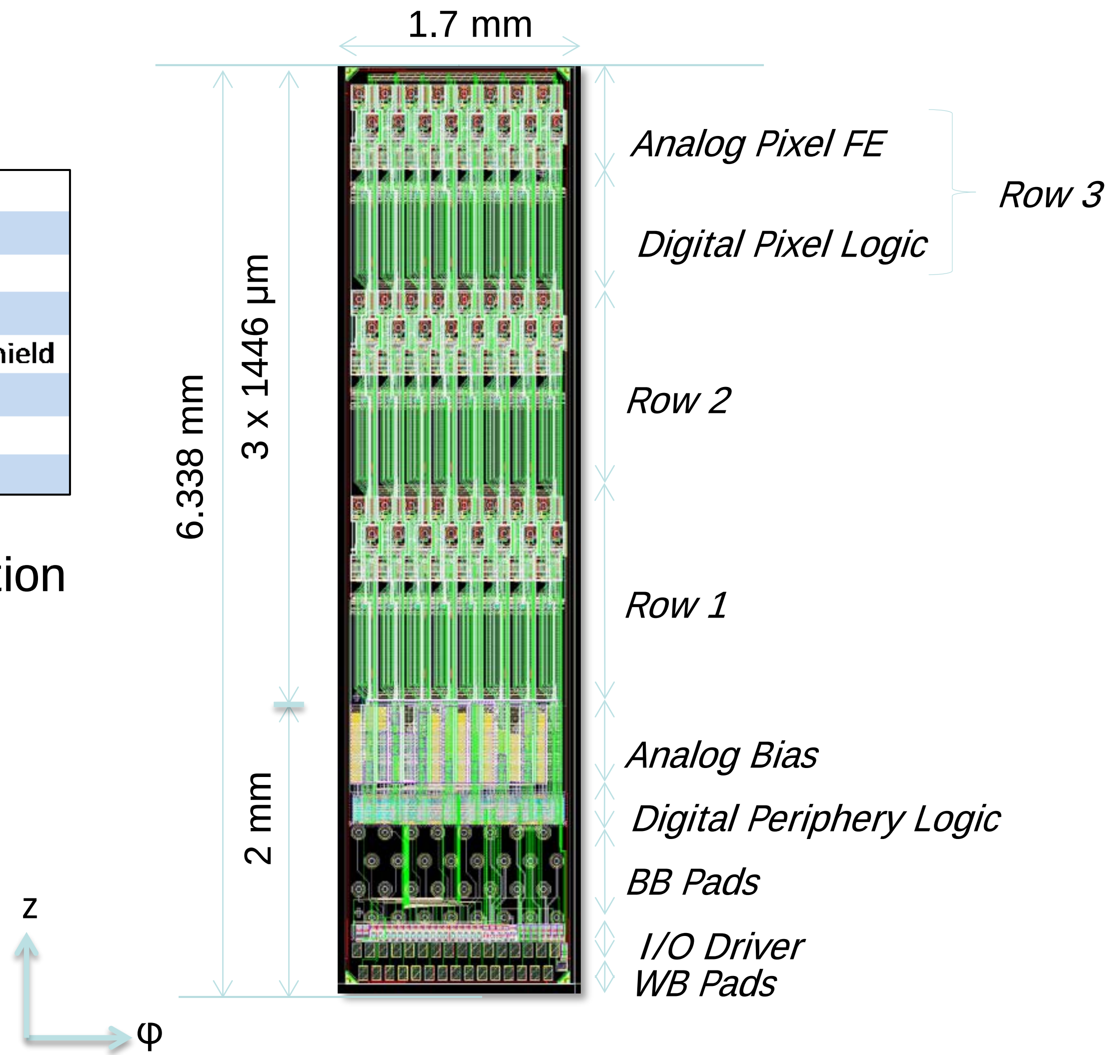


# MPA-light ASIC layout

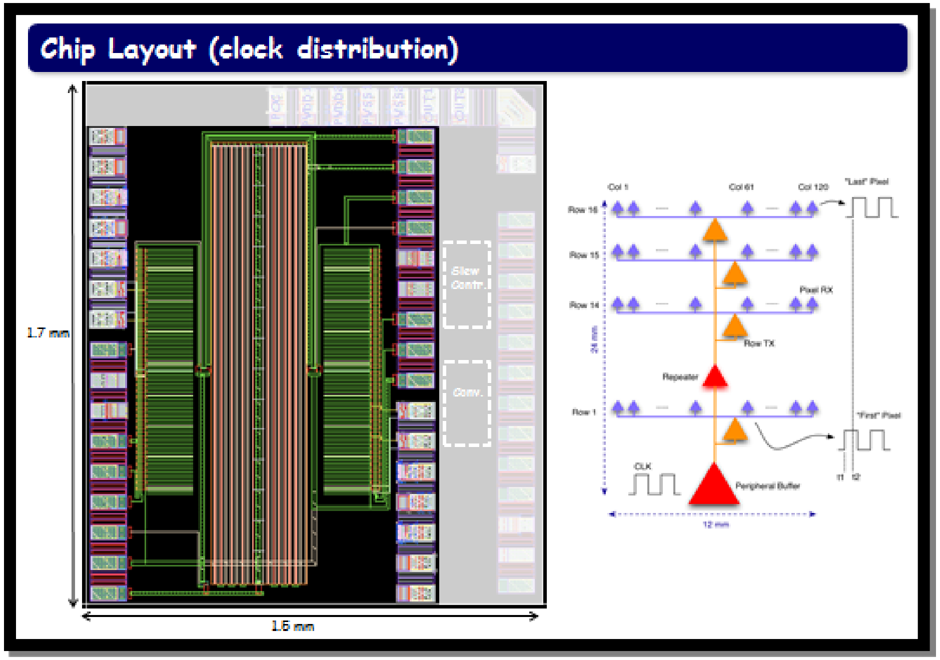
TSMC LP 65nm
8 Metal layers process option

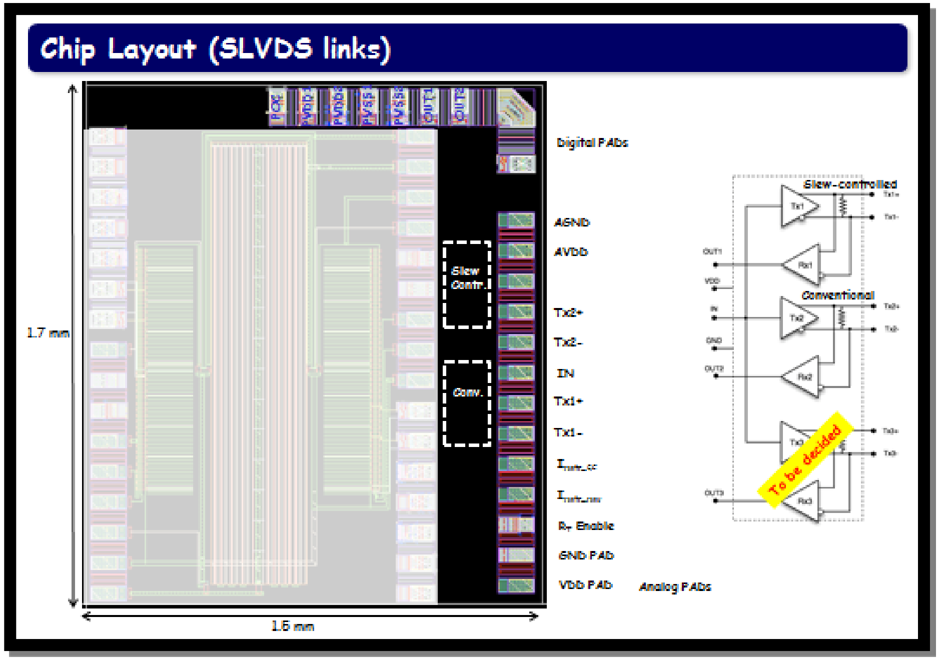
| | | | |
|---|---|---|---|
| M1 | m1 | local | cell |
| M2 | x | local | cell |
| M3 | x | local | cell and block |
| M4 | x | local | cell and block |
| M5 | x | regional | cell and group and shield |
| M6 | z | global | clk and pwr |
| M7 | u | global | clk, pwr and shield |
| M8 | RDL | global | pads and GND |

Status: Submitted for fabrication on Sept. 18, 2014



# MPA: Clock tree & sLVS IO pads

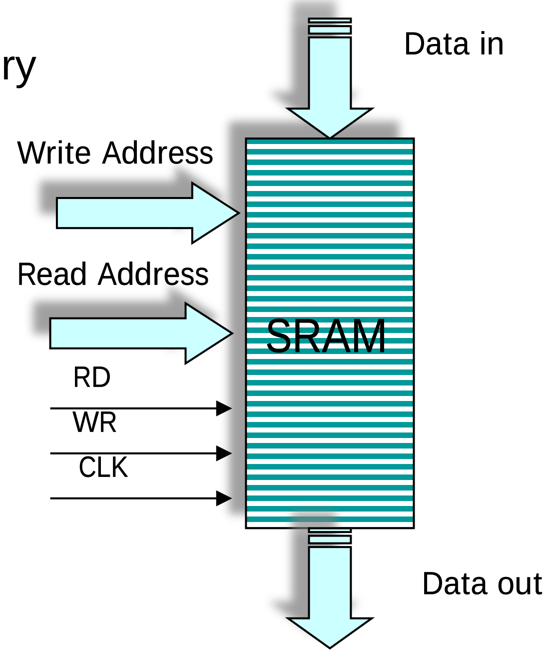


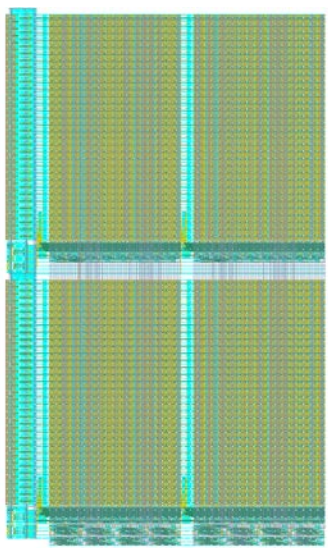



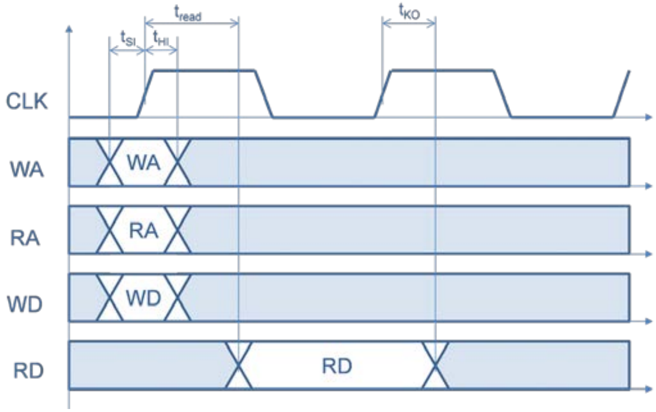

- Clock Distribution test structures
  - Low power clock distribution scheme for the MPA ASIC
- sLVS IO pad test structures
  - Differential driver & receiver pads running at 320Mbps @ 0.8V, 640Mbps @ 1.2V

# MPA: SRAM IP block test structures

- Clock synchronous, pseudo dual-port memory
  - Write/Read operation @ same clock cycle
- Operating speed: 80 MHz @ 1.2 V
- Compatible with the TSMC 65nm CMOS
  - Only lower 4 metal levels used in the SRAM block
  - Only Standard-Vt transistors
  - Special design techniques for radiation tolerance
- Memory Compiler specifications:
  - Minimum size: 128 words of 8 bit
  - Max size: 1k words of 256 bits
- Development work is outsourced
- Design Validation:
  - Prototyped 2 memory blocks of different sizes





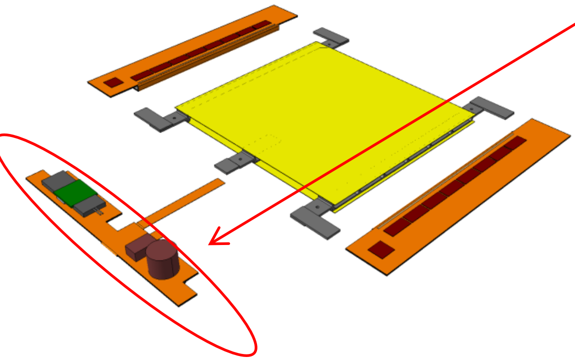
# II) The Electronics of the CMS Outer Tracker Upgrade

a) System

b) FE Electronics for 2S modules

c) FE Electronics for PS modules

d) FE Services



PH-ESE Seminar

Francois Vasey

Slide material from: G. Blanchot, J. Troska, P. Moreira, M. Pesaresi, and many others

# 1. Power

Power Dissipation per Module

- 2S
  - CBC 1.8W
  - CIC 0.4W
  - LP-GBT 0.5W

  } 2.7W@1.2V

  - VTRx+ 0.3W 0.3W@2.5V

- PS
  - SSA 0.6-1W
  - MPA 3-4W
  - CIC 0.4W
  - LP-GBT 0.5W

  } 4.5-5.9W@1.2V

  - VTRx+ 0.3W 0.3W@2.5V

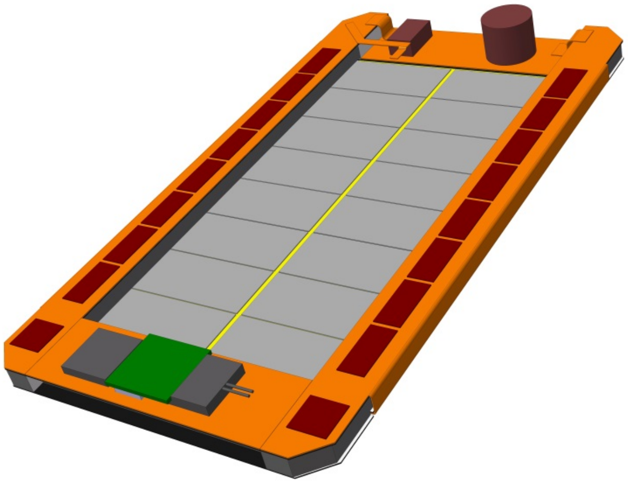
- Plus DC/DC converter (75% efficiency)

---

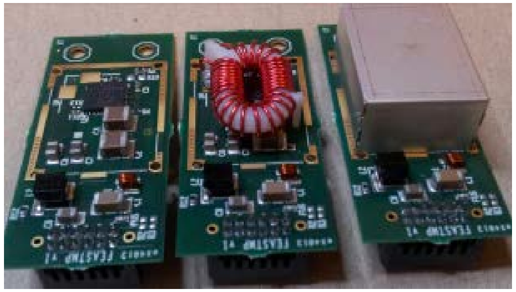
4W 6.5W – 8.5W

- Powering task force at work
  - Power requirement per module exceeds current phase IDC/DC converter capability
  - New DC/DC converters need to be developed
  - Sparing power wherever possible to maintain material budget low
    - Decrease digital supply voltage to 0.8V?

# Powering status



FEASTMP example delivers one voltage output only:



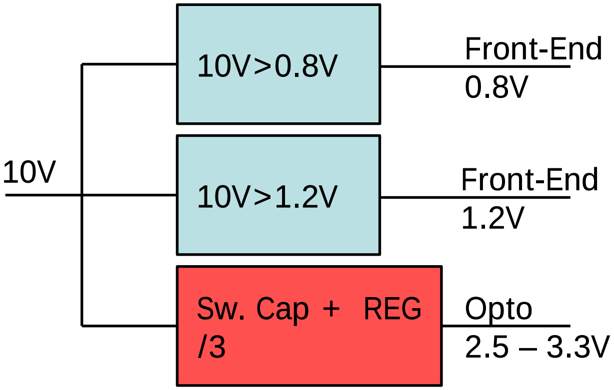
Need to fit more power devices (DCDCs or Switched Cap).

Integration needs to be much more compact.

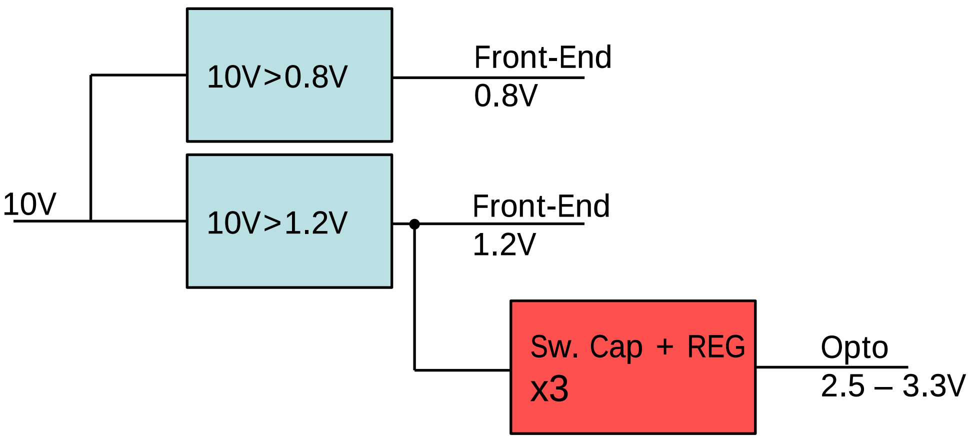
In all cases new devices or developments are required.

Powering discussions have initially identified 3 schemes to be evaluated to power the PS modules.

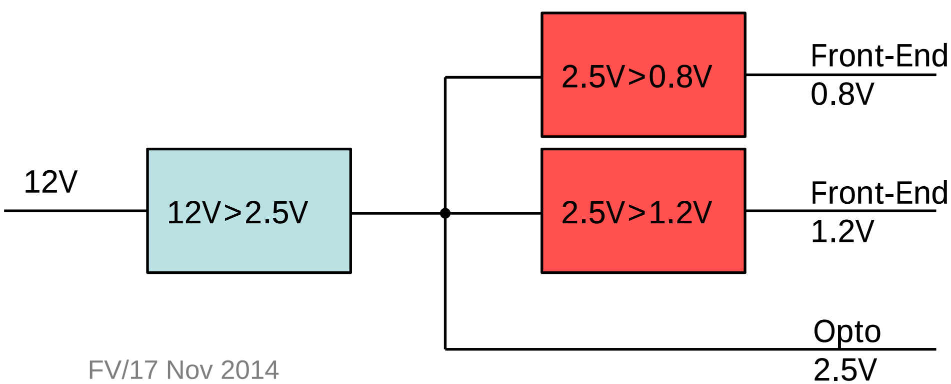
# Initial Schemes Considered




- **Scheme 1**: 2 FEASTMP + 1 SC + REG
  - Only one FEASTMP can fit today the service boards.
  - 10V Input in switched cap /3 is complex.

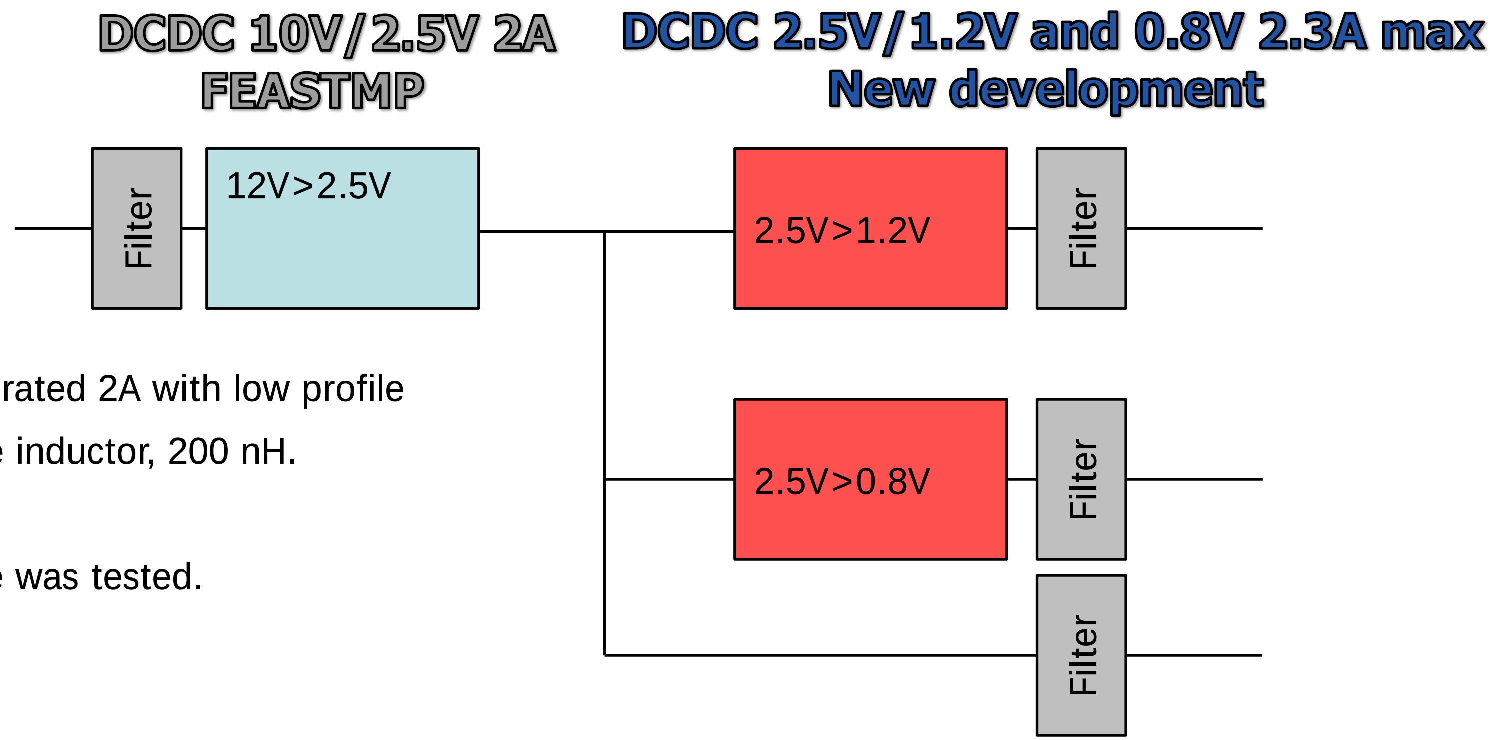



- **Scheme 2**: 2 FEASTMP + 1 CP + REG
  - 2 FEASTMP are not fitting.
  - Possibly inefficient and complex charge pump.




- **Scheme 3**: 1 FEASTMP + 2 new POL DCDC.
  - Need to fit 3 DCDCs in the end.
  - New POL DCDC might be more compact and more efficient.
  - Mid voltage can be tuned for Opto.

# Baseline Scheme Established

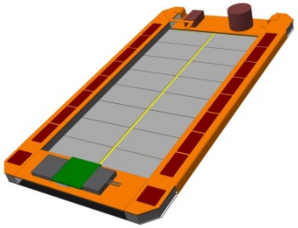



FEASTMP rated 2A with low profile

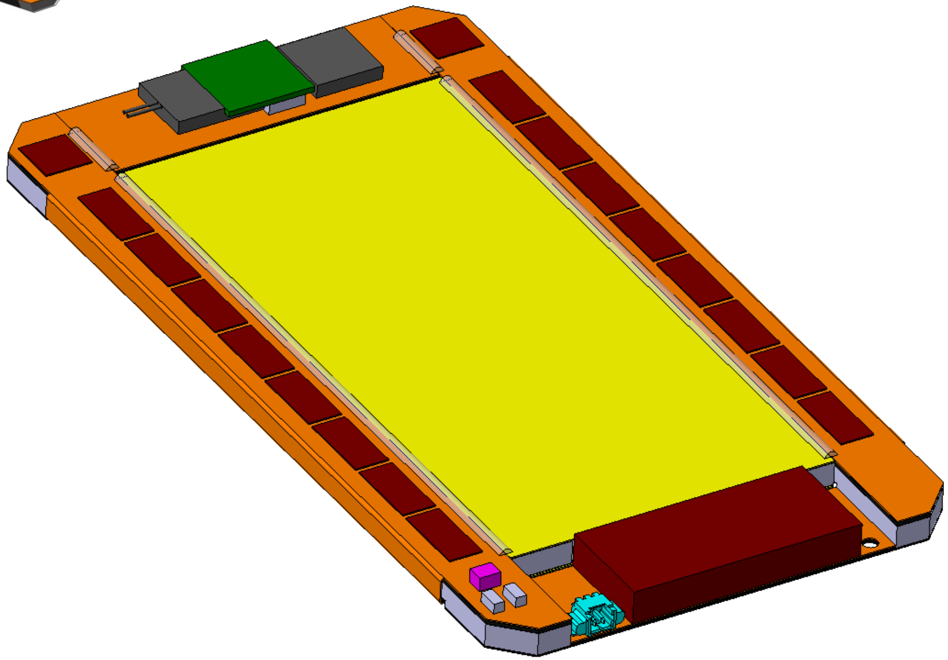
ECCA wire inductor, 200 nH.

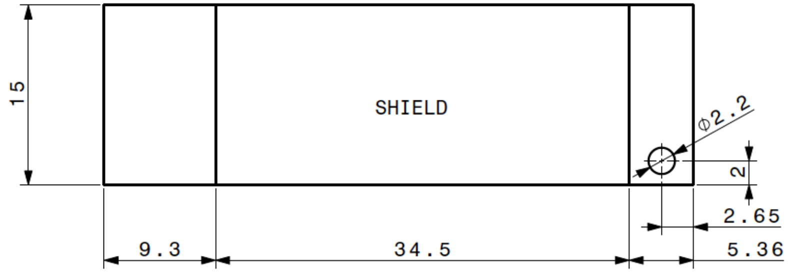
This stage was tested.

- New development. Using same low profile ECCA wire inductor, 200 nH.
- 2.5V input: no internal regulator, no bootstrap cap.
- Low input and output voltages: small size caps.
- All this allows for a more compact design by default.



# Integration on PS Module



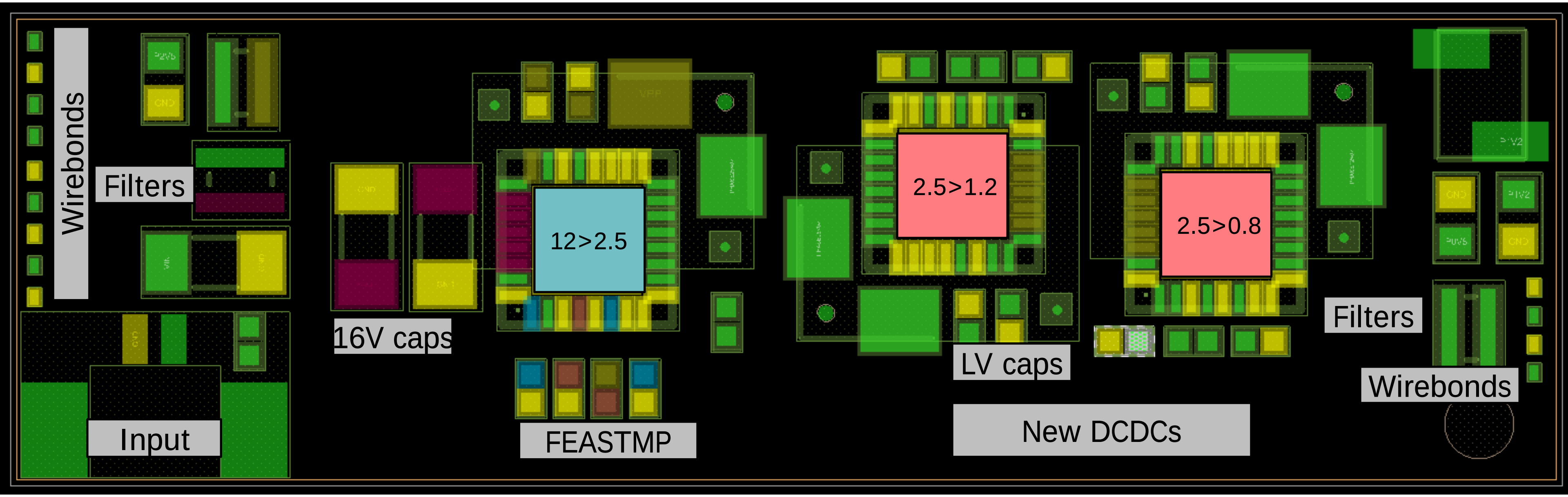



The PS module design was updated according to latest tests of DCDC integration exercises.

The HV filters are moved to the Hybrids, however the input HV cable is still placed on the service board.

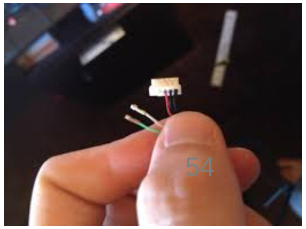
Flexible connections are today considered to link the service board with the hybrids, but this is subject to discussions also.

# Service Hybrid with Staged DCDC scheme



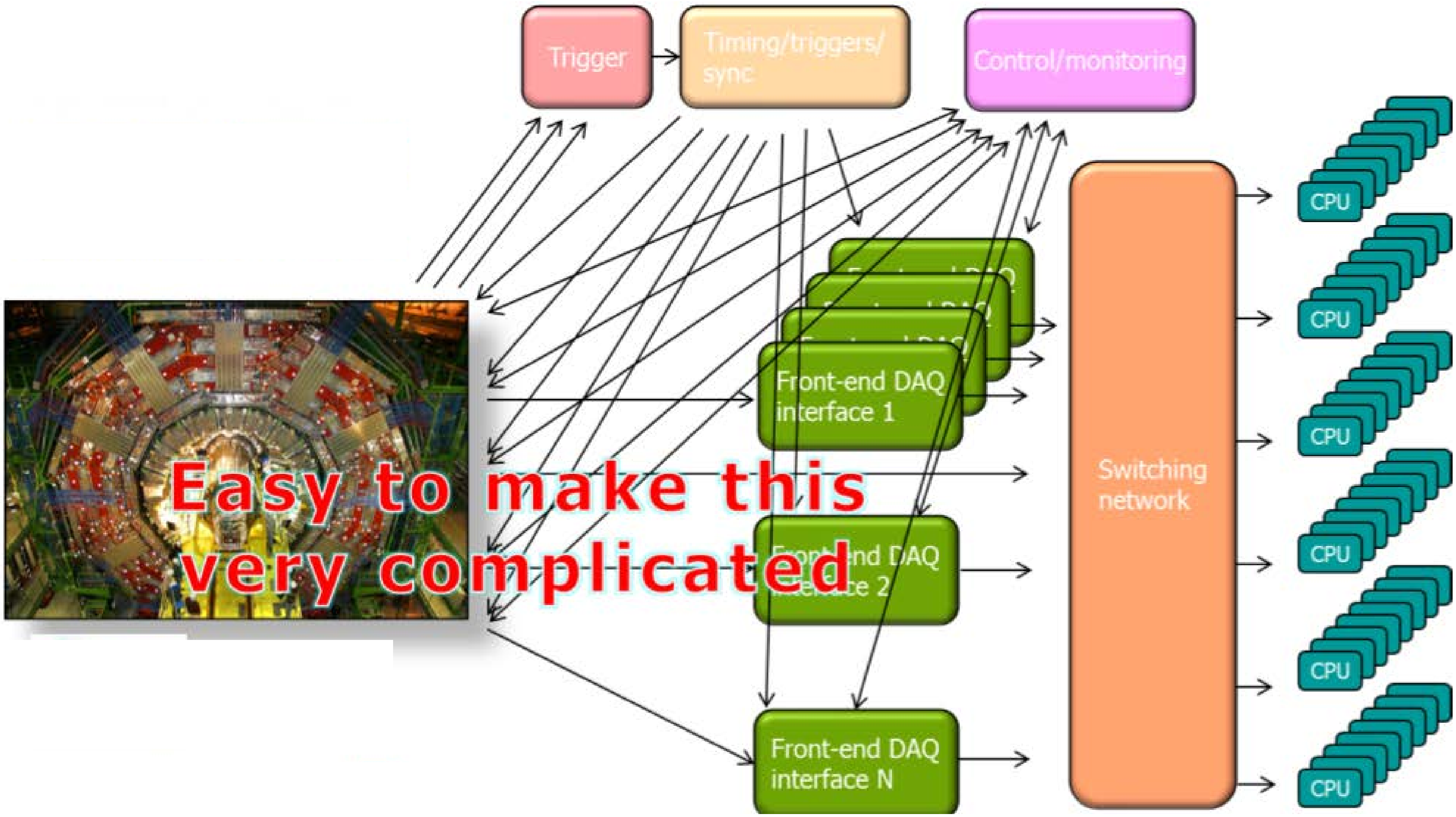

The new LV DCDCs still based on the FEASTMP geometry. However we can consider a smaller package for this chip.

The 3 DCDC stages can be fitted in the available board space without excessive compromise.

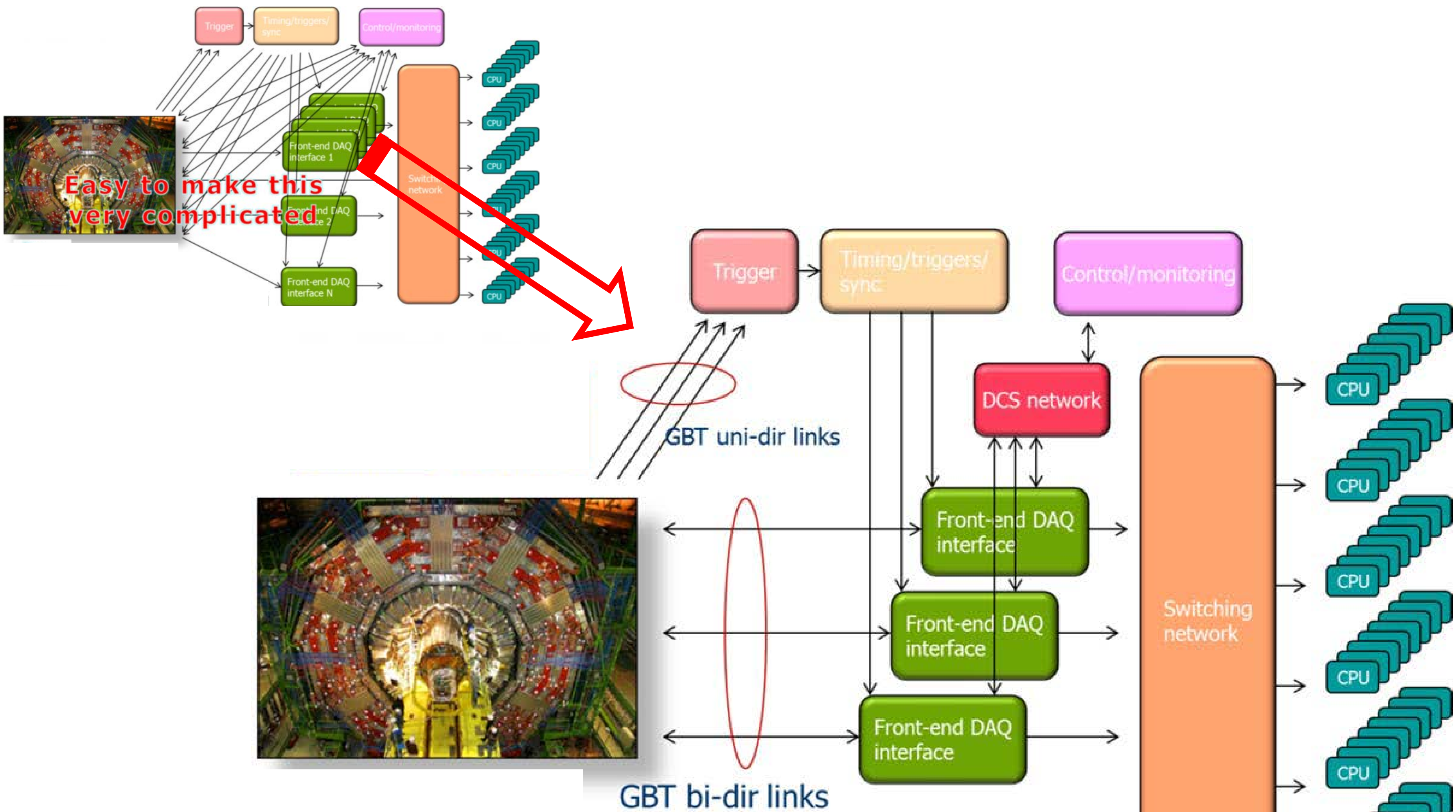


# 2. Optical Links

# Links @LHC

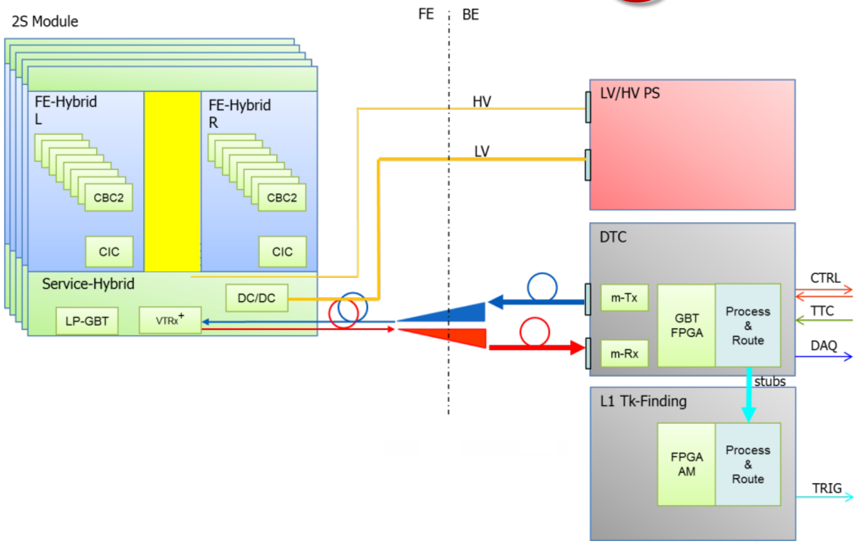

Trigger
Timing/triggers/ sync
Control/monitoring
Front-end DAQ interface 1
Front-end DAQ interface 2
Front-end DAQ interface N
Switching network
CPU
CPU
CPU
CPU
CPU
CPU
Easy to make this very complicated

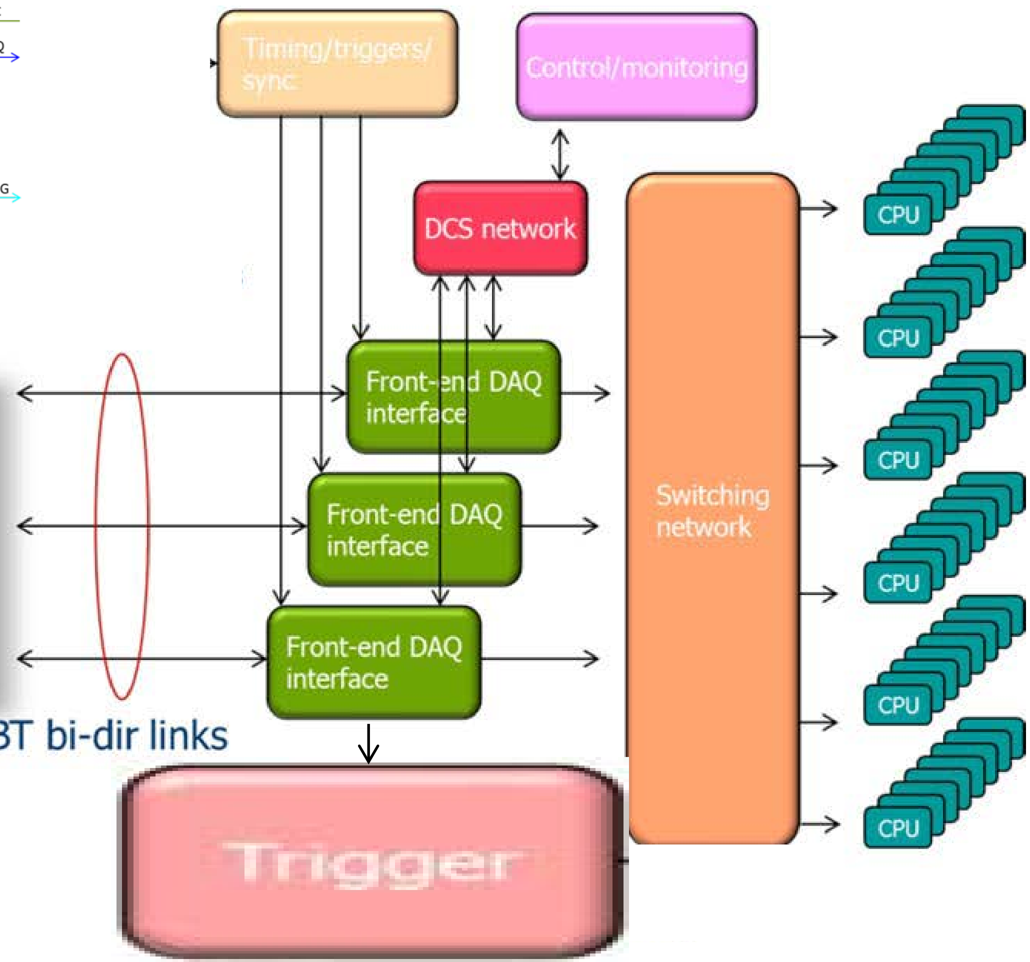
# Links@HL-LHC



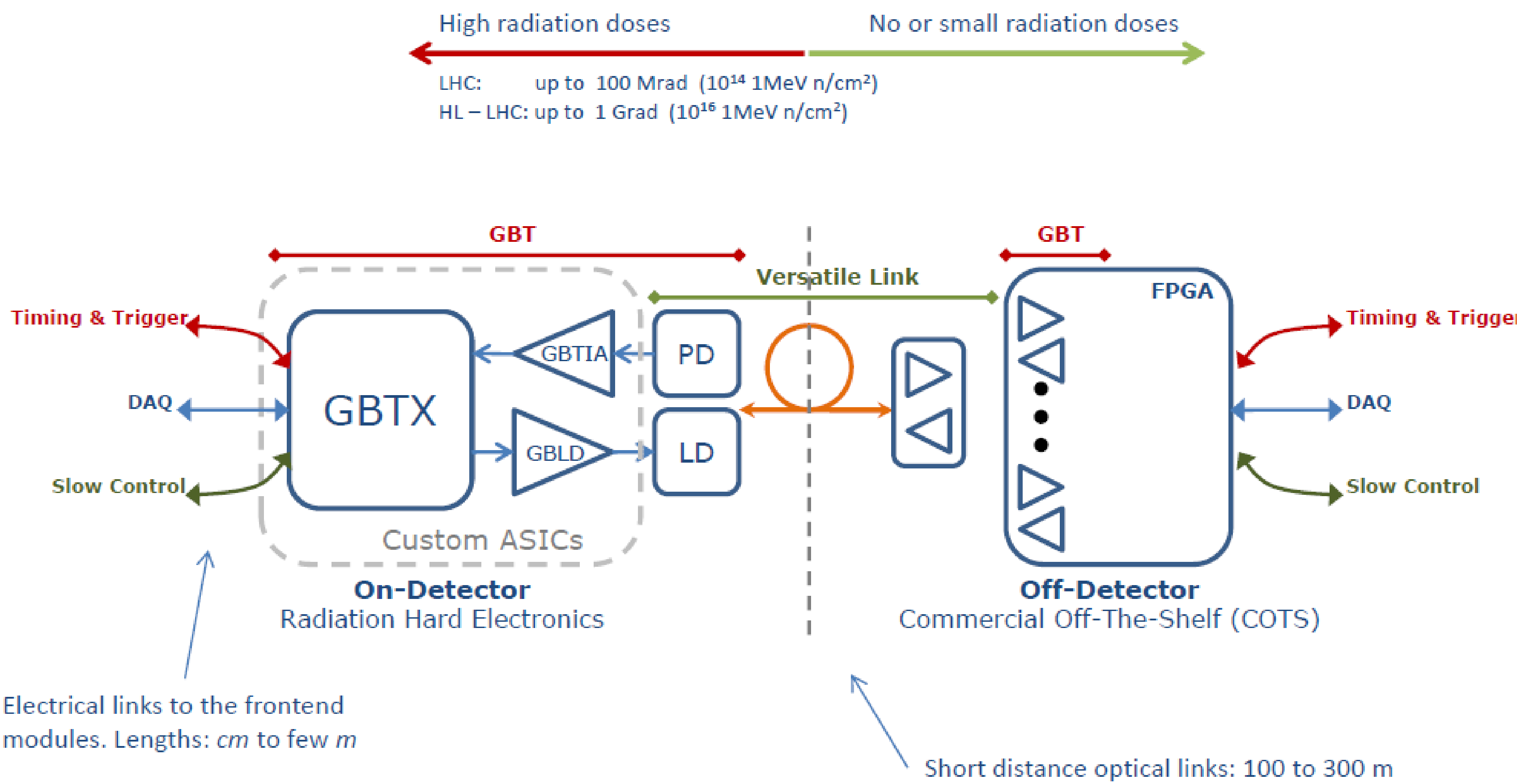

DCS network,
TTC distribution network
and DAQ network
Fully in counting house (COTS)

# Links@HL-LHC CMS Tk



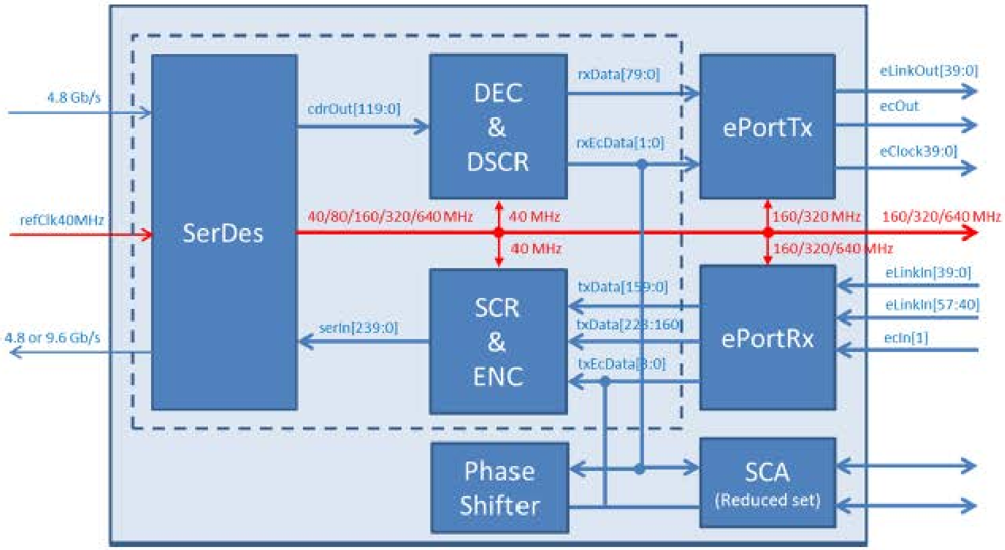



# GBT - Versatile Link Architecture



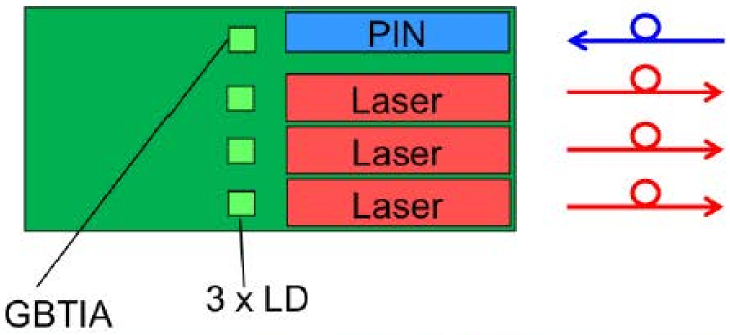
# The Low Power GBTX - LpGBT

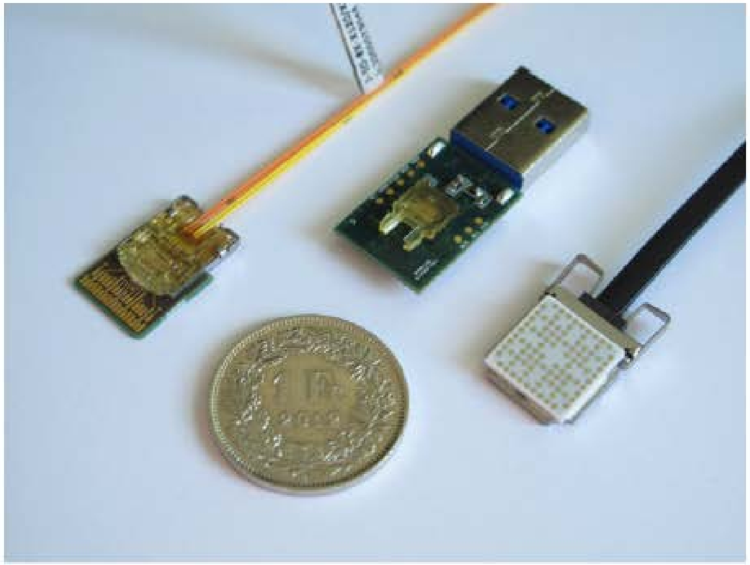
- Low Power Dissipation and Small Footprint:
  - **Target: 500 mW**
    - (GBTX: 2W)
  - Critical for pixel detectors
  - Critical for tracker/triggering detectors
- Bandwidth:
  - Low-Power mode
    - 4.8 Gb/s for Up and Down links
  - High-Speed mode:
    - 9.6 Gb/s for the Up-link
    - 4.8 Gb/s for the Down-link
- e-Links:
  - 80, 160 and 320 Mb/s for down-links
  - Low-Power Mode:
    - 80, 160 and 320 Mb/s for up-links
  - High-Speed Mode:
    - 160, 320 and 640 Mb/s for up-links
  - Programmable: Single-ended / differential
- Functionality:
  - "Replica" of the GBTX
  - Small subset of the GBT-SAC functionality will be included



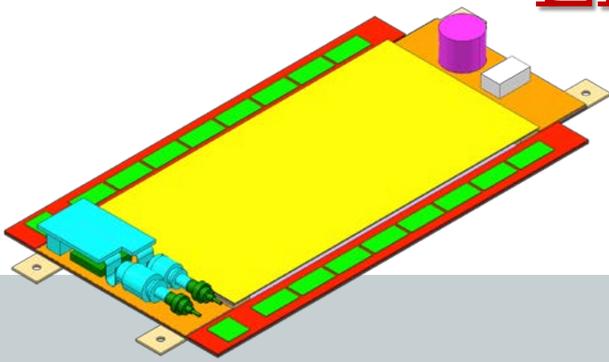
# The Versatile Link +

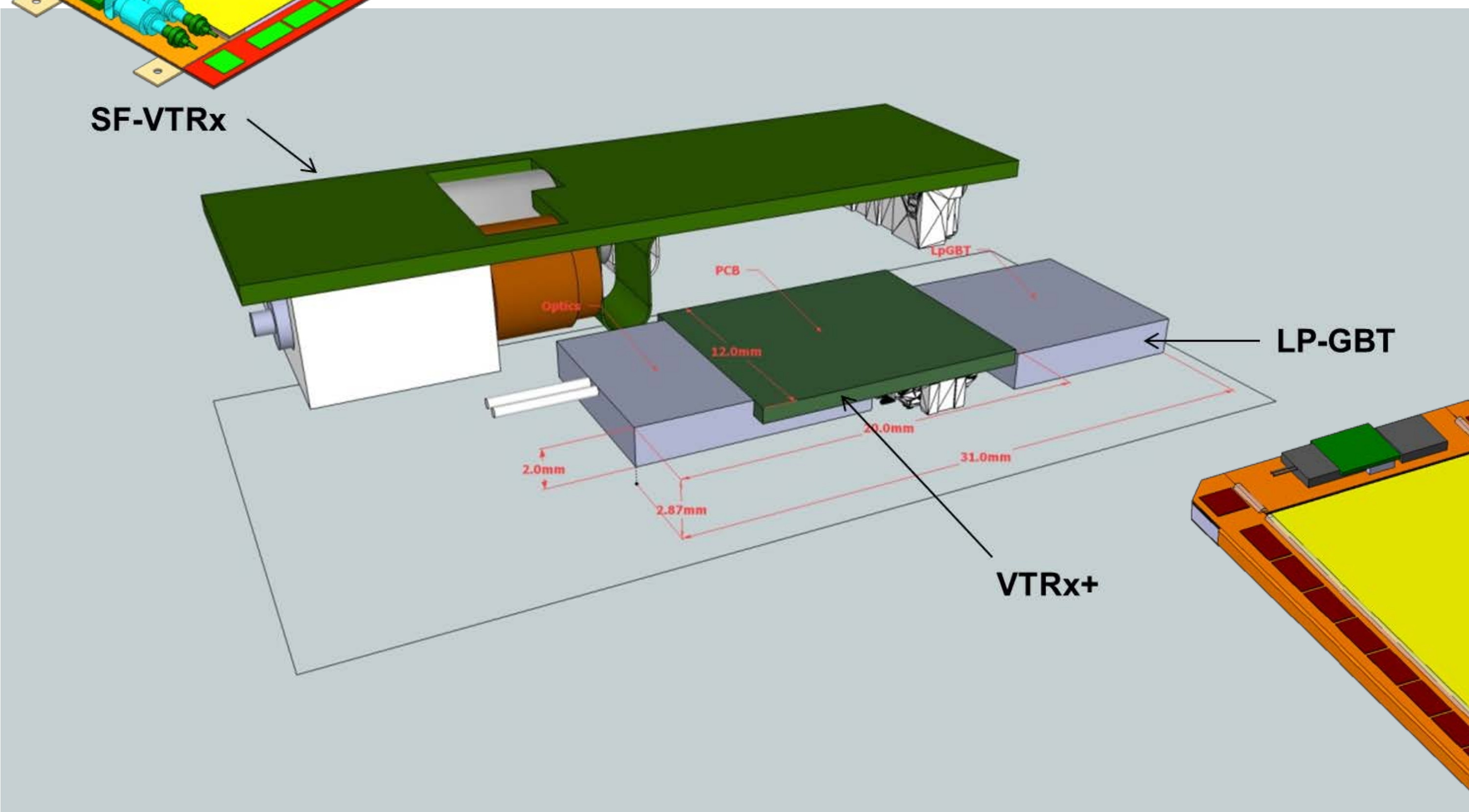
- Small form factor, high speed optical modules needed for:
    - CMS tracker modules
    - ATLAS EoS
- 5G downstream, 10G upstream:
    - Driven by GBTX evolution path
    - 10G laser driver ASIC
- Smaller
    - Revised optical interface
    - MM only
- Denser
    - Up to 4 channels
- Versatile
    - Common package
    - Number of up/down links
    - Configurable at assembly time or by turning off unused channels
- On-going work
    - 10 Gb/s tiny single/quad LD
    - Package, fibres, connectors
    - Feasibility study until fall 2015

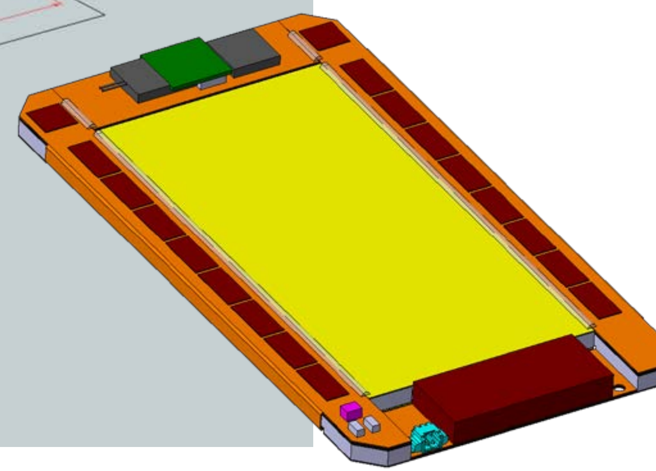


# Link Integration





# II) The Electronics of the CMS Outer Tracker Upgrade

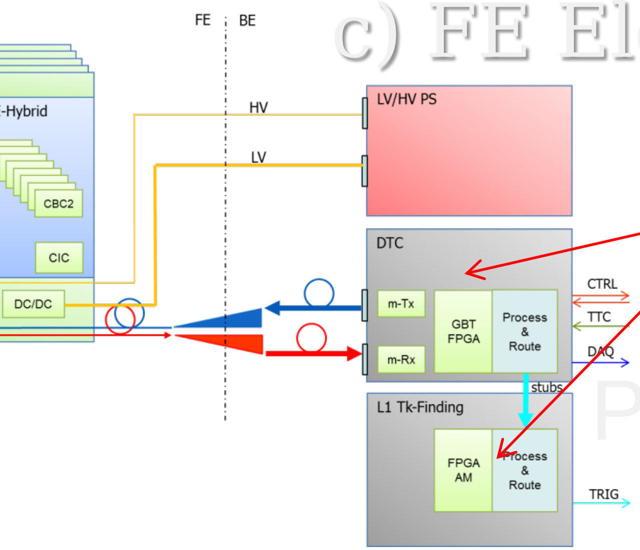
a) System

b) FE Electronics for 2S modules

c) FE Electronics for PS modules

d) FE Services

e) Back-End




PH-ESE Seminar

Francois Vasey

Slide material from: J. Olsen, M. Pesaresi, P. Vichoudis and many others

# 1. Back End DTC

Back-End DTC will be developed as late as possible to profit from latest available technology and cost reduction.

In the meantime, GLIB, FC7 and CTA boards have been developed:

uTCA FPGA-based general purpose boards suitable for production systems or prototyping/benchtop use

- Commonalities
  - Xilinx FPGA-based
  - FPGA Mezzanine Card (FMC) carriers
  - High-speed serial transceivers (GTX)
  - Advanced Mezzanine Card (AMC) format
  - Compliant with the CMS specification for uTCA systems
- Differences
  - FPGA series/families
  - Position of FMC sockets
  - GTX count and performance
  - IO pin count
  - Memory resources
  - Monitoring & other advanced features

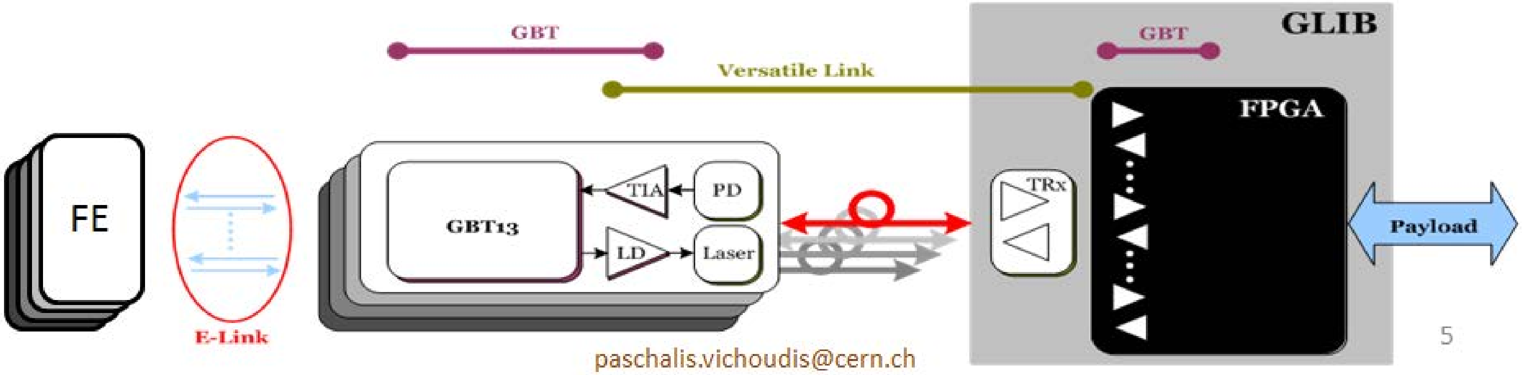
# 1.a GLIB

**GLIB** (Gigabit Link Interface Board)

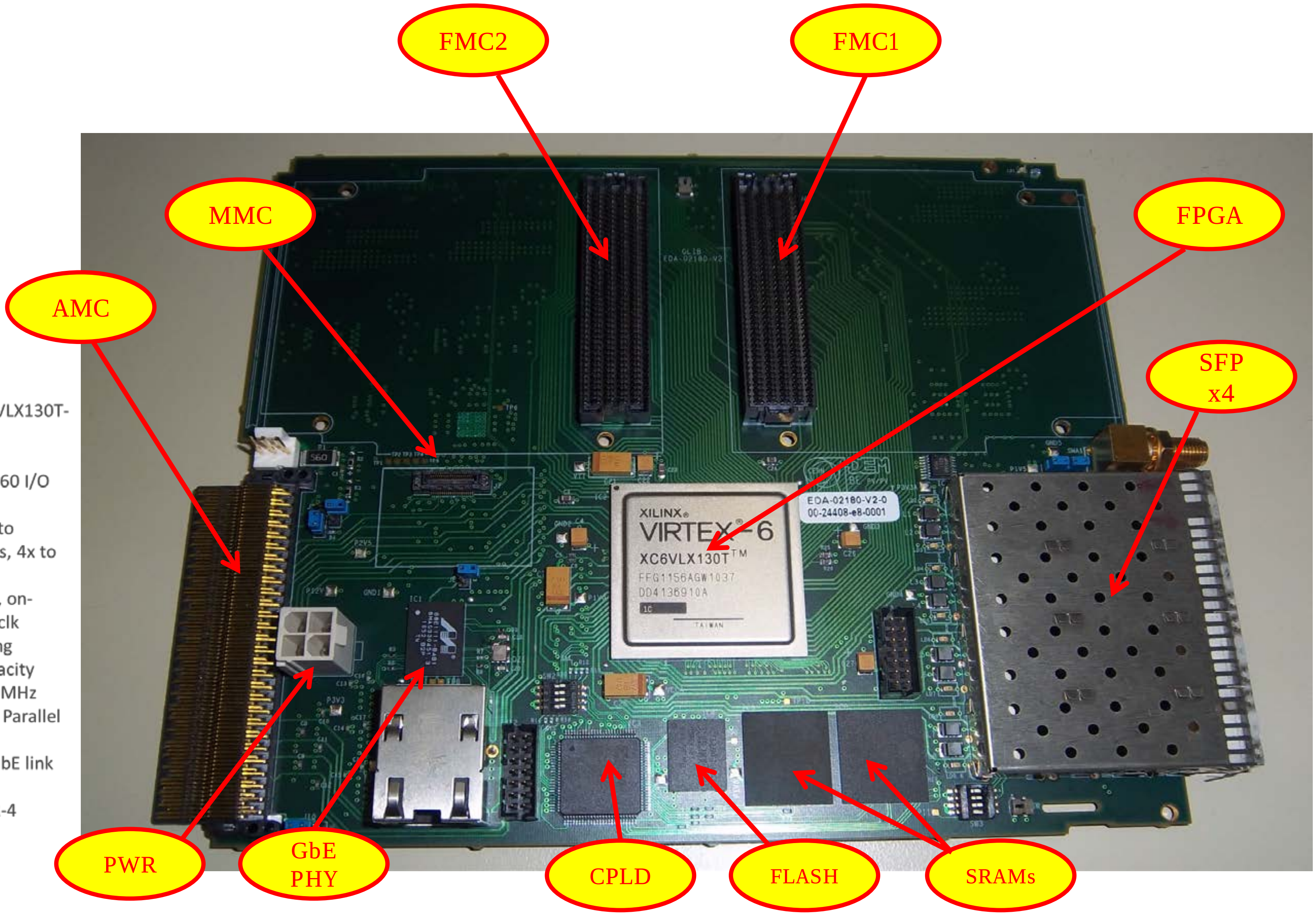
Evaluation platform and an easy entry point for users of high speed optical links

Targeted for

- optical link evaluation in the laboratory
- control, triggering and data acquisition from remote modules in beam or irradiation tests



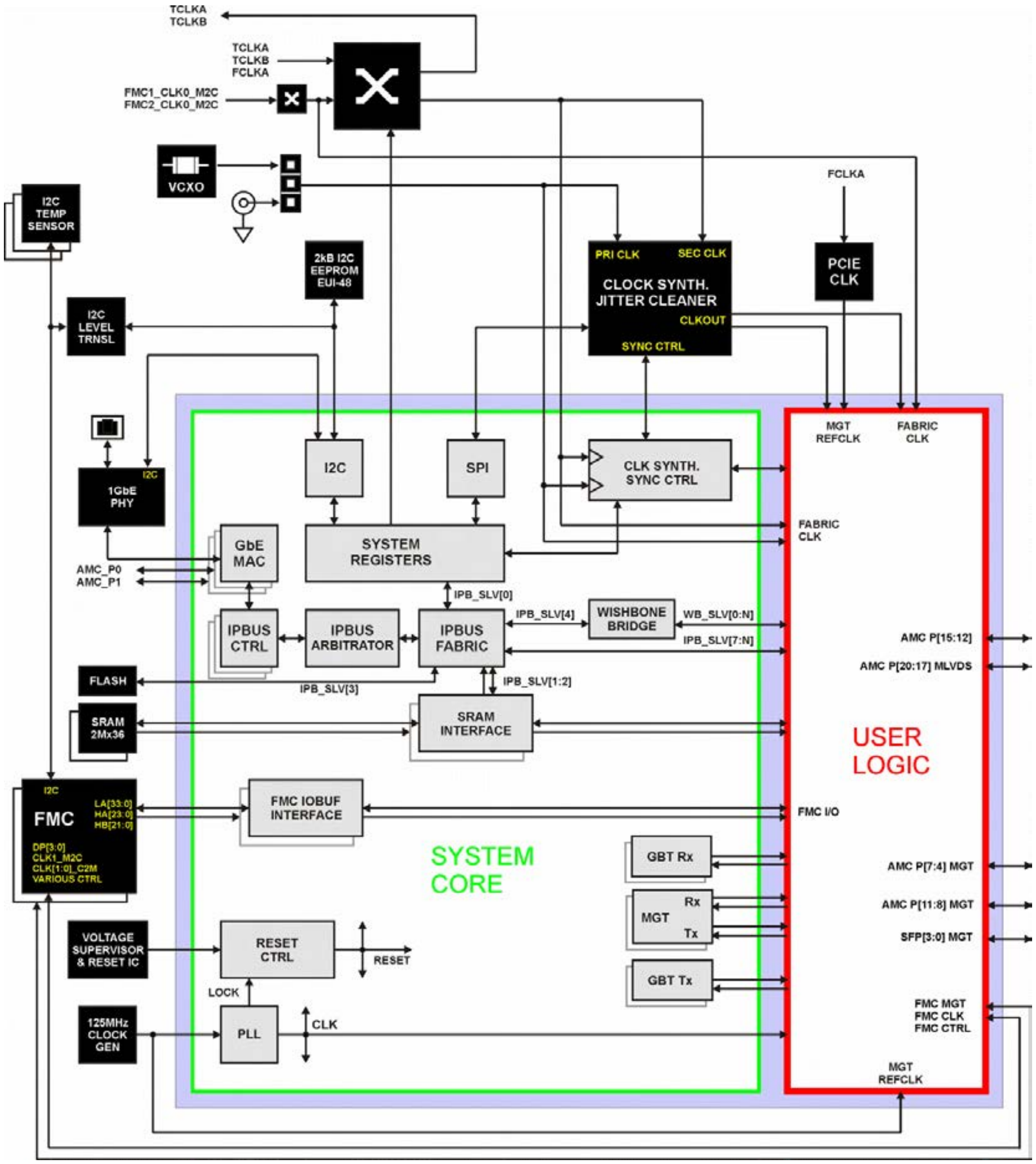
# GLIB Hardware




**Main h/w features**

- FPGA: Xilinx Virtex-6 (XC6VLX130T-1FFG1156C)
- FMC: 2x sockets (only one accessible when in crate), 160 I/O per FMC
- GTX: max rate 5Gb/s, 10x to backplane, 4x to SFP sockets, 4x to FMC1
- Clocking: x-point switches, on-board xtals, jitter cleaners, clk synthesizer, external clocking
- Memory: SRAM, total capacity 144Mb, max frequency 200MHz
- FPGA configuration: JTAG, Parallel FLASH
- Benchtop use: on-board GbE link with RJ45
- PCB laminate: standard FR-4

# GLIB Firmware



# 1.b FC7

**FC7** (FMC Carrier based on 7 series FPGA)

designed to be an evolution of

- the **Gigabit Link Interface Board (GLIB)** – a highly successful project filling a similar role, with emphasis on GBT link testing


CERN GLIB

using design components, novel features and layout guidelines from

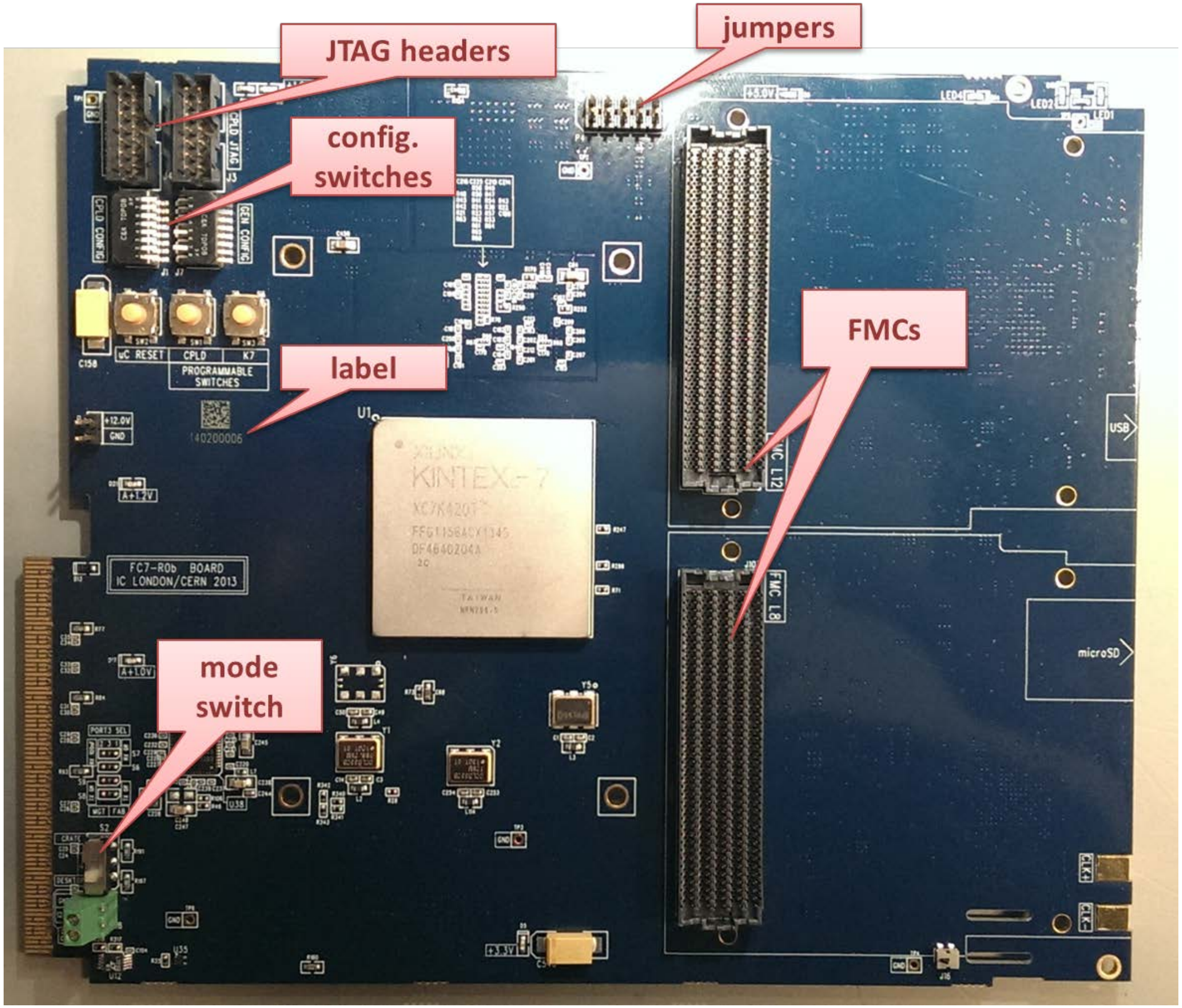
- the **MP7** – a high optical density O(Tbps) processing card to be used in the upgraded CMS Calorimeter Trigger

Imperial MP7

basing on existing hardware helps to reduce development time to maturity

- especially with regards to reuse of firmware and software components
- fewer nasty surprises!

# FC7 Hardware

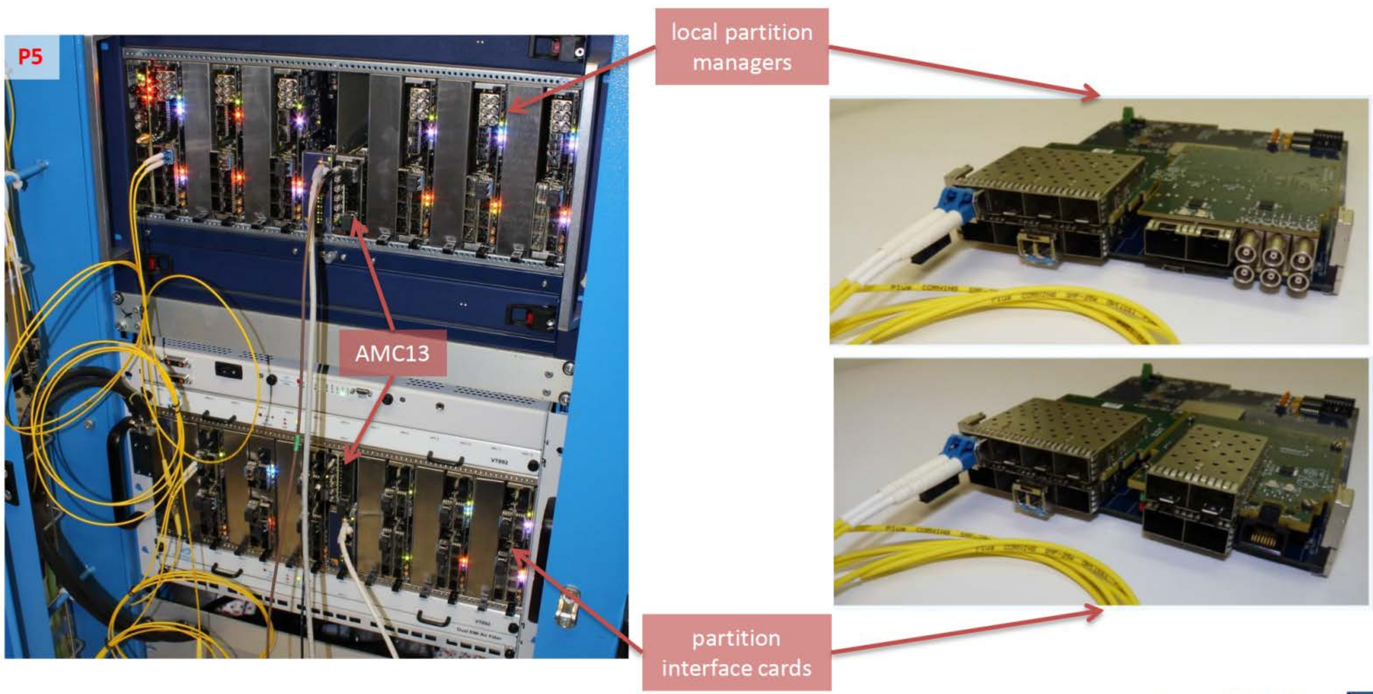



**Main h/w features**

- FPGA: Xilinx Kintex-7 (XC7K420T-2FFG1157C)
- FMC: 2x sockets (both accessible when in crate), 68 I/O per FMC
- GTX: max rate 10Gb/s, 12x to backplane, 20x to FMCs
- Clocking: x-point switches, on-board xtals, jitter cleaners, clk synthesizer, external clocking
- Memory: DDR3, total capacity 4Gb, max frequency 480MHz
- FPGA configuration: JTAG, SD card (for fast loading)
- Benchtop use: when used with the AMC bridge add-on card
- PCB laminate: NELCO N4000-13 EP SI

# FC7 for CMS-TCDS

- With 3 custom FMCs, the FC7 satisfies the role of 2 objects for the TCDS system
  - Local partition manager (interfaces with AMC13, DAQ, etc.
  - Partition interface (interfaces with partition managers and FEDs)
- 70pcs produced with >95% yield, 30pcs more to come



# 1.c CTA

**CTA** (**C**MS **T**racker **A**MC)

- flexible, uTCA compatible card for generic CMS data acquisition/control uses

- suitable for production systems or prototyping/benchtop use

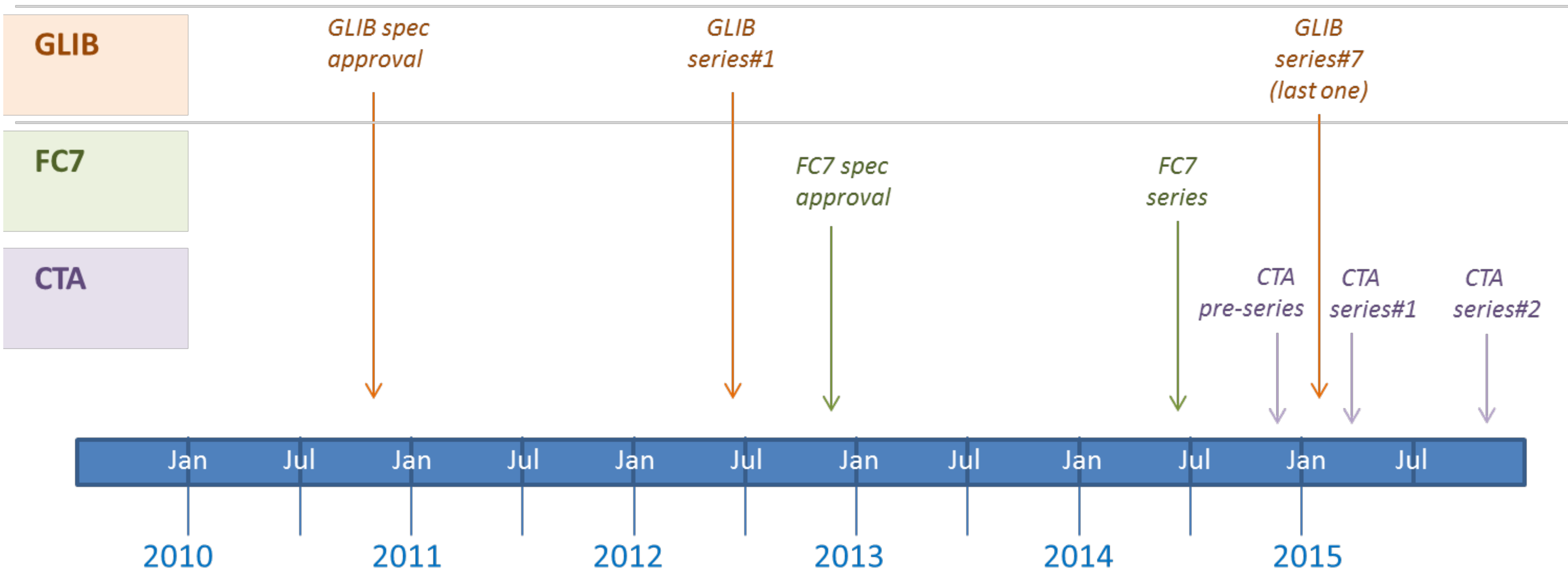
- collaborative effort between CERN & UK

- evolution of existing board designs (CERN GLIB & Imperial MP7)

- firmware partitioning is identical to GLIB

**CTA is an alias name of the 1st revision of the FC7 (aka FC7_R1)**

# Timeline

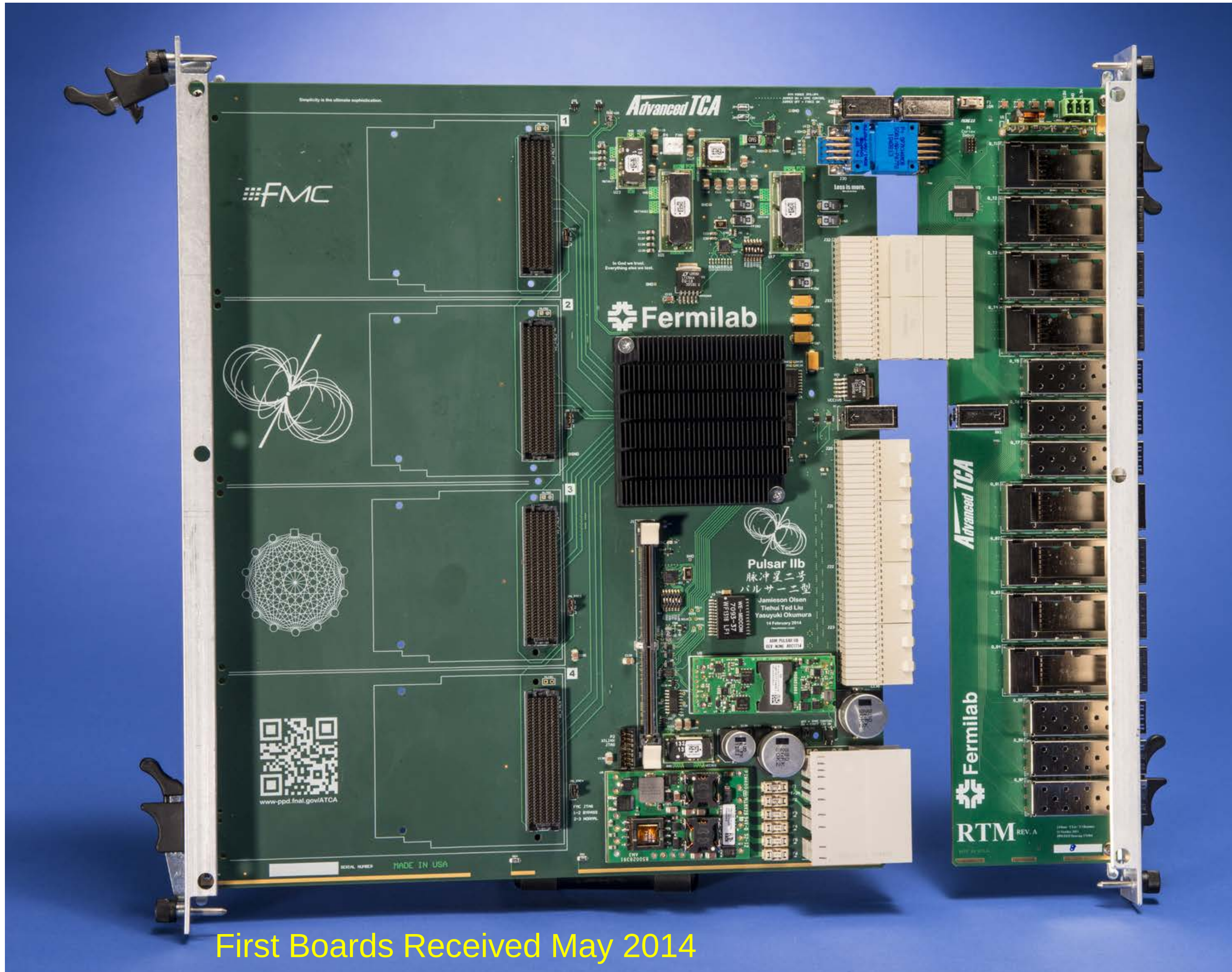

GLIB
FC7
CTA
GLIB spec approval
GLIB series#1
GLIB series#7 (last one)
FC7 spec approval
FC7 series
CTA pre-series
CTA series#1
CTA series#2
Jan
Jul
Jan
Jul
Jan
Jul
Jan
Jul
Jan
Jul
Jan
Jul
2010
2011
2012
2013
2014
2015

# 2. L1 Track Finding

- Three approaches currently under study
  - Associative Memory – based
  - Tracklet – based
  - Time Multiplexing – based
- All implement parallel processing, pipelined algorithms and time multiplexing
- All rely on latest generation FPGAs
  - AM-based approach relies also on high performance Associative Memory ASIC development
- Large and challenging system
  - beyond the scope of this lecture
- Two dedicated boards have up to now been presented
  - Pulsar IIb for AM-based approach
  - MP7 for Time Multiplexing approach

# 2.a Pulsar IIb, an FPGA-Based Full Mesh ATCA Processor Board and RTM

- Xilinx Virtex 7 FPGA
  - XC7VX415T – XC7VX690T
- Up to 80 GTH transceivers
  - 40 for RTM
  - 28 for Fabric
  - 12 for Mezzanines
- Four FMC Mezzanines
  - 35W, up to 60W possible
  - LVDS up to 34 Gbps unidirectional
  - 3 x GTH up to 30 Gbps bidirectional
- IPMC Mezzanine Card
- Backplane clock distribution
  - M-LVDS on CLK3A and CLK3B

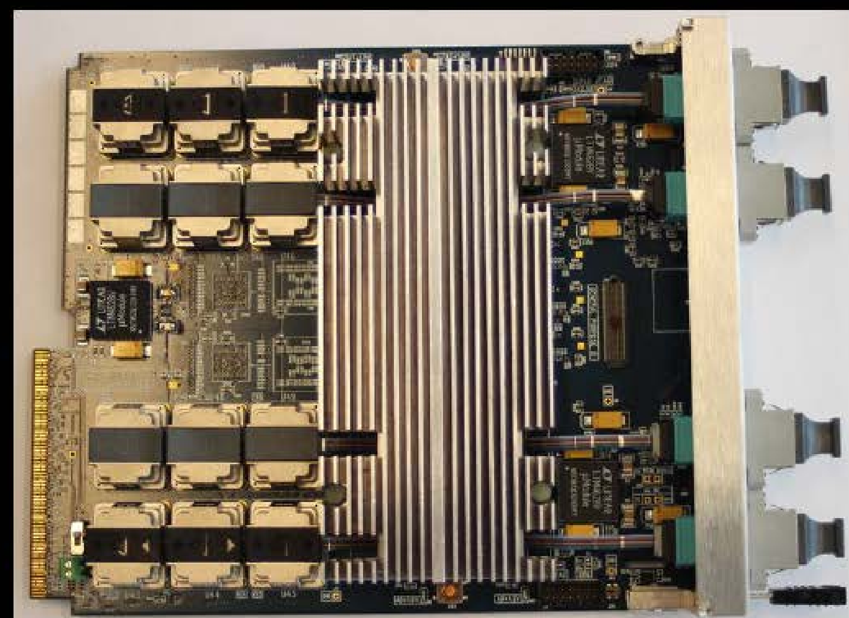


First Boards Received May 2014

# 2.b MP7

## The Master-Processor, Virtex-7 (MP7)

- uTCA form factor
- 72Tx+72Rx 13Gbps optical links
- 0.9 + 0.9Tb/s optical stream processor
- Xilinx Virtex-7 FPGA
- GbE, AMC13/TTC/TTS, PCIe, SAS, SATA, SRIO
- On-board firmware repository
- Pin-compatible FPGAs allow cost-performance balance
- 2×144Mbit 550MHz QDR RAM (optional)



# II) The Electronics of the CMS Outer Tracker Upgrade

a) System

b) FE Electronics for 2S modules

c) FE Electronics for PS modules

d) FE Services

e) Back-End

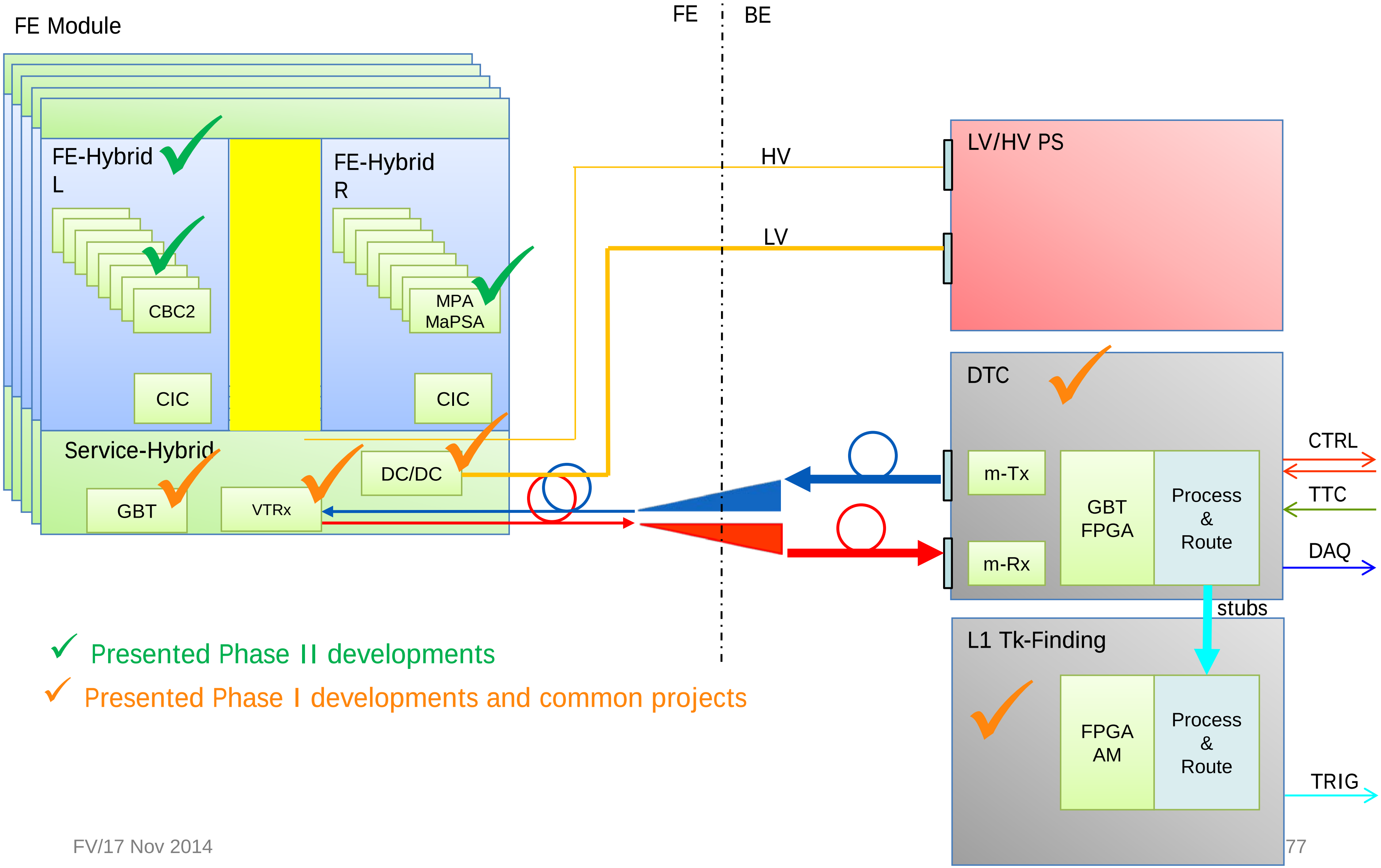
## f) System Demonstrator

PH-ESE Seminar

Francois Vasey

Slide material from: A. Honma, S. Mersi, M. Pesaresi and many others

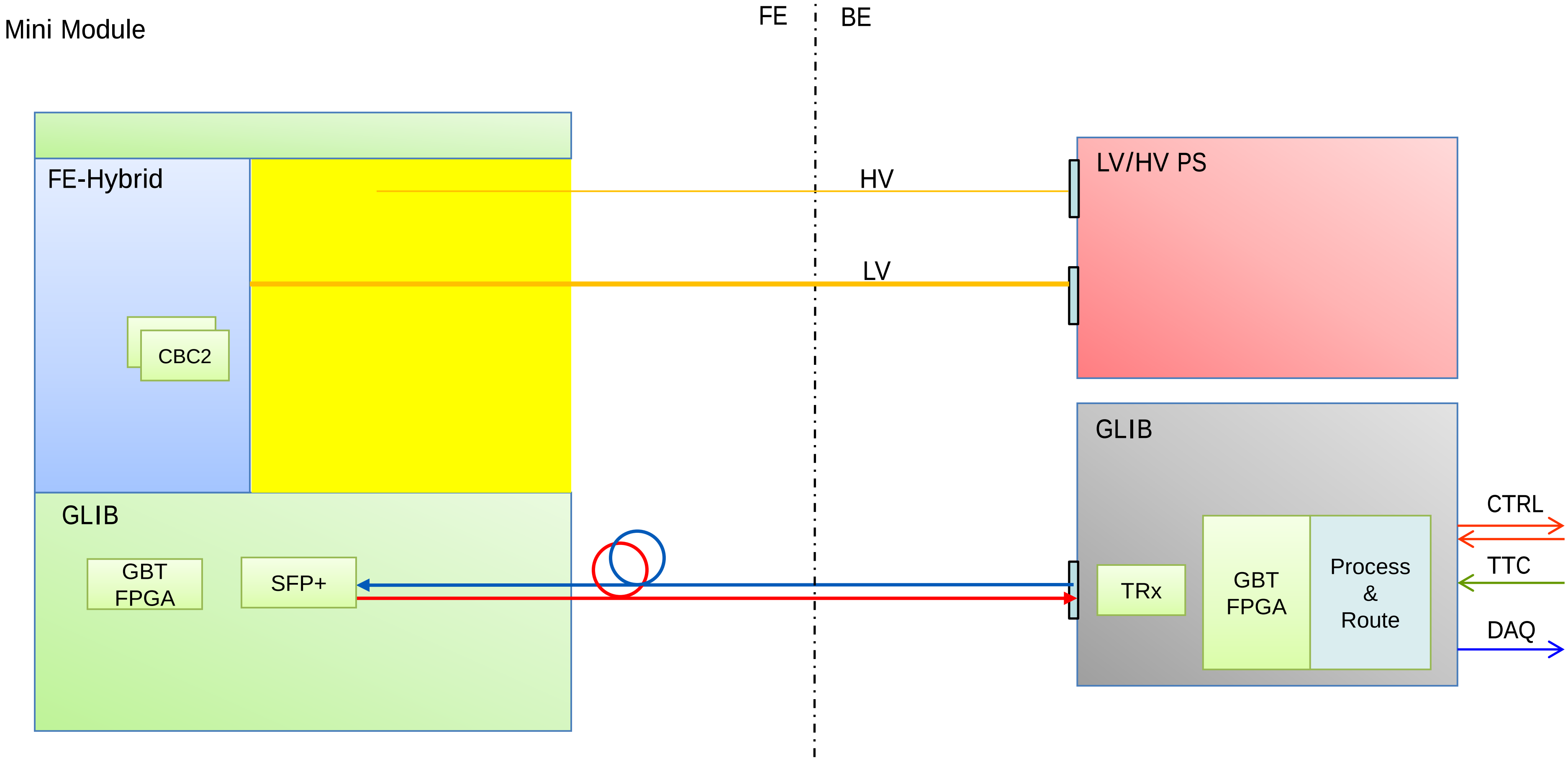
# Electrical System: Recap



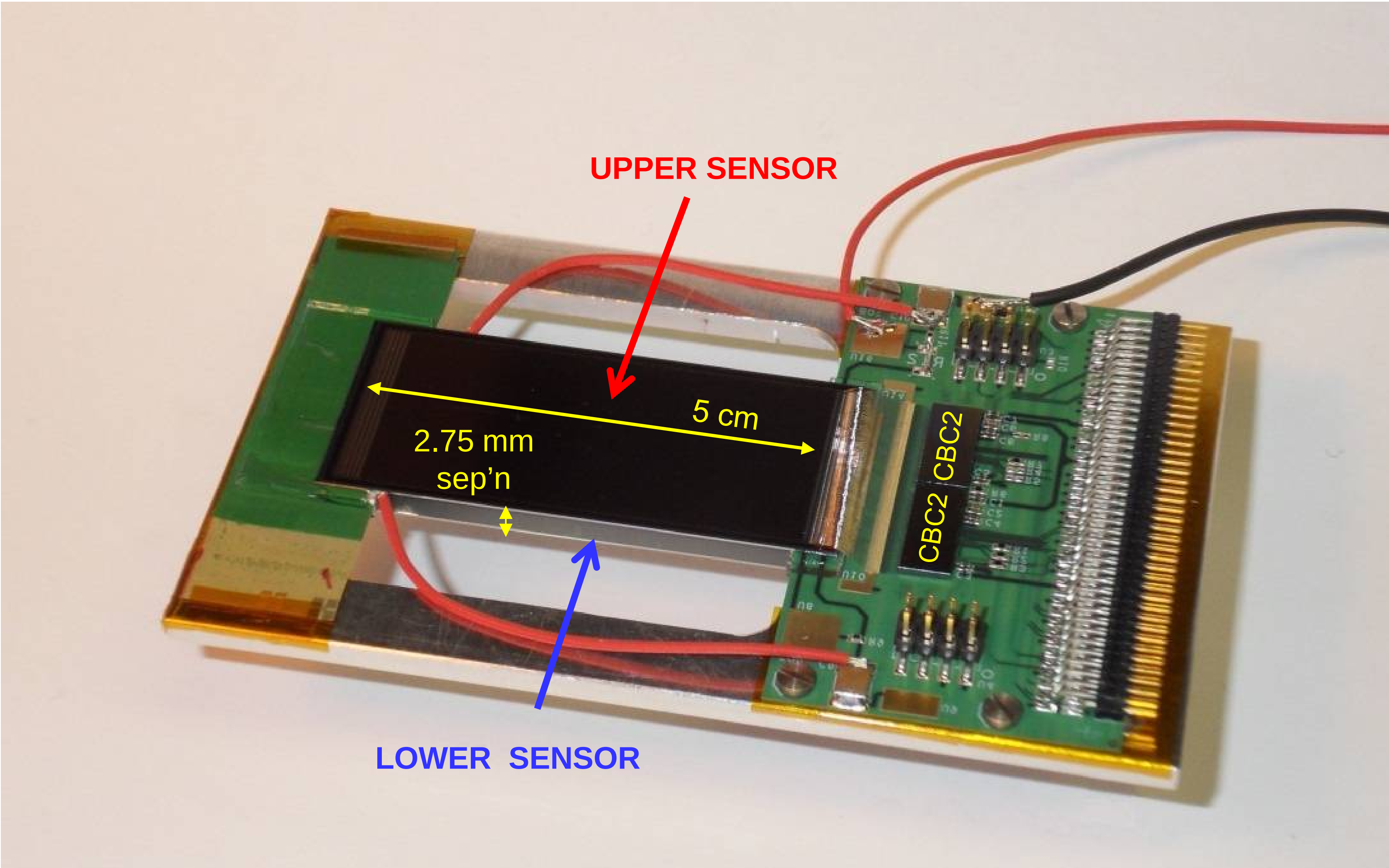

✓ Presented Phase II developments

✓ Presented Phase I developments and common projects

# Electrical System Demonstrator

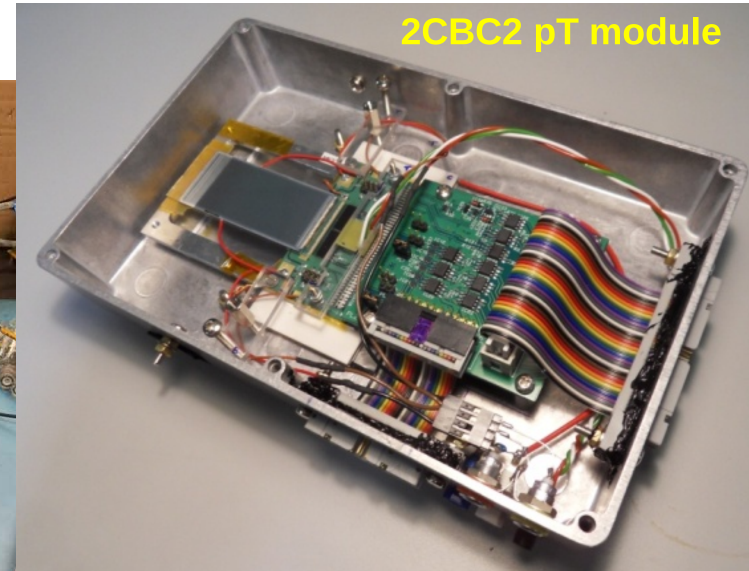


# Mini 2S-Pt Module




each CBC2 chip takes 127 inputs from upper sensor and 127 inputs from bottom sensor

# GLIB-GLIB DAQ Chain



# Desy test beam

25th November - 1st December 2013

Datura telescope + 2 pT modules

(1 rotatable to simulate B-field effect)

1) CNM sensors: p-on-n

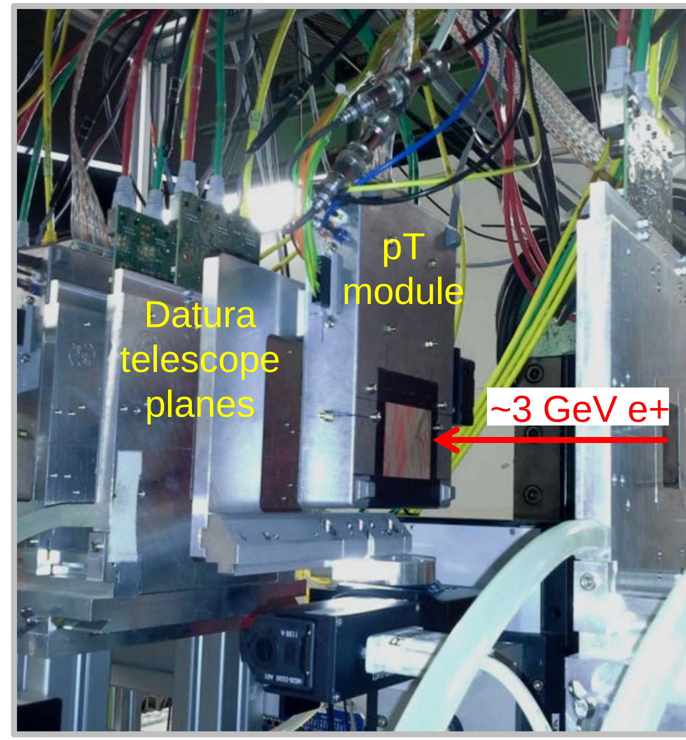
5 cm, 90 μm pitch

2) Infineon sensors: n-on-p

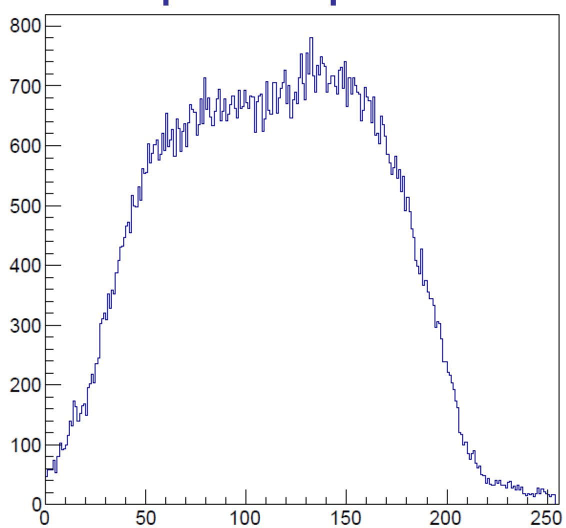
5cm, 80 μm pitch

control and DAQ based on CERN GLIB emulating GBT functionality

analysis ongoing

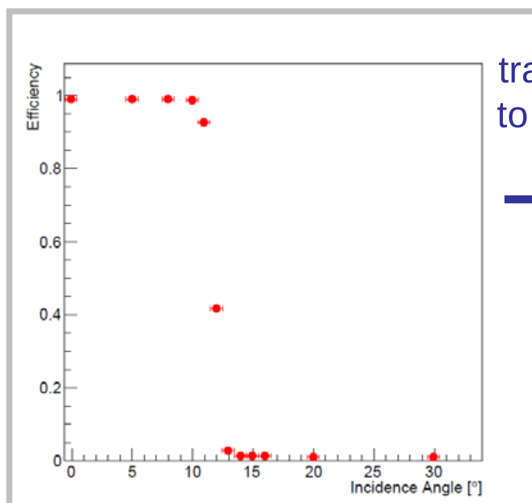



**beam profile in pT module**

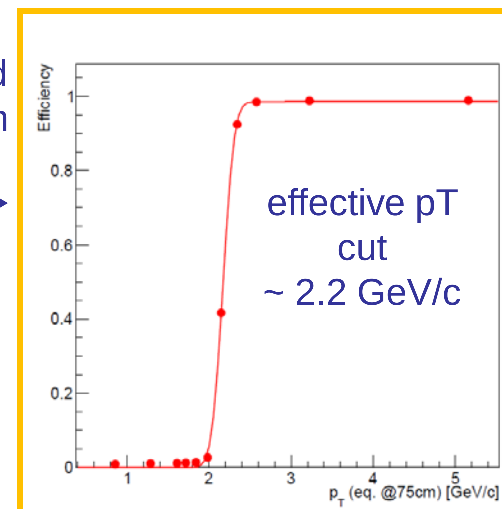



**angular scan of CNM module in beam**

window width = +/-7




translated to r=75cm layer




FV/17 Nov 2014

# II) The Electronics of the CMS Outer Tracker Upgrade

a) System

b) FE Electronics for 2S modules

c) FE Electronics for PS modules

d) FE Services

e) Back-End

f) System Demonstrator

g) a side look at Pixels

Slide material from: J. Christiansen

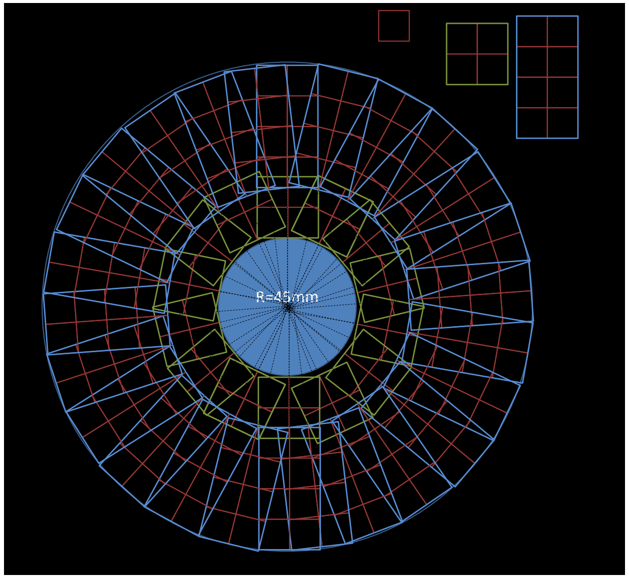
# The Phase II Pixel Electronics

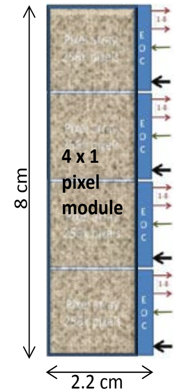
- How does it differ from the outer tracker one?
  - Pixel chip
  - Pixel module
  - Power distribution
  - Readout links

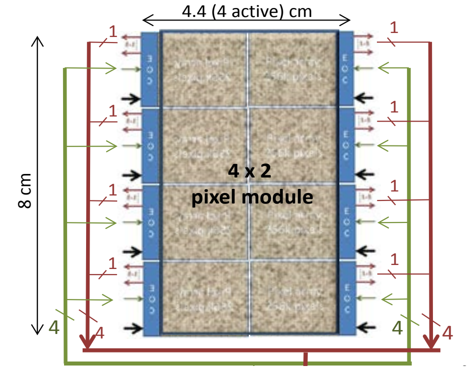
# Pixel Chip

- RD53 Collaboration with ATLAS
- 65nm TSMC
- Common IP blocks being designed and prototyped
- Radiation hardness qualification to 1GRad

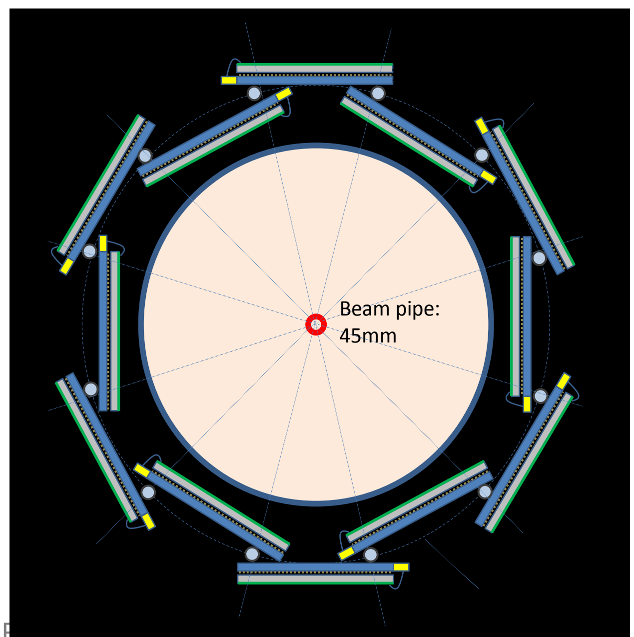
# Pixel Module

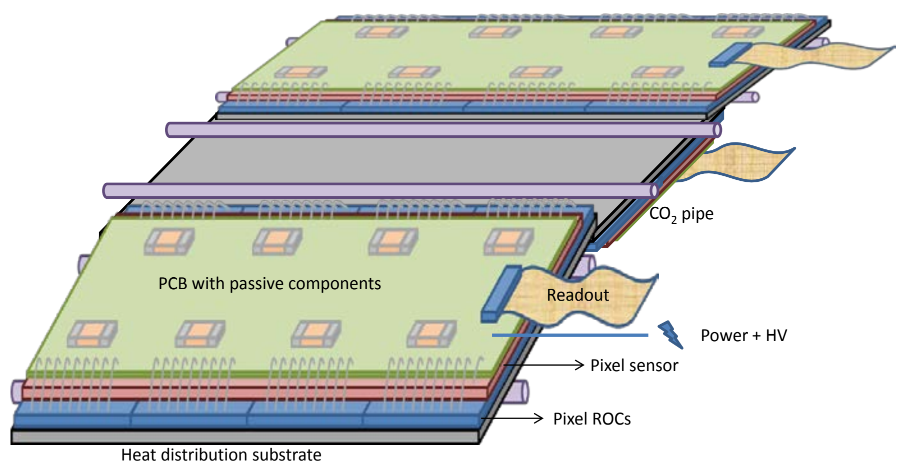



50x50 to 100x100 μm$^2$ pixels

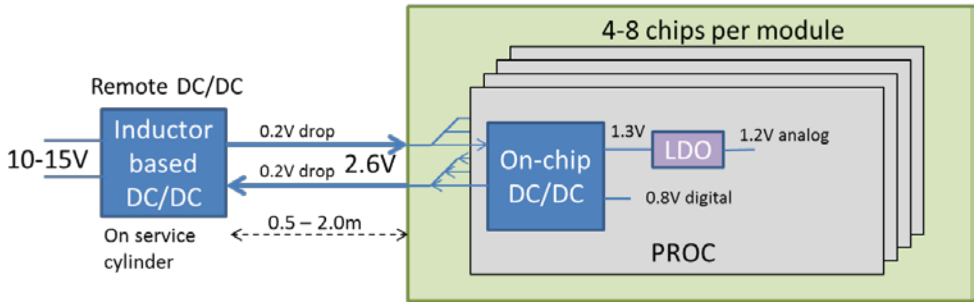


# Pixel Power Distribution

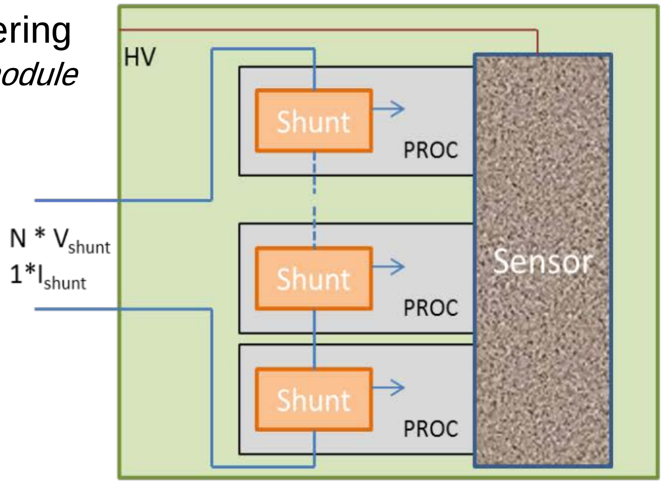
- Up to 3W per Pixel Read Out Chip (PROC)
- Power and material to be optimized
- Two alternatives under study:

- DC/DC powering

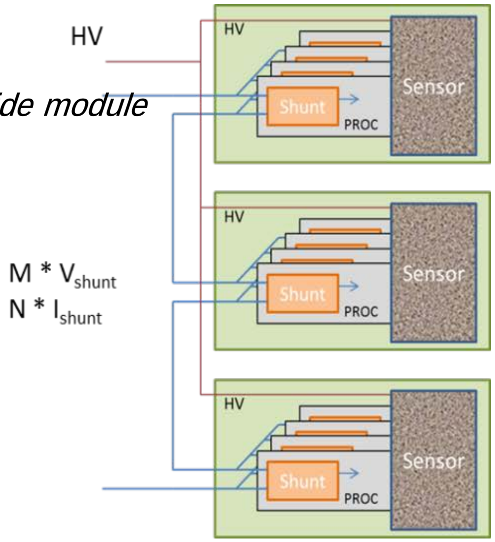



- Serial powering

*Within module*

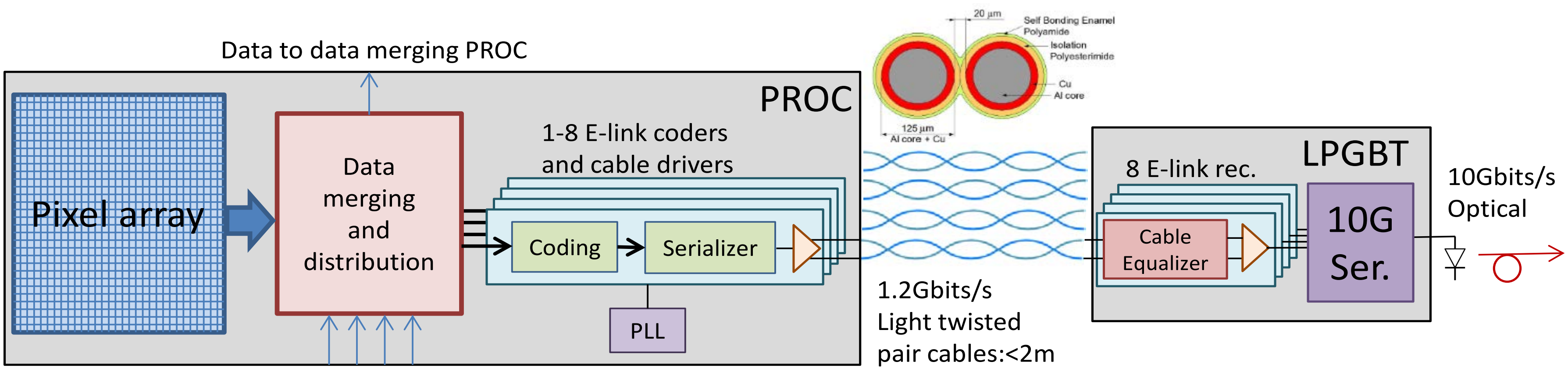



*Outside module*



# Pixel Links

- Optoelectronics will not survive Pix environment
- Fast low mass electrical links to be developed
  - More copper, more power



# III) The Electronics of the CMS Outer Tracker Upgrade
# Conclusions

PH-ESE Seminar

Francois Vasey

# Conclusions (I)

- Electronics design driven by
  - Foreseen HL-LHC operating conditions
  - Module specified as autonomous unit with own services
  - 0.5 – 1.0 MHz L1 trigger rate, 12.5us L1 latency
  - Tracker to Trigger data feed (stubs) at BX rate
- Stub finding at FE has deep impact on chips, boards and overall system design
  - 80% of data is TRIG data
- Phase II electronic system well advanced
  - $4^{+}$ years of R&D
  - 2S chain prototypes characterized and available
- Both 130nm and 65nm CMOS technologies used
  - Optimal performance balanced with development/production costs and history
- Flexible, high density interconnects are an enabling technology, commercial manufacturing and assembly processes are targeted from the start
- Services rely heavily on CERN driven Phase I common projects

# Conclusions (II)

- Developments for 2S and PS module electronics proceed in parallel. 2S system is the precursor, with a full chain already demonstrated
- FE developments are well under way, anticipating long qualification time. BE developments to be frozen as late as possible, but feasibility to be demonstrated.
- Requirements are still evolving, driven by physics, cost optimization, new data from simulation or characterization, new ideas, slipping schedule, etc.
  - However, large past R&D investment and optimization must be protected
  - Long design cycles and qualification times must be respected
  - Tracker performance must not be degraded
- System-level feasibility to be demonstrated by TDR timescale (end-2016)
- Challenges ahead:
  - Back-End
    - Demonstrate track finding processor at L1
  - Front-End
    - Assemble MaPSA module
    - Demonstrate CIC
    - Reduce the power dissipation and supply the 6-8W needed by the PS module
    - Route and manage traffic to/from concentrator

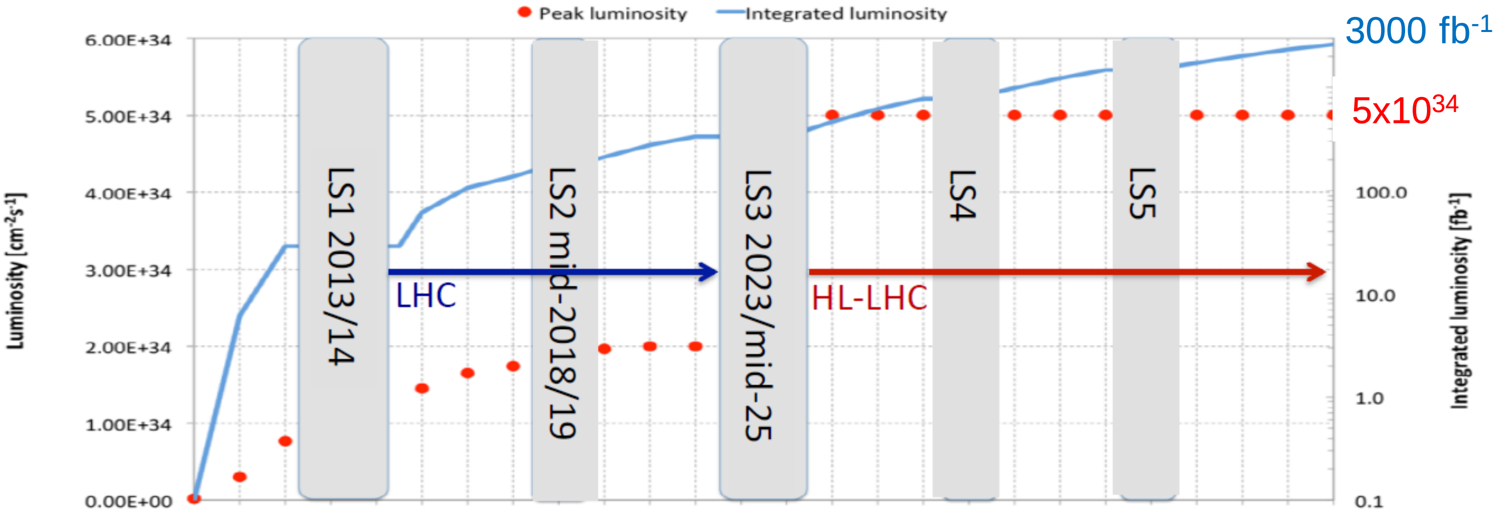
# Conclusions (III)

- 10 years to go to HL-LHC
- Many interesting development projects still welcome newcomers
- Prototype chains available for users to experiment with and give feedback
- Electronics evolves rapidly outside HEP community
  - Disruptive technologies may still … disrupt us
  - Do not keep or study this presentation for too long !

# Backups

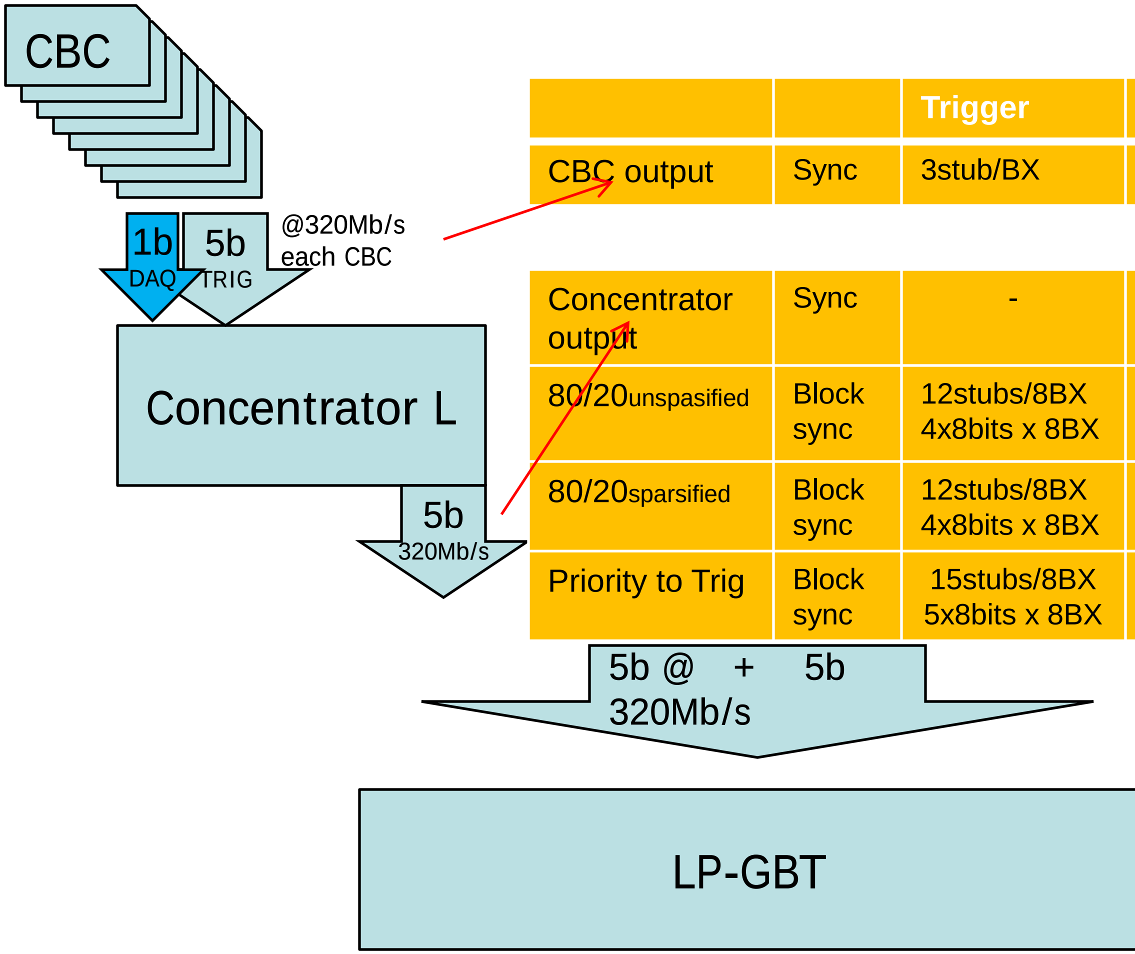
# CMS Upgrade Program

Phase 1: Complete LHC physics program at luminosity up to ≥ 2 x $10^{34}$ $cm^{-2}s^{-1}$
Prepare for 50 PU, through LS3, with margin up to 70 PU
Detectors can sustain up to 500 $fb^{-1}$



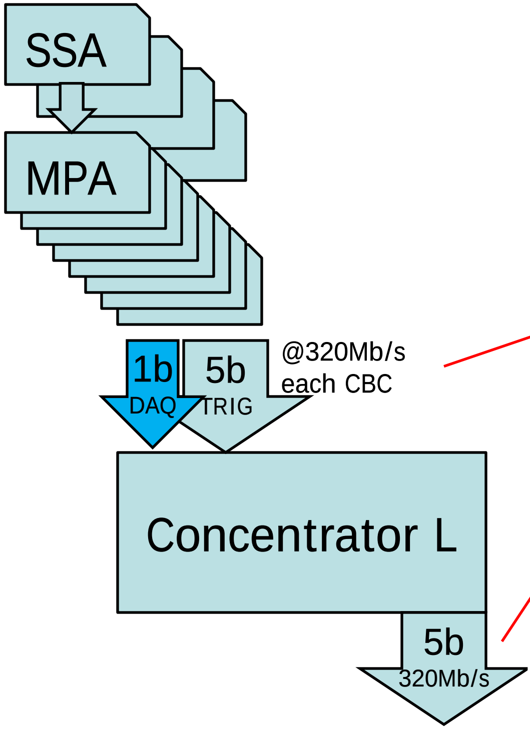

Phase 2: HL-LHC program for 3000$fb^{-1}$ integrated luminosity
Solve detector aging, high occupancy and radiation hardness issues, target performance at 5 x $10^{34}$ $cm^{-2}s^{-1}$ (with leveling) for ~125-140 pile-up with operation margin up to ~200 for higher luminosity if performance allows

# 2S Electronic System Capacity

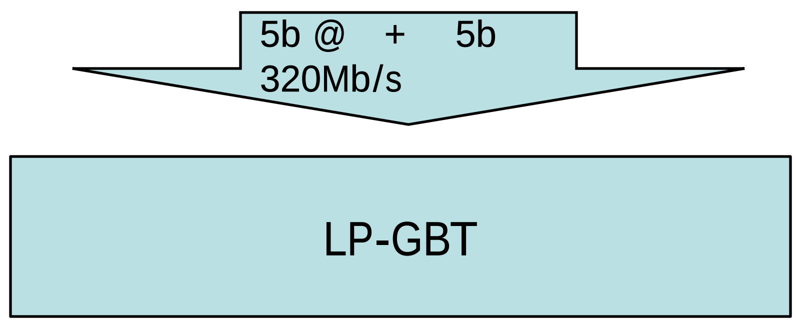



| | | Trigger | L1 Readout | |
|---|---|---|---|---|
| CBC output | Sync | 3stub/BX | Unsparsified, 276b/frame | |
| Concentrator output | Sync | - | Unsparsified 5x8 bits @40MHz | 2208b/frame 725kHz avg L1 |
| 80/20unspasified | Block sync | 12stubs/8BX 4x8bits x 8BX | Unsparsified 1x8 bits @40MHz | 2208b/frame 145kHz avg L1 |
| 80/20sparsified | Block sync | 12stubs/8BX 4x8bits x 8BX | Sparsified 1x8 bits @40MHz | 20clust @1MHz 42clust @500kHz |
| Priority to Trig | Block sync | 15stubs/8BX 5x8bits x 8BX | 5x8 bits @40MHz | During gaps |

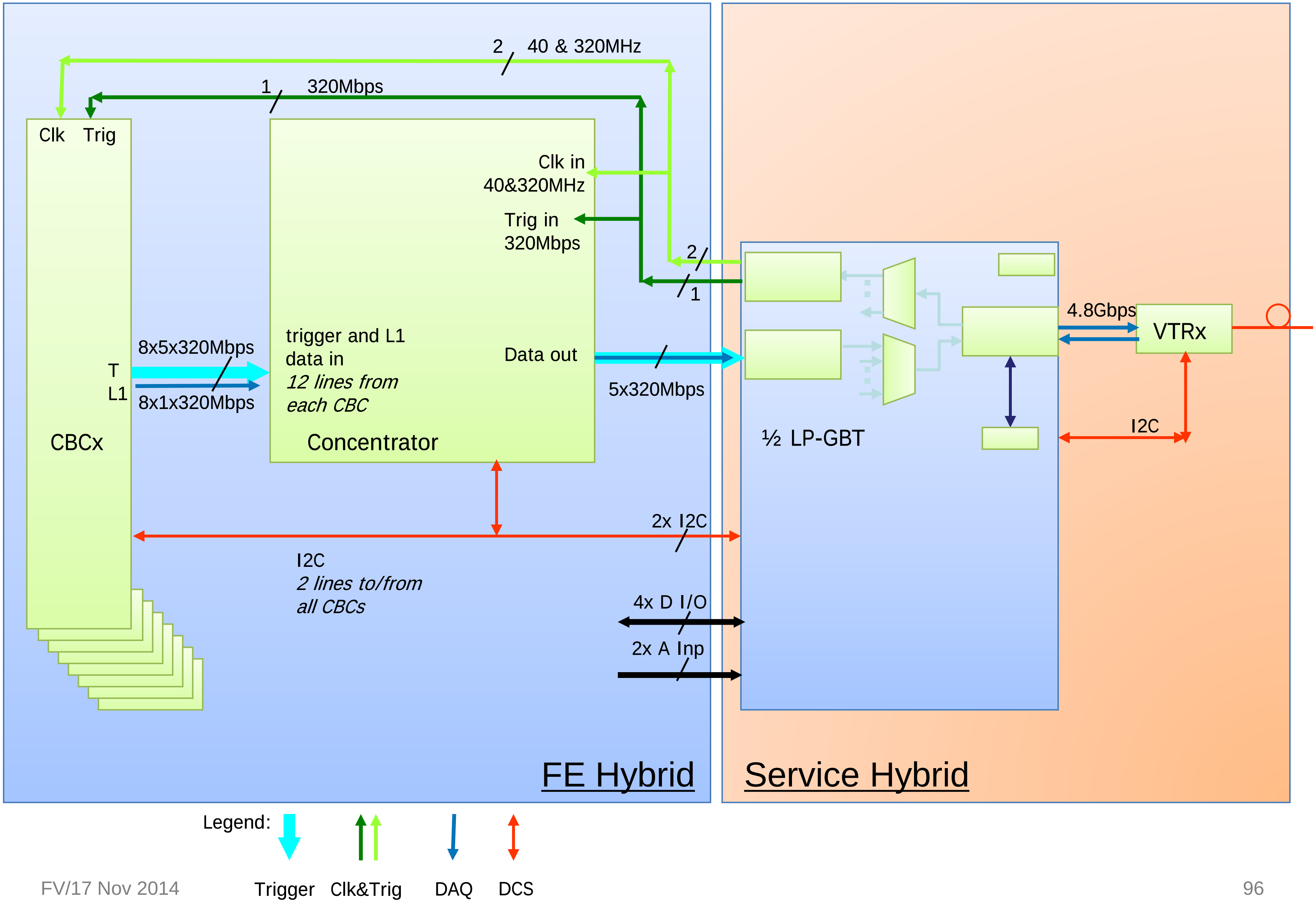
# PS Electronic System Capacity




| | | Trigger | L1 Readout | L1 Rate |
|---|---|---|---|---|
| MPA output | Block sync | 4stub/2BX | Sparsified | Up to 1MHz |
| Concentrator output | | | | |
| 80/20sparsified | Block sync | 10stubs/8BX<br>4x8bits x 8BX | Sparsified<br>1x8 bits @40MHz | 18clust @1MHz<br>39clust @500kHz |
| Priority toTrig | Block sync | 12stubs/8BX<br>5x8bits x 8BX | 5x8 bits @40MHz | During gaps |



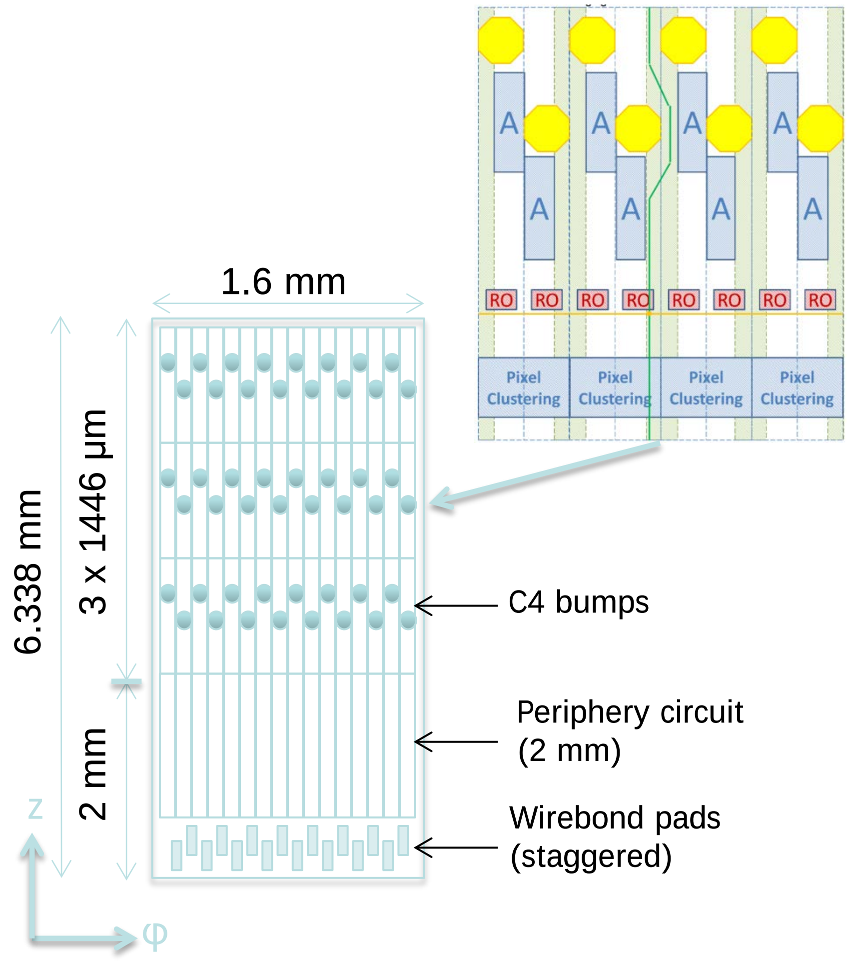
# Simplified Front-End Block Diagram



# The MPA-Light Demonstrator

- A reduced size MPA design
  - 16 x 3 pixels (instead of 120 x 16)
  - Size of single pixel (as final): 100 x 1446 um
  - Bump-bond pad size: 90 mm
  - Pitch 200 um horizontal, 200 um vertical
  - Wirebond pads for hybrid connections
  - Pixel floorplanning similar to the final MPA
  - Scalable to the final design

- Purpose
  - Prototype & qualify the analog FE circuitry
  - Facilitate the development of the sensor
  - Understand and solve the numerous technical aspects of the Module Assembly



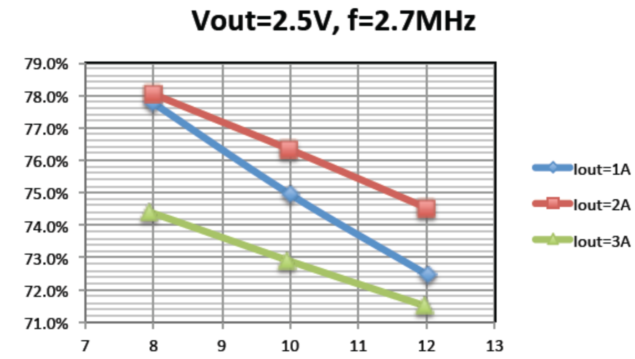
# FEASTMP size reduction

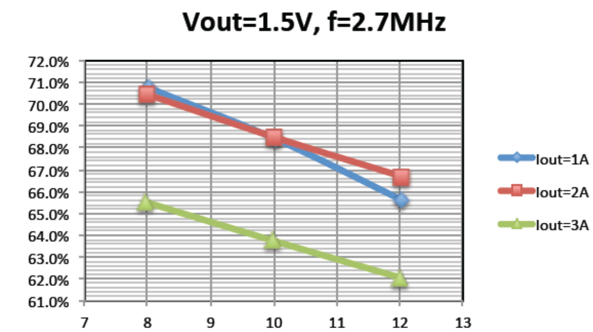
**All configurations require one or several FEASTMP, not designed for trackers**

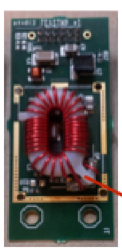
- Need to reduce the board area
- Need to reduce the material budget.
- Need to match the 2.3A max output current (today it delivers more than 4A).

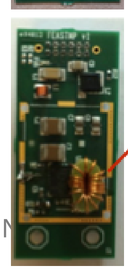
**Introducing the ECCA wire, 200 nH instead of 400 nH.**

- Coil much smaller.
- Material budget contributed by coil divided by one order of magnitude.
- Good efficiency up to 2A.





| Inductor | Wire length (mm) | Wire diameter (mm) | Wire volume (mm³) | Wire Cu volume (mm³) | Wire Al volume (mm³) |
|---|---|---|---|---|---|
| 400 nH Coilcraft, bulk copper | 360 | 0.5 | 70.65 | 70.65 | 0 |
| 197 nH prototype, ECCA wire | 160 | 0.38 | 18.1 | 5 | 13.1 |

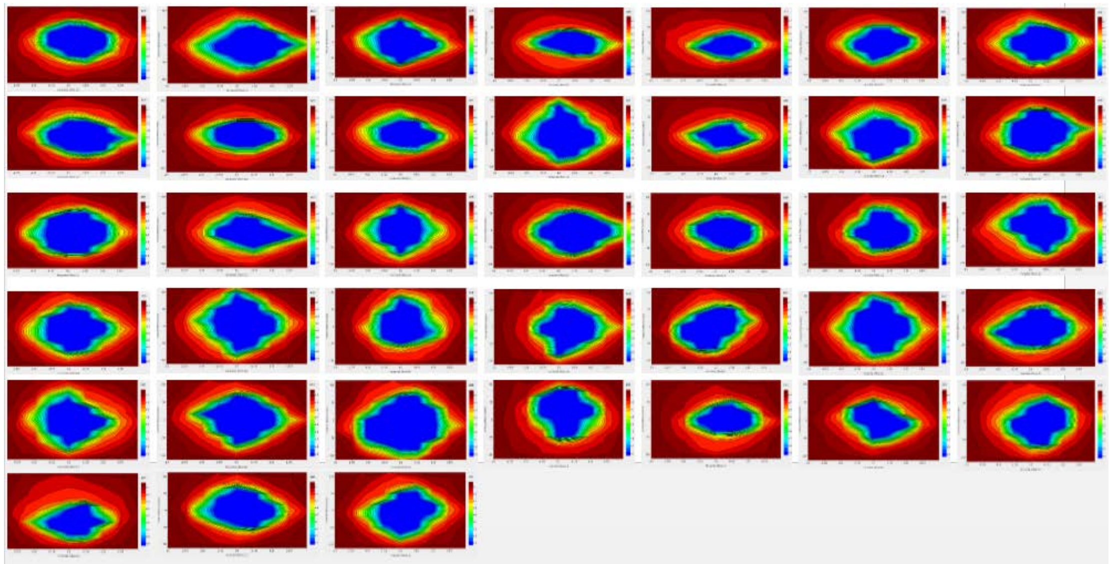
Cu volume = 70.65 $mm^3$

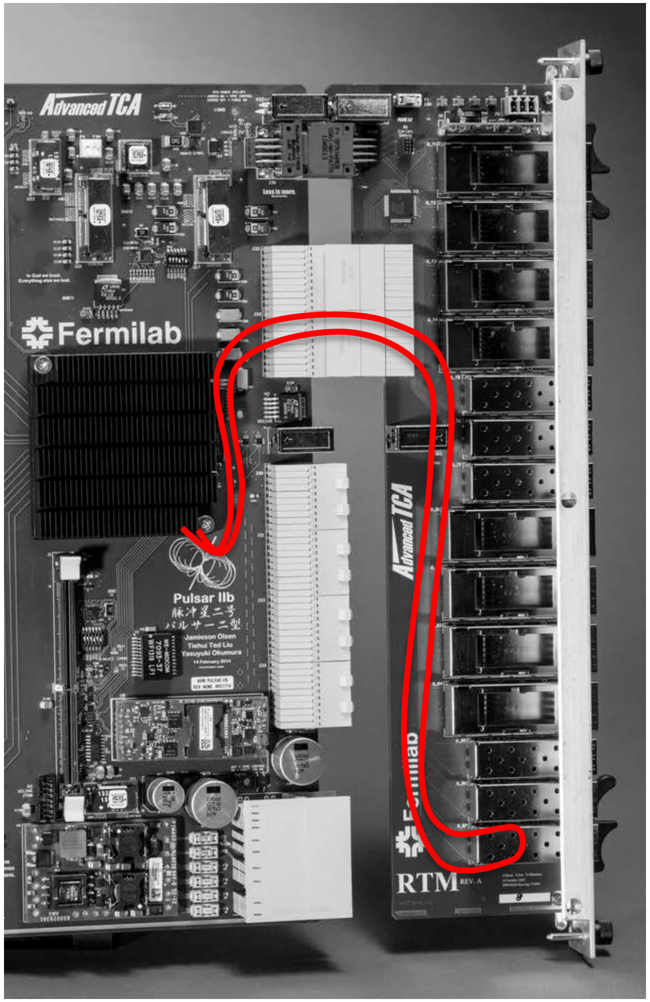
equivalent Cu volume = 7.1 $mm^3$

**ECCA based FEASTMP is now our reference for the 3 schemes.**

# Pulsar IIb RTM testing

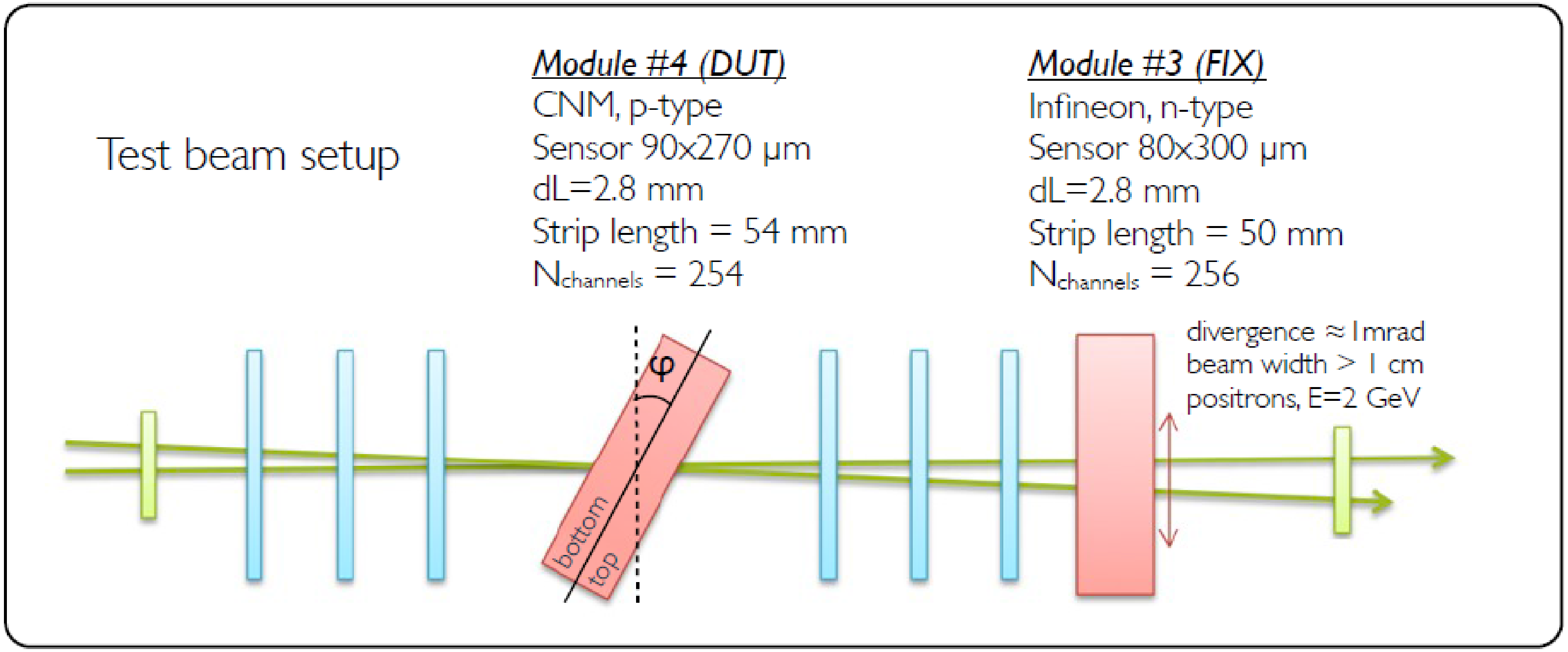
- Tested with (older) RTM version 1.1
- 38 Channels @ 10 Gbps
- SFP+, QSFP+ 0dB passive loopback modules and active optical cables
- Improved RTM 2.0 expected Fall 2014





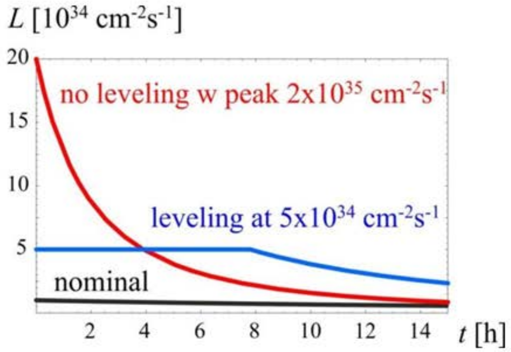
# Test Beam Setup

DESY, Nov-Dec 2013

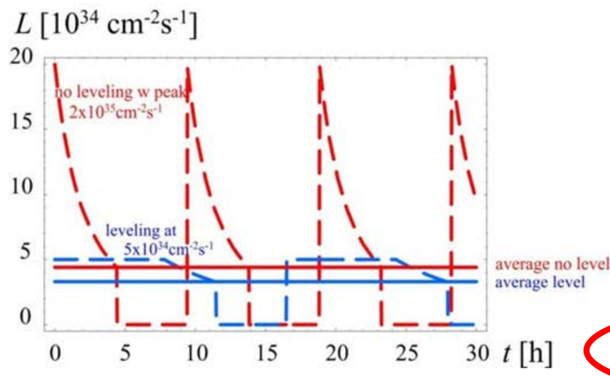


# HL-LHC Machine Parameters

## Luminosity Levelling, a key to success




- High peak luminosity
- Minimize pile-up in experiments and provide "constant" luminosity




- Obtain about 3 - 4 fb$^{-1}$/day (40% stable beams)
- About 250 to 300 fb$^{-1}$/year

| | 25 ns | 50 ns |
|---|---|---|
| # Bunches | 2808 | 1404 |
| p/bunch [$10^{11}$] | **2.0 (1.01 A)** | **3.3 (0.83 A)** |
| $\varepsilon_L$ [eV.s] | 2.5 | 2.5 |
| $\sigma_z$ [cm] | 7.5 | 7.5 |
| $\sigma_{\delta p/p}$ [$10^{-3}$] | 0.1 | 0.1 |
| $\gamma\varepsilon_{x,y}$ [μm] | **2.5** | **3.0** |
| β* [cm] (baseline) | 15 | 15 |
| X-angle [μrad] | **590 (12.5 σ)** | **590 (11.4 σ)** |
| Loss factor | 0.30 | 0.33 |
| Peak lumi [$10^{34}$] | 6.0 | 7.4 |
| Virtual lumi [$10^{34}$] | 20.0 | 22.7 |
| $T_{leveling}$ [h] @ 5E34 | **7.8** | **6.8** |
| #Pile up @5E34 | 123 | 247 |

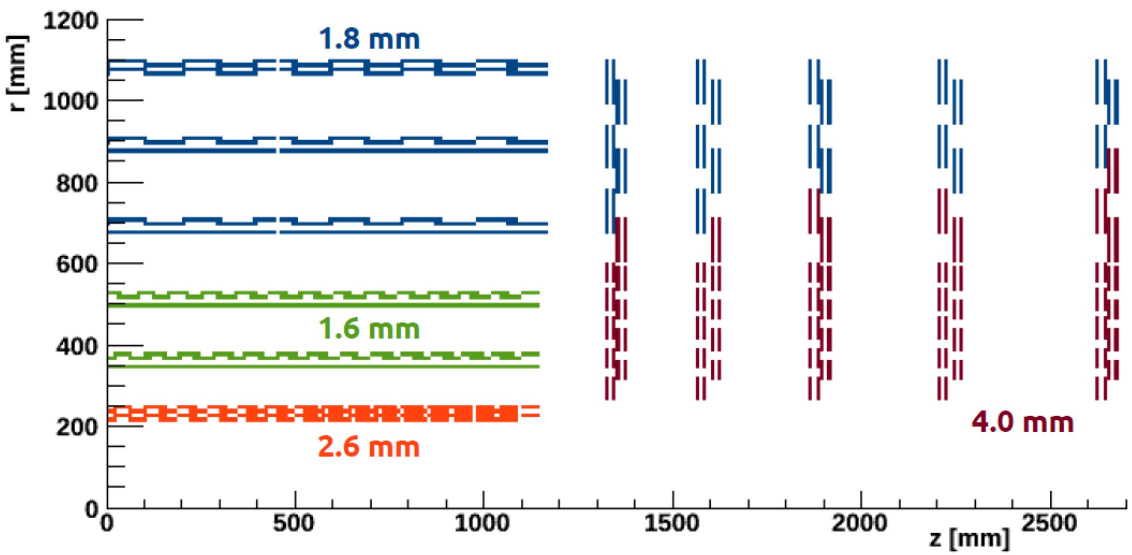


Courtesy Oliver Brüning

# sensor spacing

must be tuned along with search windows

Mersi – ACES 2014
CMS Tracker Upgrade
layout and requirements



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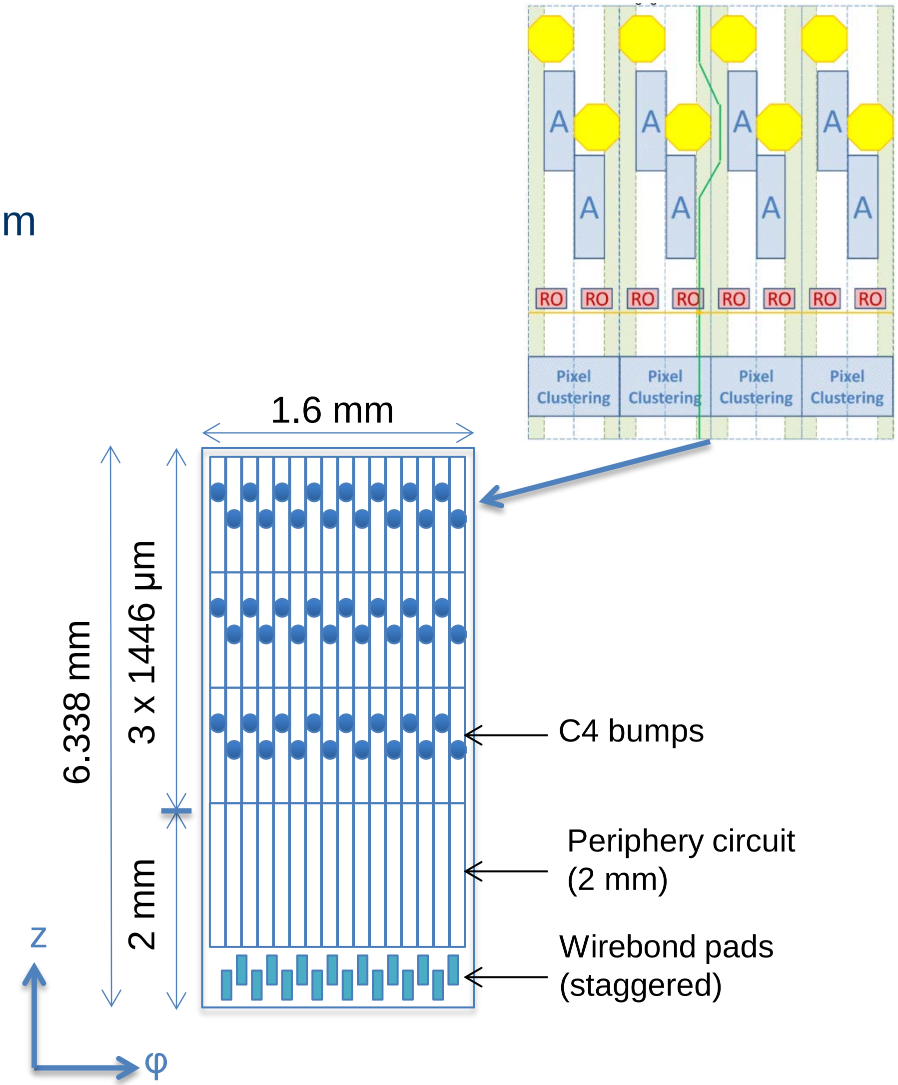
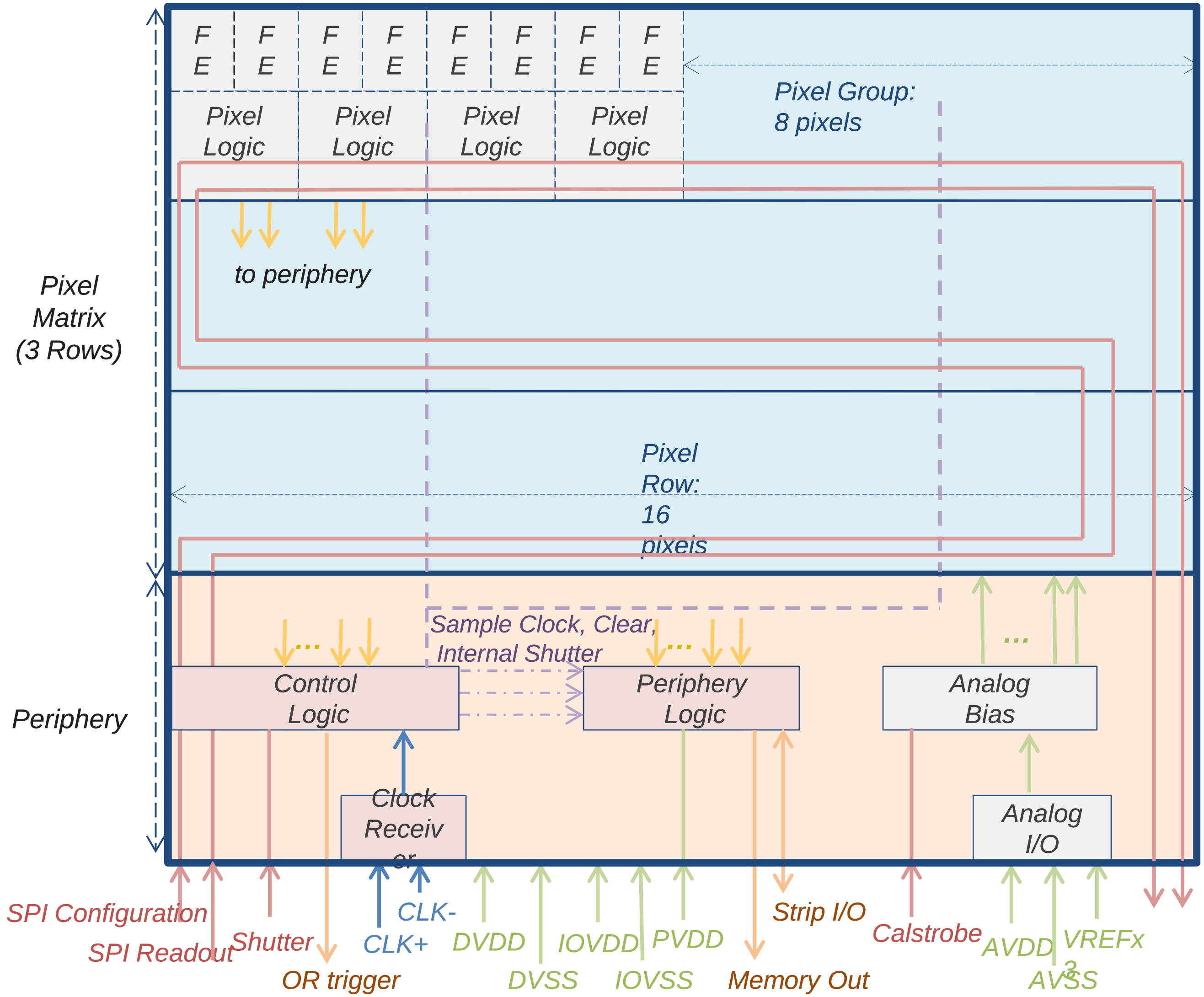
  - Scalable to the final design

- Purpose
  - Prototype & qualify the analog FE circuitry
  - Facilitate the development of the sensor
  - Understand and solve the numerous technical aspects of the Module Assembly



# MPA-light Block Diagram

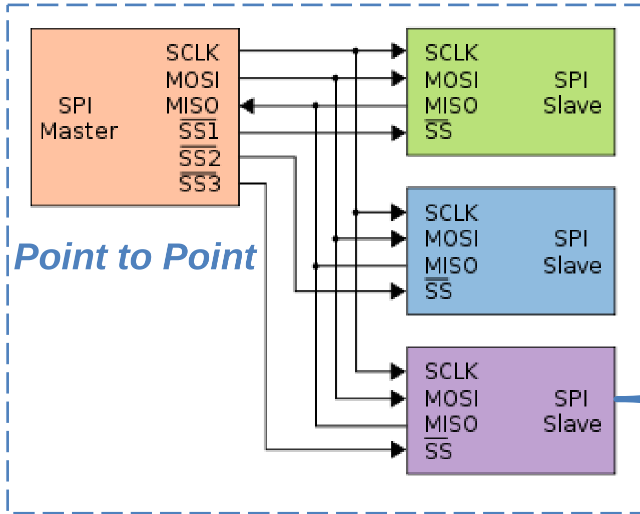


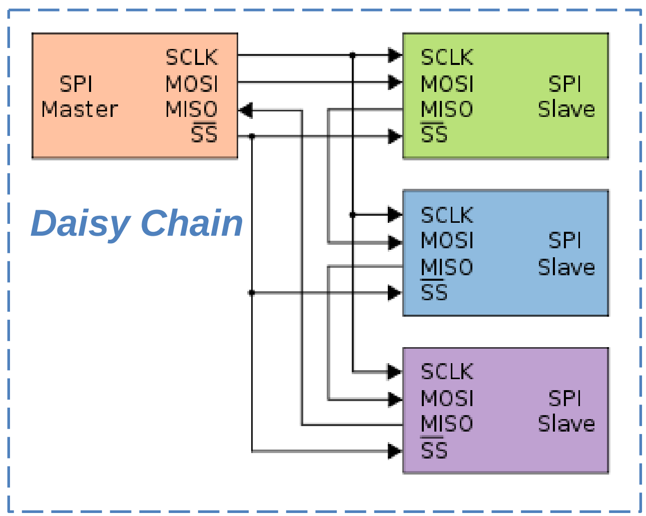
# Serial readout and configuration

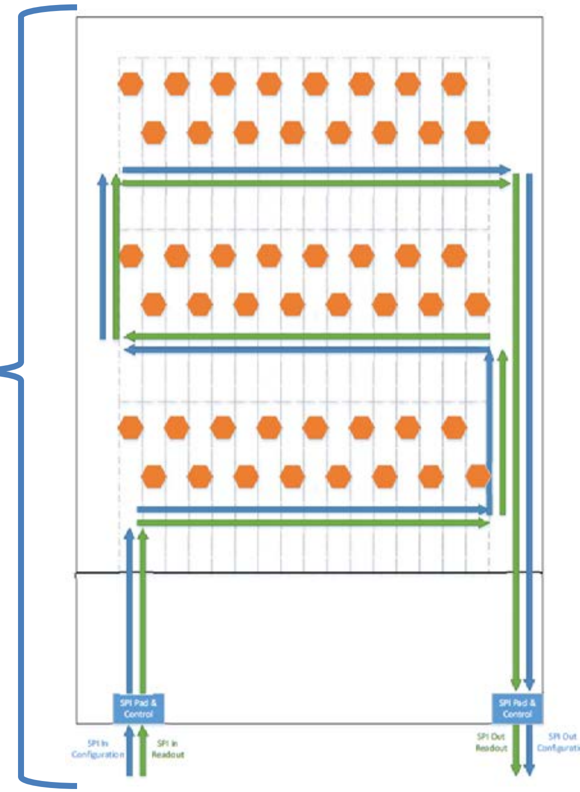
- Each MPA-Light is an SPI slave.
- SPI Master will be on FPGA
- 2xSPI buses for Configuration and Readout.

- Possible Configuration are:
  - Point to point
  - Daisy Chain

- SPI pads for each MPA-light (8):
  - RO clk In
  - RO data In
  - RO enable (Shutter)
  - RO data Out
  - Configuration clk In
  - Configuration data In
  - Configuration enable
  - Configuration data Out



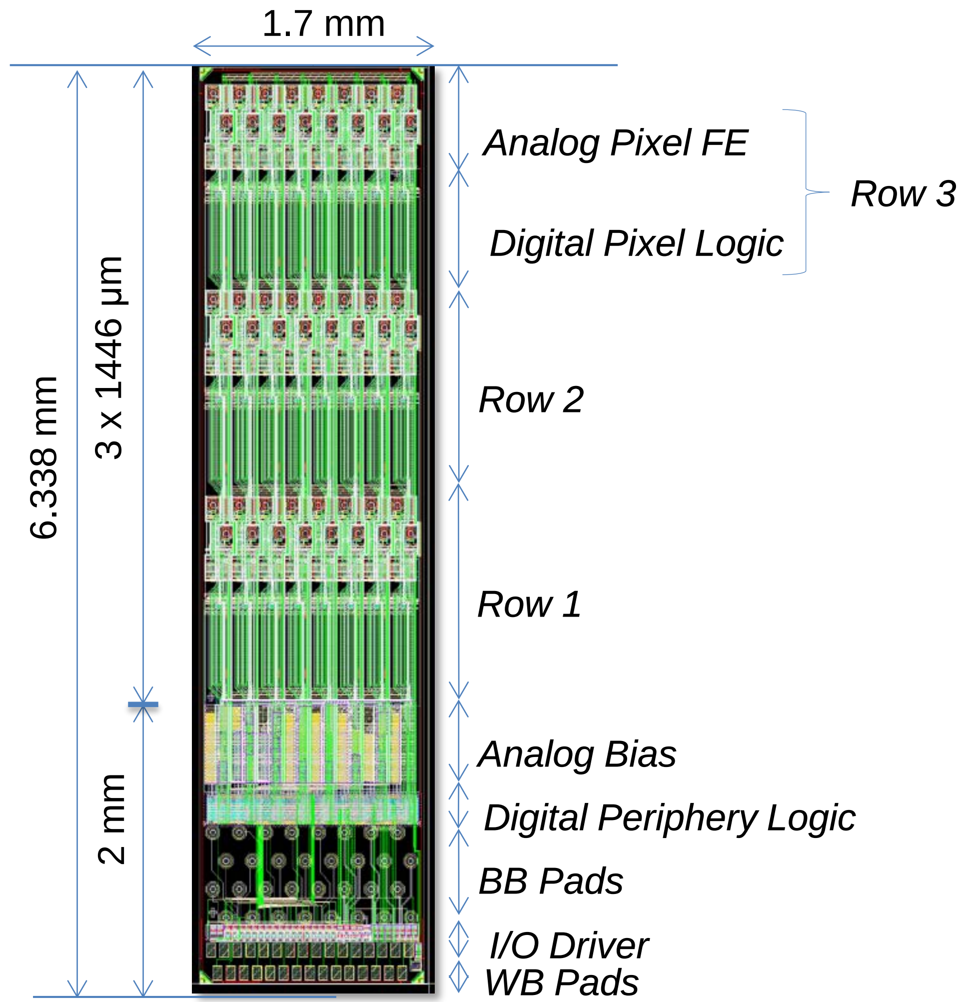



# MPA-light ASIC layout

TSMC LP 65nm
8 Metal layers process option

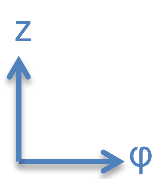
| | | | |
|---|---|---|---|
| M1 | m1 | local | cell |
| M2 | x | local | cell |
| M3 | x | local | cell and block |
| M4 | x | local | cell and block |
| M5 | x | regional | cell and group and shield |
| M6 | z | global | clk and pwr |
| M7 | u | global | clk, pwr and shield |
| M8 | RDL | global | pads and GND |

Status: Submitted for fabrication in Sept. 18, 2014

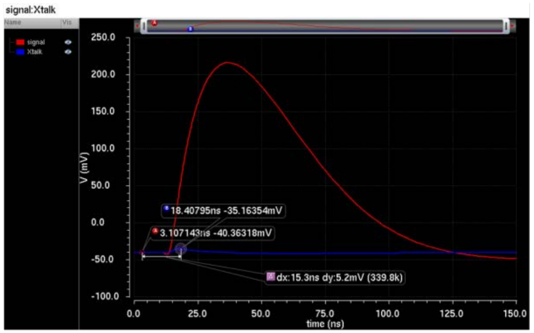




Davide Ceresa
Jan Kaplon
Rui Francisco De Olivera
Alessandro Marchioro
Kostas Kloukinas

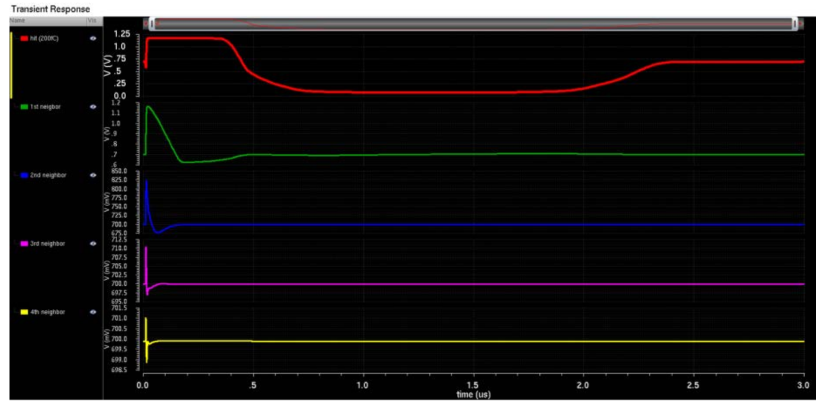



# MPA Front-End Performance (sim.)

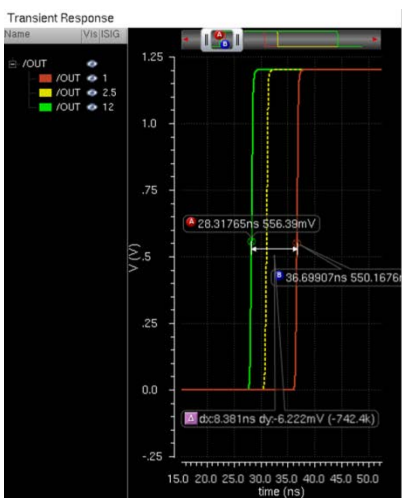



- Cross talk: 2%
- Detector model:

150fF to backplane, 60fF in between the channels

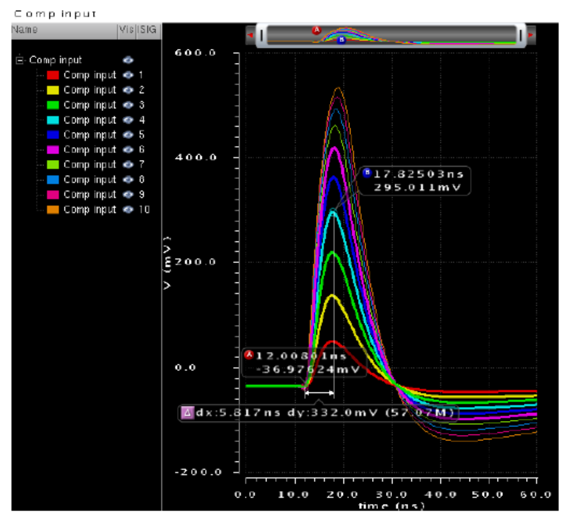



200fC signal in channel (red trace for hit channel, traces below: neighbors). Recovery in hit channel <3us, signal in 3rd neighbor negligible)




Time walk for signals 1 to 12 fC (0.5 fC threshold);

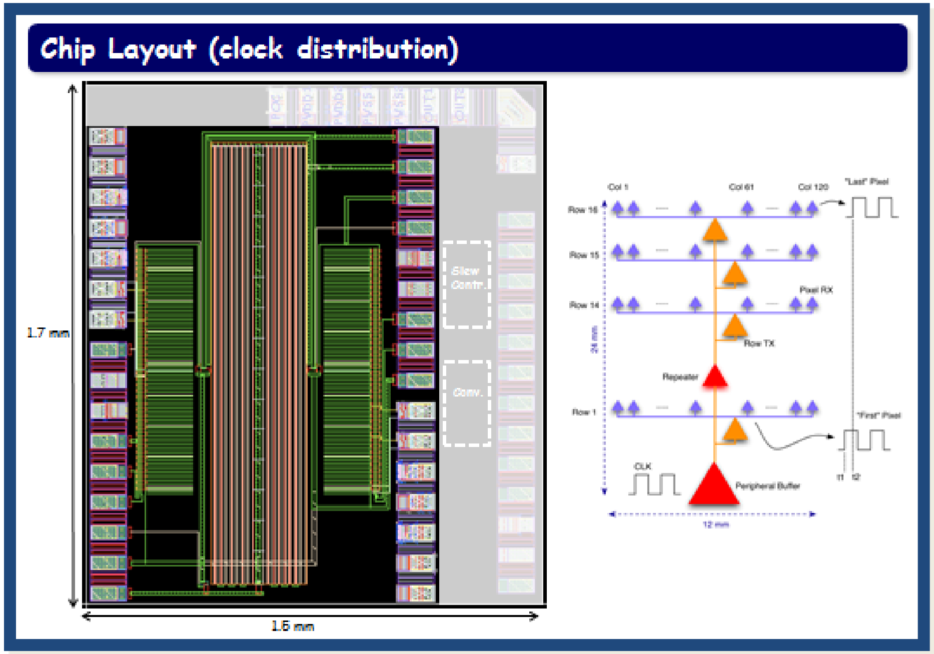
<9 ns

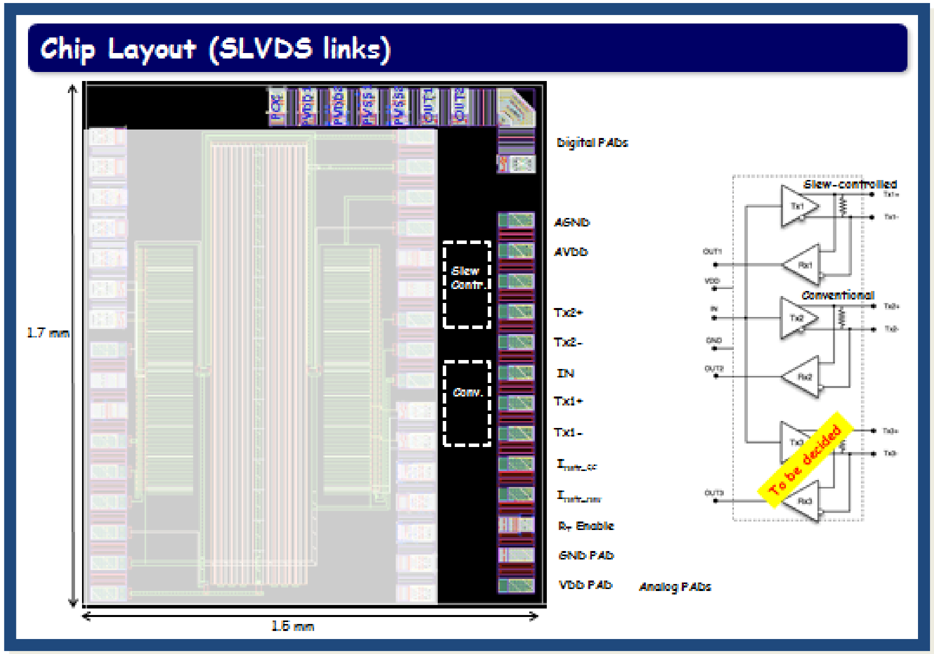



Signals ranging from 0 to 4fC, threshold set to 0.6fC;

INL<4%

# Clock tree & sLVS IO pads



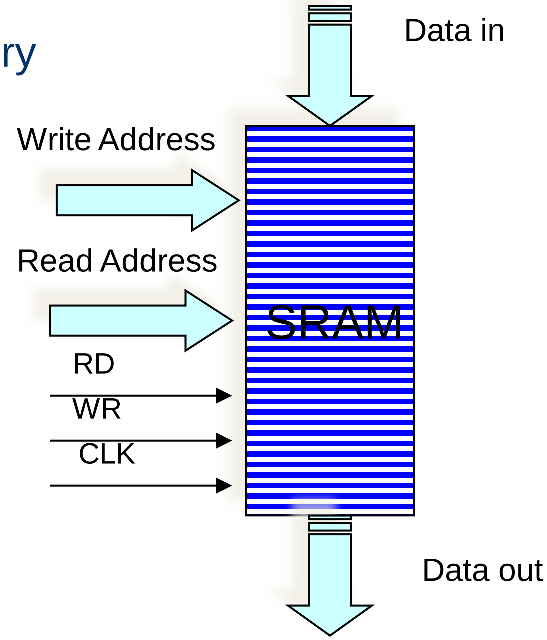



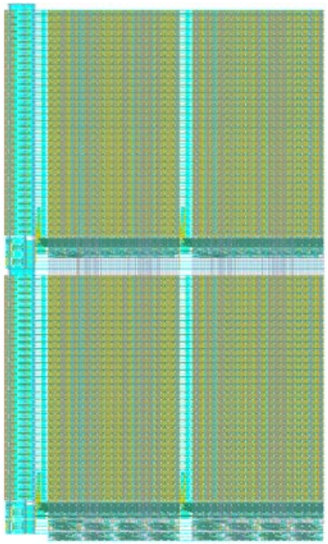

- Clock Distribution test structures
  - Low power clock distribution scheme for the MPA ASIC
- sLVS IO pad test structures
  - Differential driver & receiver pads running at 320Mbps @ 0.8V, 640Mbps @ 1.2V

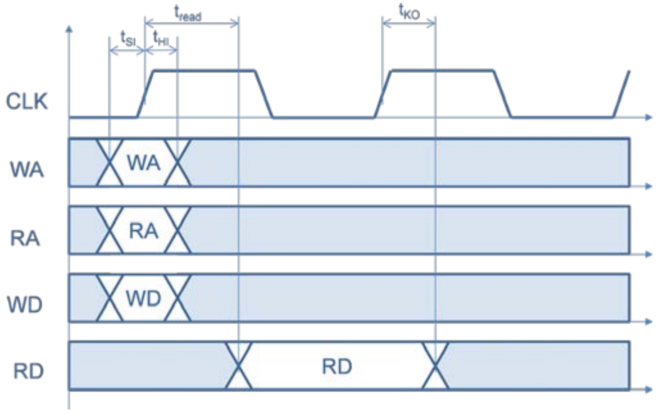
*V. Re, G. Traversi, L. Gaioni, F. De Canio – Univ. of Pavia and INFN Bergamo*

# SRAM IP block test structures

- Clock synchronous, pseudo dual-port memory
  - Write/Read operation @ same clock cycle
- Operating speed: 80 MHz @ 1.2 V
- Compatible with the TSMC 65nm CMOS
  - Only lower 4 metal levels used in the SRAM block
  - Only Standard-Vt transistors
  - Special design techniques for radiation tolerance
- Memory Compiler specifications:
  - Minimum size: 128 words of 8 bit
  - Max size: 1k words of 256 bits
- Development work is outsourced
- Design Validation:
  - Prototyped 2 memory blocks of different sizes






*S. Bonacini, A. Marchioro, K. Kloukinas*

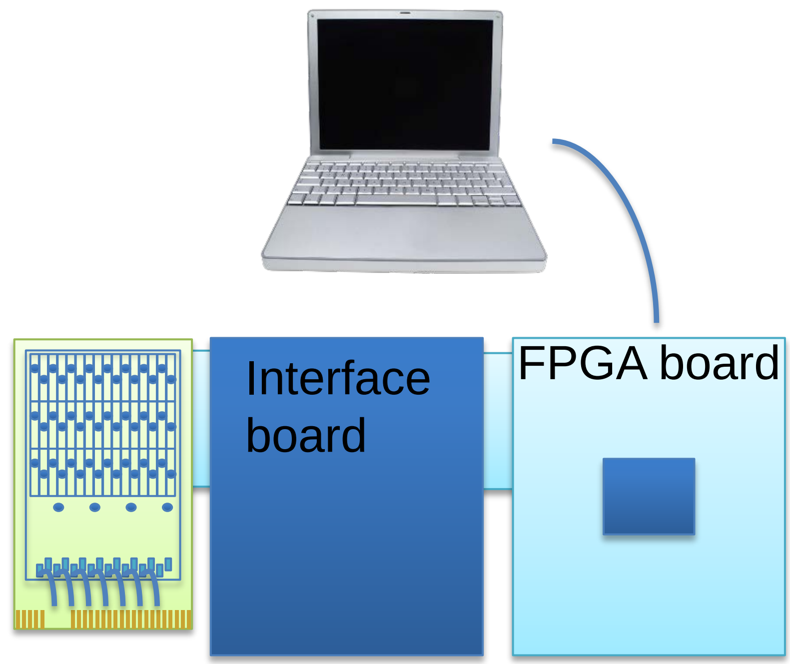
# Prototyping & Plans for Testing

- All structures are submitted on a common MPW run on a 65nm TSMC Cybershuttle in Sept 18, 2014. Estimated TAT: 1.5 months

- **MPA-Light**
  - MPA-light test bench @ CERN
- **SRAM IP**
  - Test bench @ CERN by S. Bonacini & I. Kremastiotis
- **Clock Tree test structures**
  - Test bench by INFN Bergamo
- **sLVS IO test structures**
  - Test bench by INFN Bergamo for IO pad characterization
    - Test PCB is in design phase
  - Test bench at CERN for validating data transmission over flex kapton media with different topologies (G. Blanchot, M. Covacs)

# MPA-Light Test Bench 1/2

- Test the MPA-light prototype ASIC
  - Functionality tests of digital logic
  - Performance tests of the analog front-end circuitry
- Exchangeable load board to host the ASIC
  - Wirebond Die on PCB
- Interface board with voltage level translators
- MPA-light communication handled on FPGA
- Based on the CLICKpix test system of Szimon Kulis




*A. Caratelli*

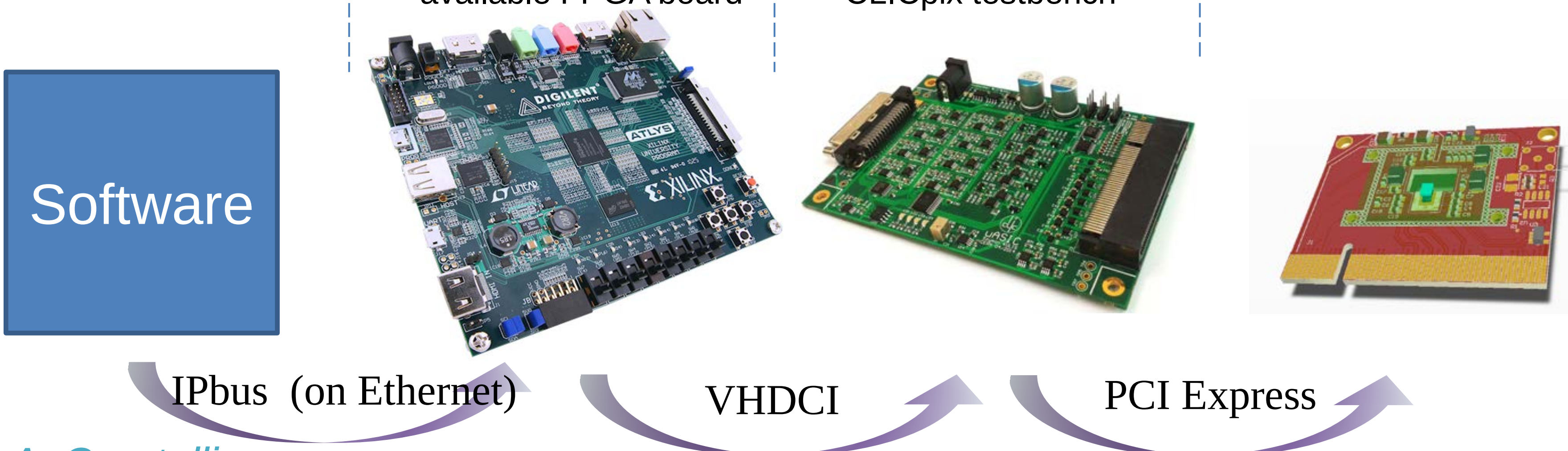
# MPA-Light Test Bench 2/2

## Software layer
- Specific test routines
- Set of routines for accessing the MPA light ASIC (configure, read-out, etc)
- Use IPbus HAL

## FPGA firmware
- Handle the configuration
- Handle the read-out from the MPA light
- Control the interface board
- Commercially available FPGA board

## Interface board
- Voltage level translators
- Adjustable voltage regulators
- ADCs/DACs
- Current monitors
- Existing card from CLICpix testbench

## Load PCB
- MPA light ASIC wirebonded
- very simple
- Easy exchangeable
- Needs to be designed




*A. Caratelli*

# Software

## Specific test routines

- Testing configuration and read-out
- Analog front-end analysis
  - S curves
  - Trimming
  - etc.
- Test the digital logic
  - including stub finding logic
- Test the logic at different supply voltages

## MPA-Light Main routines

- Configuration
  - 16 bit digital, 16 bits analog bias, 10 bits/pixel
- Acquisition
  - Open shutter, send certain number of strobe..
- Read-out
  - Pixel counter and digital logic memory
- Calibration
- Software checks

## IP bus

- Communication with the firmware
  - UDP/IP

*A. Caratelli*

# Reusable modules for other assemblies

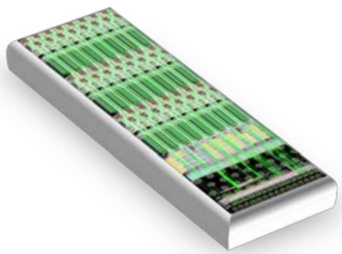
- Firmware → fully reusable
- MPA-light routines → fully reusable
- Test routines → are though for specific tests but can be reused
- Interface card → depends on the assembly (limited number of connection lines)
- Load board → probably no

*A. Caratelli*

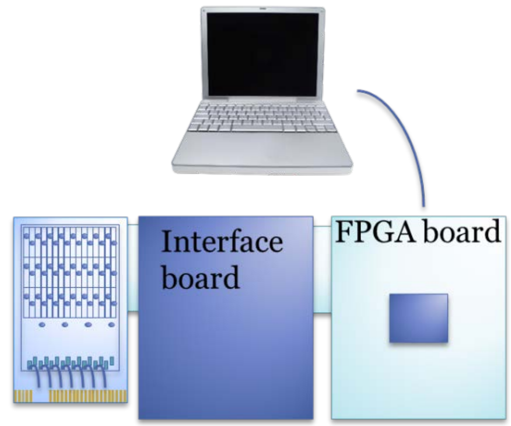
# Status and Planning

- Hardware
  - Design and production of the load PCB ➞ started
  - Other boards ➞ already available
- Software/Firmware
  - Communication with the firmware and the load board from a simple python script ➞ already tested
  - Firmware and function to control the MPA-Light ➞ started

# MPA-Light and MaPSA-Light Test plans



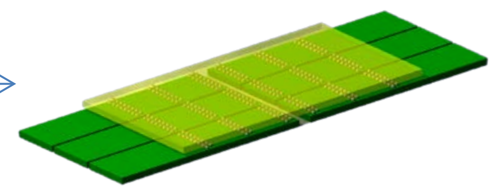
100 pieces at the end of Nov. 2014



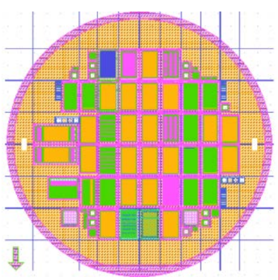

Analog FE circuitry
Digital Pixel Logic
Stub Finding Logic

Pixel sensor prototypes

MaPSA Light



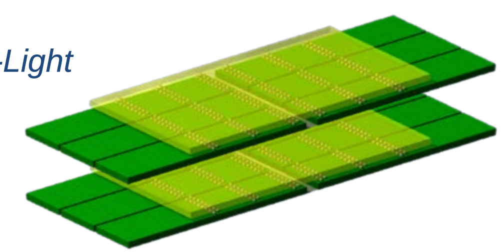
MPA-Light test with sensor
Sensor Test



Design by A. Dierlamm, M. Dragicevic,
M. Printz.

PS-like
mini module

2x MaPSA-Light



# MAPSA-light assembly Technical Description and Call for Tender

- A **technical description** document has been reviewed with purchasing office.
  - See attached document.
  - Minor updates on drawings in August (Davide, Pierre).
- **Considerations**:
  - The MPA-Light is not bumped and is delivered diced.
  - The Sensor-Light is delivered on 4 inch wafers, without bumps.
  - The contractor has to provide UBM on the Sensor-Light and on the MPA-Light, and ball-bump one of those.
    - This activity can be subcontracted but must be handled by the assembler.
- **Deliverables**:
  - 1: Assembly process description: process, critical steps, specific requirements.
  - 2: Prototype production and assembly report.
- **Call for Tender:**
  - 3 companies were contacted by end of June to deliver their quotations for the listed deliverables on the basis of the technical description.
  - The 3 quotations were received by end August. Review with P.O. took place on September 1st.
  - New companies have been contacted.

# CONCLUSIONS

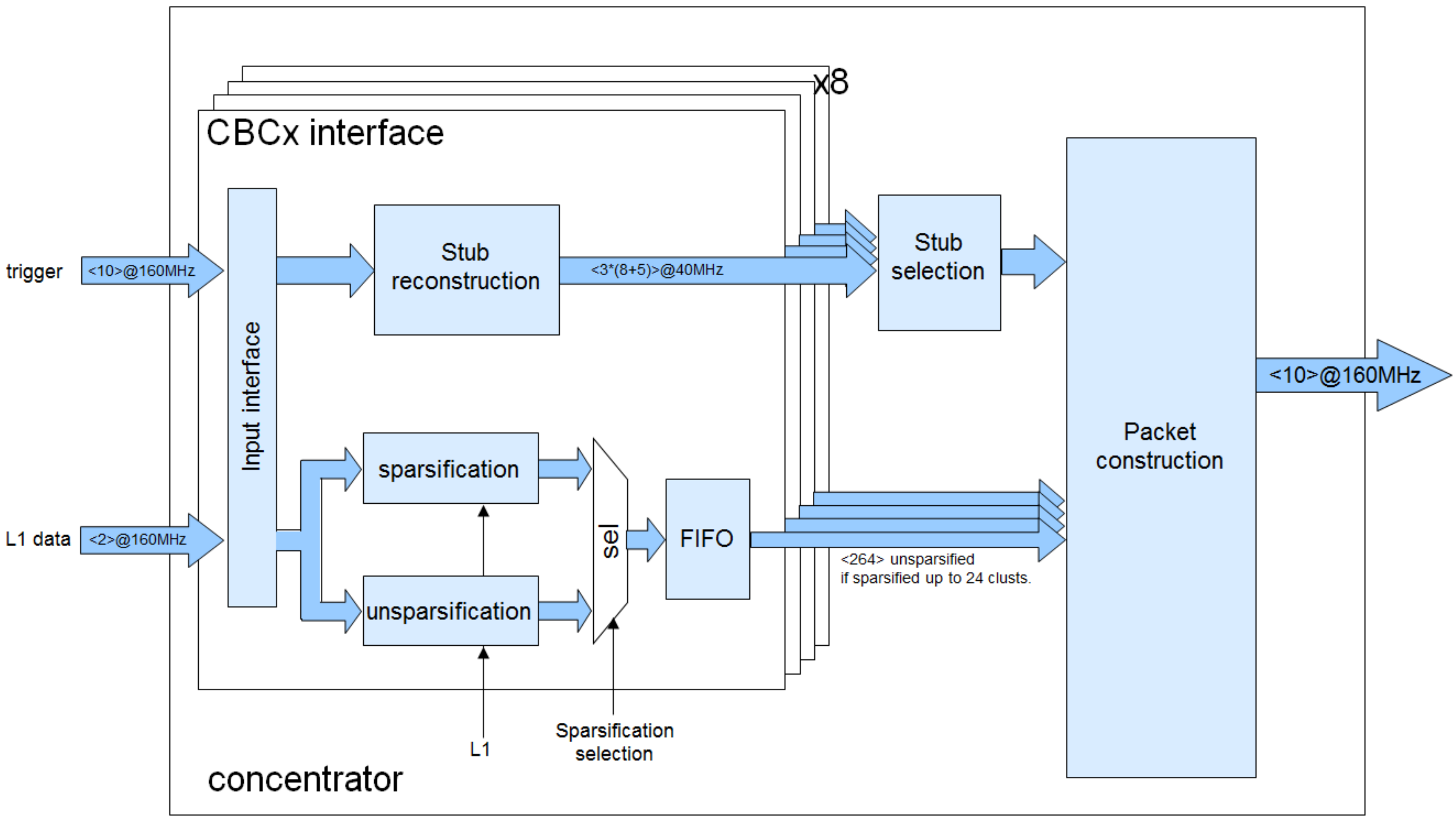
Macro Pixel ASIC gets to the prototyping phase

Designs Submitted for fabrication at the end of Sept. 2014
Estimated turn around time is 2 months

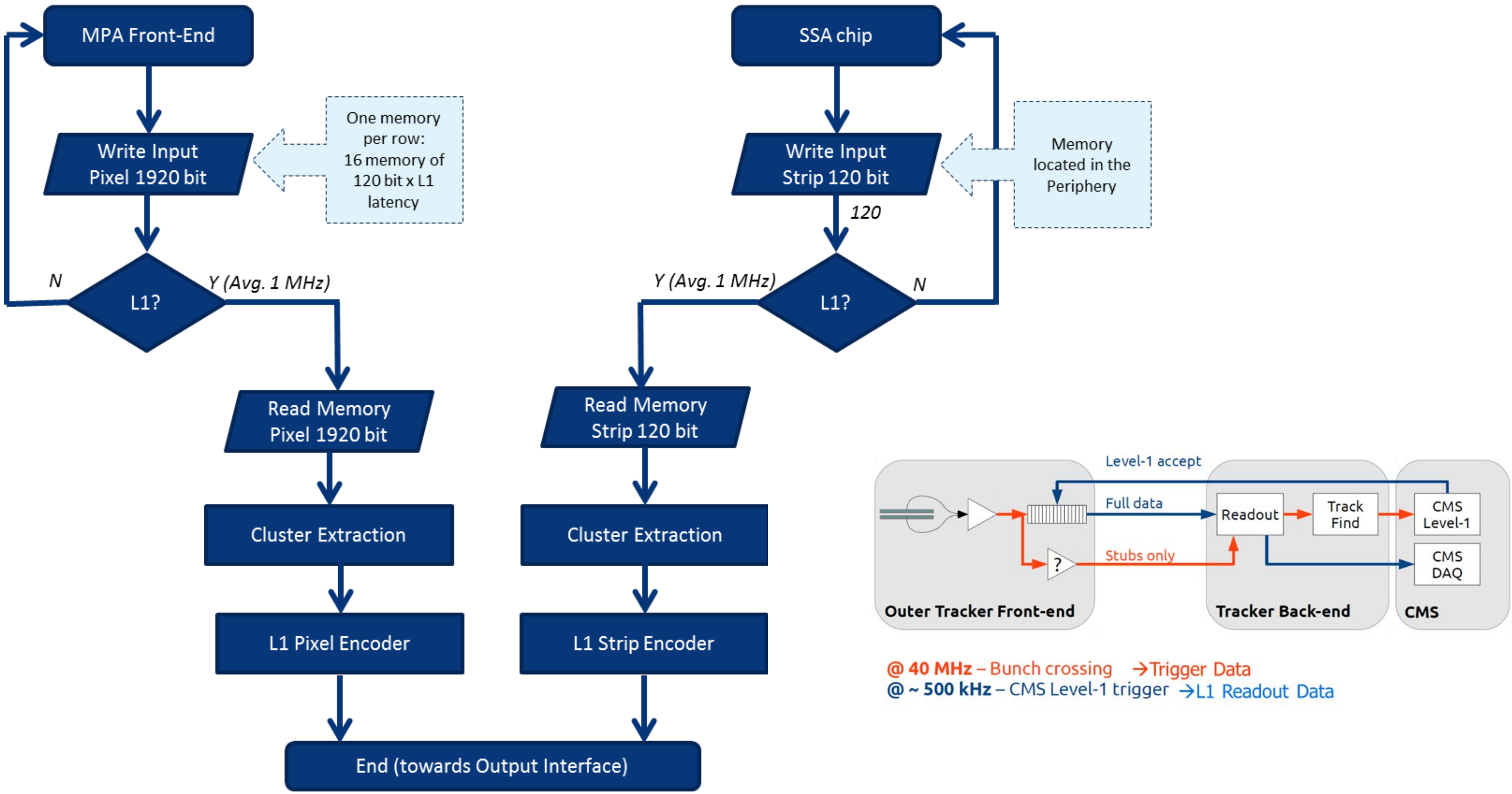
Tests will begin in December 2014

*Tests will be long, and require significant effort.*
*Results will provide important information*
*for the design of the final MPA ASIC*

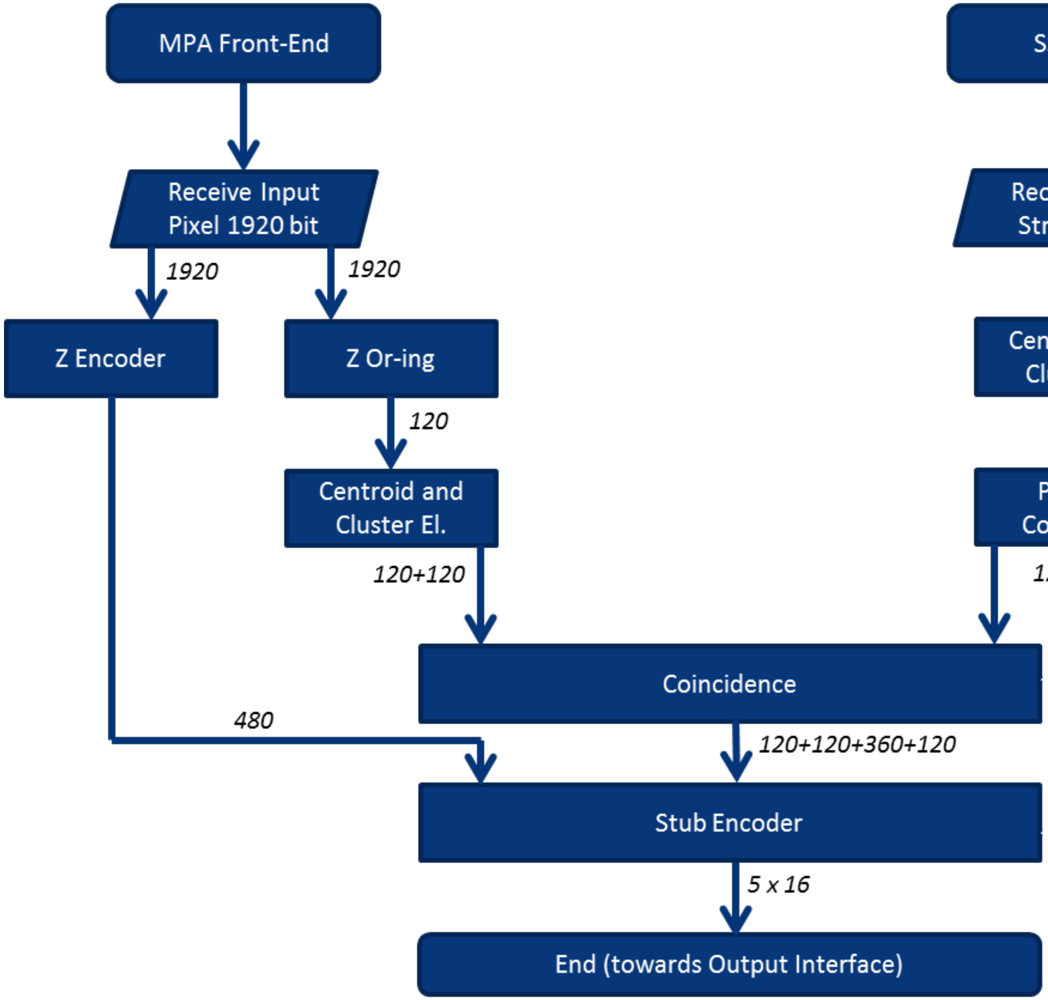
# Concentrator Data Flow

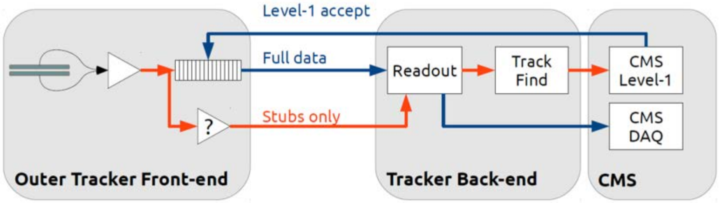


# PS L1-Readout Data Flow



# PS Trigger Data Flow

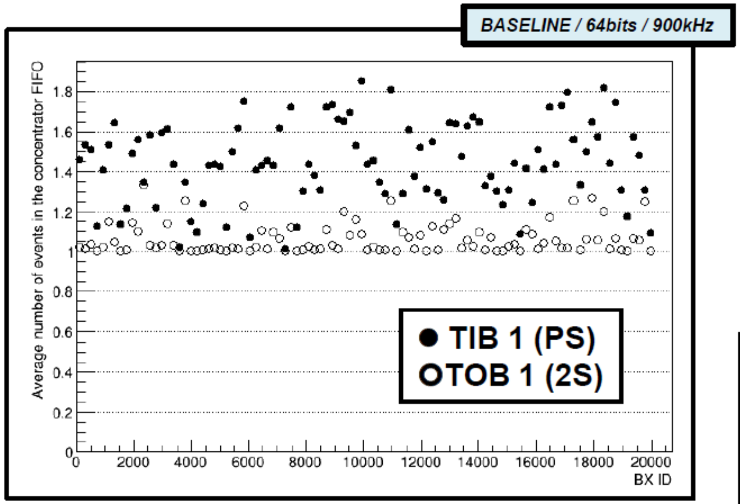



@ 40 MHz – Bunch crossing →Trigger Data
@ ~ 500 kHz – CMS Level-1 trigger →L1 Readout Data

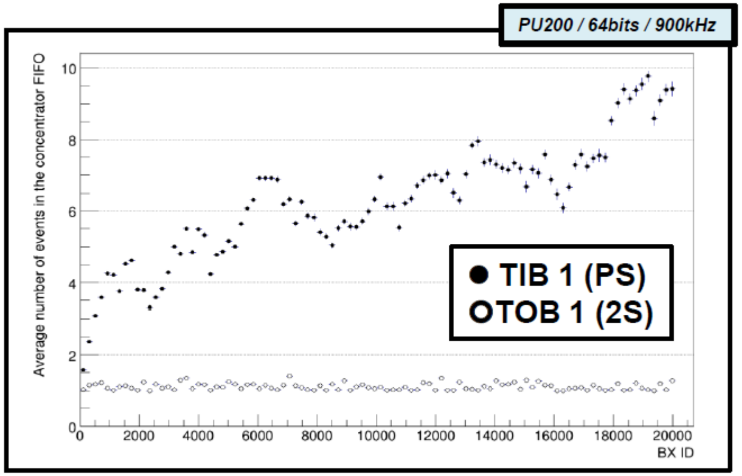
## → 2S concentrator to GBT (*L1 block*), results using PU<***>+4tops events:

→ Evolution of the FIFO vs time



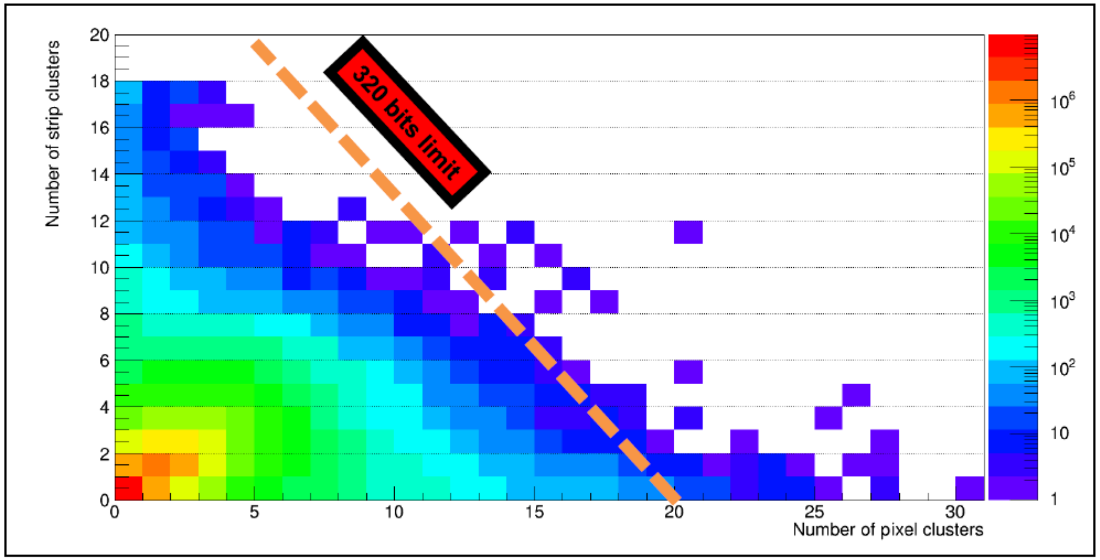

→ The transmission of L1 block over 64 bits from the 2S concentrator is robust against pile-up at 900kHz

→ Not true for the PS block (*see following slides*)



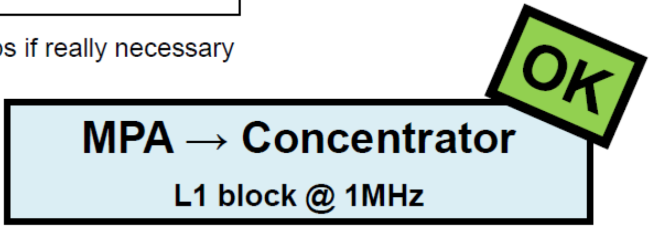
## → MPA to concentrator (*L1 block*):

→ Cluster multiplicity per MPA chips for PU140+4T events:




→ Cluster limit is not reached for the pixels, might be increased for the strips if really necessary

→ Vast majority of the chips have lower multiplicities and don't reach the 320 bits limit. **Relatively small MPA FIFO size should be sufficient to transmit L1 info at 1MHz** (*need to be evaluated, but storing 3-4 events should be sufficient*)



## → PS concentrator to GBT (*trigger block*):

| TRG size (in bits) | Bend coding | Stub losses (in %) | | | | | |
|---|---|---|---|---|---|---|---|
| | | All stubs | | | Good stubs | | |
| | | TOB 1 | TOB 2 | TOB 3 | TOB 1 | TOB 2 | TOB 3 |
| 256 | 5 | 15.3 | 1.9 | 0.6 | 19.4 | 2.2 | 0.3 |
| | 3 | 12.3 | 1.3 | 0.5 | 15.9 | 1.4 | 0.2 |
| | 0 | 7.2 | 0.7 | 0.5 | 9.8 | 0.7 | 0.1 |
| 288 | 5 | 10.7 | 1.1 | 0.5 | 14.2 | 1.2 | 0.2 |
| | 3 | 8.2 | 0.8 | 0.5 | 11.1 | 0.8 | |
| | 0 | 4.6 | 0.5 | 0.4 | 6.3 | 0.4 | |
| 312 | 5 | 8.2 | 0.8 | 0.5 | 11.1 | 0.8 | |
| | 3 | 6.1 | 0.6 | 0.5 | 8.4 | 0.5 | 0.1 |
| | 0 | 3.3 | 0.4 | 0.4 | 4.6 | 0.3 | |
| 320 | 5 | 7.4 | 0.7 | 0.5 | 10.1 | 0.7 | |
| | 3 | 5.6 | 0.5 | 0.4 | 7.7 | 0.5 | |
| | 0 | 3.0 | 0.4 | 0.1 | 4.1 | 0.3 | |

→ **The innermost layer is clearly problematic.** Even if one allows the complete bandwidth to trigger and pass no bend info **we loose at least 4% of the good stubs.**

→ **288 bits/ 3 bend bits**, is an acceptable working point for the other layers.

→ For TIB1, we need to see what we could gain if we add some stub sorting at the concentrator level.

**Critical for TIB1**

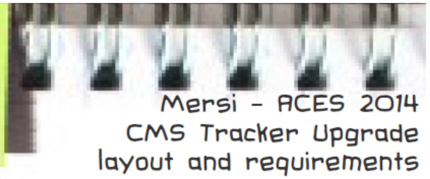
**PS Concentrator → GBT**

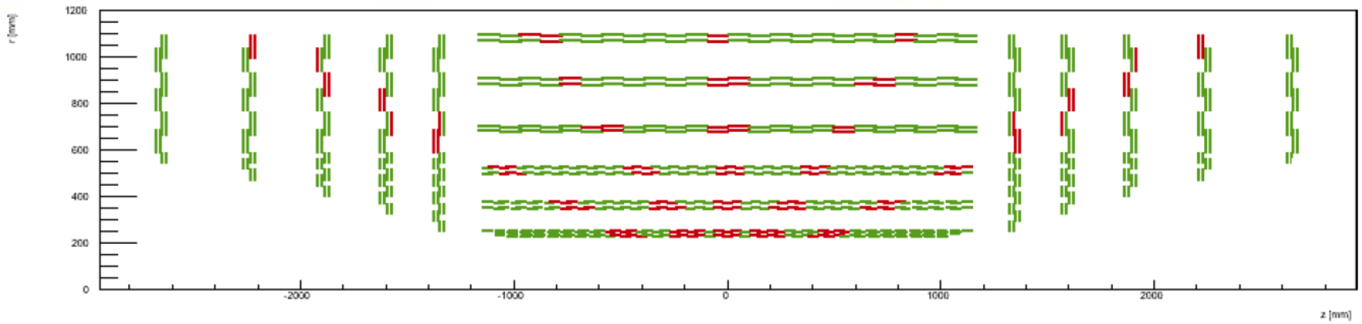
**Trigger block @ 40MHz**

# L1 Tk finding

# Track finding at Level-1

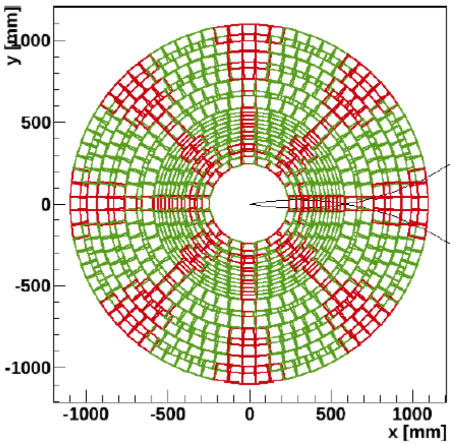
Divide & impera!



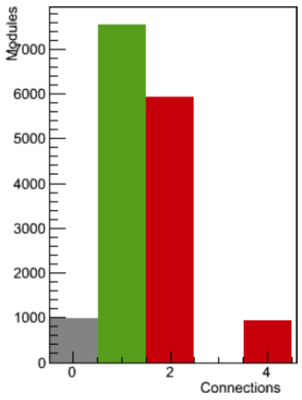




Working hypothesis:

- Each sector independent
- Overlap regions function of
  - Luminous region Δz
  - Minimum pT cut

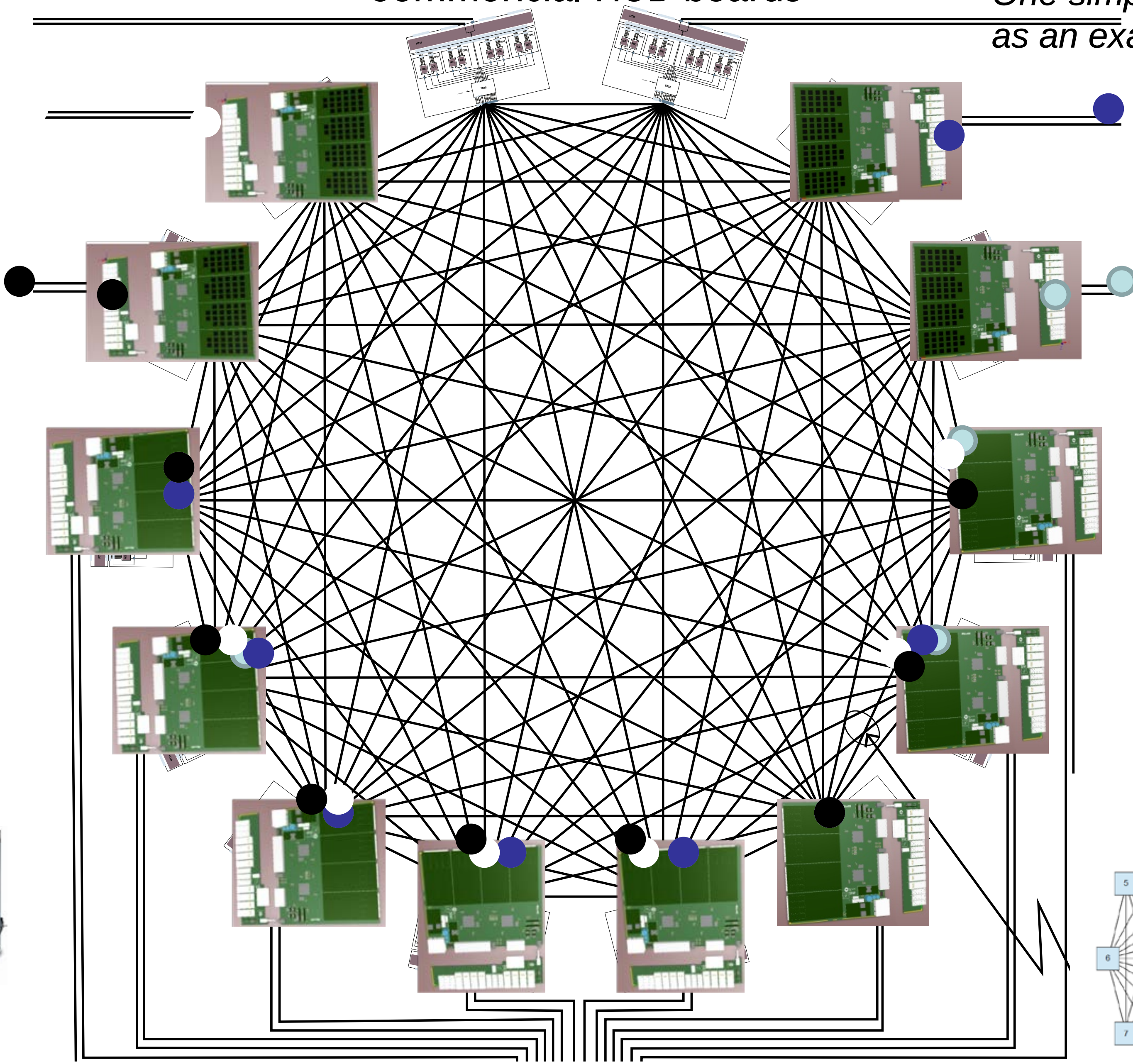


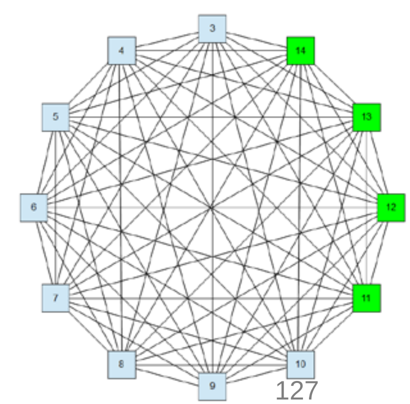

Number of sectors connected to a module



# Commericial HUB boards

*One simple configuration as an example*

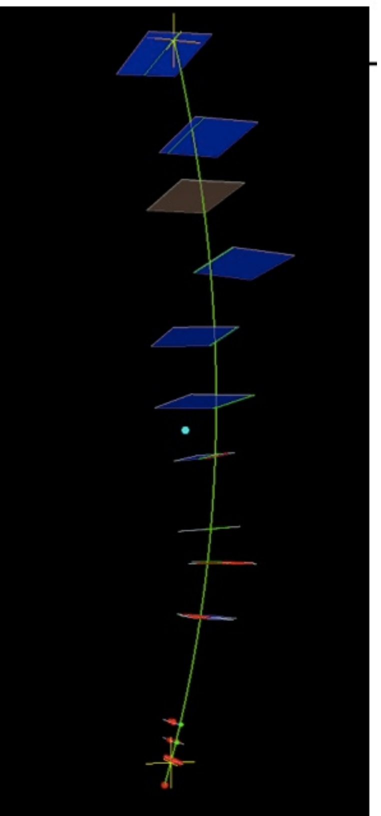


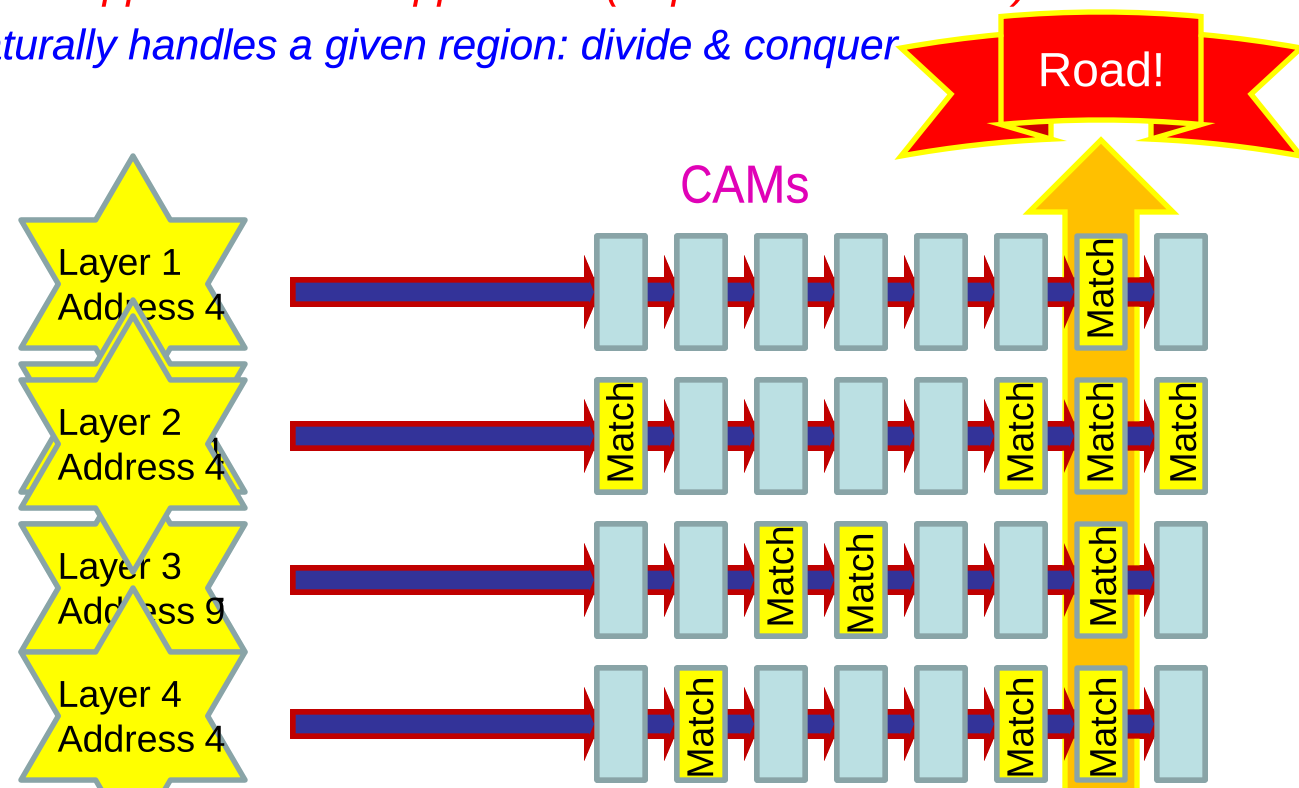



# The AM approach

- Pattern Recognition Associative Memory
  - Based on *CAM cells to match and majority logic to associate* hits in different detector layers to a set of pre-determined hit patterns (simple working unit, yet massively parallel)
  - *Pattern Recognition  finishes right after all hits arrive (fast data delivery important)*
  - *Potentially good approach for L1 application (require custom ASIC)*

*A PR engine naturally handles a given region: divide & conquer*






*Linearized track fitting can follow each road found (FPGA implementation)*