Electronics for Muon upgrades

G. De Lentdecker
Université Libre de Bruxelles (ULB)
Brussels, Belgium

Outline

- Motivations
- Introduction
  - Signal amplification, CMS trigger
- Current CMS muon electronics
- Upgrades of the CMS muon electronics
- GEM electronics

Motivations for muon upgrades

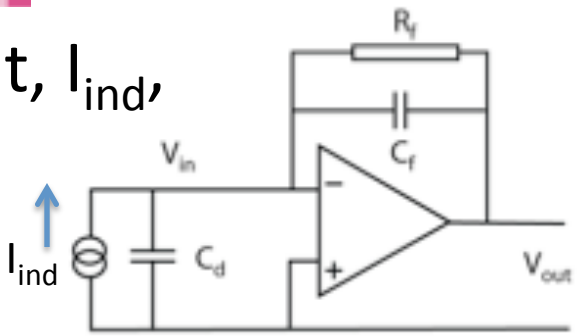
- Aging and longevity
  - The present muon system installed in 2007 must continue to operate w/o significant degradation after higher irradiation and longer operation time than expected
- Trigger
  - Increased particle rates and pile-up require more selective triggering to keep the trigger efficient and the trigger rate under control
    - At high luminosity the L1 muon trigger in the forward region is compromised
  - This typically requires improved tracking for P_T selection and fake trigger rejection
    - This problem can be addressed by the addition new forward muon stations.
- η-coverage
  - If tracker and endcap calorimeter are extended up to η = 4, the coverage for muon identification can be greatly extended with the addition of a small but precise muon detector built into the back of the new endcap calorimeter
- Electronics
  - All muon system will have to upgrade some parts of their electronics, because:
    - Higher radiation levels
    - Higher data volumes
    - Higher Triger rates
    - Longr L1 latency
    - Faster and smarted data processing

Signal formation

- The signal is not due to charges entering the electronics from the detector, it is due to induction by moving charge
- Once the charge has actually arrived at the electrode the signal is over !
- The longer the amplifier integration time the more charge is integrated
- The design of the amplifier should consider
  - Signal formation in the detector
  - Intrinsic gain of the detector
  - Input capacitance
  - …

Charge sensitive preamplifier

- The detector acts as a source of current, I_{ind}, with some capacitance C_d.



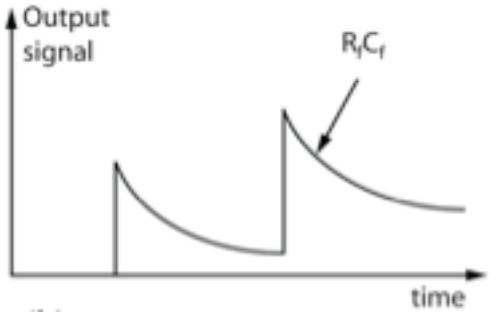
- The preamplifier has a very large input impedance → I_{ind} flows to the feedback loop and charge C_d . The charge is « integrated » on the capacitor:

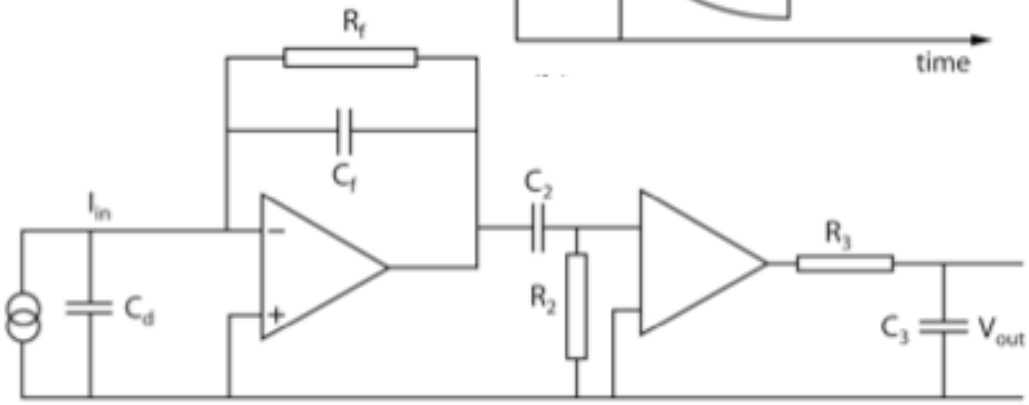
$$V_{out} = -\frac{1}{C_f}\int I_{ind}(t)\,dt = -\frac{Q}{C_f}$$

- The needed gain determines C_f
- Gain is independent on C_d (nor parastic capacitance)
- R_f is needed to discharge the capacitance ($\tau = R_f C_f$)

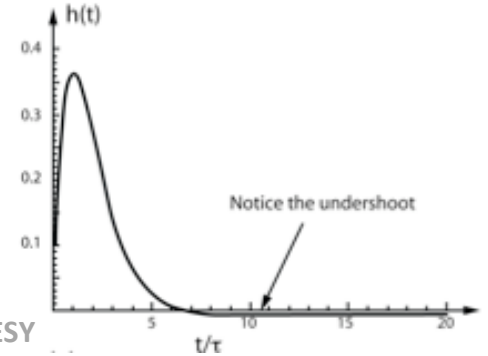
Shaping

- The response of a charge integrating amplifier to a current pulse will be a sharp rising edge at the moment the pulse arrives, followed by an exponential decay with a time constant R_fC_f, of the order of 40-50 µsec.
- This severely limits the counting rate
- Need a way to make output pulses shorter
- → shaping stages after preamp
  - Typically CR-RC stages:
    - Pulse is filtered at low and high (RC) frequenci





- Usually $C_2R_2=R_3C_3 << R_fC_f$
- Drawbacks: presence of undershoot:

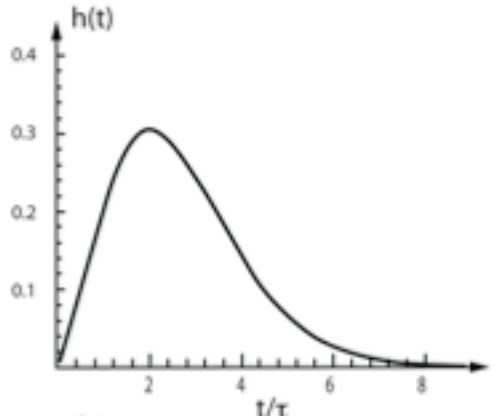


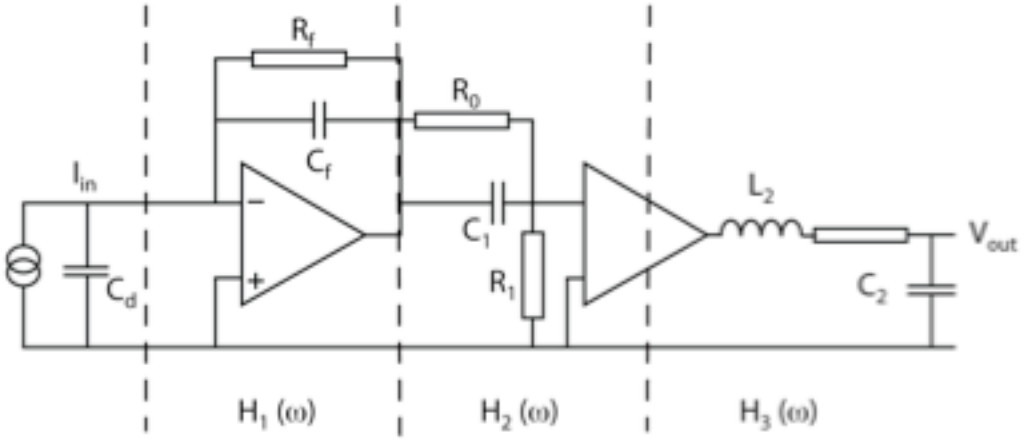
Pole-zero cancellation

- The long negative tail after the main pulse (called undershoot) is due to the differentiation (CR) of finite length pulses. Theoretically no undershoot would occur if these tail pulses were infinitely long.

- Without entering into details there are several ways to cancel the undershoot. These are called ‘pole zero cancellation’. One way is illustrated in the picture:

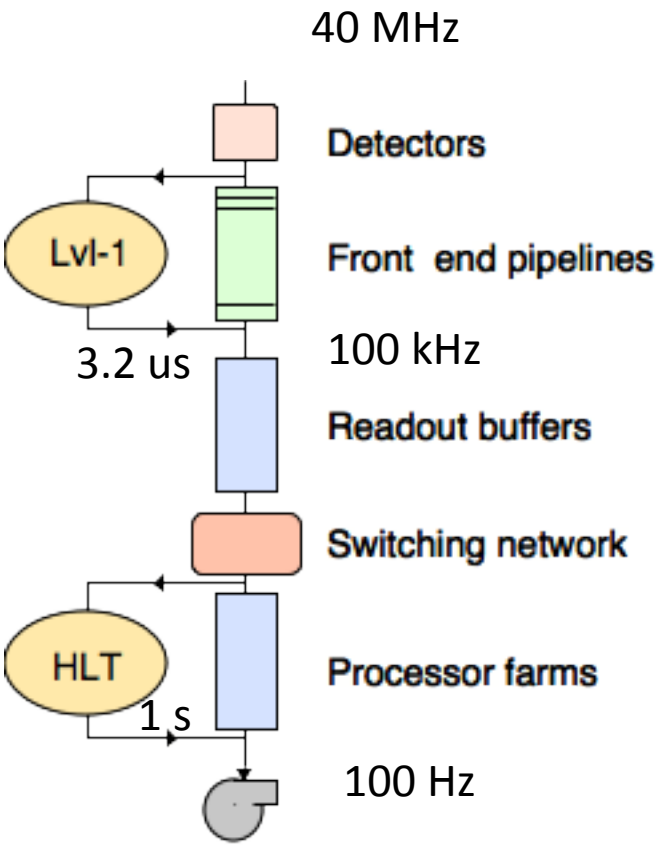
- This circuit gives the following output pulse:





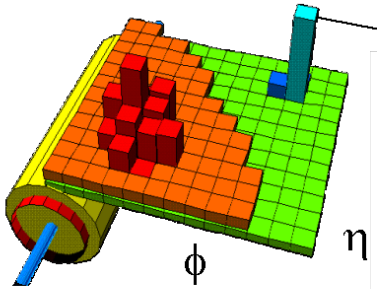
Before we start

- Electronics is not only the front-end amplifier connected to your detector
- Front-end electronics is strongly dependent on the trigger and data acquistion architecture of the experiment
- Nowadays the first levels of the trigger system of HEP experiments are performed in hardware by digital electronics
- CMS has a two-level trigger and DAQ system



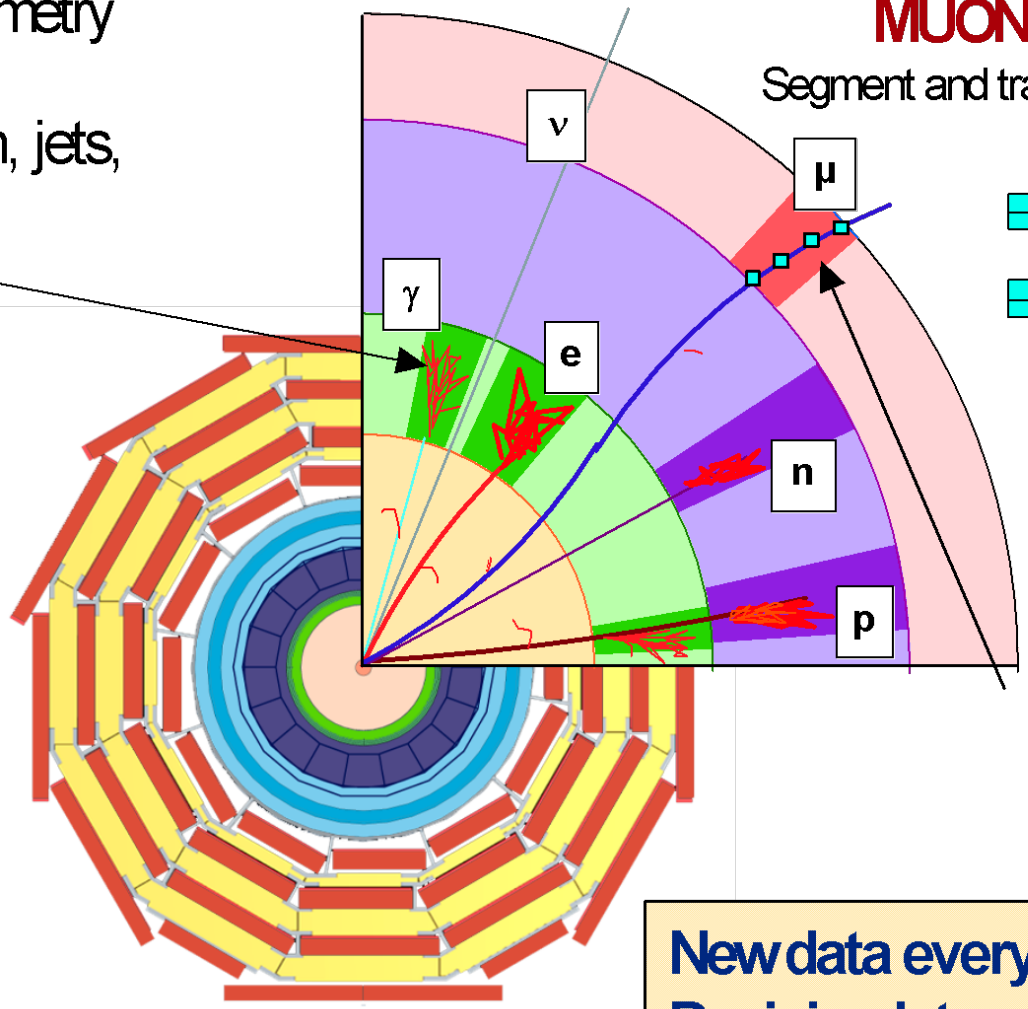
Before we start (cont'd)

Use prompt data (calorimetry and muons) to identify:
High p_t electron, muon, jets, missing E_T



CALORIMETERs
Cluster finding and energy deposition evaluation

MUON System
Segment and track finding

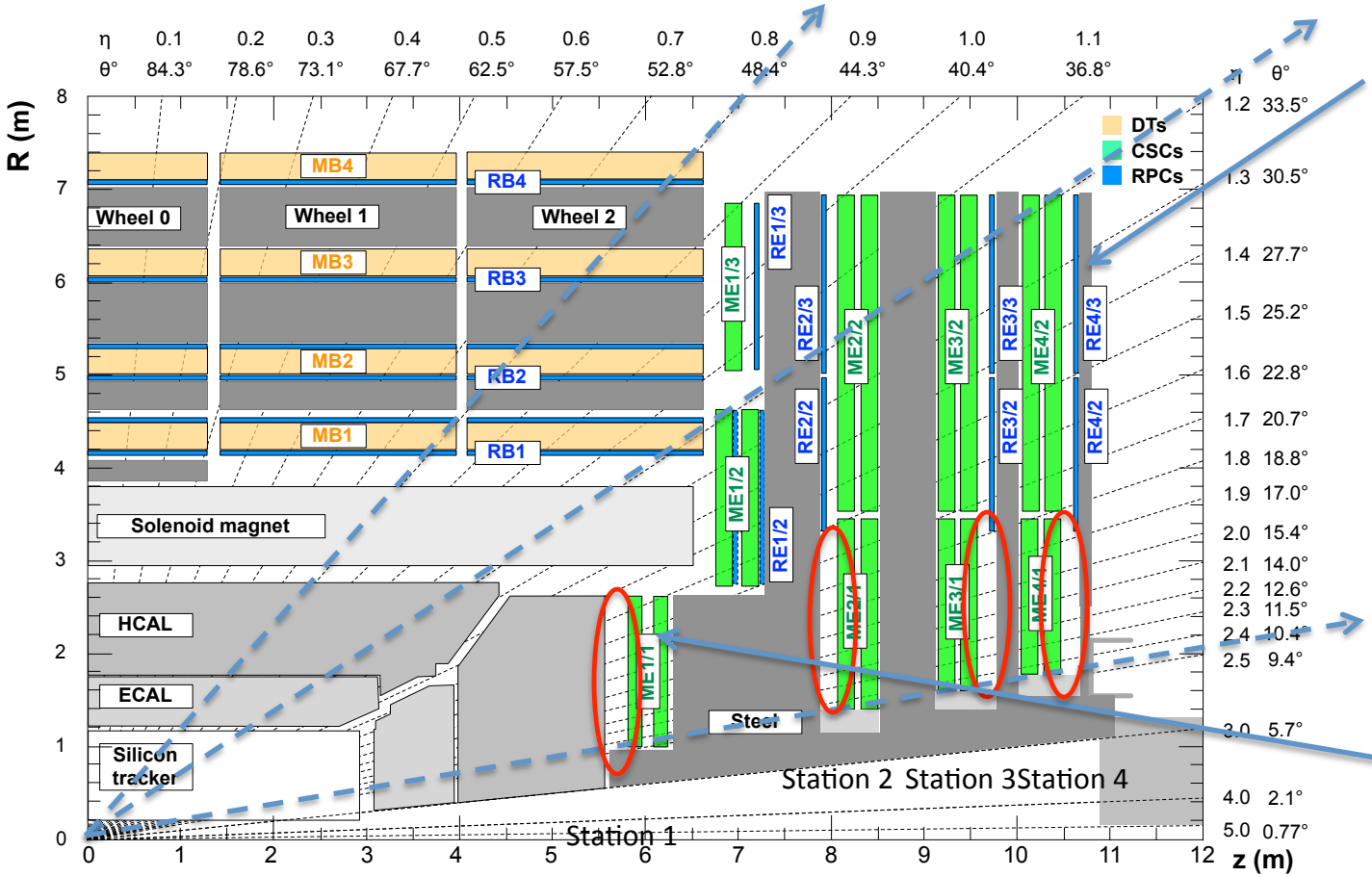


New data every 25 ns
Decision latency ~ μs

The CMS Muon system (post LS1)

- Highly redundant
- High performance tracking and triggering
- Use 3 gaseous detector technologies

Drift Tube (DT) – Barrel only
Cathode Strip Ch. (CSC) – Endcap only
Resistive Plate Chamber (RPC)

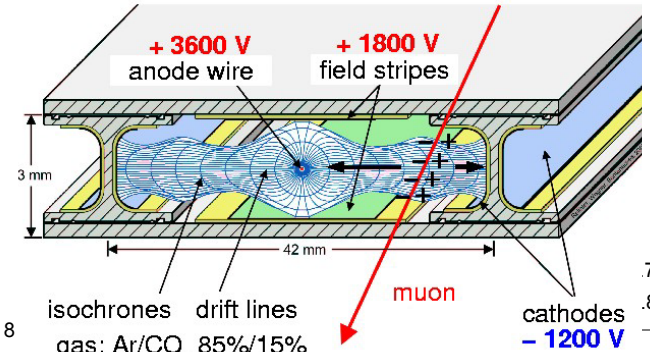


RE4 installed during LS1

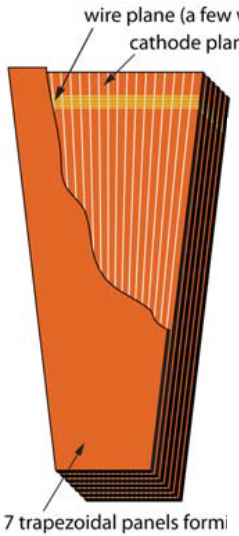
Other LS1 upgrade: New ME1/1 front and backend electronics

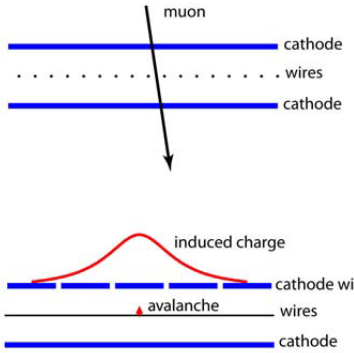
The CMS Muon system (post LS1)

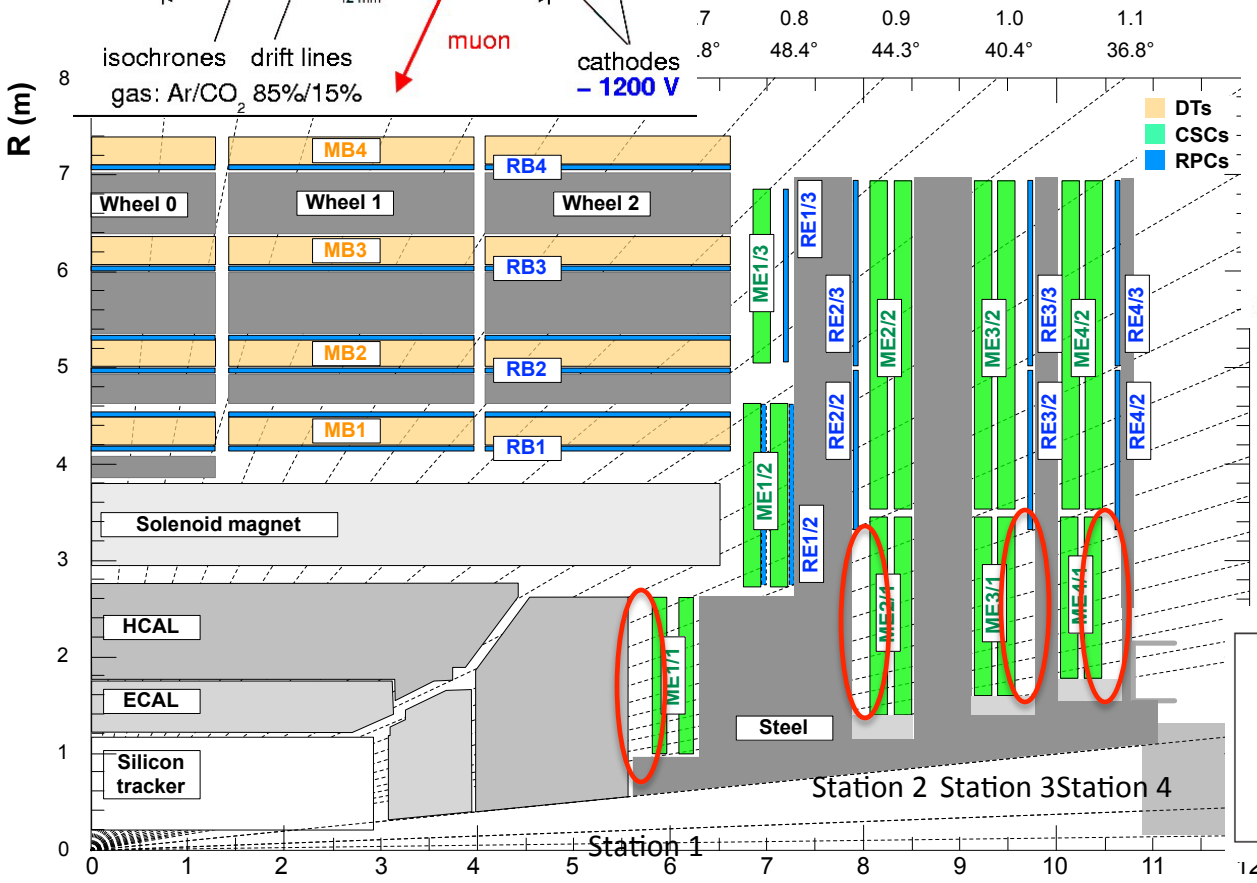
Drift Tube (DT) – Barrel only



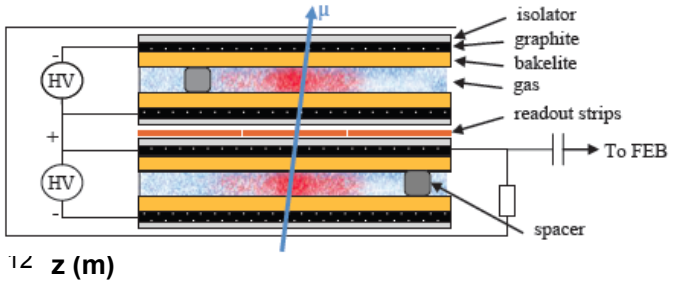
Cathode Strip Ch. (CSC) – Endcap only







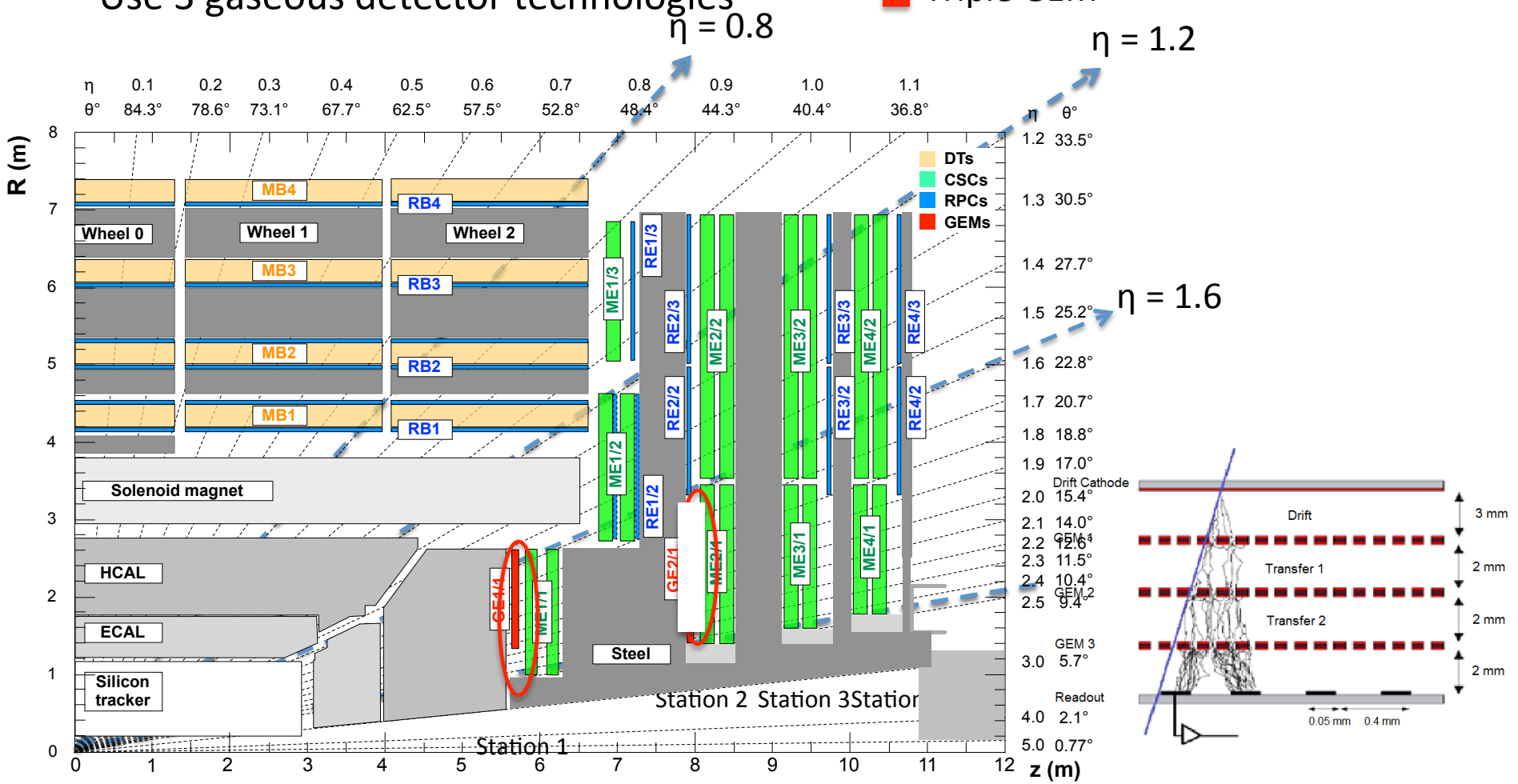
Resistive Plate Chamber (RPC)



The CMS Muon system (post LS2)

- Highly redundant
- High performance tracking and triggering
- Use 3 gaseous detector technologies

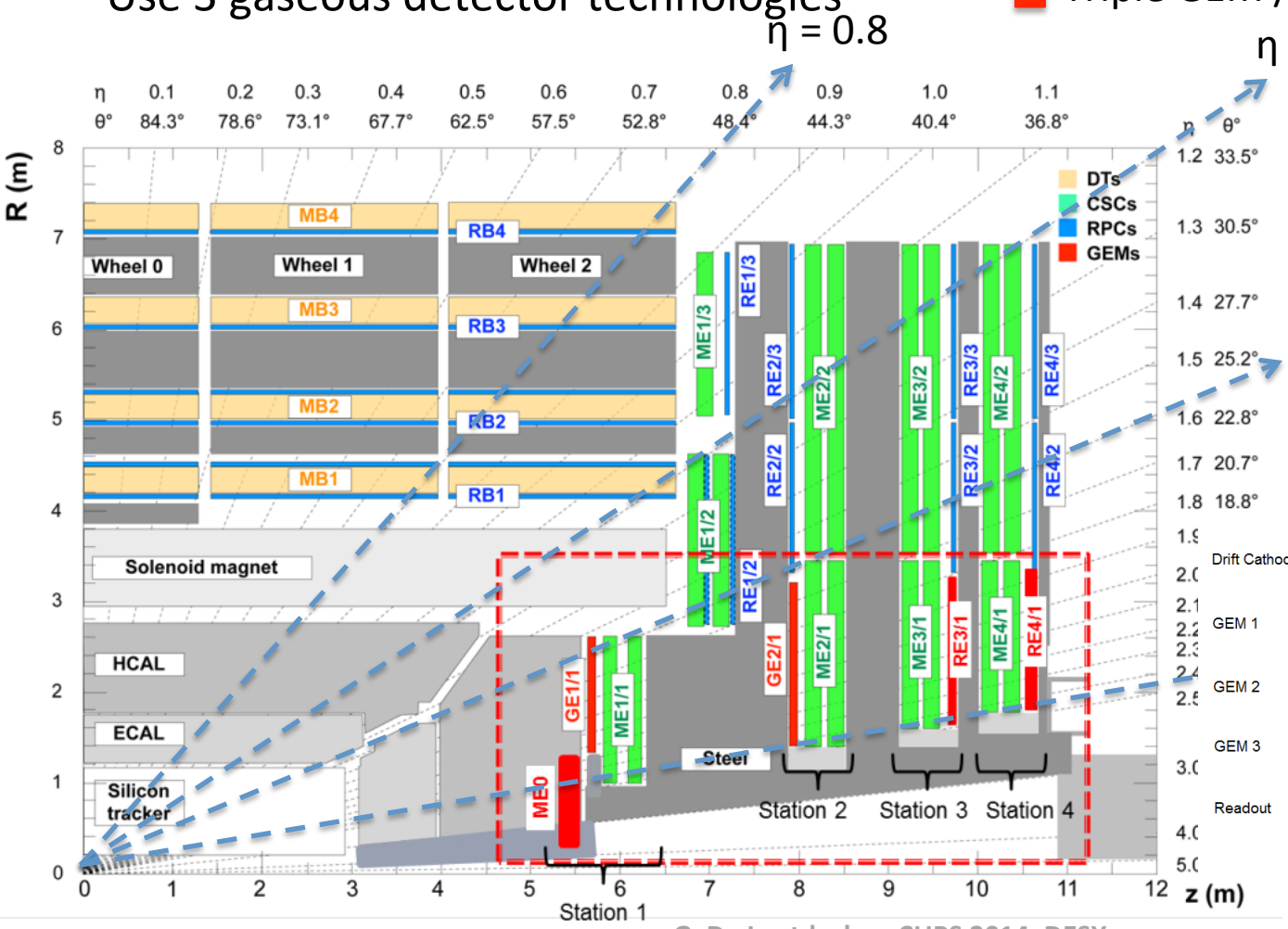
Drift Tube (DT) – Barrel only
Cathode Strip Ch. (CSC) – Endcap only
Resistive Plate Chamber (RPC)
Triple GEM

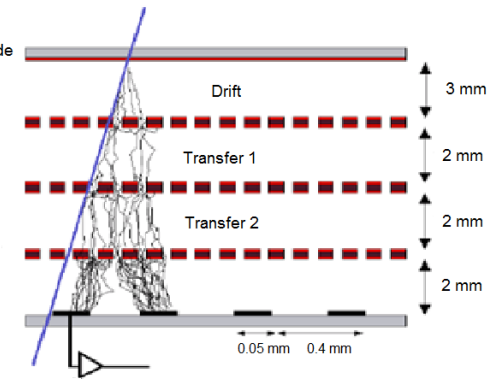


The CMS Muon system (post LS3)

- Highly redundant
- High performance tracking and triggering
- Use 3 gaseous detector technologies

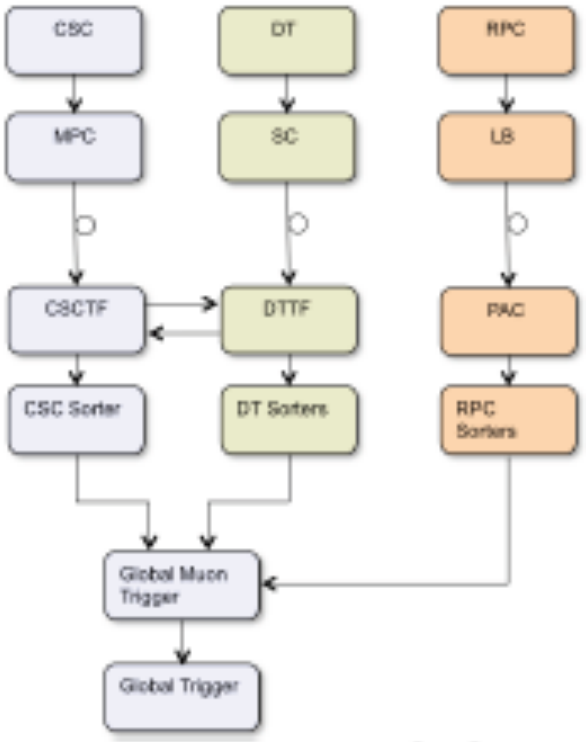
Drift Tube (DT) – Barrel only
Cathode Strip Ch. (CSC) – Endcap only
Resistive Plate Chamber (RPC)
Triple GEM /iRPC





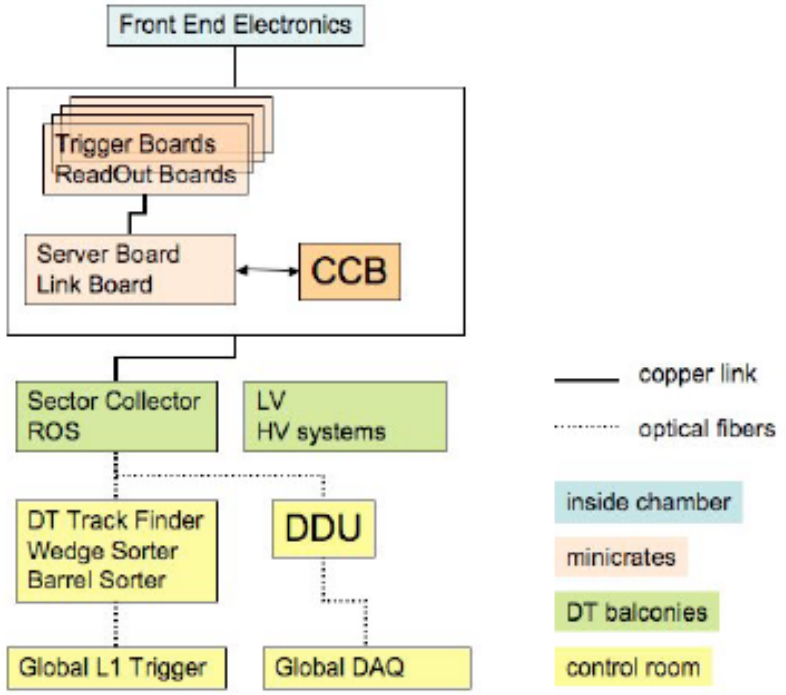
Current Muon Trigger

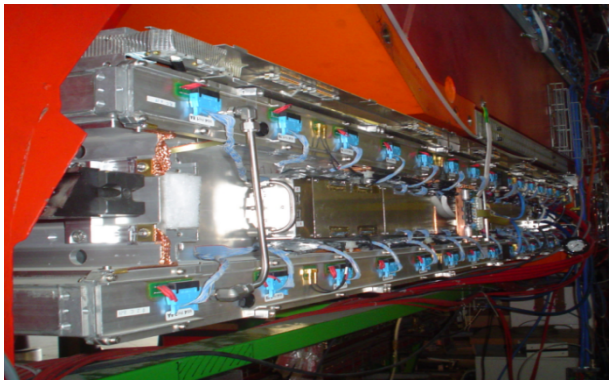
- FE trigger primitive generator electronics identify tracks segments from the hits registered in multiple gas planes of a single measurement station
- These segments are transmitted through optical links to Track-Finders (TF) in USC
- TF apply pattern recognition algorithms
- Information is shared between DTTF and CSTF for the overlap region (|η| ~ 1)
- Hits from RPC are directly sent from FE electronics to Pattern Comparator (PAC) logic board
- The 3 regional TFs sort the μ candidates and transmit to the Global Muon Triger (GMT):
  - Up to 4 (CSCTF and DTTF) or 8 (RPC) candidates
- GMT merges the muon candidates found by more than one system and can suppress muons of bad quality



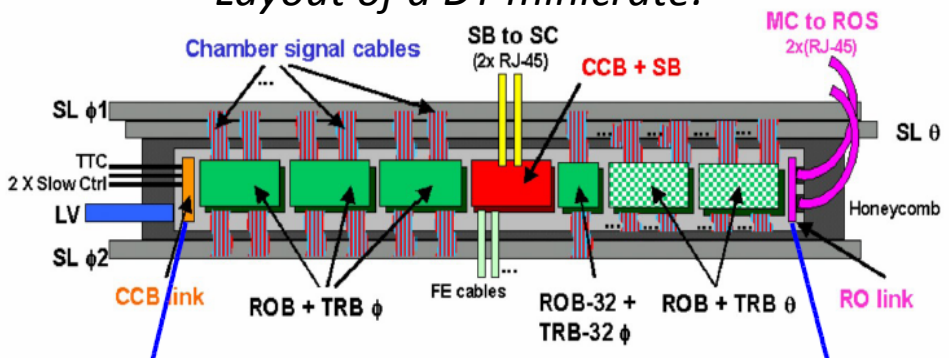
Drift Tubes electronics

- Front End
  - MAD ASIC (800 nm)
  - 4 ch pre-amplifier+shaper
- Read-Out Board (ROB)
  - Located in minicrates
  - Perform time digitization by HPTDC
- Read-Out Server (ROS)
  - Racks located beside the wheels (30 m from mini crate
  - Merges data coming from chambers of one sector (70 m optical link) to DDU
- DDU (Detector Dependent Units)
  - = DT Front-End-Driver (FED)
  - Located in USC





Layout of a DT minicrate:



Trigger Board (TRB); Chamber Control Board (CCB)

DT local trigger

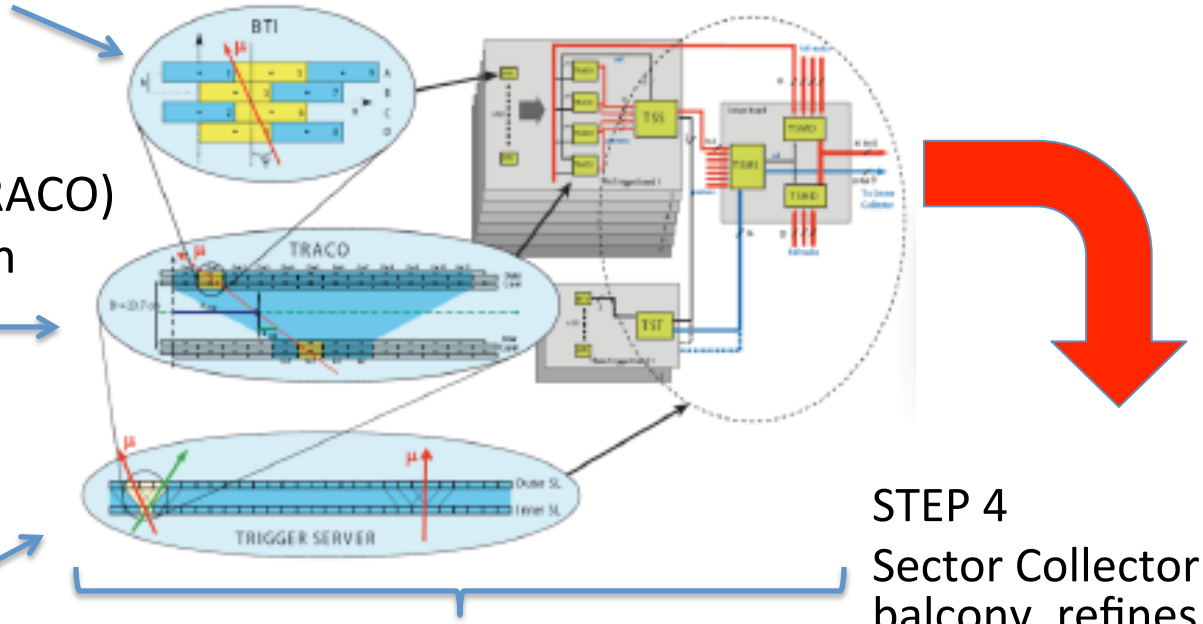
STEP 1

Signals from wires are processed by Bunch and Track Identifier (BTI):

- Rough track fitting within a Super Layer (SL)

STEP 2

TRAck COrrelators (TRACO) match the information from two φ-SLs



Within minicrate

STEP 3

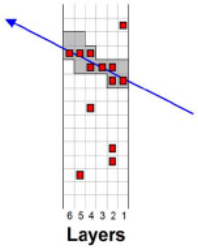
Trigger Server (TS) performs a quality based selection on segments coming from TRACOs

STEP 4

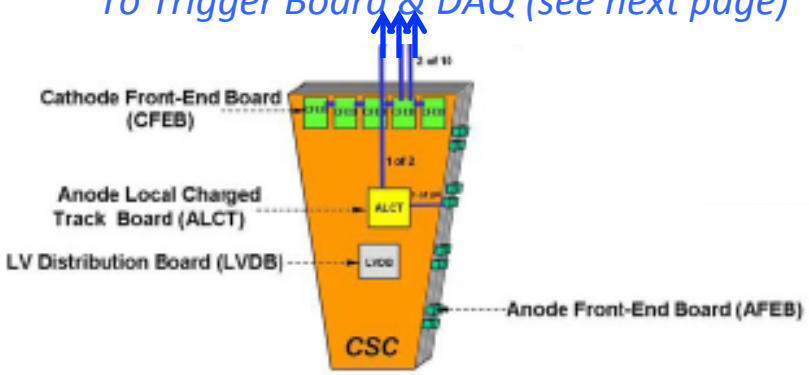
Sector Collector (SC), on balcony, refines the sorting per sector and performs BX alignments before sending data to DTTF

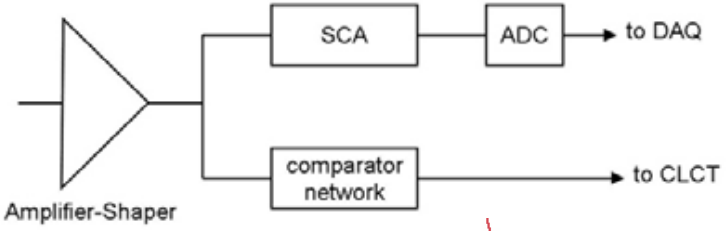
CSC electronics

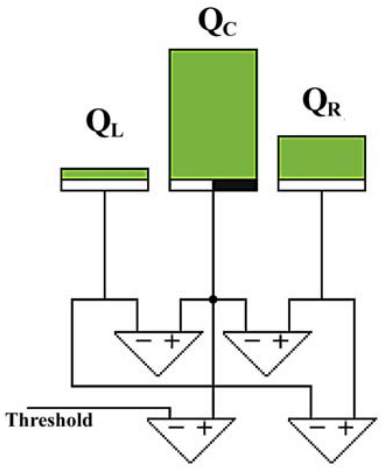
- Anode FE Board (AFEB):
  - 16 ch amplifier-discr. (τ = 30 ns)
- ALCT board:
  - FPGA: searches for patterns every 25 ns
  - 225 ns to form the primitive (incl. drift time)
- CFEB:
  - Serves 6 (planes) x 16 strips
  - Amplifier-shaper (τ = 100 ns)
  - Comparator network compares signals on triplets of adjacent strips
  - Can identify muon with one half of strip width

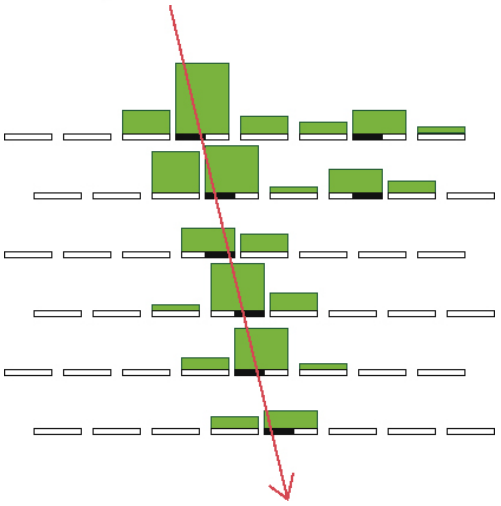


To Trigger Board & DAQ (see next page)

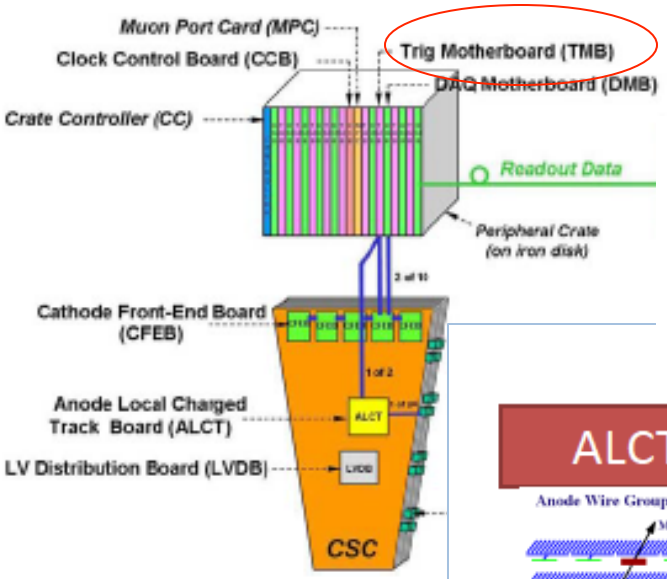


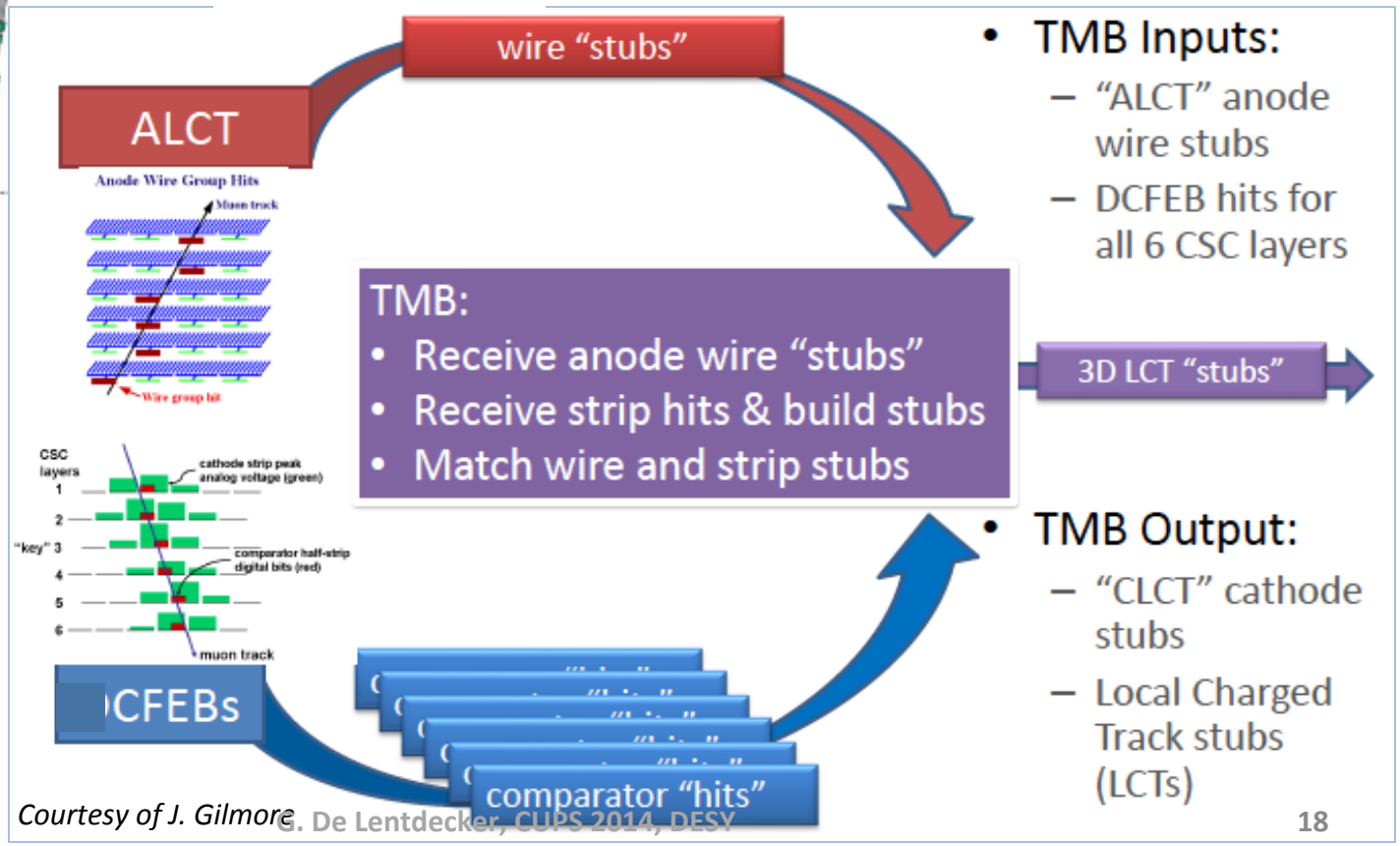






CSC Trigger Mother Board

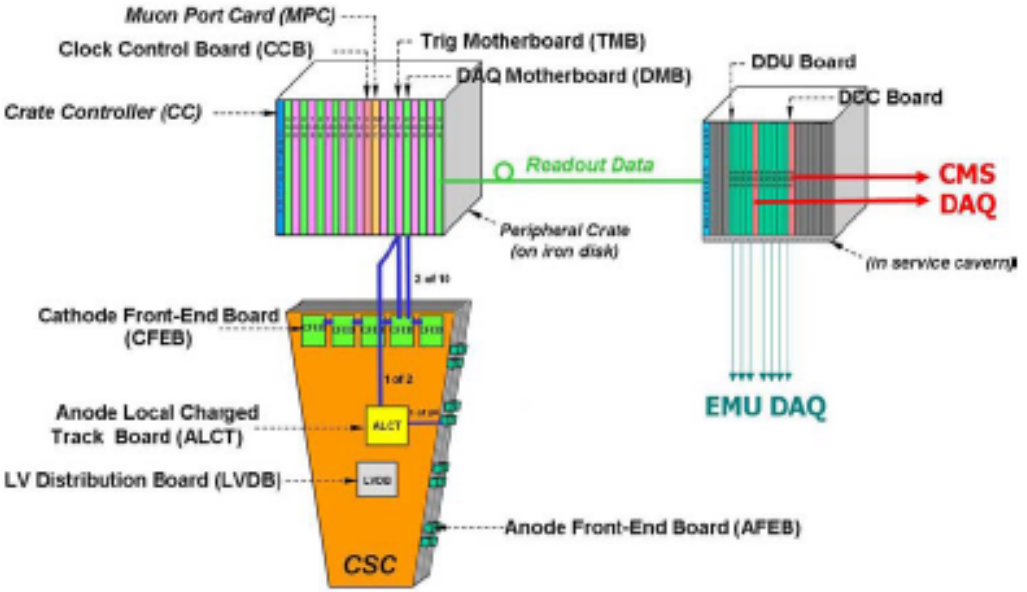




Courtesy of J. Gilmore

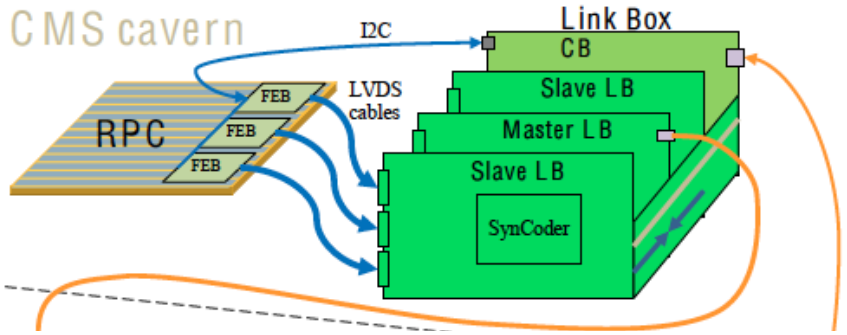
CSC Trigger

- Trigger Mother Board (TMB)
  - Receives data from ALCT & CLCT
  - 1 TMB per chamber
  - sends 2 LCTs trough custom backplane to Muon Port Card (MPC)
- MPC
  - Can receive data from 9 CSCs
  - LCTs are sorted and 3 best ones sent to CSCTF over optical fibers
- CSCTF
  - Partitioned into sectors of 60° in φ
  - Each CSCTF is a 9U VME card
  - Three 1.6 Gbps optical links from each of five MPCs per board
- CSCTF track finding
  - Pairwise comparison of track segments in different stations
  - Compatibility in φ and η with IP
  - P_T calculated from large LUT.
  - After sorting the best 4 candidates are sent to GMT

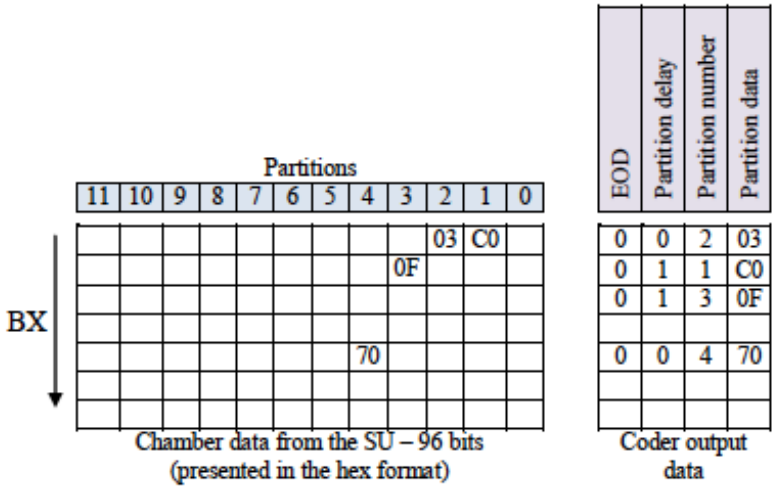


RPC electronics

- FEB:
  - 2 (barrel)/4(endcaps) FEC chips
  - 16 (barrel) / 32 (endcaps) channels
  - preamp. + zero-crossing discriminator
  - Binary output (LVDS)

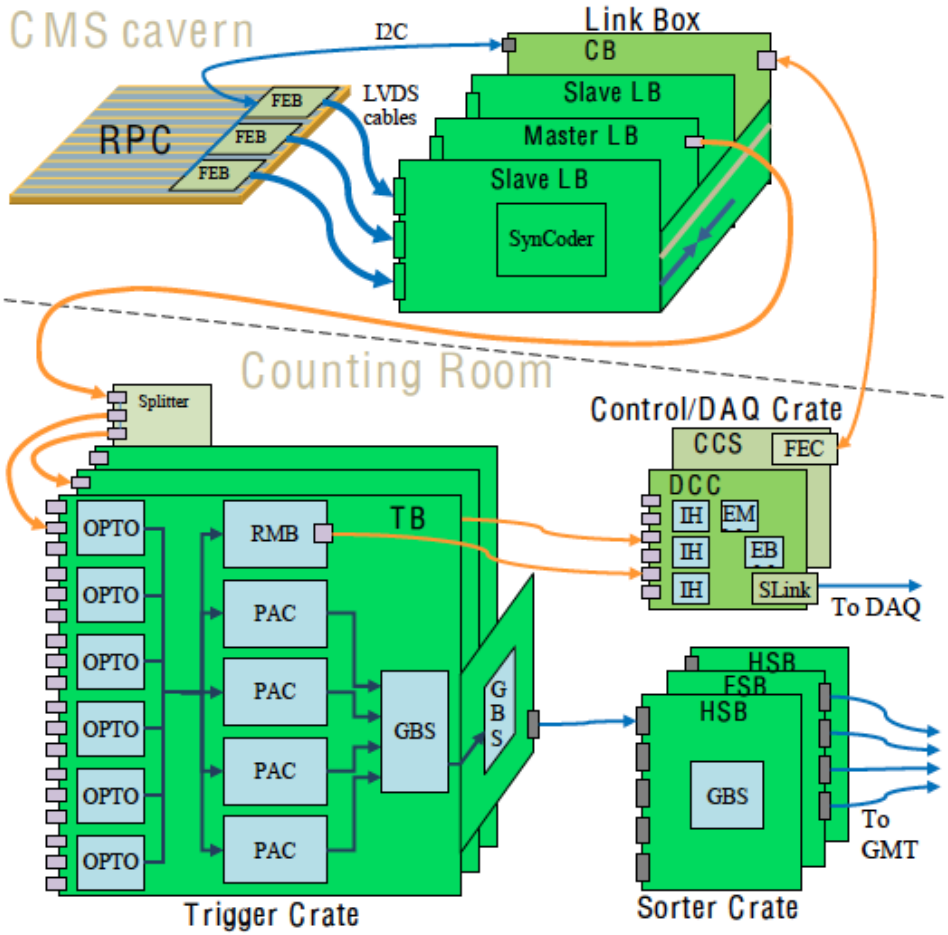


- Link Boxes (LB)
  - Synchronize signals from FEB and assign them to the proper BX
  - zero compression:
    - 96-bit input data vector of a given clock (BX) is divided into 12 partitions of 8 bits. The module select the non-empty partitions and send them one-by-one in the consecutive BX
    - Exemple:

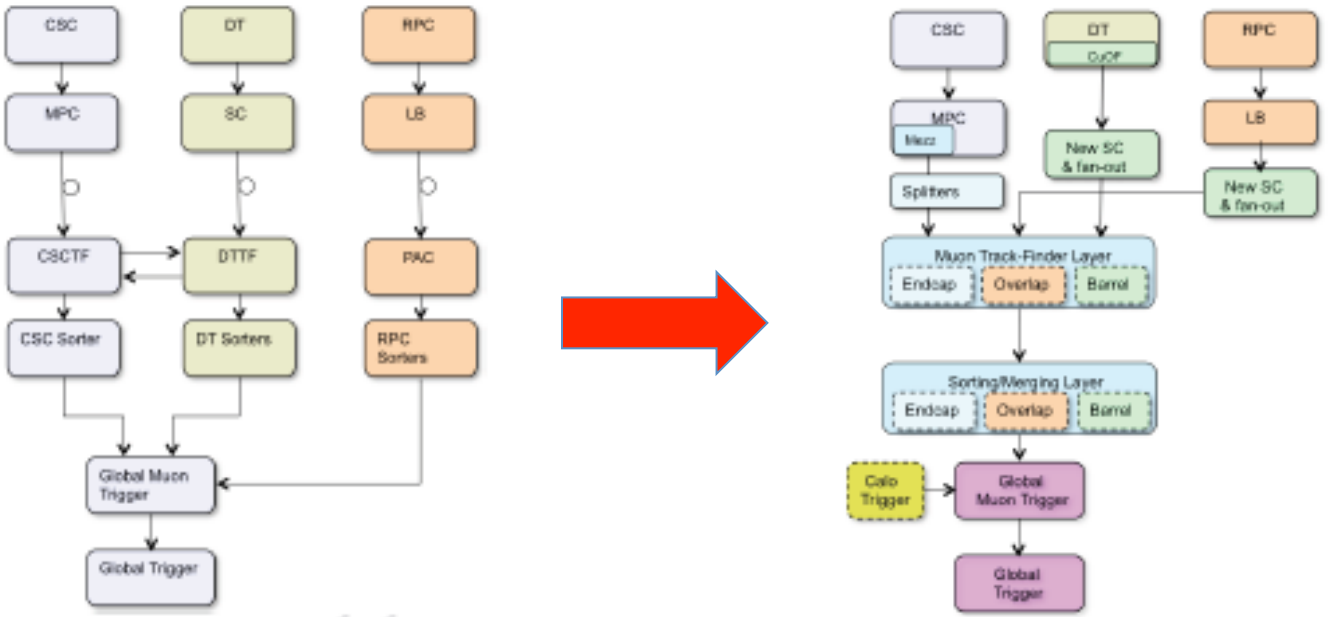


RPC trigger

- The data from 2 Slave LB and one Master LB are sent to the Trigger crate through the GOL optical link (1.6 Gbps)
- PAttern Comparator
  - Each PAC FPGA receive data from 18 optical links
- Trigger Crate
  - 3U VME crate
  - 1U standard VME backplane
  - 2U custom backplane for GBS
- Ghost Busting & Sorting (GBS)
  - Final sorting before being sent to GMT



Muon Trigger Upgrade



- Strategy of the muon upgrade:

  Make use of the redundancy of the muon systems earlier in the trigger chain

- Homogeneous Track-Finder

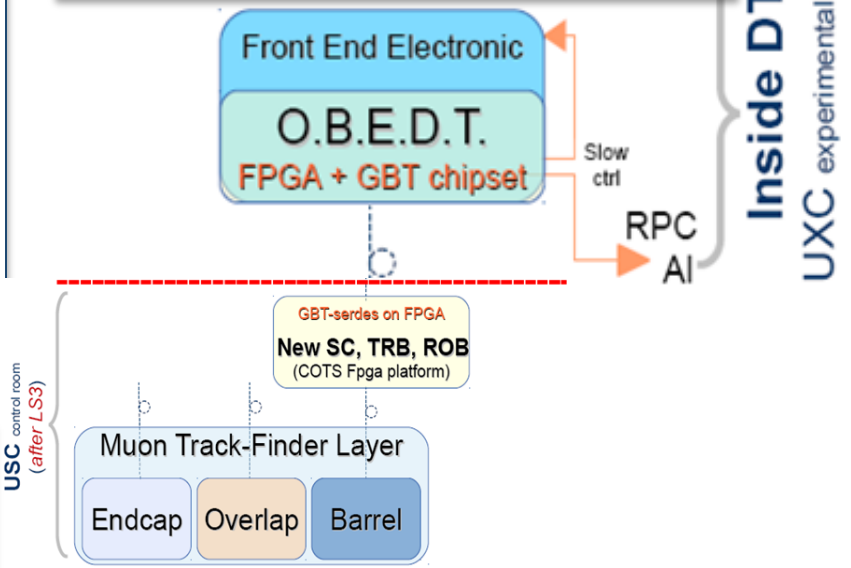
DT Electronics update (phase 2)

- Replacement of the minicrates:
  - aluminum structure attached to the DT chamber
  - 6 types of boards highly integrated, lots of interconnections and dense connectors
  - 85 Watts through water cooling
  - *Survival of this old system will require maintenance in UXC that looks very problematic taking into account the harsh environment foreseen for HL-LHC:*
    - Further radiation tests required (some parts showed failures in past tests at high lumi)
    - ROB will limit L1A rate to 300 kHz
    - Some reliability issues in the past force us to limit the number of power on/off cycles
    - 25% of the Minicrates intervened in LS1 (to recover only the 1% failures) → Hard to maintain
    - Large and costly power supply system to be maintained

DT Electronics update (phase 2)

- *New low cost time digitization electronics in UXC*
  - *1 Microsemi FPGA has already accommodated ~100 TDC of 5bit/1ns resolution*
- *Timing info from all the wires will be serialized and made available to USC using high bandwidth data link:* ***highest chamber resolution available for Level 1***
- *Produce* ***improved trigger system*** *by using algorithms not based in on-chamber ASICs but in high performance processor systems.*

OBEDT **(On Board Electronics for DT)**
~800 analog FE channels
TDC temporal resolution required ~1 ns
HL-LHC barrel radiation environment



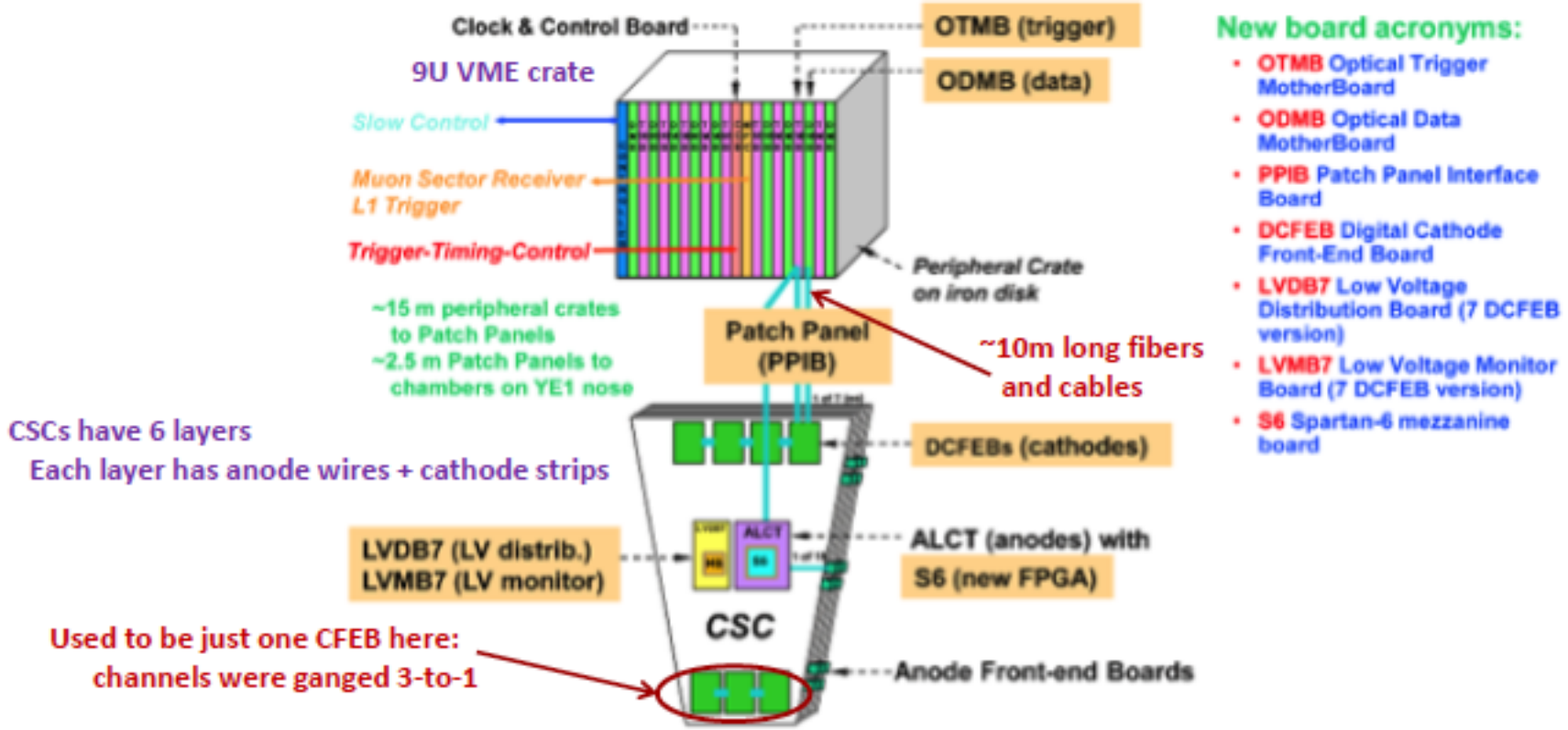
*Use ***off the shelf high performing*** devices (uTCA with powerful FPGA? ... 2023...)*

** Exercise of migration of present Bunch Crossing and Track Identifier (BTI ASIC) and Track Correlator (TRACO ASIC) algorithms*

→ *20 million gates of logic*

==1 or 2 Virtex 7 biggest part 7V2000T per chamber

CSC upgrade during LS1



New board acronyms:

- OTMB Optical Trigger MotherBoard
- ODMB Optical Data MotherBoard
- PPIB Patch Panel Interface Board
- DCFEB Digital Cathode Front-End Board
- LVDB7 Low Voltage Distribution Board (7 DCFEB version)
- LVMB7 Low Voltage Monitor Board (7 DCFEB version)
- S6 Spartan-6 mezzanine board

- New: unganged CFEBs for the high-Eta end of ME1/1
  - This is a critical step for making trigger rates manageable
    - These are by far the highest rate chambers in the CMS Endcap Muon system
- Digital CFEB: digital storage on the DCFEB replaces old analog SCA technology
- The extra channels necessitate the change to optical readout
  - Upstream boards redesigned with optical components: Optical Trigger Motherboard

J. Gilmore TWEPP 2014 3

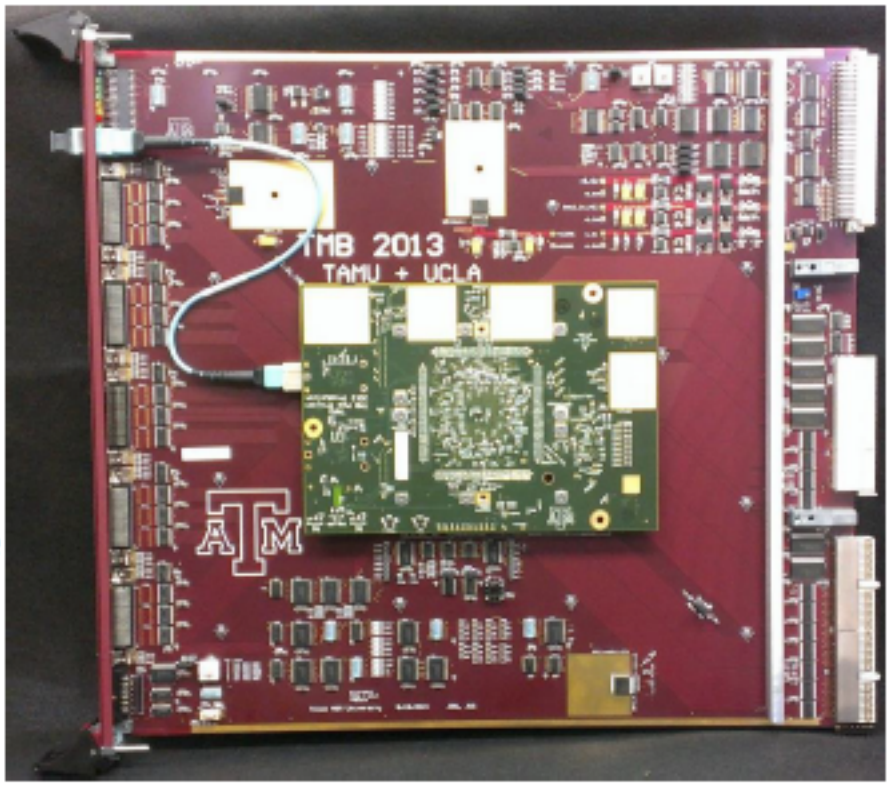
Optical Mother Board

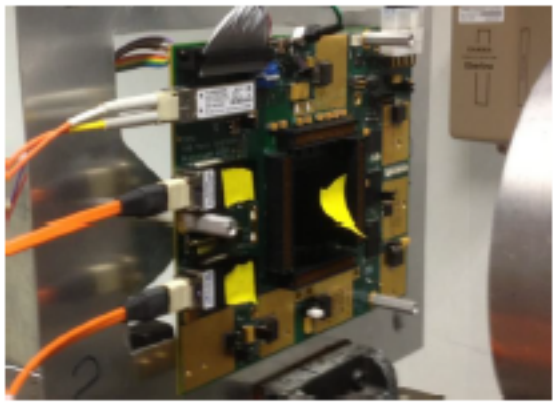
Requirements for the OTMB design

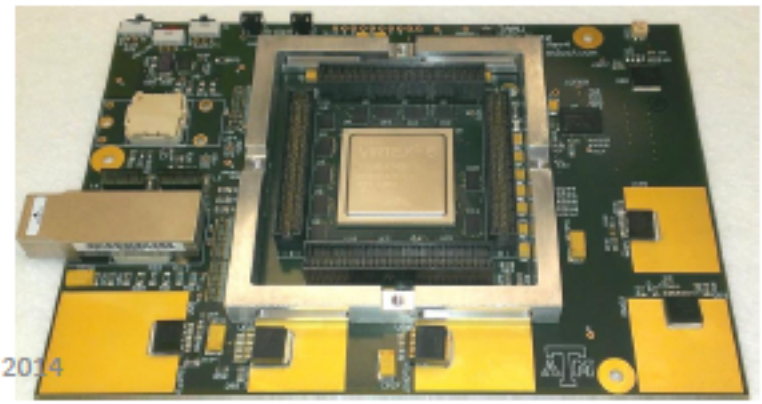
- Receive fiber optic data from 7 DCFEBs using 3.2 Gb/s links on ME1/1 CSCs
  - Optical Trigger Motherboard interface is required for the new DCFEBs
- Provide a programmable logic platform that allows for greater CSC trigger complexity
  - FPGA that is larger and faster than the old model
  - Necessary for efficient HL-LHC trigger operation
- Full backwards compatibility with the copper cable data links used on other CSCs with old CFEBs
  - OTMB could be used on any CSC in a future upgrade
- Operate reliably in the CMS endcap environment
  - Magnetic field concerns
  - Verify the system is sufficiently radiation tolerant

Optical Mother Board R&D

- OTMB Features:
  - Mezzanine is a 12-layer PCB with impedance control layers
    - Virtex-6 FPGA
    - Snap12 optical receiver
  - Baseboard is a 10-layer PCB
    - 9U VME module, 400 mm deep
    - Design very similar to old board
- Extensive Radiation Testing
  - Reactor tests for neutron exposure
    - Texas A&M Nuclear Science Center
  - SEU studies in proton beams
    - Texas A&M Cyclotron, 55 MeV
    - UC Davis Cyclotron, 63 MeV







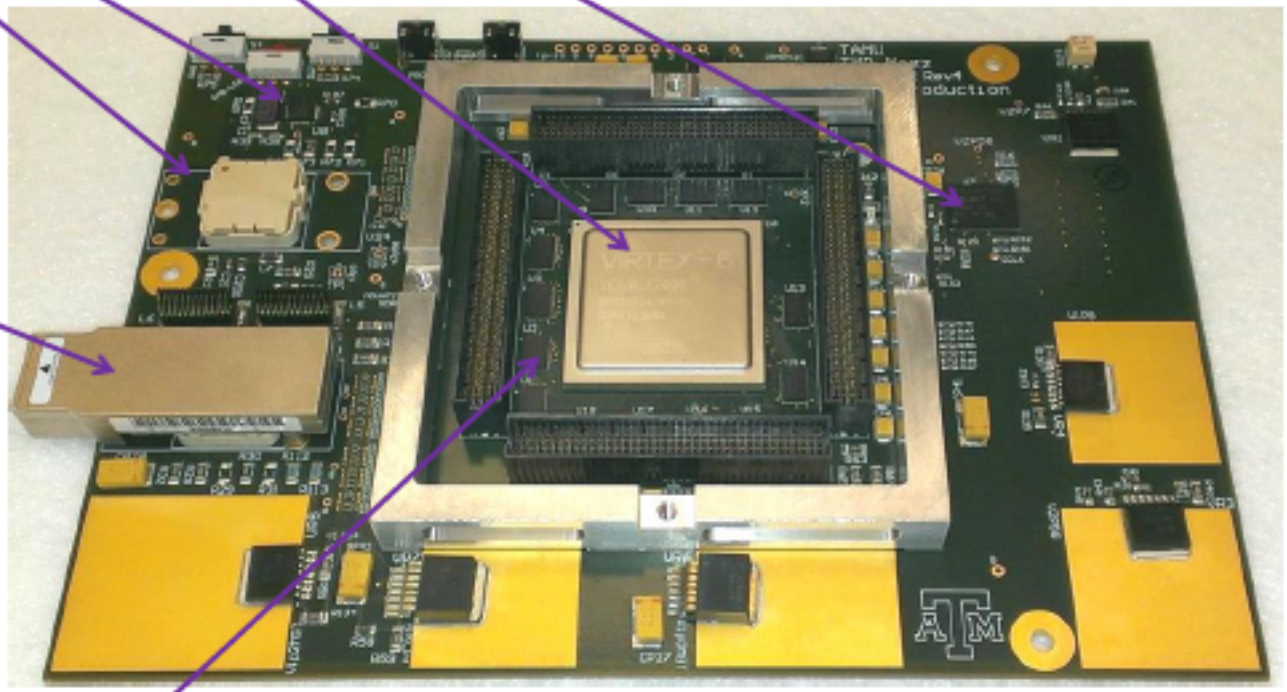
OTMB Mezzanine

Virtex-6 FPGA + PROM

The FPGA: XC6VLX240T-1FFG1156C

Cern QPLL

Snap12 Fiber Transmitter
- an option only available for special tests



Snap12 Fiber Receiver
- rated at 3.5 gbps
- fibers from 7 CFEBs
- 5 fibers available for future plans

I/O Voltage-level shifters, 3.3 V to 2.6 V

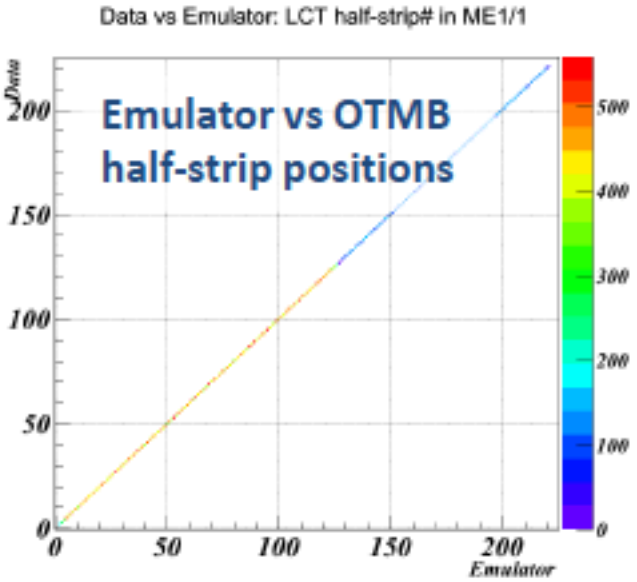
PCB Dimensions: 7.5" long by 5.25" wide
11 mm clearance from TMB base board

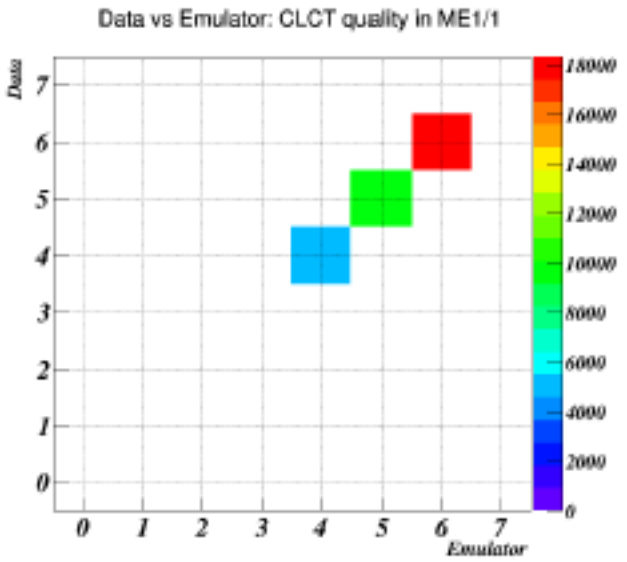
Installation and Commissioning

- 87 OTMBs were built, with 72 installed in CMS
  - 100% of the boards passed all production tests (after fixing a few bad solder joints)
- All of the installed boards have been commissioned
  - Validated communication with other boards in the system
  - Cosmic ray tests & timing studies are ongoing
  - Currently working to improve some monitoring features in software & firmware…
  - Plan to take advantage of speed in the faster FPGA
    - Expect new firmware will reduce trigger latency by ~100 ns
- Effort is ongoing to prepare the new OTMB trigger algorithm for phase 1

OTMB performance

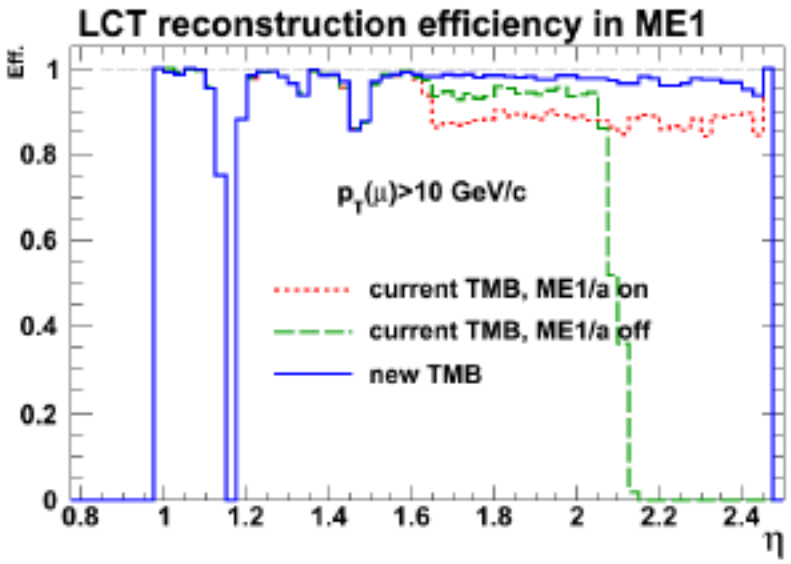
- LHC is still down… just cosmics for now
- Collect data using an ME1/1 chamber with new electronics
  - The data saved contains all the raw inputs to the trigger
- Run the TMB Trigger Emulator on raw cosmic ray data
  - Software based trigger emulation
  - Takes the same inputs used in the TMB trigger decision
  - Enables detailed comparison of trigger primitives including reconstructed positions, stub parameters, quality, etc.
  - Validation of trigger results with the emulator is an ultimate test of performance
- We see perfect agreement in the trigger emulator
  - The OTMB is working exactly as expected

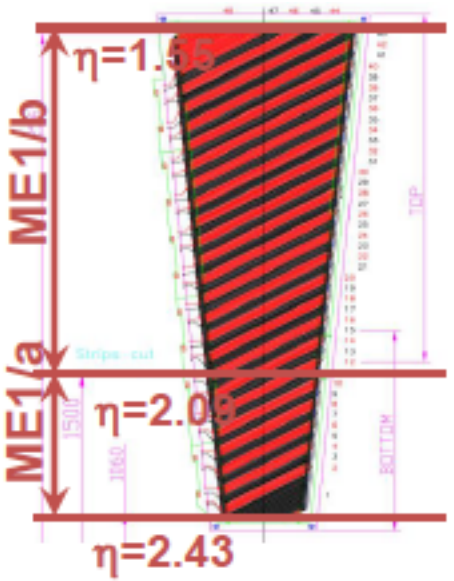




Ongoing efforts : CSC Trigger Optimization

- Improvements in CSC trigger efficiency due to unganging the strips at high-eta ME1/1 part:

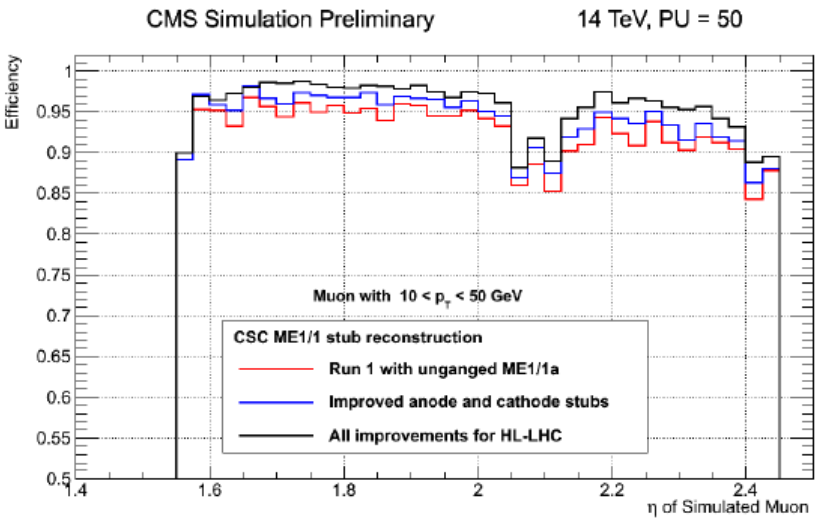


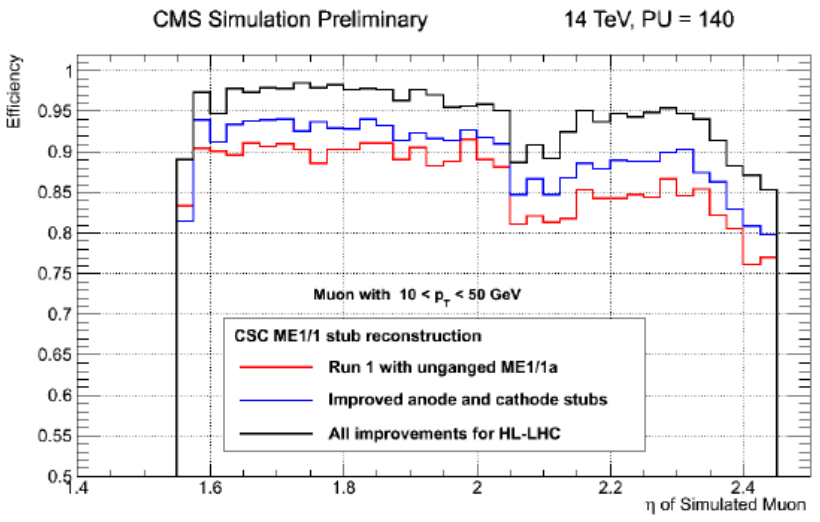


- Additional improvements expected by changing OTMB trigger algorithm:
  - Improved ghost cancellation for anode track stubs
  - Improved handling of dead-time for cathode stubs
  - Optimized matching for anode + cathode combination

OTMB Trigger Improvements

- Projected effect on CSC efficiency for different levels of algorithm optimization
  - Already we see significant impact at PU=50.

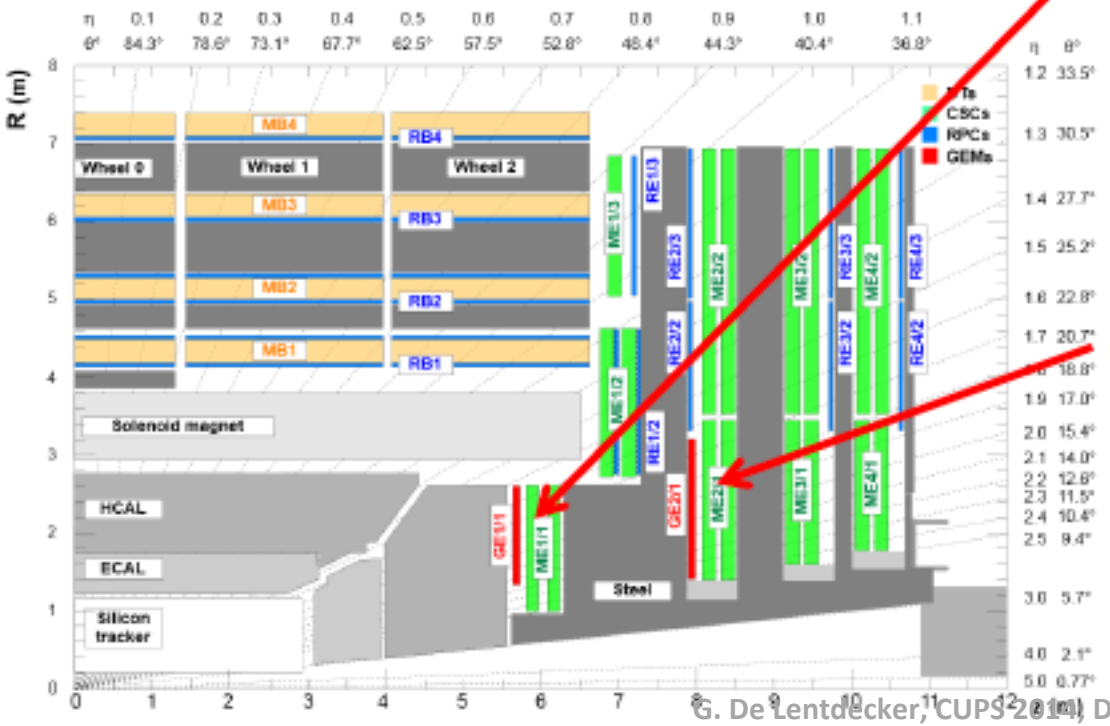




  - The expected impact of the new algorithm at PU=140 is substantial

LS2 and beyond: integration of GEMs

- Triple-GEM detectors to be installed during LS2 (and possibly LS3)
  - Redundancy to CSC system in the very forward region, where especially high trigger rates are expected at HL-LHC
- Possible to treat GEM + CSC as combined system
  - Allows for an integrated “8 layer” trigger

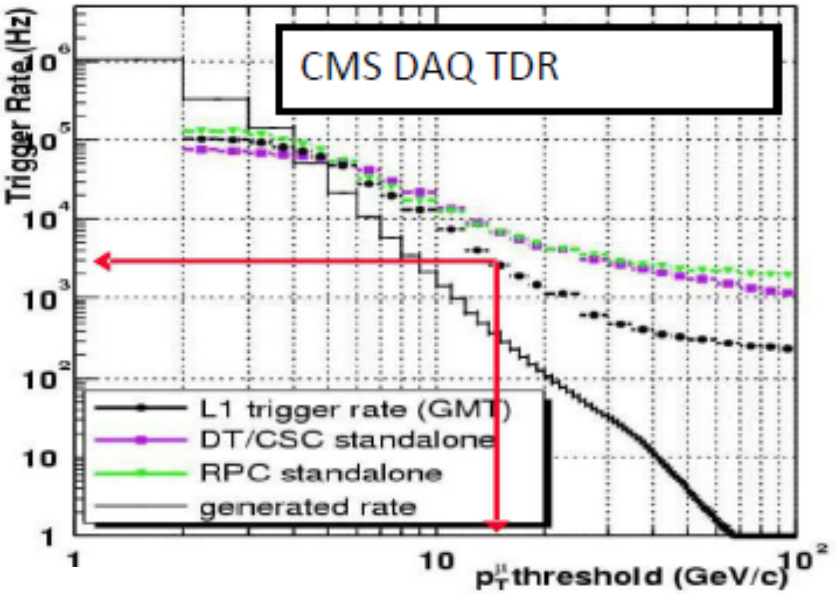


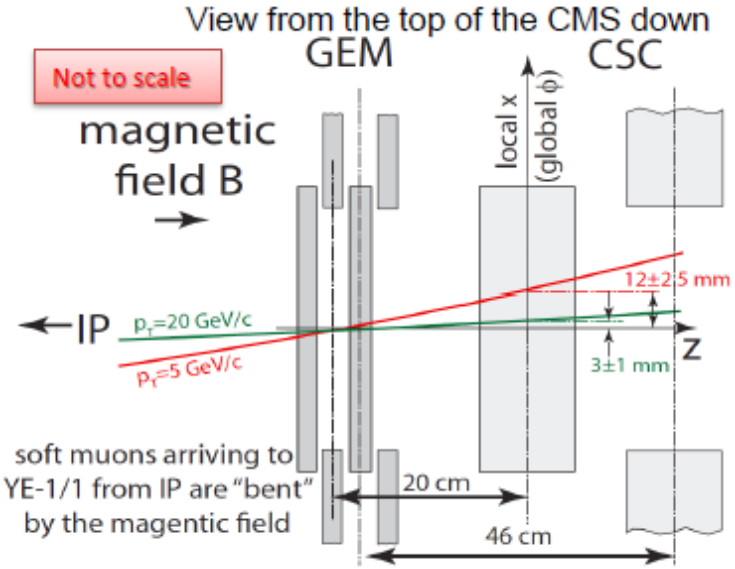
GE1/1 GEM GE1/1 detector planned for LS2 CMS upgrade period (2018)

GE2/1 Possible installation of a second GEM station (GE2/1) for LS3 CMS upgrade period

Impact of GE1/1 on L1 muon Trigger

- Scattering of soft muons in the iron yoke flattens the trigger rate curve
  - Promotion of low-p_T muon to high-p_T
- Additional muons stations can help to reduce the trigger rate
- Efficiency of single muon trigger at 20 GeV is about 85% in high η region

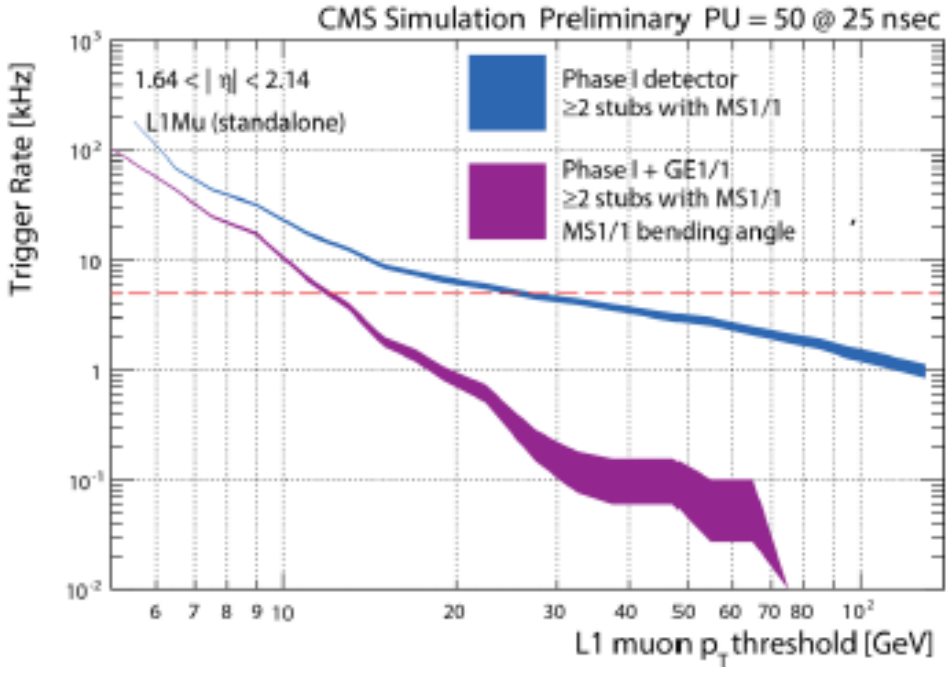


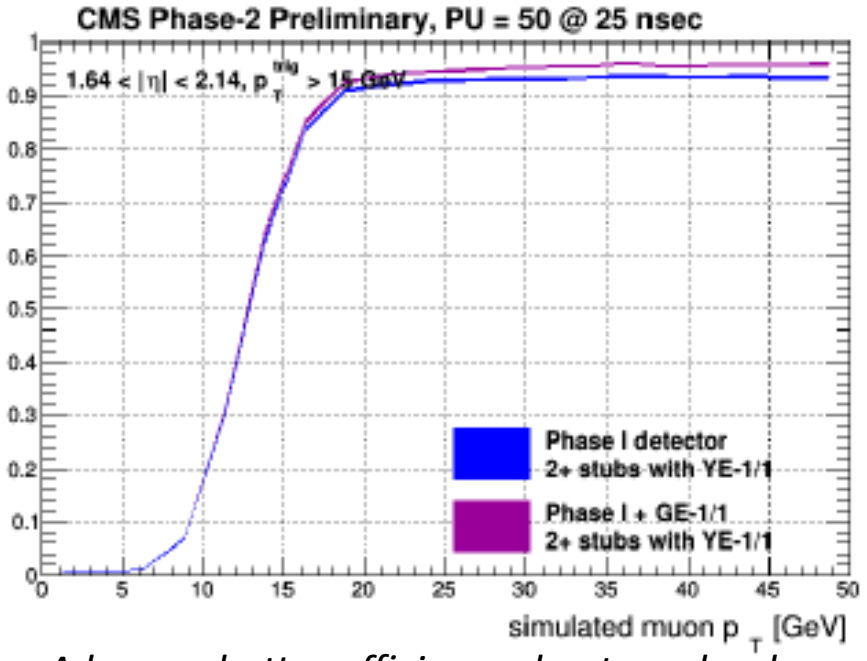


- With additional GEM detector in front of ME1/1 one can measure muon bending angle in magnetic field.
- By letting the GEM and CSC **talk to each other** we get a powerful new tool
  - **Rate reduction with GEM-CSC bending angle**

  Typical trigger rate reduction for 20GeV muon: **20kHz/cm² to 2kHz/cm²**
  - **Stub efficiency recovery in ME1/1 CSC TMB**

GEM + CSC as an “integrated detector”

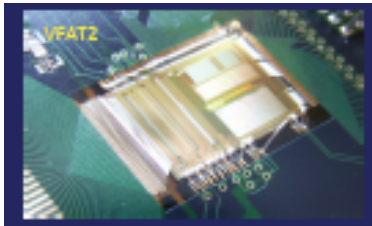


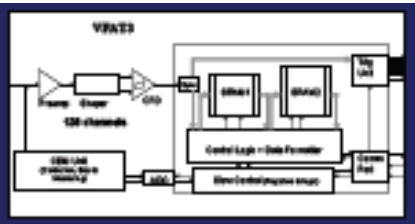


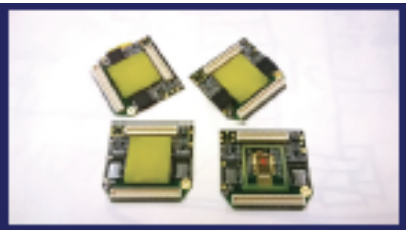
A bonus: better efficiency due to redundancy

Bending angle : dramatic improvement in trigger rate

GEM Electronics in a nutshell





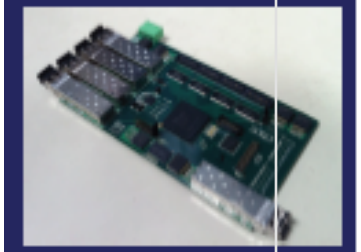


VFAT3 front-end ASIC development

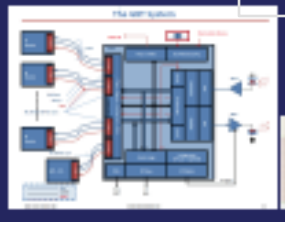
MP7

GEM Electronic Board (GEB)

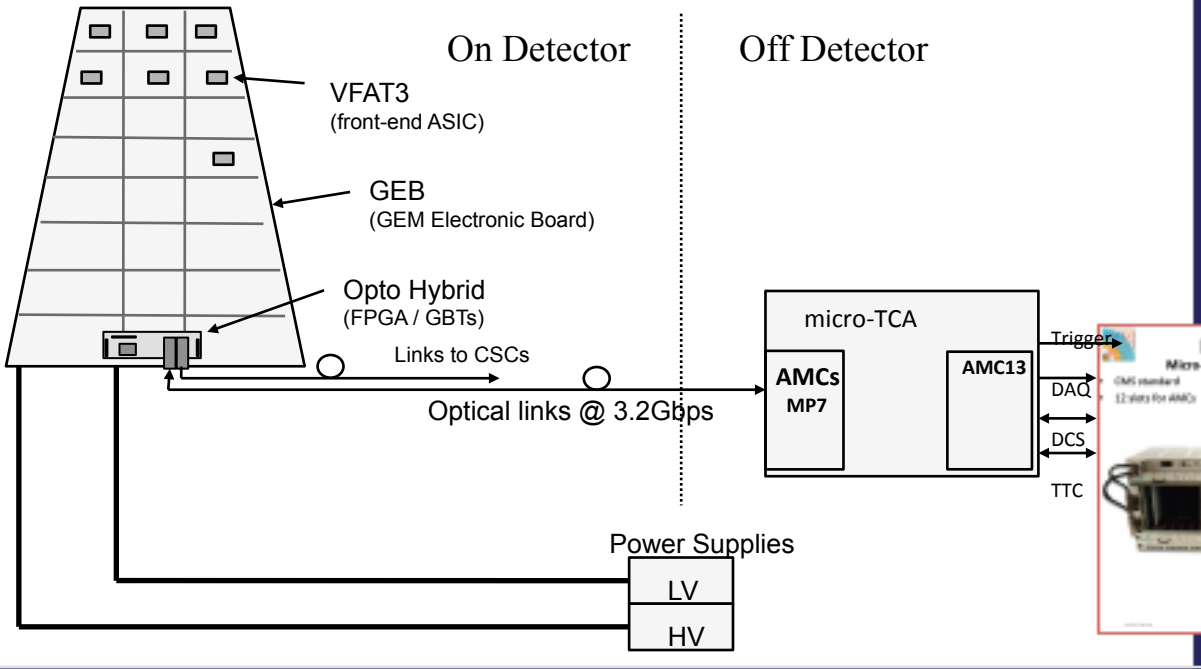
Opto-Hybrid (OH)



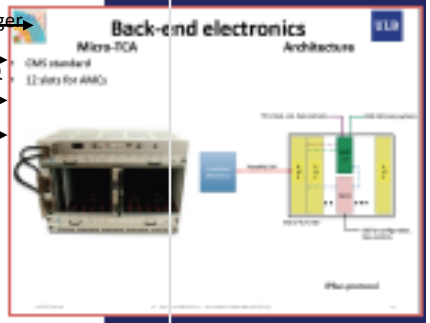
GBT



Versatile Link



µTCA
AMC13, MCH



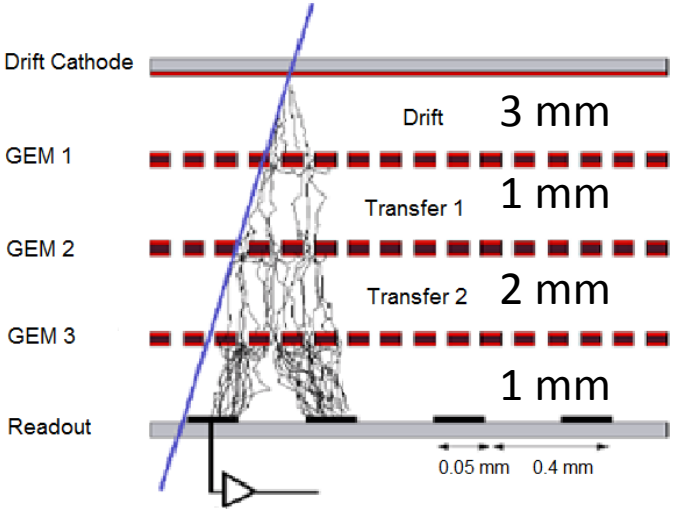
Use of many common developments such as GBT, Versatile Link, µTCA backend

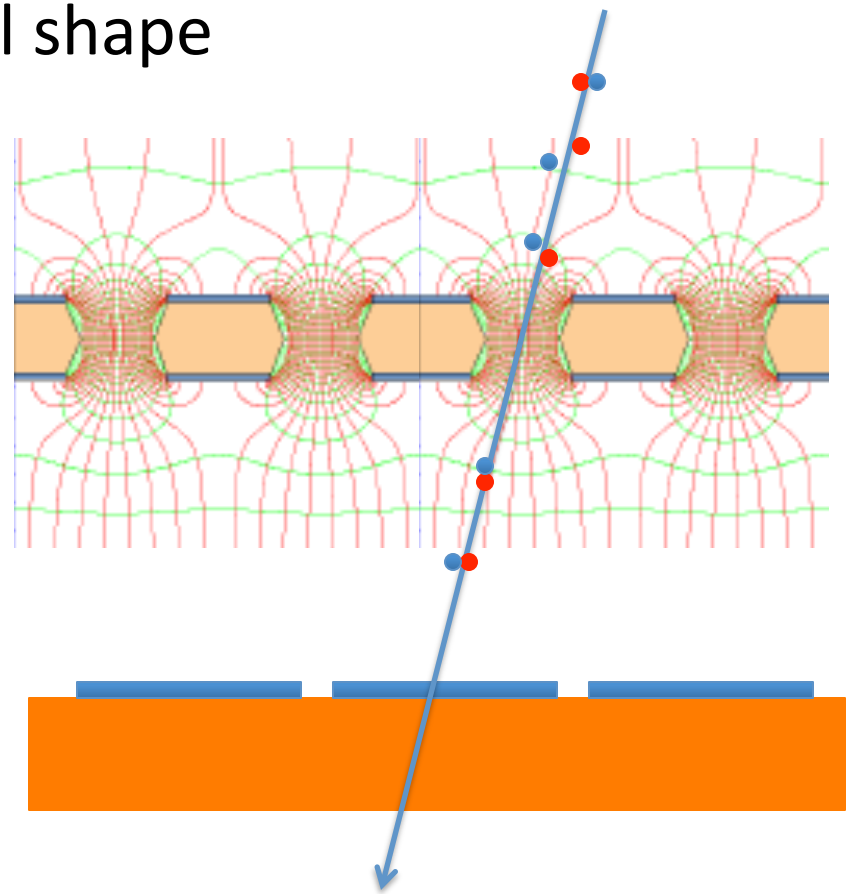
LS2 : GE1/1 Installation
LS3: GE2/1 and ME0

Courtesy of P. Aspell

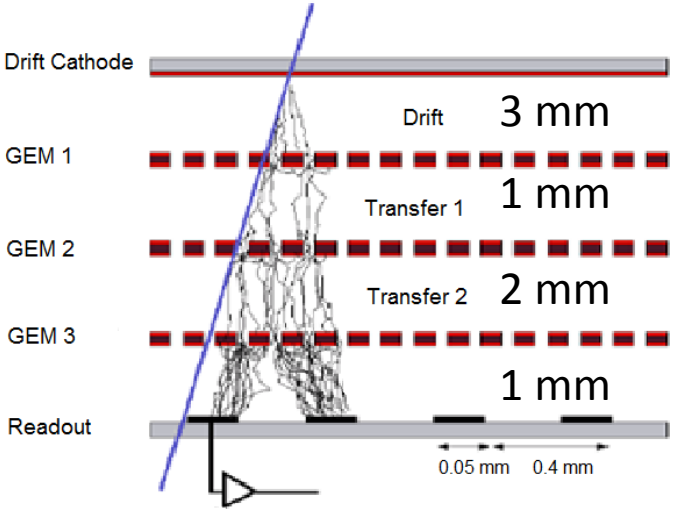
Signal in Triple-GEM detectors

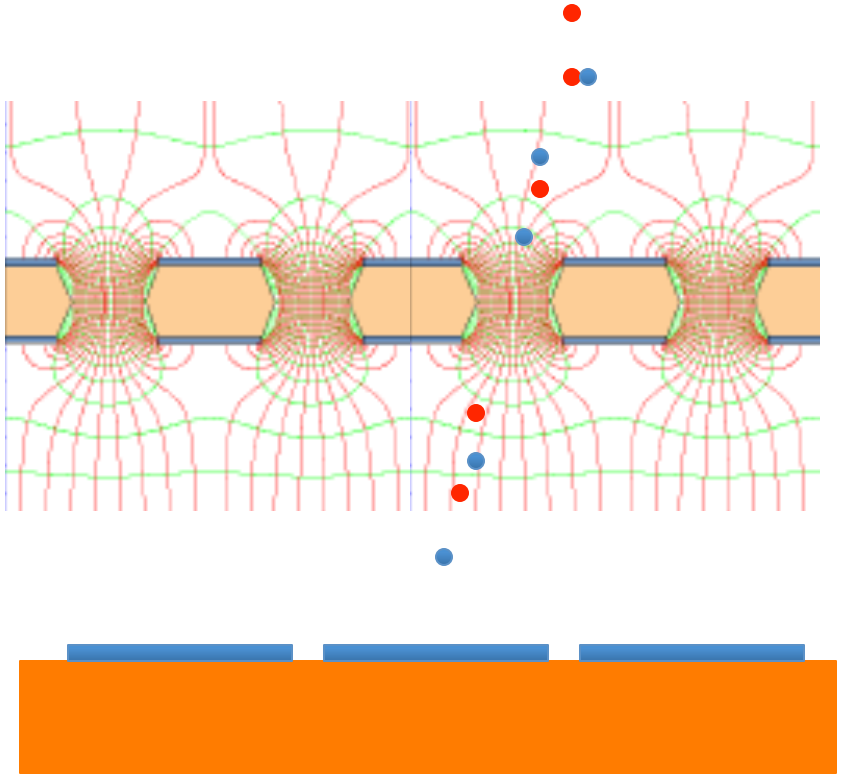
- Before designing a new FE ASIC, it is important to understand the detector signal shape



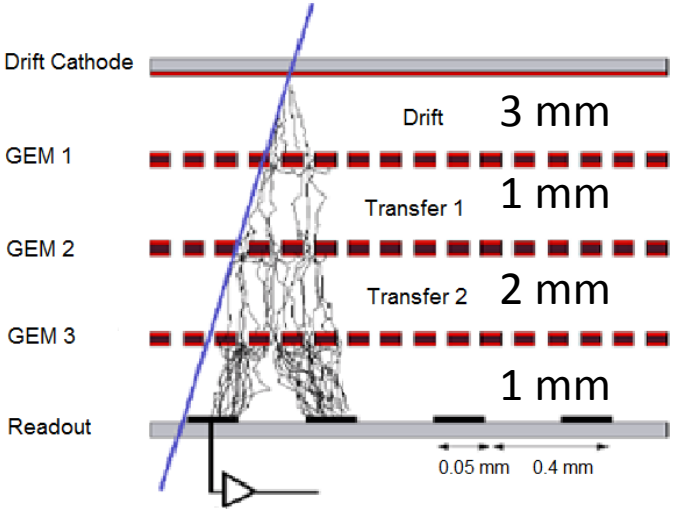


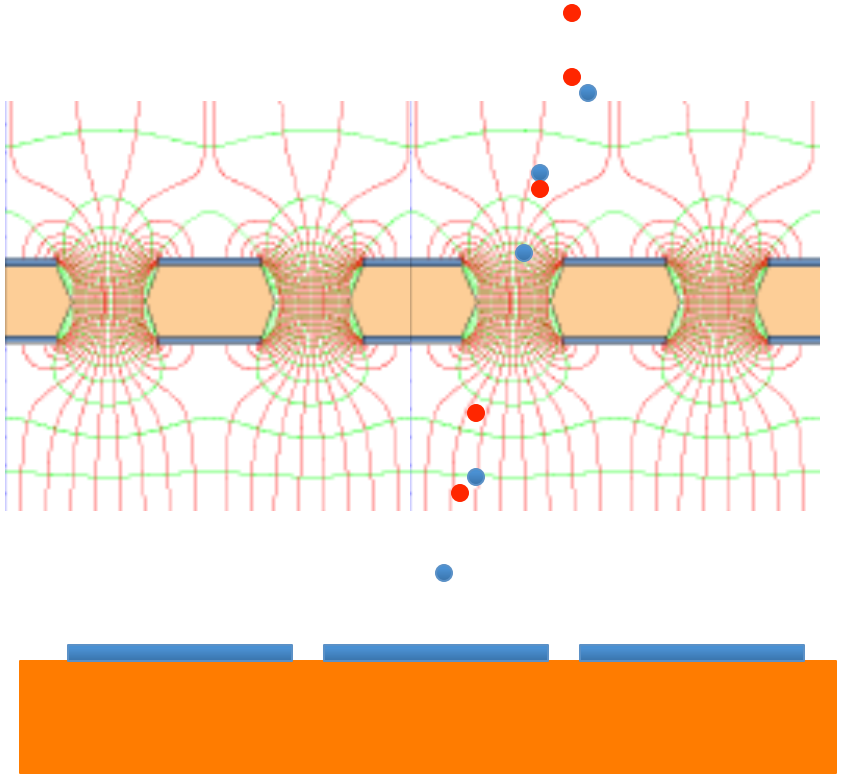
Signal in Triple-GEM detectors



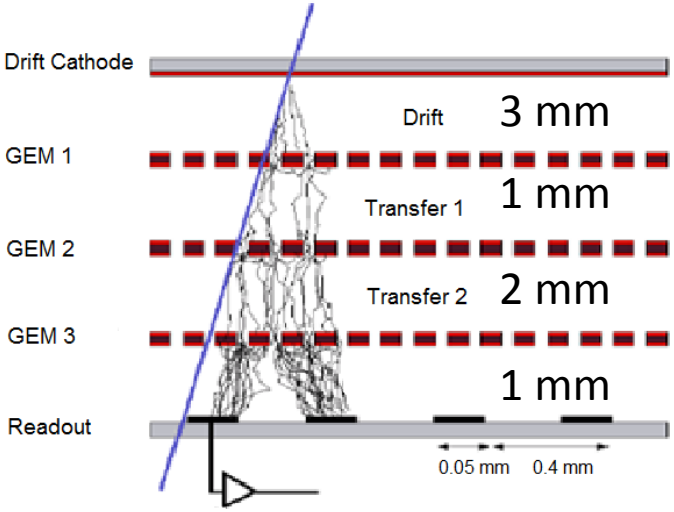


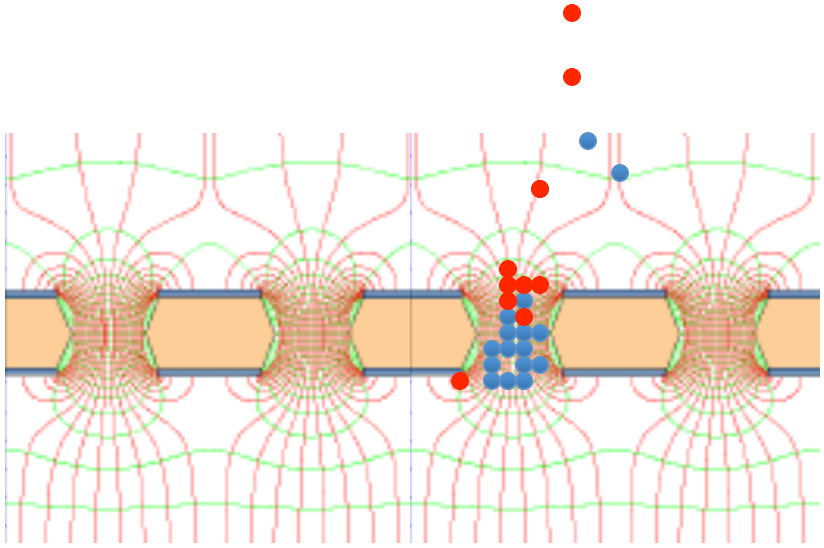
Signal in Triple-GEM detectors



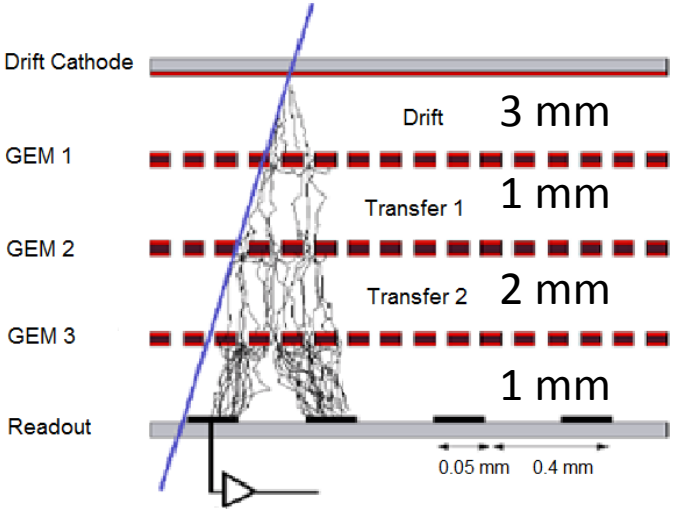


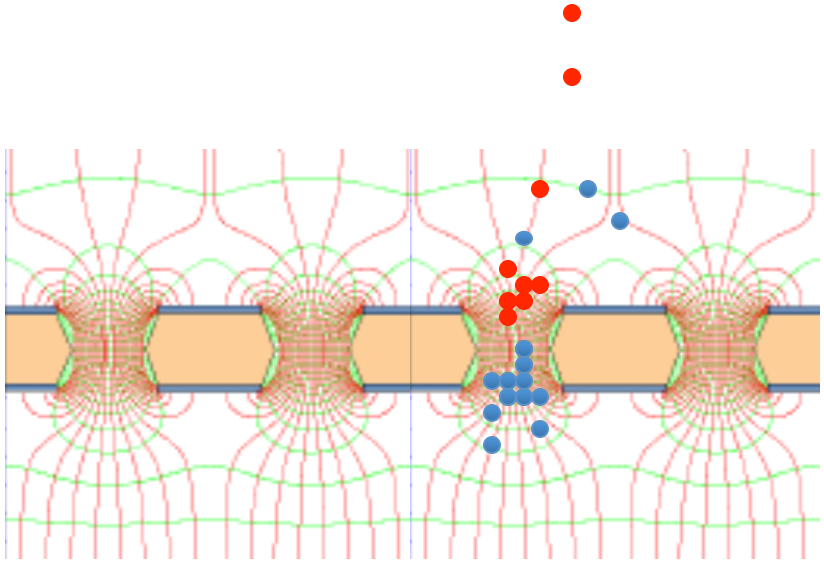
Signal in Triple-GEM detectors

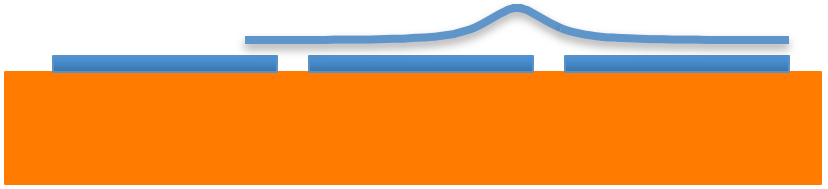




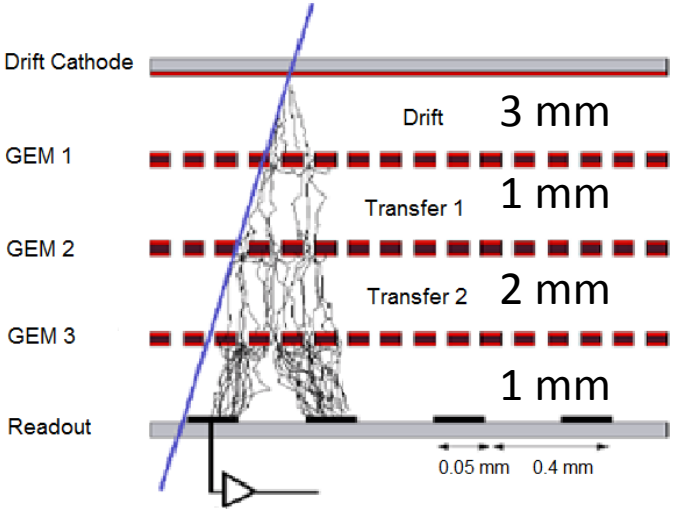
Signal in Triple-GEM detectors

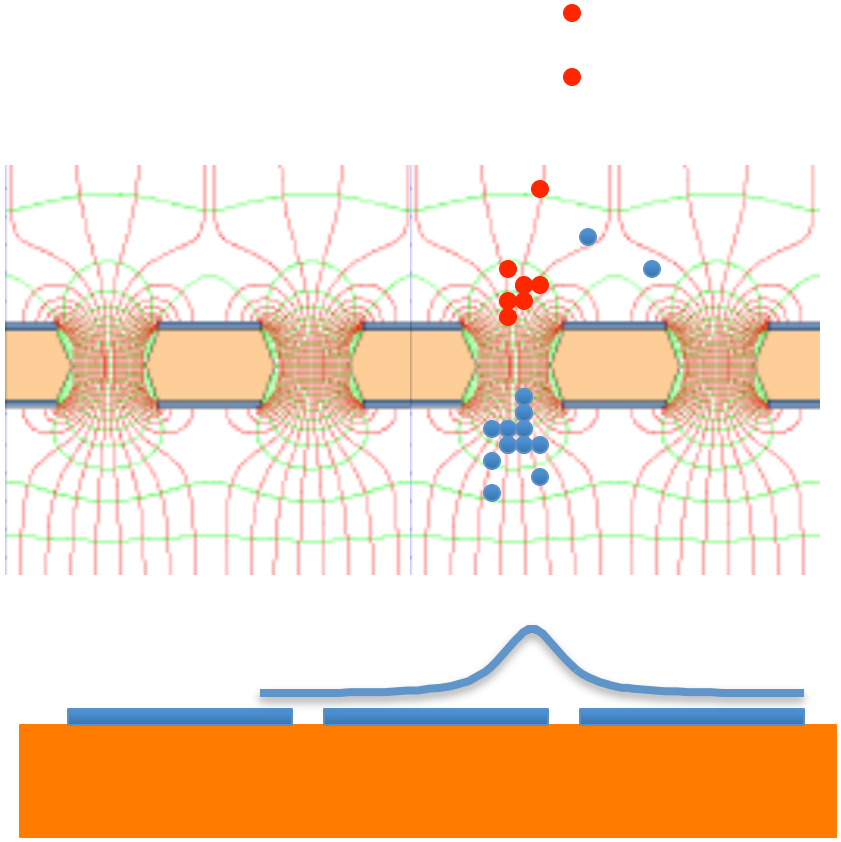




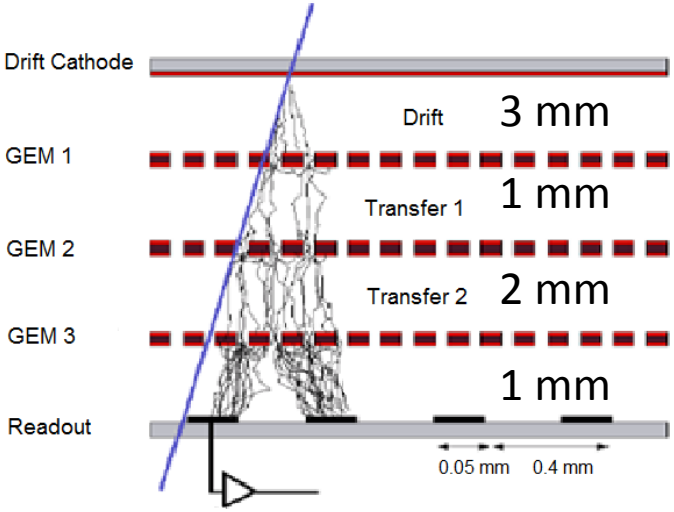


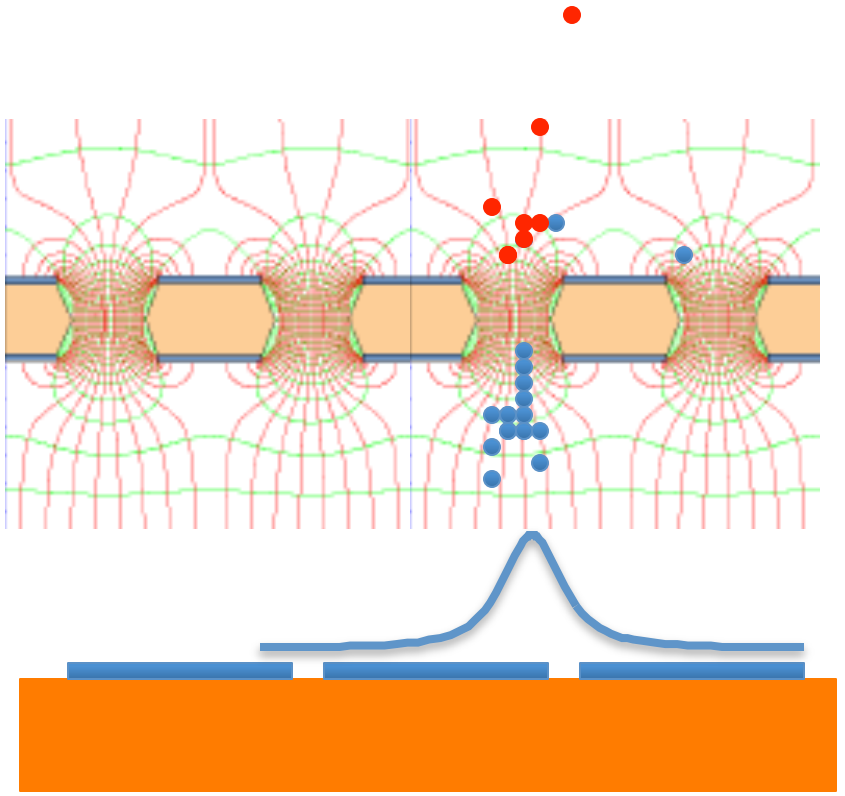
Signal in Triple-GEM detectors



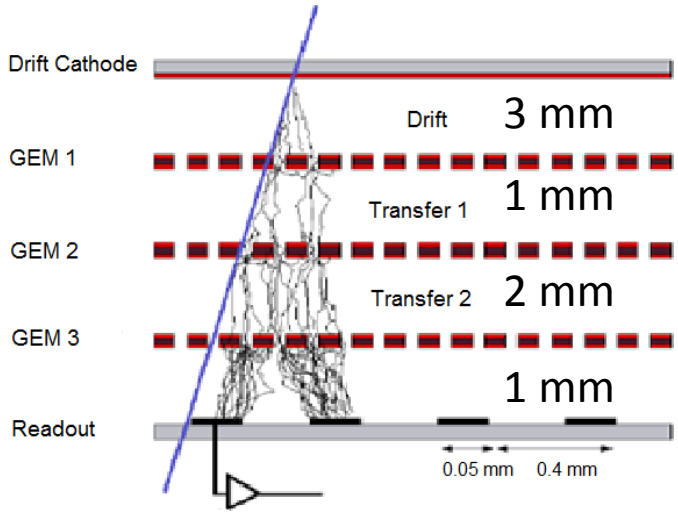


Signal in Triple-GEM detectors



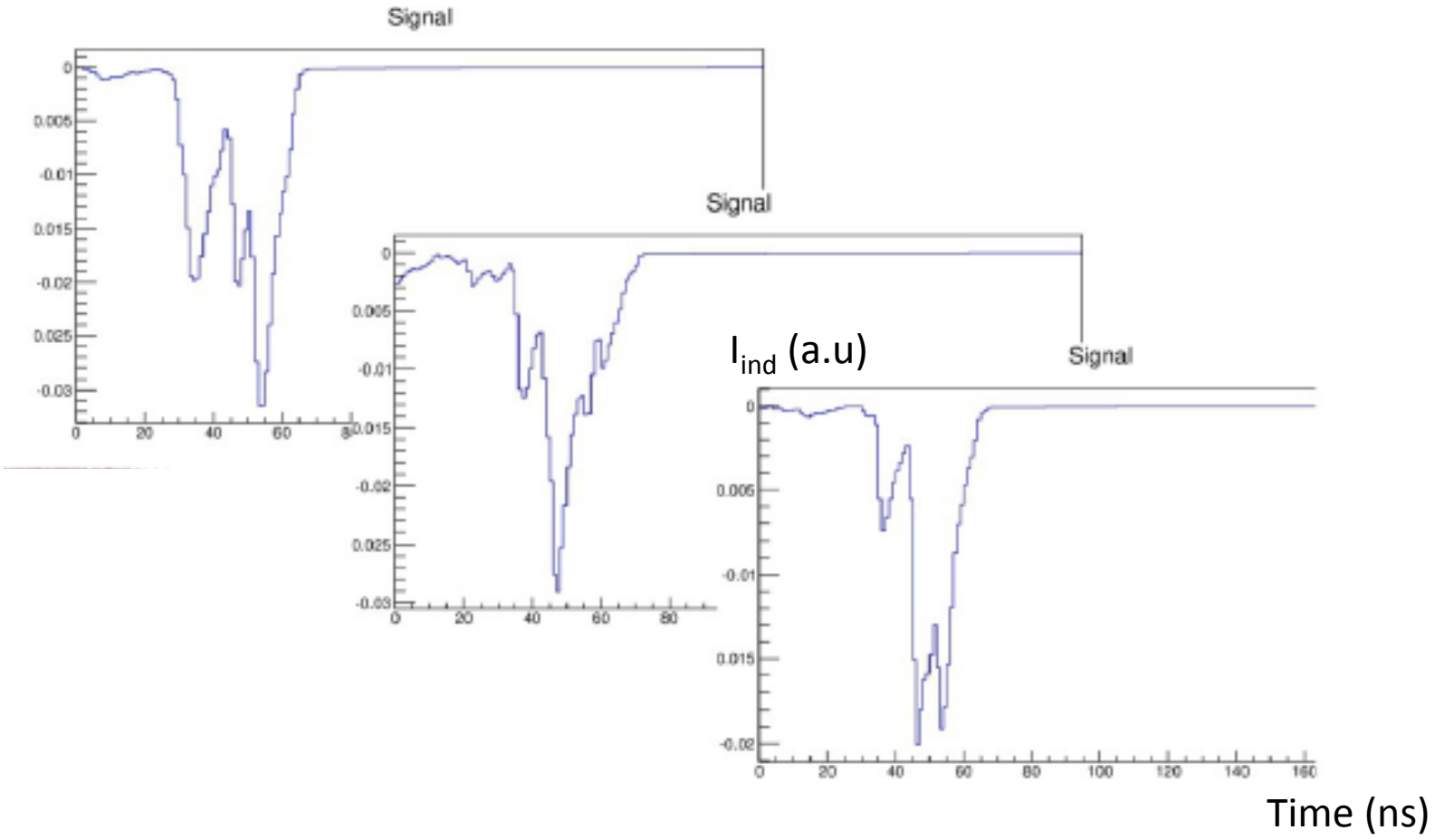


Signal in Triple-GEM



- Only the signal induced by electrons drifting in the induction gas is « seen » by the electronics
  - Fast signal (it takes ~10 ns to drift of 1mm)
- All electrons produced from ionisation in the drift gap takes max 60 ns to reach the induction gap
- Primary electrons are spread randomly over the whole length of the detector
  - Most important electrons for the signal are the one released in the drift gap

With realistic primary ionisation

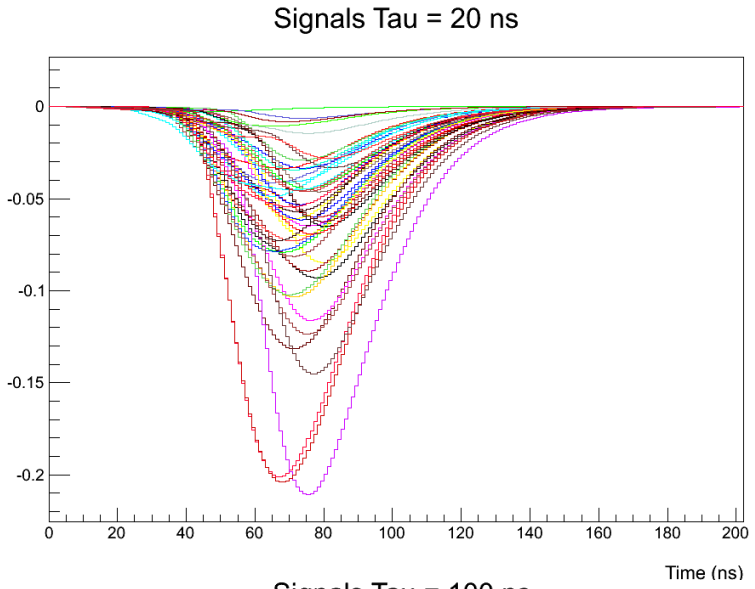


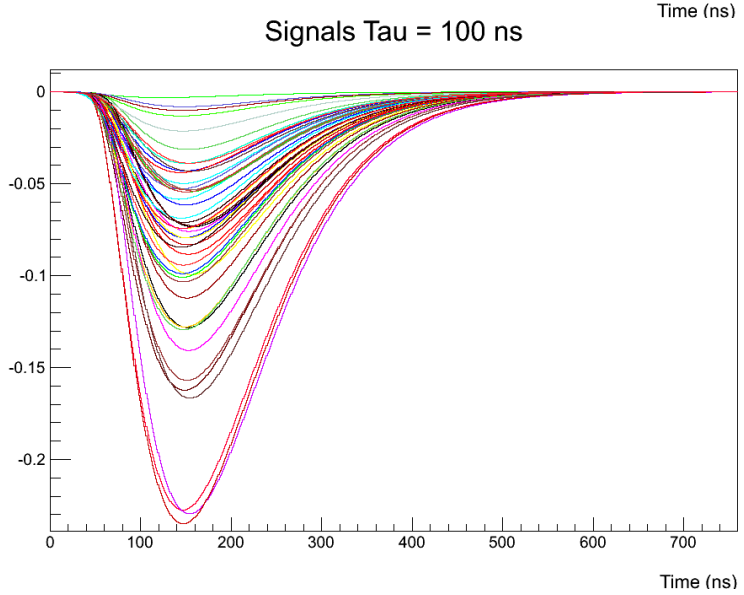
Effect of the shaping time

- Electronics response:

$$f(t) = \left(\frac{t}{\tau}\right)^n \exp(-\frac{nt}{\tau})$$

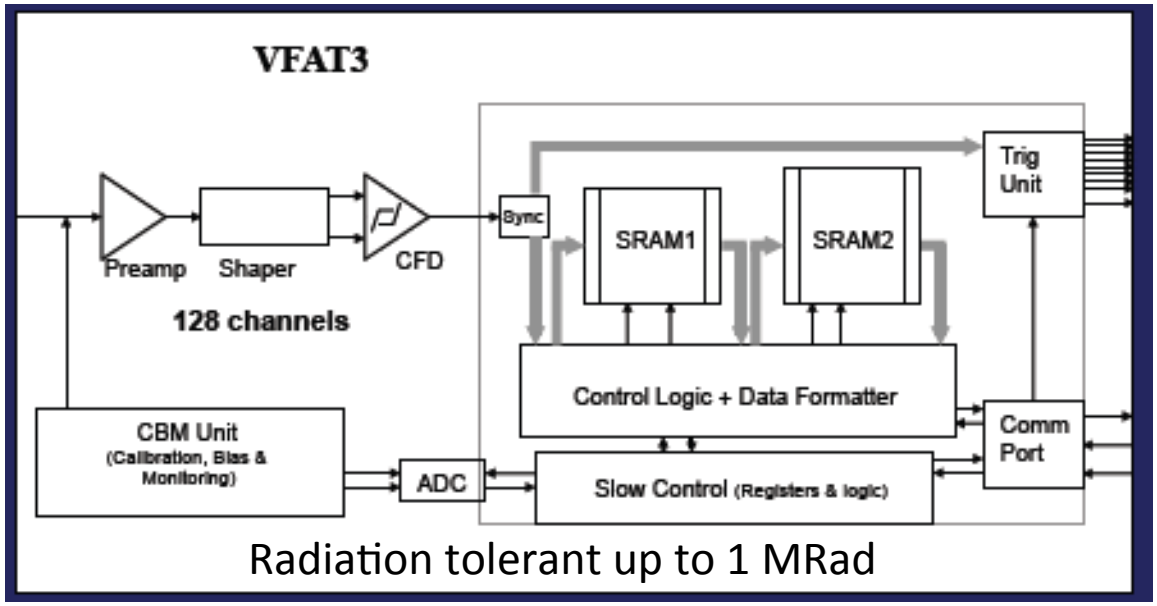
$$n = 2$$





VFAT3

- Evolution of the VFAT2 chip (used with GEM in TOTEM)



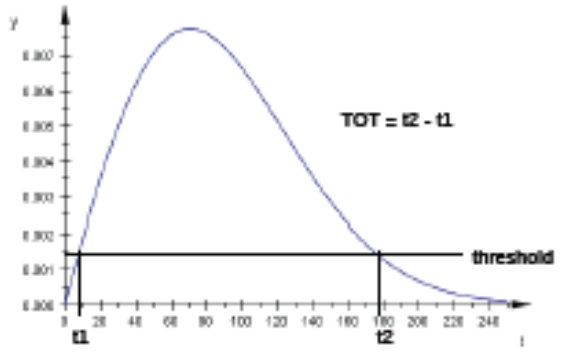
Trigger data: provide fast OR data with fixed latency & synchronous with LHC clock

Tracking data: provide full granularity data upon L1A signal

	VFAT2	VFAT3
Trigger granularity	16 strips	2 strips
Shaping time	25 ns, fixed	Programmable (25, 50, 100, 200 ns)
Data output rate	Limited to 40 MHz	320 Mbps e-link, comaptible with GBT
Max. L1 latency	6.4 us	20 us
Max L1A rate	200 kHz	1 MHz

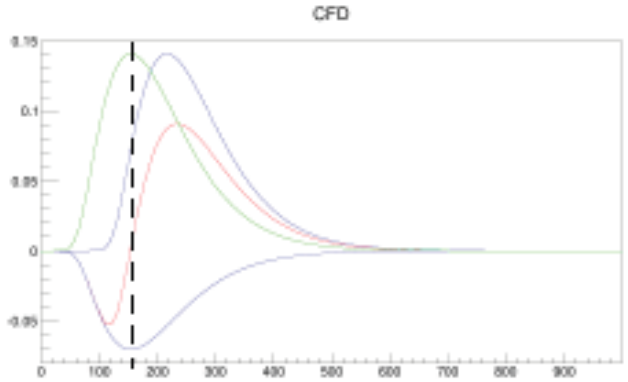
Time resolution

Time Over Threshold (TOT)



TOT → # clock cycles → Look Up Table (LUT) → T1
Compare T1 from LUT to real T1 of the signal

Constant Fraction Discriminator



The zero crossing and the signal maximum occur at the same time.

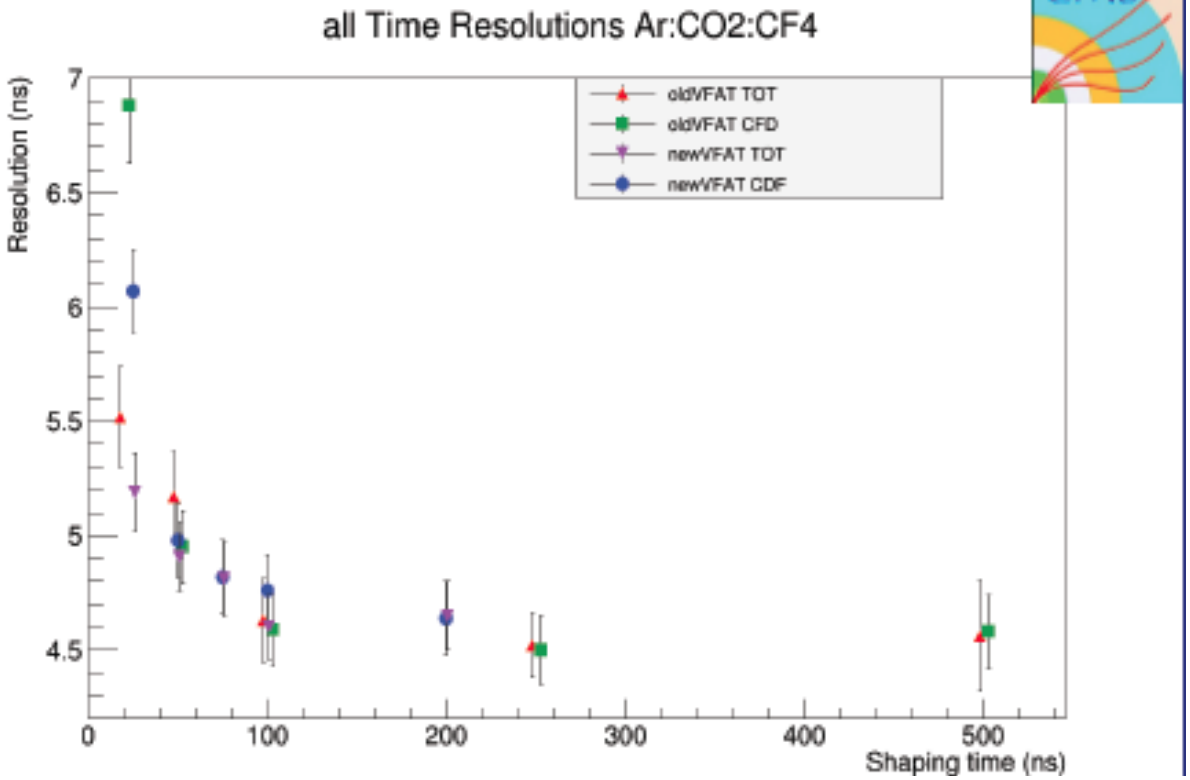
Comparison of TOT (Time Over Threshold) and CFD (Constant Fraction Discriminator) techniques:

Goal : Allow long shaping times to boost S/N by reducing ballistic deficit and at the same time retain good timing resolution.

TOT maintains timing resolution by correcting time walk through a LUT (look up table).

CFD corrects time walk internally in the comparator.

Time resolution



Th. Maerschalk

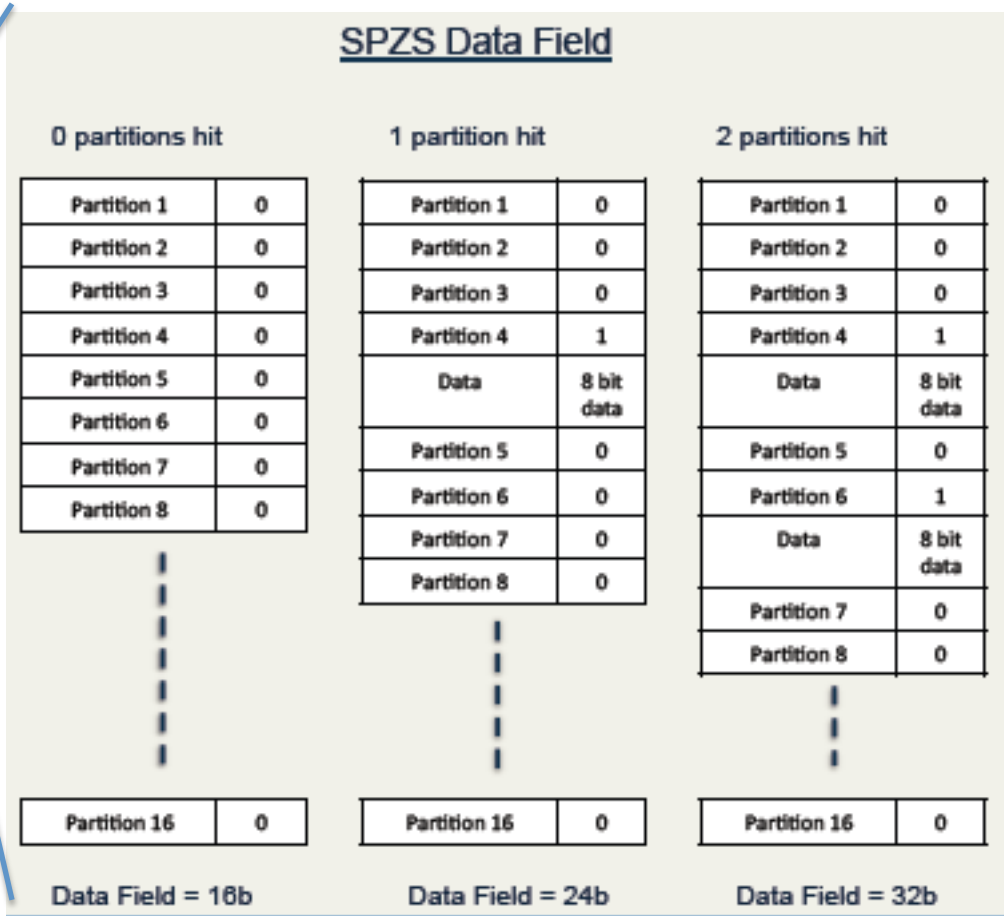
- *Both TOT and CFD methods provides good timing resolution*
- *TOT takes more latency and requires a LUT → requires more resource on chip*
- *CFD has been chosen*
- *Note : longer shaping time means boosted S/N ratio (less balistic deficit)*

VFAT3 data format

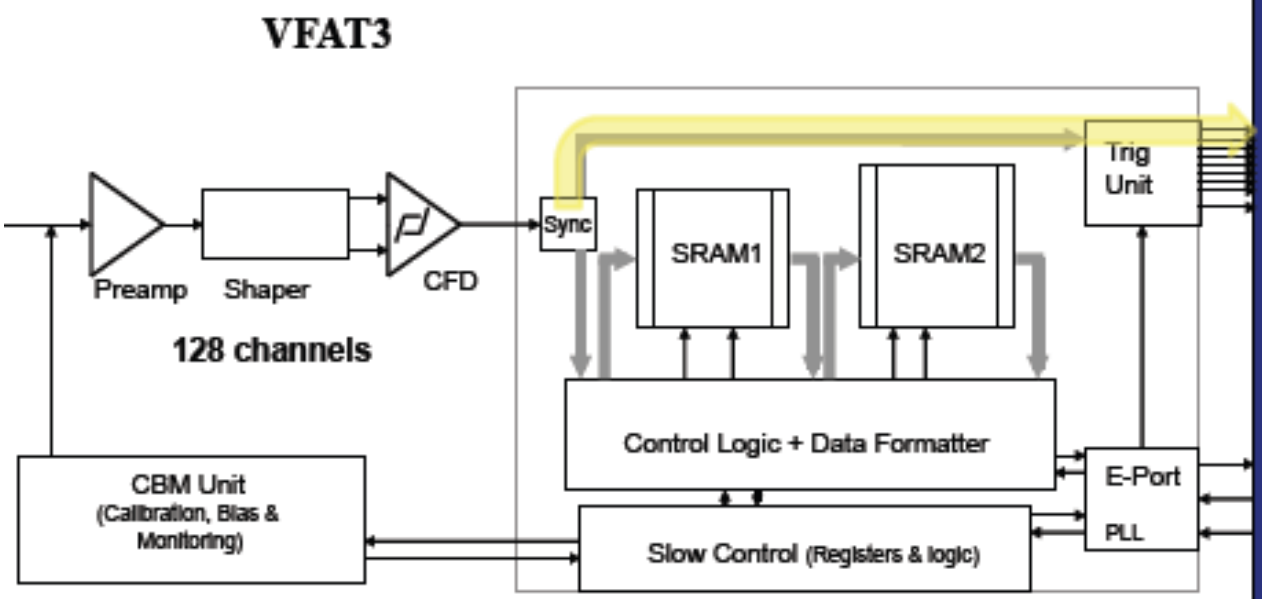
- Sequential Partial Zero Suppression
  - 128 channels divided in 16 partitions of 8 strips
  - A variation on the RPC data format

Data Packet	No. Bits
Header I / Header IW	*8*
EC+BC / EC / BC	*8 - 48*
Data	*16 - 144*
CRC	*16*

16 bits in total for partition identification
8 bits per partition



Fixed latency trigger part



Trigger path = 8 LVDS pairs @ 320Mbps

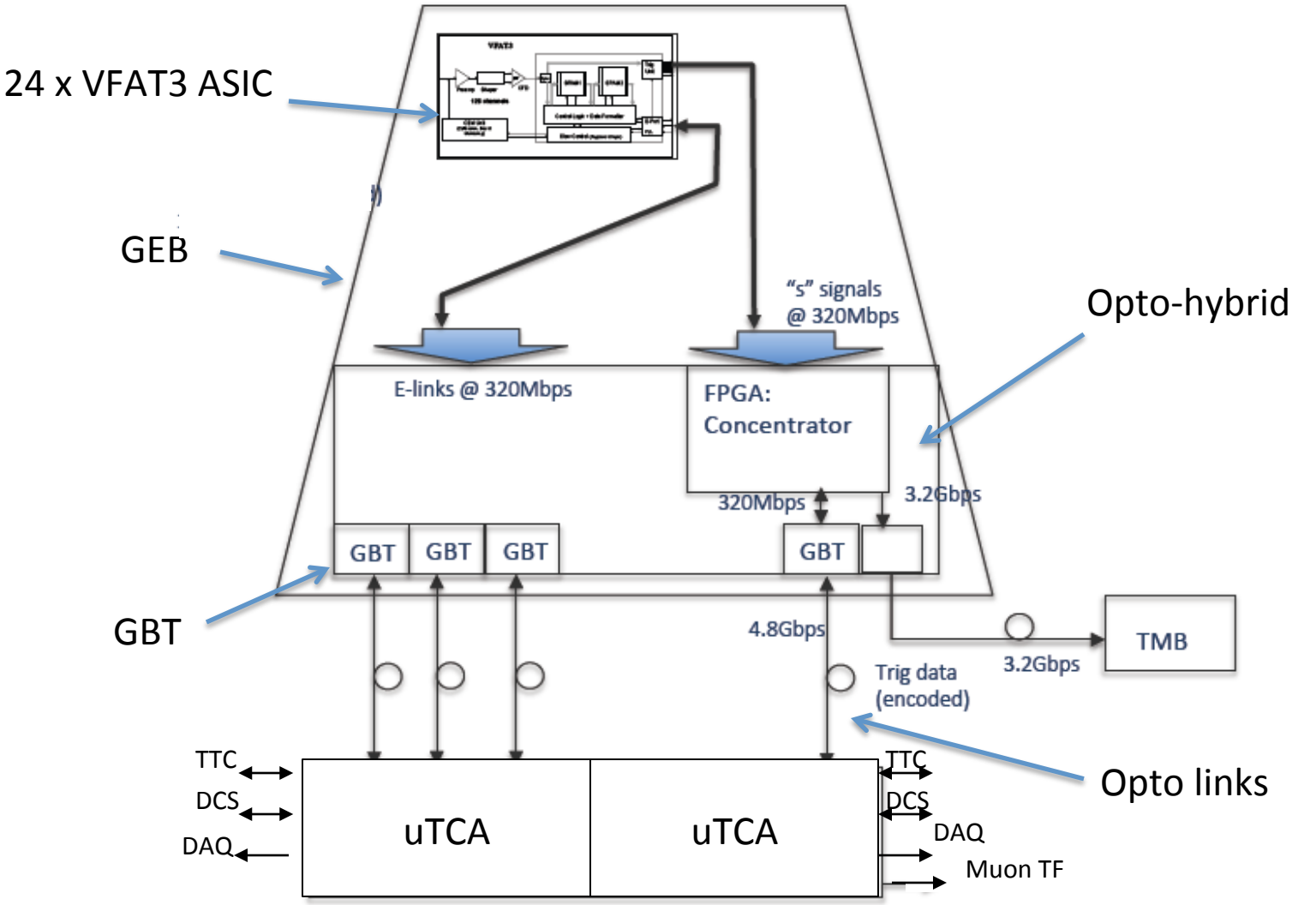
Therefore 64 bits/bx

Fast OR :
Each pair of channels

SPZS:
Up to 6 partitions / bx

DDR :
Able to transmit 128 bits/bx hence full granularity.

The GE1/1 electronics

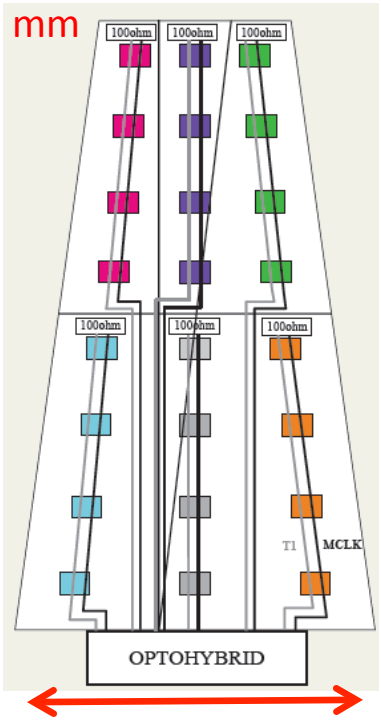


GEB & Opto-hybrid

- GEB board
  - GEM Electronics Board: large PCB to avoid cables along GEM
  - Plugged on the GEM readout board
  - Strips segmented in 8η x 3ϕ partitions, each readout by 1 VFAT
- Opto-hybrid (OH)

Board equipped with concentrator FPGA, collecting signals from all VFATs and handling the optical links

Long=234.1 mm
Short=234.1 mm

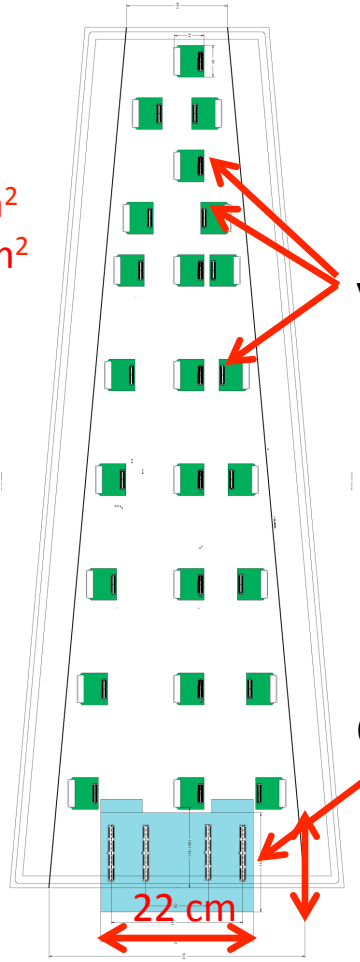


Area Long=4.11 10^5 mm^2
Area Short=3.47 10^5 mm^2

Long=1209 mm
Short=1060.844 mm

Long=445.858 mm
Short=419.934 mm

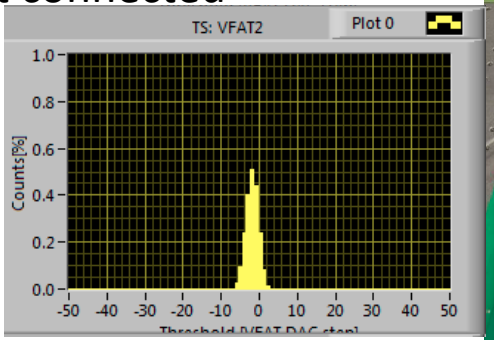
GE1/1 GEB
Not at scale

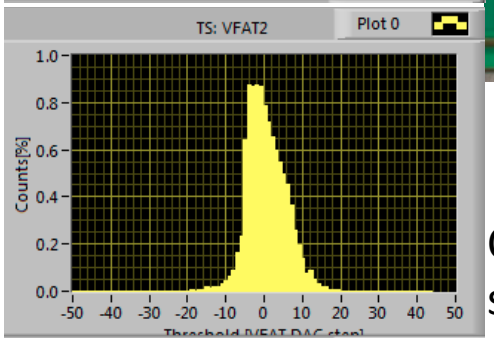


GEB & Opto-hybrid

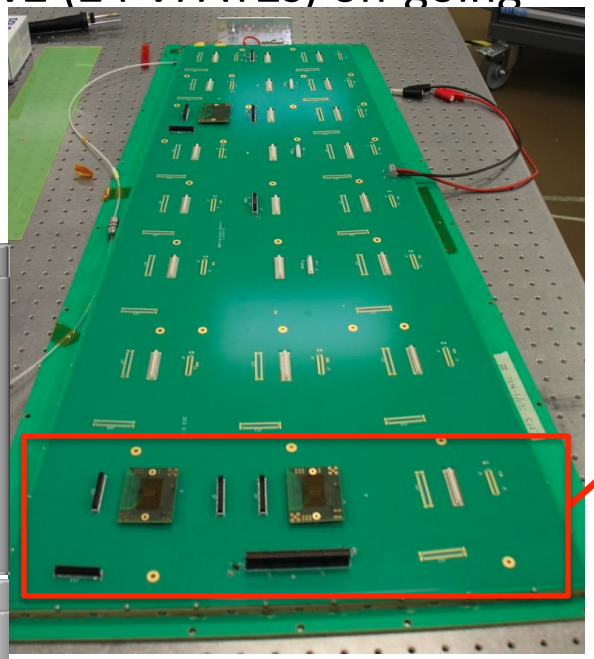
- GEB and Opto-hybrid v1 (6 VFAT2) available since beginning of 2014
  - Signal integrity at 40 MHz ☑
- Design of GEB-Long v2 (24 VFAT2s) done, production on-going
- Design of Opto-hybrid v2 (24 VFAT2s) on-going

New VFAT2 hybrid
not connected

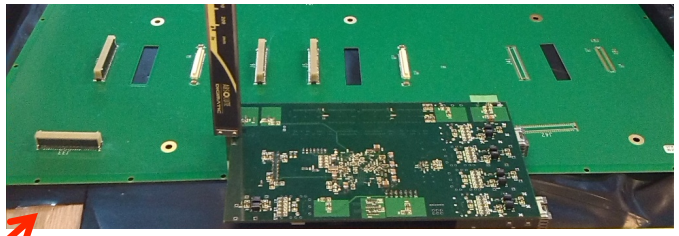


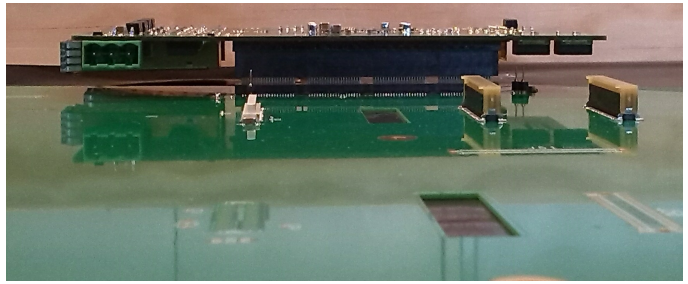


Connected but
strips floating



GEB v1 & OH v1



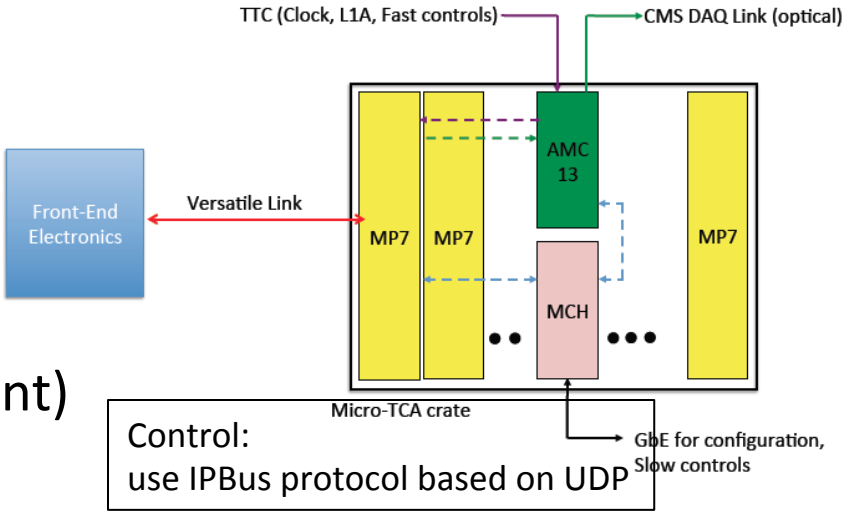


Future version of the OH

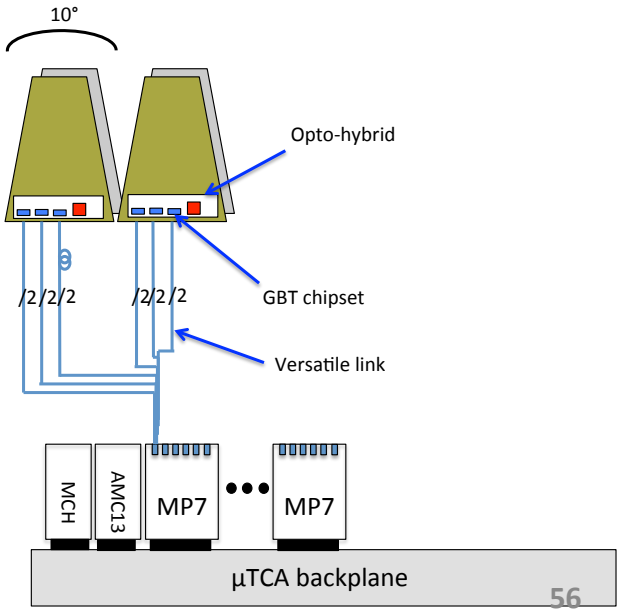
- Constraints on the opto-hybrid
  - Need to be connected to all VFAT3s to collect trigger data and sent them to μ-TCA back-end electronics & CSC TMB→FPGA
  - 4 optical links: 4 GBT chipset + 1 to CSC TMB (~~GBT~~)
  - Space : 22 x 14 cm^2 x 1.9 cm
  - Power: targeting ~ 15 W
  - Number of lines : ~ 400 I/Os
  - Radiation environment
    - →need to implement SEU mitigation techniques
    - →Will perform irradiation tests
  - → Aiming for largest Artix 7 (500 I/Os)

Backend electronics

- Optohybrid-µTCA optical link: versatile link and GBT protocol
- µTCA crate:



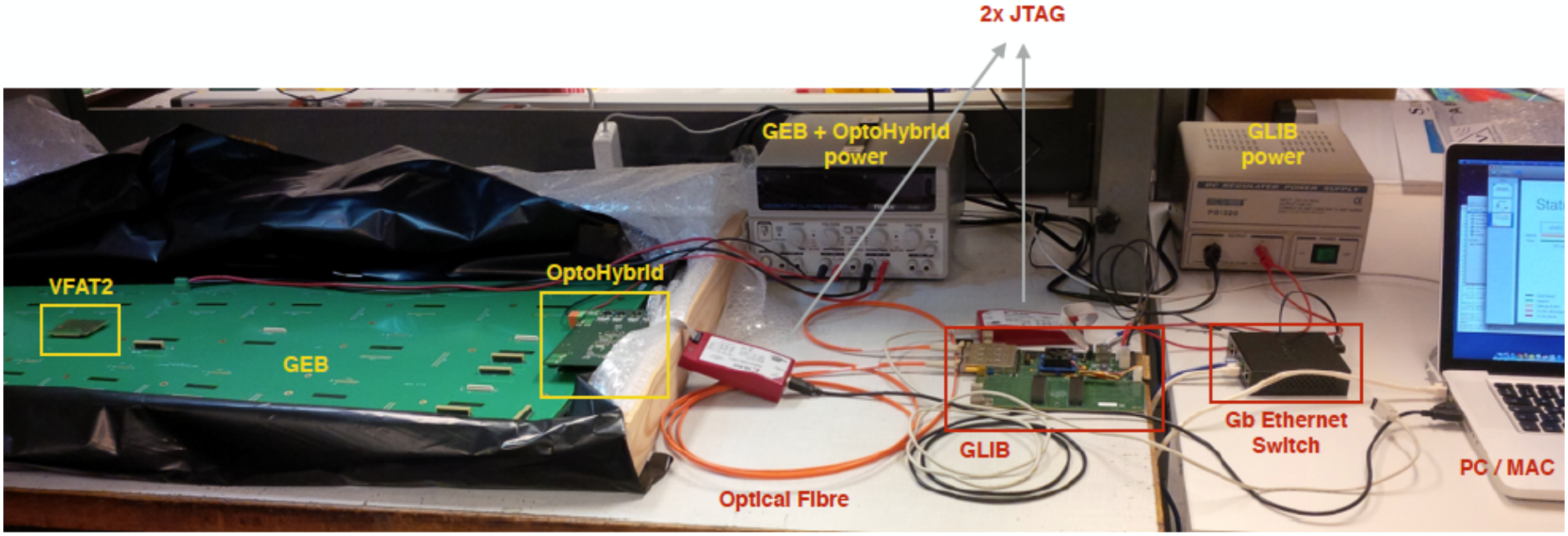
- AMC boards in crate:
  - MP7 boards (GLIB for development)
  - 1 AMC13
- µTCA crate: Vadatech VT892



- *MP7 boards*
  - *72 optical input + 72 optical output*
- *3 MP7s to readout 1 GE1/1 endcap*

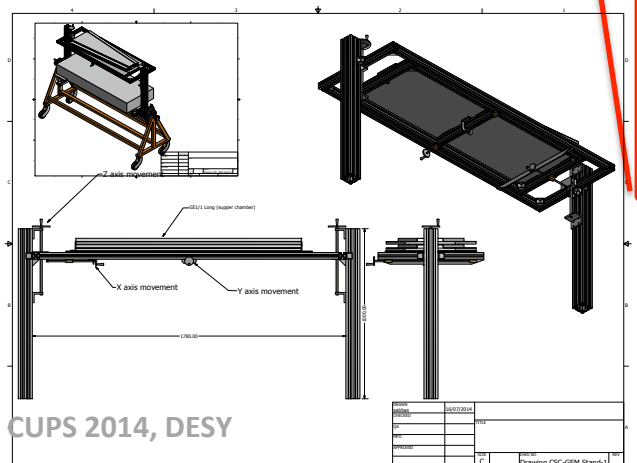
1st DAQ prototype

- VFAT – OH – GLIB communication working (also through µTCA)
  - OH FPGA recovering clock from optical link
  - Use IPBus protocol for control
- + separate test bench for GBT testing (with µTCA crate)



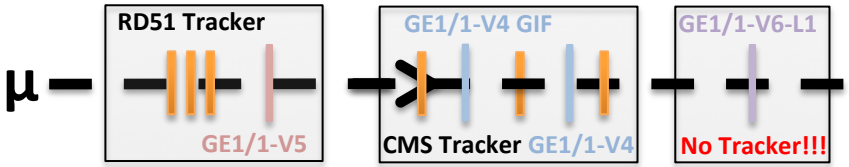
Integration with CSC has started

- Goal : Slice test readiness
  - CSC-GEM Trigger integration
  - CSC-GEM synchronization
  - plus integration of AMC13
- Electronics work started on Sept 1st.
- test-bench for GE1/1 completed



Next step: test beam

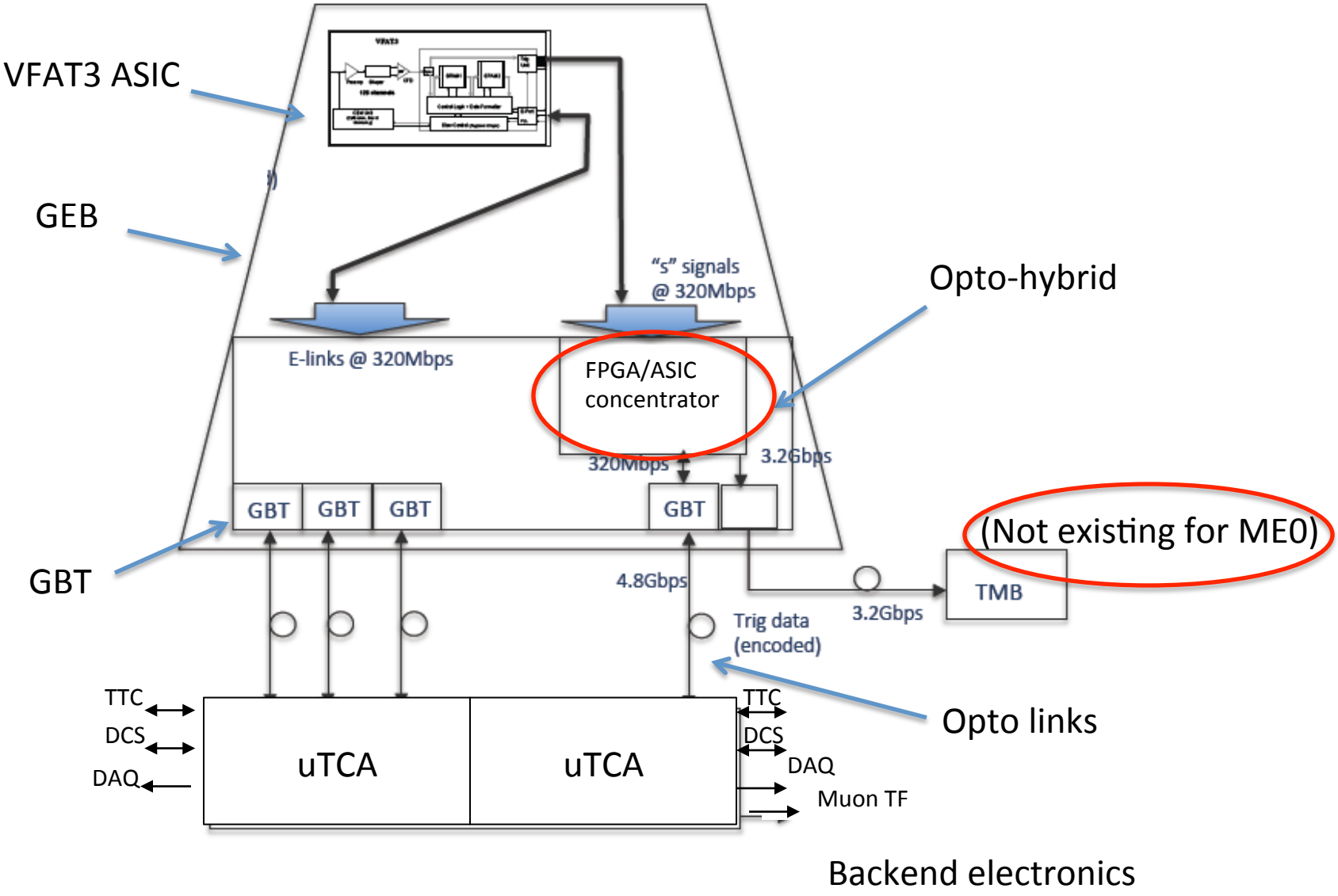
- H4 Test Beam w/Magnet
- Nov 26th – Dec 15th



- Timing sensitive performance measurements with **B**=0
- Study impact of radiation dose on performance
- Test of version two of GEM electronics

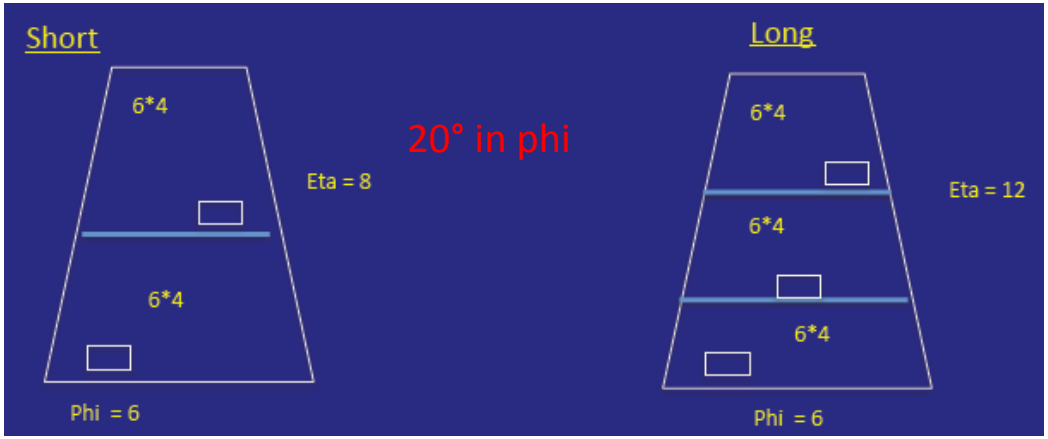
- First data taking with new GEM electronics !

GE2/1 and ME0

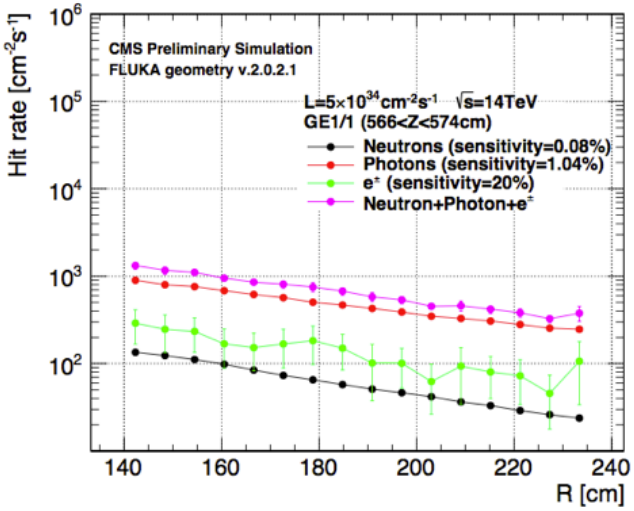

VFAT3 ASIC
GEB
"s" signals
@ 320Mbps
Opto-hybrid
E-links @ 320Mbps
FPGA/ASIC
concentrator
320Mbps
3.2Gbps
GBT
GBT
GBT
GBT
GBT
(Not existing for ME0)
4.8Gbps
TMB
3.2Gbps
Trig data
(encoded)
TTC
DCS
DAQ
uTCA
uTCA
TTC
DCS
DAQ
Muon TF
Opto links
Backend electronics

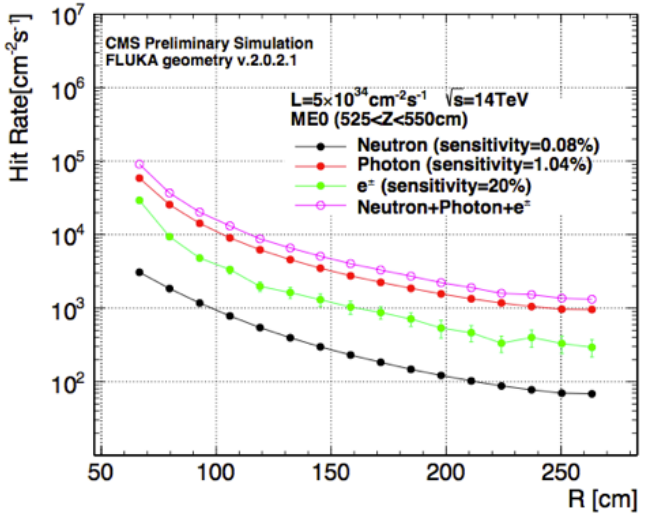
GE2/1 and ME0 system considerations

- GE2/1 Long= 1816mm > manufacturer capability
  - Investigating segmentation of GEB board :



- ME0 will be exposed to rates > 10 x GE1/1 rates
  - Investigating data rates and bandwidth requirements





ME0 tracking and trigger rates

- Probability to hit the optical link bandwidth limit (3.2 Gbps / link):

Trigger	Data rate (Gbps)	Prob with 2 links	Prob with 3 links
Fast OR ZS	2.68	1.34%	0.02%

  - Still investigating other data format
  - Note: optical link bandwidth based on GBT. For LS3, higher speed GBT probably available

Tracking (L1A @ 1MHz)	Data rate (Gbps)	Prob with 1 links	Prob with 3 links
SPZS*	2.15	$<10^{-7}$	$<10^{-7}$

- GE1/1 Probability to hit the optical link bandwidth limit (3.2 Gbps / link):

Trigger	Data rate (Gbps)	Prob with 1 links	Prob with 2 links
Fast OR ZS	0.05	$6\ 10^{-5}$ %	$<10^{-7}$

Conclusions

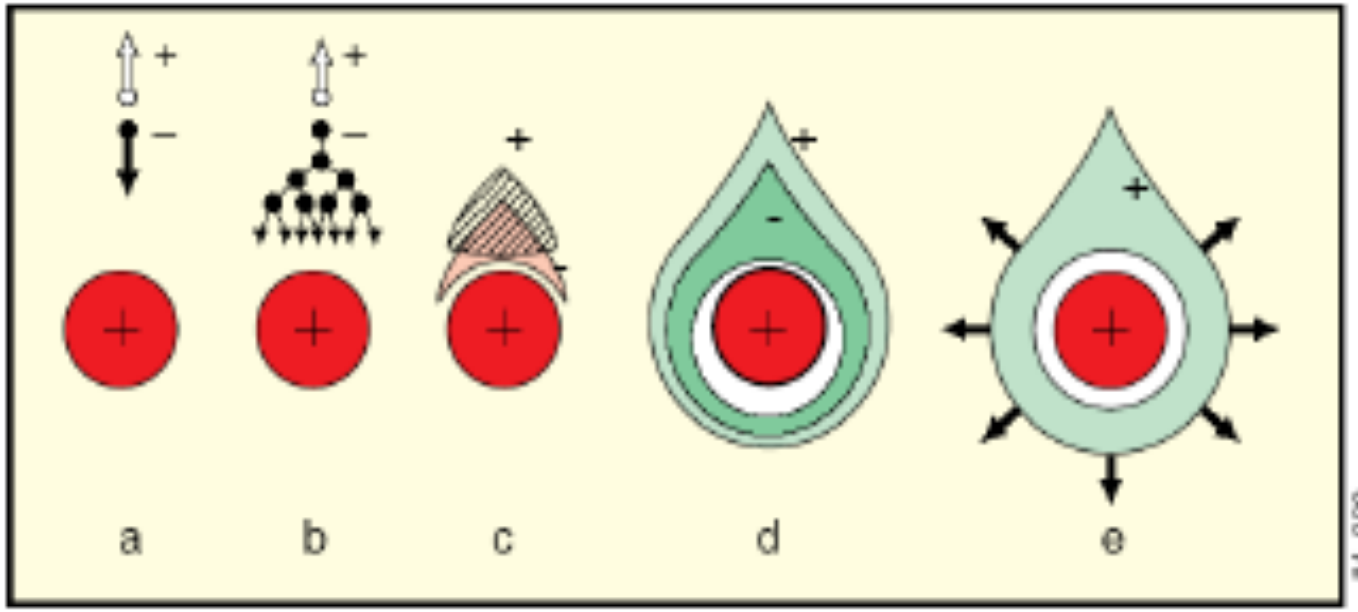
- A lot of work ahead !

- Please, join the effort ;-)

BACK-UP

Reminder on signal formation

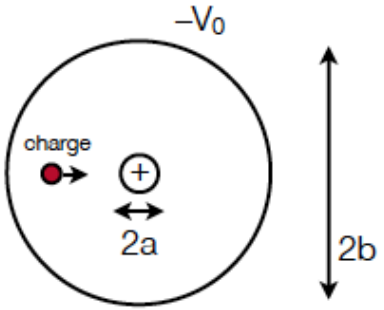
- Back to basics: the single wire proportional counter



Time

Pulse formation and shape

- The signal is formed by induction due to the movement of charges between the electrodes



Electric field:

$$E(r) = \frac{CV_0}{2\pi\epsilon_0}\,\frac{1}{r} \qquad \text{with } C = \frac{2\pi\epsilon_0}{\ln b/a}$$

[Capacity per unit length]

Electric potential:

$$\phi(r) = -\frac{CV_0}{2\pi\epsilon_0}\,\ln\frac{r}{a}$$

Consider charge q:
[Assume fast charge movement ...]

No compensation by power supply

$$dW = q\,\frac{d\phi(r)}{dr}\,dr$$ change in potential energy

$$dW = l\,CV_0\,dV$$ electrostatic energy

$$\rightarrow \quad q\,\frac{d\phi(r)}{dr}\,dr = l\,CV_0\,dV$$

$$dV = \frac{q}{lCV_0}\,\frac{d\phi(r)}{dr}\,dr$$

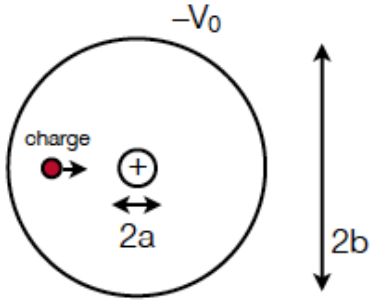
from: $W = {}^1/_2\,l\,CV_0^2$
[Capacity: lC !]

Integrate ...

Pulse formation and shape

Integrate ...

$$dV = \frac{q}{lCV_0}\frac{d\phi(r)}{dr}dr \qquad \text{with} \quad \phi(r) = -\frac{CV_0}{2\pi\epsilon_0}\ln\frac{r}{a}$$



Total induced voltage for electrons:

$$V^- = -\frac{q}{lCV_0}\int_{a+r'}^{a}\frac{d\phi(r)}{dr}dr = -\frac{q}{lCV_0}\left[\frac{CV_0}{2\pi\epsilon_0}\ln\left(\frac{a+r'}{a}\right)\right]$$

$$= -\frac{q}{2\pi\epsilon_0 l}\ln\left(\frac{a+r'}{a}\right)$$

Total induced voltage for ions:

$$V^+ = \frac{q}{lCV_0}\int_{a+r'}^{b}\frac{d\phi(r)}{dr}dr = -\frac{q}{2\pi\epsilon_0 l}\ln\left(\frac{b}{a+r'}\right)$$

Cross check:

$$V = V^+ + V^- = -\frac{q}{lC}$$

$$\text{with } C = \frac{2\pi\epsilon_0}{\ln b/a}$$

Ratio of V^+ and V^-:

$$V^-/V^+ = \frac{\ln(a+r'/a)}{\ln(b/a+r')}$$

With typical numerical values:
a = 10 µm, b = 10 mm, r' = 1 µm

$V^-/V^+ = 0.013$

Signal almost entirely due to ions ...

Pulse formation and shape

Ignoring electron signal
and setting r(0) = a ...

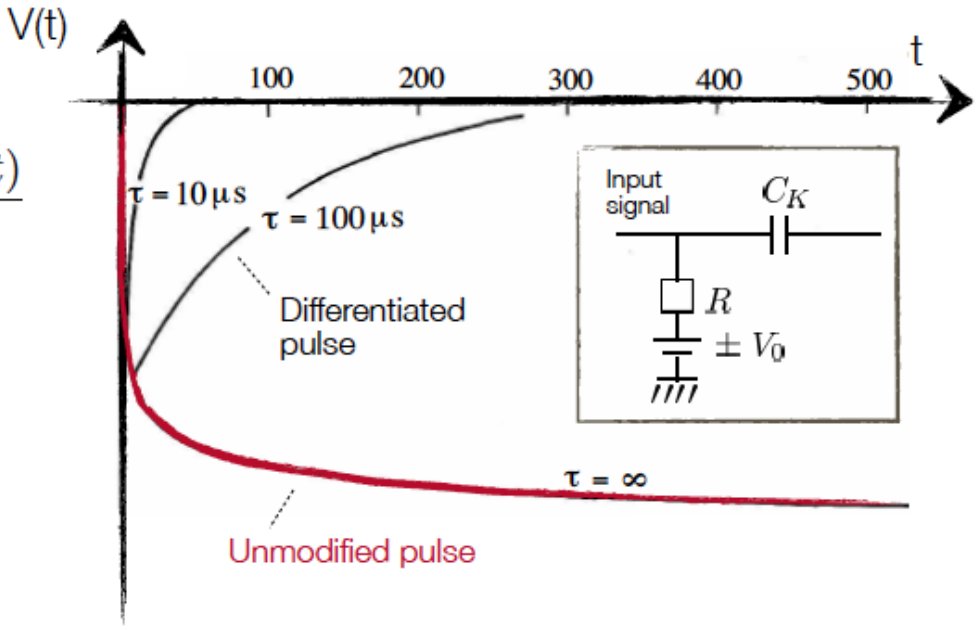
$$V(t) = \int_{r(0)}^{r(t)} \frac{dV}{dr} dr = -\frac{q}{2\pi\epsilon_0 l} \ln \frac{r(t)}{a}$$

Calculation of r(t):

$$v_D = \frac{dr}{dt} = \mu E(r) = \frac{\mu C V_0}{2\pi\epsilon_0} \frac{1}{r}$$

$$r\,dr = \frac{\mu C V_0}{2\pi\epsilon_0} dt$$

$$\rightarrow \quad r(t) = \left(a^2 + \frac{\mu C V_0}{\pi\epsilon_0} t \right)^{1/2}$$



Differentiator:
Measure output voltage across resistor ...

Voltage time dependence:

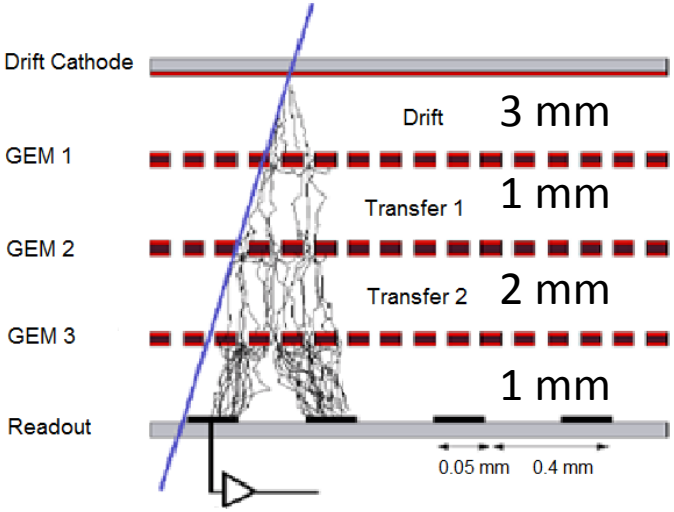
$$V(t) = -\frac{q}{4\pi\epsilon_0 l} \ln \left(1 + \frac{\mu C V_0}{\pi\epsilon_0 a^2} t \right) = -\frac{q}{4\pi\epsilon_0 l} \ln \left(1 + \frac{t}{t_0} \right)$$

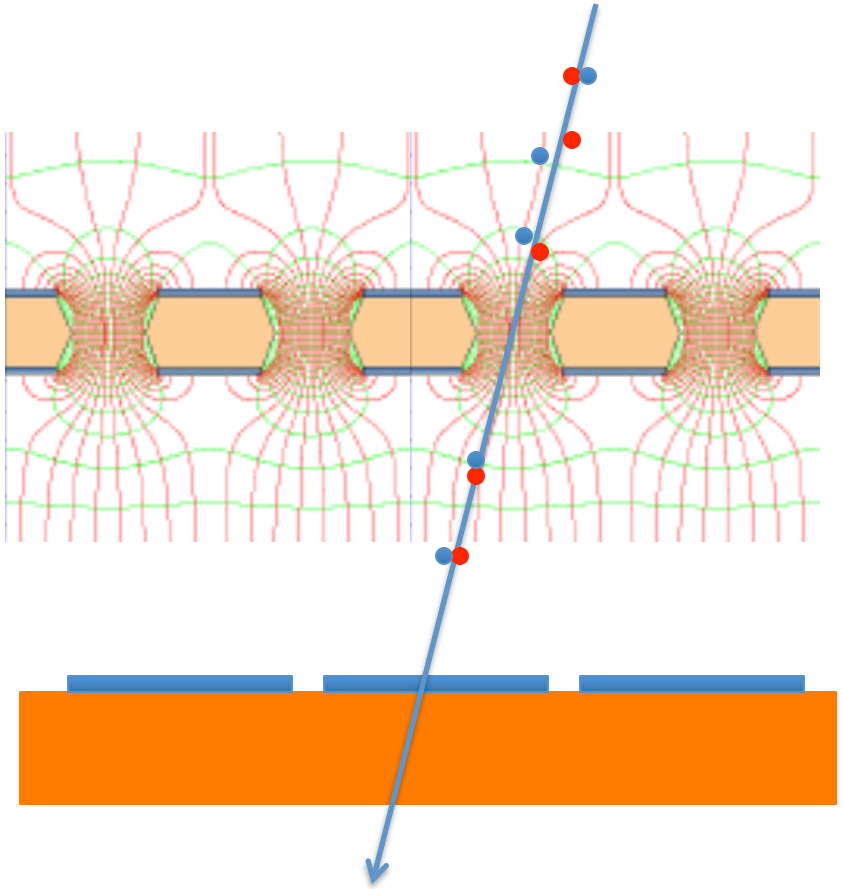
with:
$t_0 = \pi\epsilon_0 a^2 / \mu C V_0$

→ **Definitely too slow to be used at the LHC**

Signal in MPGD

- Let's take a random example: the Gas Electron Multiplier (GEM)





Signal calculation

- To compute the signals induced by a moving charge on electrodes:
  - We compute the particle trajectory in the real electric field
  - The induced current on electrode *n* is calculated in the following way:
    - One removes the charge q from the setup, puts the electrode n to voltage V_0 while keeping all ther other grounded. This results in an electrif field $E_n(x)$, called the Weighting Field. (Ramo's theorem)
    - The induced current is then computed by : (see also castoldi)

$$I_n(t) = -\frac{q}{V_0}\vec{E}_n\left(\vec{x}(t)\right)v(t)$$

Ramo's theorem