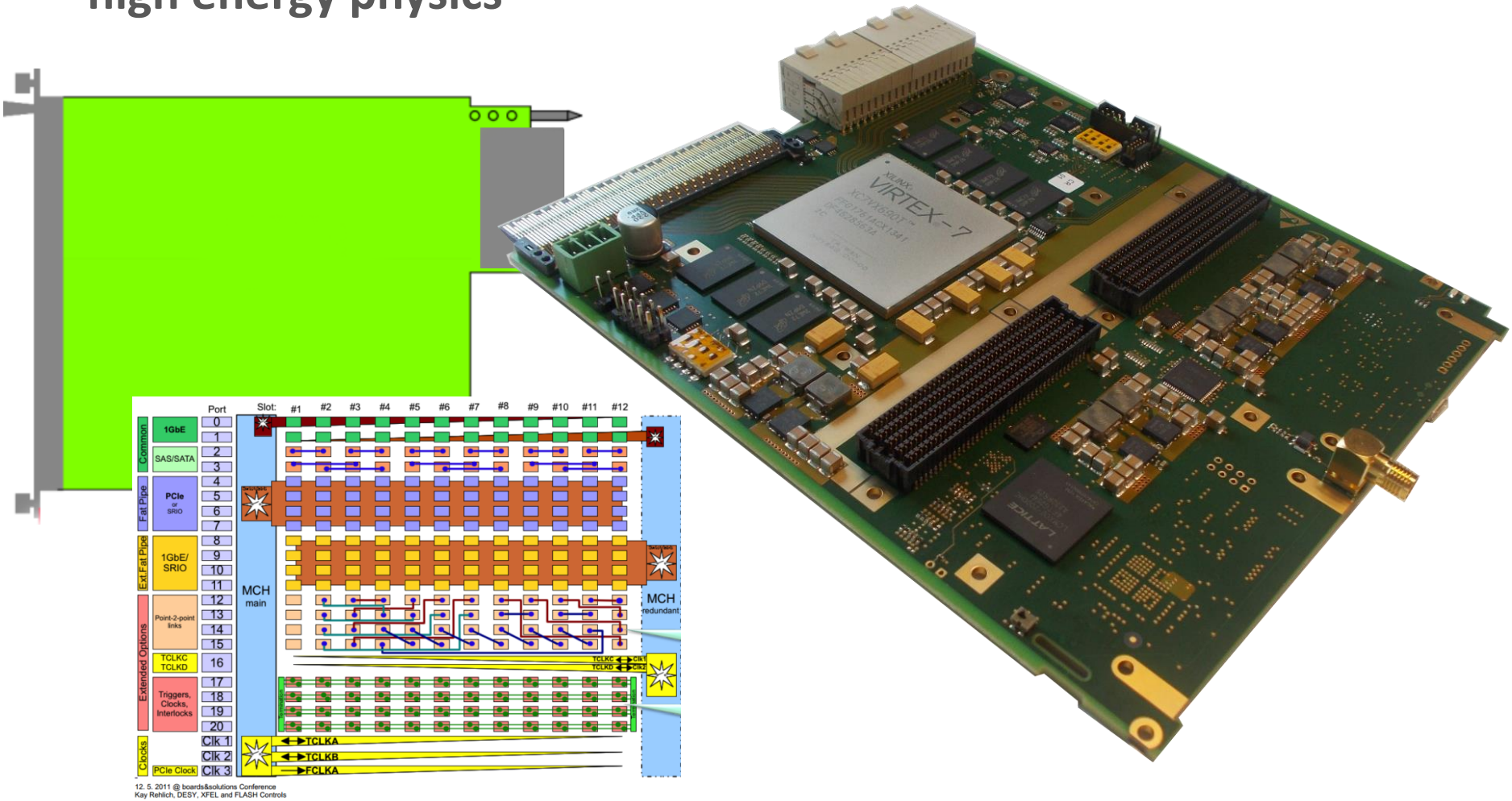
MTCA.4 Workshop 2014
Virtex-7 FPGA carrier
From 10 MHz to 2.6 GHz

IC-FEP-TCAa

A new range of signal processing MTCA.4 boards dedicated to high energy physics



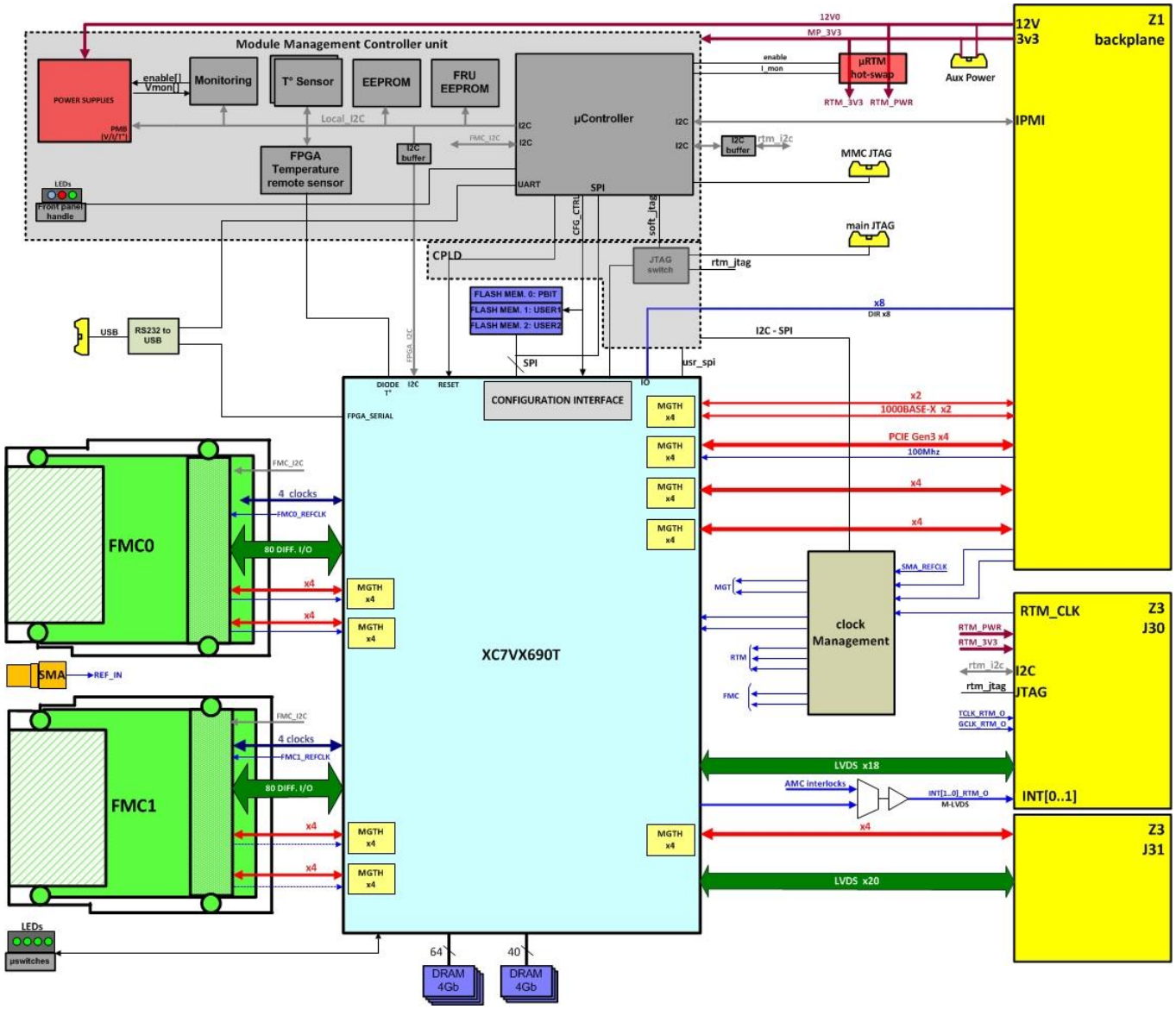
IC-FEP-TCAa

- The same carrier board for sampling from 10 MHz to 2,6 Gb/s
- Only one set of FPGA Reference Designs and Example Designs for easy development (DMA Engine)
- 8 channels per MTCA.4 slot -> competitive solution on cost per channel

IC-FEP-TCAa

- MTCA.4 Double –width mid-size Advanced Mezzanine Card form factor
- One XILINX VIRTEX -7 XC7VX690T (or XC7VX330T)
- Two DDR3 memory banks (first 64 bits wide 2GB and second 40 bits wide 1,25 GB) with up to 1800 MT/s
- Two VITA57.1 HPC FMC slots each one having 4*clocks, 80*differential pairs and 8*Multi-gigabit transceivers (12 Gb/s)
- To the backplane:
  - 16*FPGA Multi-gigabit transceivers on Z1 (12 Gb/s)
  - 38*LVDS and 4*FPGA Multi-gigabit transceivers on Z3
- On board flash memory for FPGA configuration (3*256Mb SPI Mirror flash each for an FPGA image)
- One Module Management Controller (IPMI, FPGA configuration, on-board monitoring)

IC-FEP-TCAa


Module Management Controller unit
POWER SUPPLIES
Monitoring
T° Sensor
EEPROM
FRU EEPROM
µController
FPGA Temperature remote sensor
Local_I2C
FMC_I2C
I2C buffer
LEDs
Front panel handle
UART
SPI
CFG_CTRL
soft_jtag
CPLD
JTAG switch
FLASH MEM. 0: PBIT
FLASH MEM. 1: USER1
FLASH MEM. 2: USER2
USB
RS232 to USB
FPGA_I2C
DIODE T°
I2C
RESET
CONFIGURATION INTERFACE
FPGA_SERIAL
XC7VX690T
MGTH x4
FMC0
FMC1
FMC_I2C
4 clocks
FMC0_REFCLK
FMC1_REFCLK
80 DIFF. I/O
SMA
REF_IN
LEDs
pswitches
64
40
DRAM 4Gb
DRAM 4Gb
12V0
MP_3V3
enable
I_mon
µRTM hot-swap
RTM_3V3
RTM_PWR
Aux Power
12V
3v3
Z1
backplane
IPMI
MMC JTAG
main JTAG
rtm_jtag
rtm_i2c
x8
DIR x8
I2C - SPI
usr_spi
x2
1000BASE-X x2
PCIE Gen3 x4
100Mhz
x4
SMA_REFCLK
MGT
RTM
FMC
clock Management
RTM_CLK
Z3
J30
RTM_PWR
RTM_3V3
I2C
JTAG
TCLK_RTM_O
GCLK_RTM_O
LVDS x18
AMC interlocks
INT[1..0]_RTM_O
M-LVDS
INT[0..1]
Z3
J31
LVDS x20

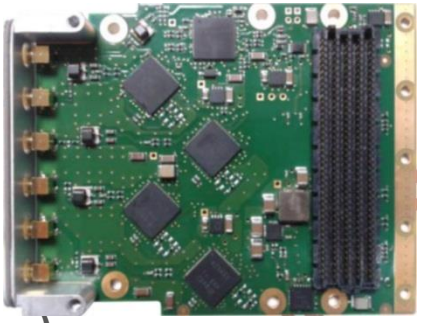
INTERFACE CONCEPT

ADVANCED ELECTRONIC SOLUTIONS

www.interfaceconcept.com

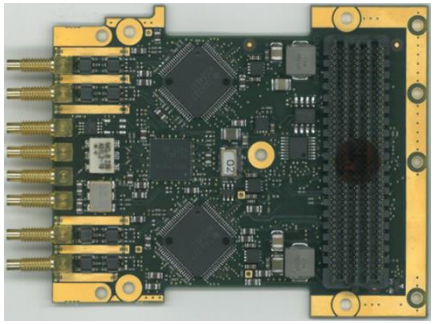
ADC-FMC
covering from 10 MHz to 2,6 GHz

FMC Modules



IC-ADC-FMCa

- A/D/A Converters :
  - IC-ADC-FMCa unit : Quad 16-bit, 135Msps
  - IC-ADC-FMCb unit : Quad 14 bit, 400 Msps (or Quad 12 bit, 500 Msps)
  - IC-ADC-FMCc unit : Quad 12 bit, 1.4Gsps (Q2/14)
  - IC-ADA-FMCa unit : Dual DAC / Dual ADC 12-bits 1Gsps (TBC)
  - IC-DAC-FMCa : quad 16-bit 800Msps
  - IC-DAC-FMCb : quad 16-bit 1Gsps



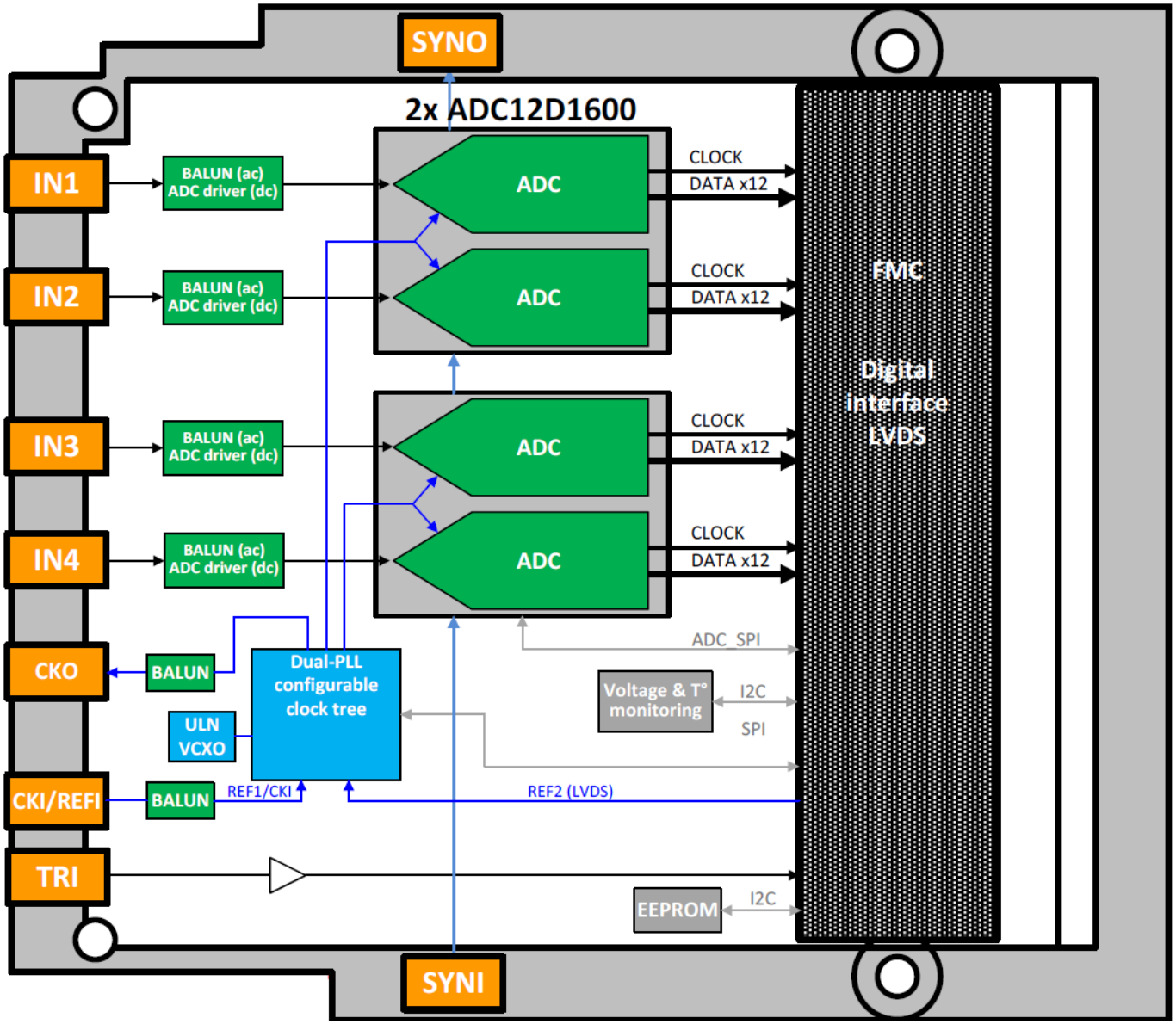
IC-ADC-FMCb

- IO Modules :
  - IC-IO-FMCa : Dual SFP+ ports

IC-ADC-FMCc

IC-DAC-FMCa

IC-ADC-FMCc


SYNO
2x ADC12D1600
IN1
IN2
IN3
IN4
BALUN (ac)
ADC driver (dc)
ADC
CLOCK
DATA x12
FMC
Digital
interface
LVDS
CKO
BALUN
Dual-PLL
configurable
clock tree
ULN
VCXO
CKI/REFI
REF1/CKI
REF2 (LVDS)
ADC_SPI
Voltage & T°
monitoring
I2C
SPI
TRI
EEPROM
SYNI

IC-ADC-FMCc

- Four channels using two ADC12D1600. Single width, High Pin Count FMC
- Full scale amplitude : 0,8 V peak to peak. Analog input bandwidth: 5-2200 MHz
- SSMC connectors. 50Ω, AC coupled
- On board clock tree, based on a dual PLL.
- Clocking options:
  - use front panel input (CKI) for ADC sampling,
  - generate sampling clock from reference clock input (REFI) from front panel,
  - generate sampling clock from reference clock input from FMC connector (carrier board)
- One clock ouptut
- One trigger input (DC coupled LVPECL buffered and LVDS output to the carrier
- Performance very close to the performance of the TI 12D1600 ADCs, that proves the quality of design of the FMC
- Power dissipation 12W
- Run on IC-FEP-VPX3c, IC-FEP-VPX6b and IC-FEP-TCAa