uTCA and MTCA.4 hardware used at KEK

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(KEK)

Contents:

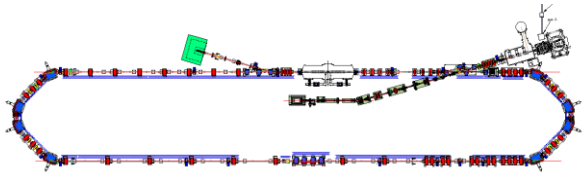
- Facilities using TCA at KEK
- Boards used at KEK
- Performance of uTCA boards
- MTCA.4 board

Facilities using TCA Hardware at KEK

High Energy Accelerator Research Organization (KEK)

Superconducting RF Test Facility (STF)

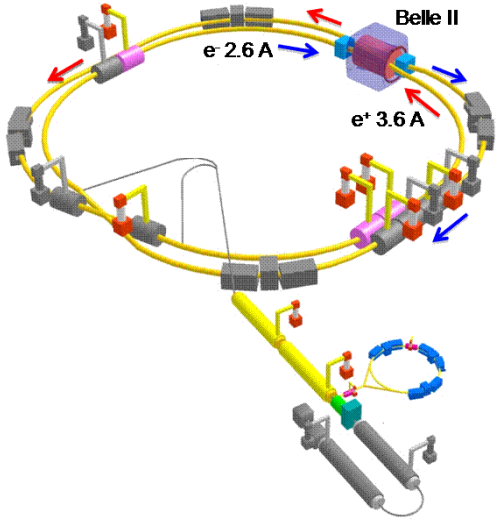
- ILC R&D facility
- 1.3GHz pulse SC



Compact Energy Recovery Linac (cERL)

•Test facility for a future 3 GeV ERL

•1.3GHz CW SC



SuperKEKB

•Electron-positron collider

•40x higher luminosity as the previous KEKB

•Explore new physics beyond the standard model

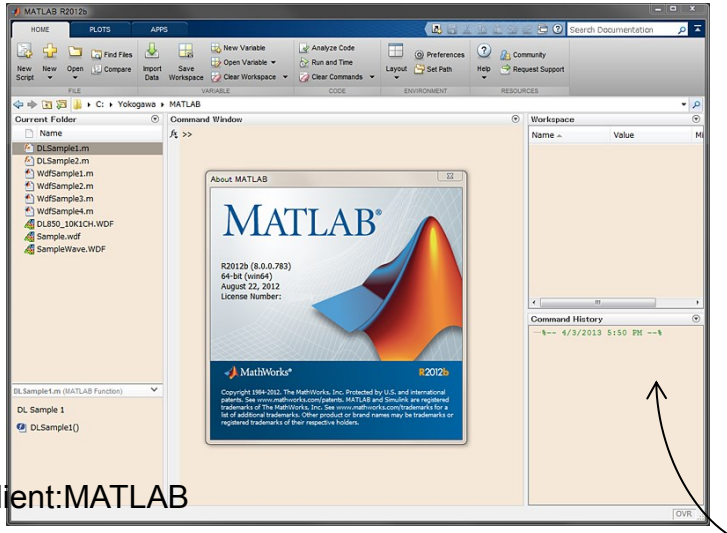
•509MHz CW NC&SC

Boards developed at KEK

Past, present, and future TCA hardware used at KEK developed by KEK and manufactured by Mitsubishi Electric Tokki Systems Corporation

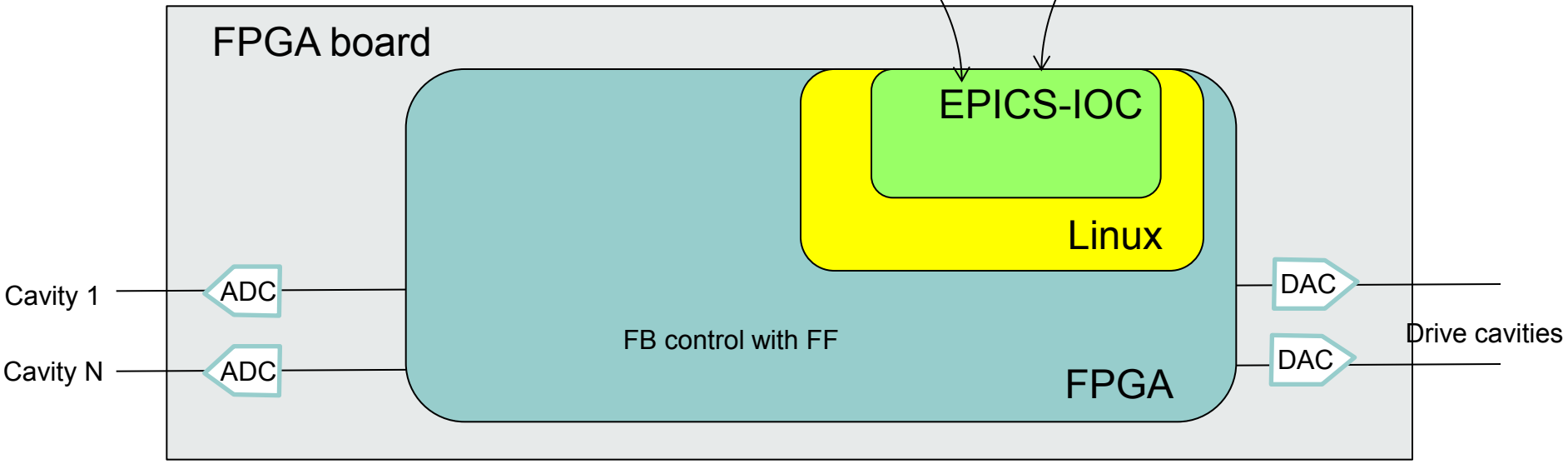
	AD/DA/FPGA	Software	Application
Board 1: uTCA	4 16 bit ADCs (LTC2208 130 MSPS) 4 16 bit DACs (AD9783 500MSPS) Virtex-5 FX	EPICS /Wind Rvier Linux on PowerPC	cERL LLRF STF LLRF SuperKEKB LLRF SuperKEKB BPM
Board 2: uTCA	2 14 bit ADCs (ADS5474 400MSPS) Virtex-5 FX	EPICS /Wind Rvier Linux on PowerPC	SuperKEKB LLRF cERL LLRF
Board 3: MTCA.4	14 16 bit ADCs (AD9650,105MSPS) 2 16 bit DACs ((AD9783 500MSPS) Zynq-7000 FPGA	EPICS /Xilinx Linux on ARM	STF-2 LLRF

FPGA board and software



Client:MATLAB

Client:Control System Studio (CSS)



µTCA AMC Board (Board 1)

Two daughter boards

Motherboard

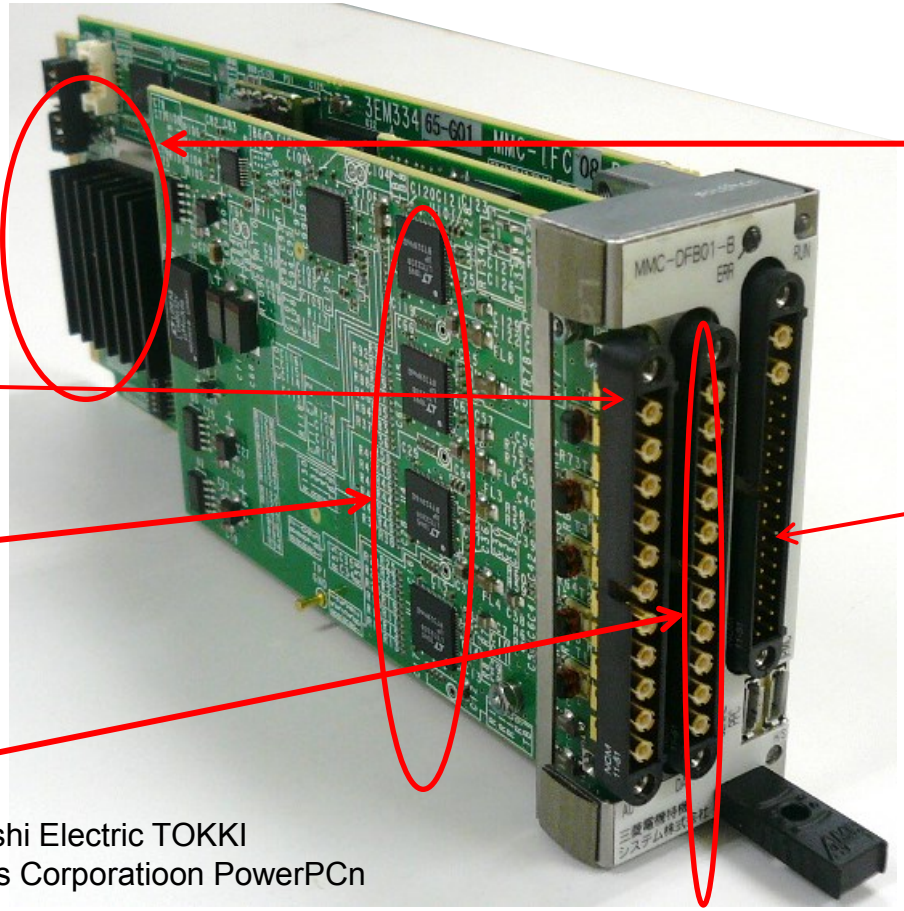
FPGA
Virtex 5 FX
Linux installed on PowerPC
→ EPICS-IOC

Clock input

4 x 16-bit ADC
(LTC2208)

4 x 16-bit DAC
(AD9783)

Digital I/O

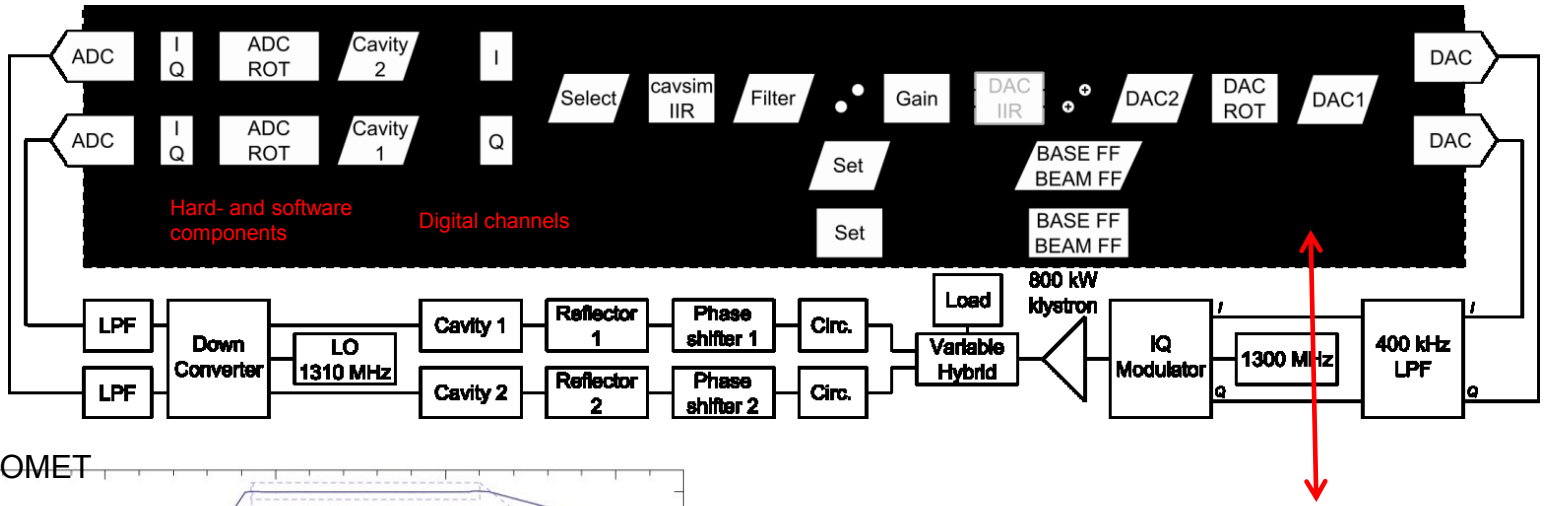


Mitsubishi Electric TOKKI
Systems Corporatioon PowerPCn

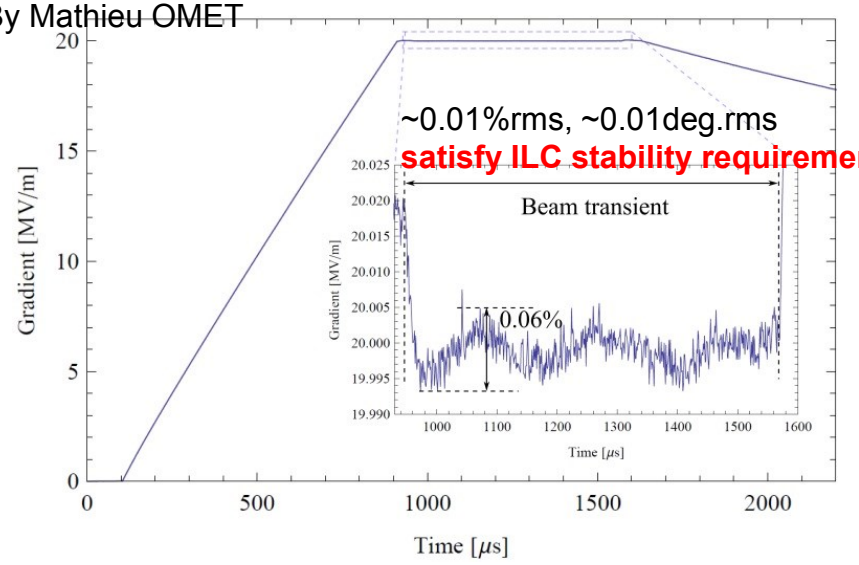
Board 1at STF

LLRF Control Loop at STF

RF: 1.3 GHz pulsed (5 Hz)



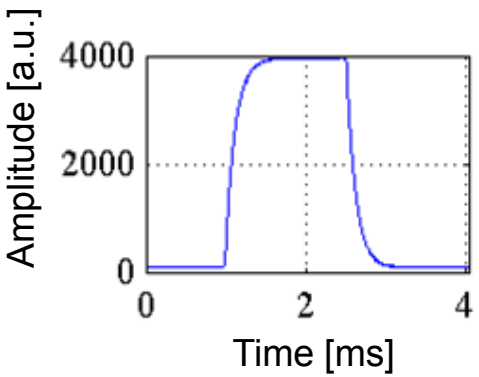
By Mathieu OMET



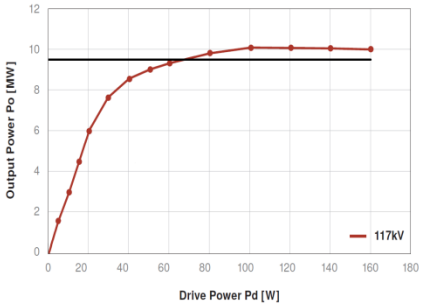
Klystron & cavity simulator

- Klystron simulator based on two direct lookup tables
- Cavity simulator based on the time discrete cavity differential equation

Kly. / cav. sim. output



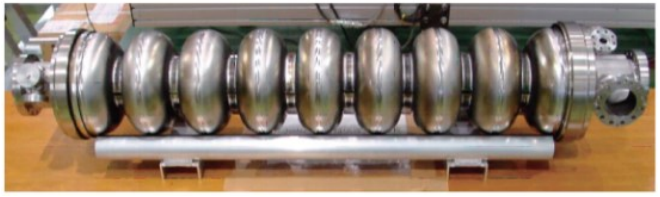
Klystron
Non-linearity



By Mathieu OMET

FPGA-based
µTCA AMC board

$$\dot{V}_c = -\omega_{1/2} V_c + \omega_{1/2} R_L (2I_g - 2I_{b0})$$



Super-
conducting
Cavity with beam

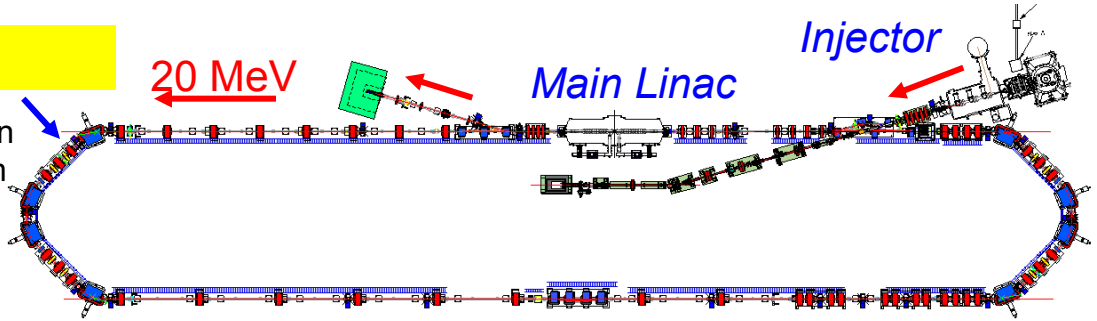
Board 1 at cERL

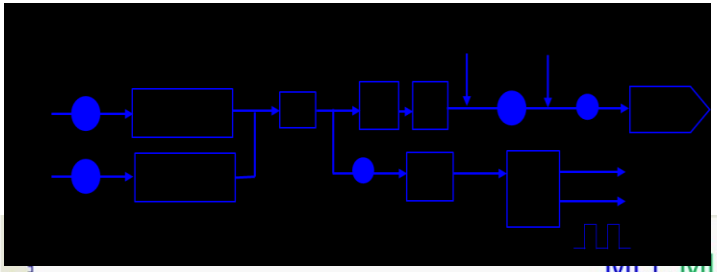
	NC cavity	SC cavities			
	BUN	Inj1	Inj2 & Inj3	ML1	ML2
Amplitude	0.05% rms	0.01% rms	0.01% rms	0.013% rms	0.013% rms
Phase	0.06° rms	0.02° rms	0.02° rms	0.014° rms	0.015° rms

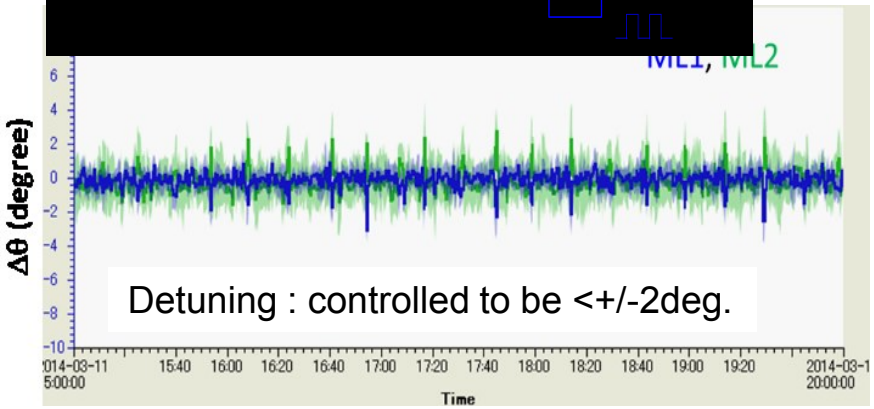
Requirements: 0.1%rms, 0.1deg.rms

RF field control
And
Piezo/Tuner control

Screen
Monitor
Dispersion
=0.487m

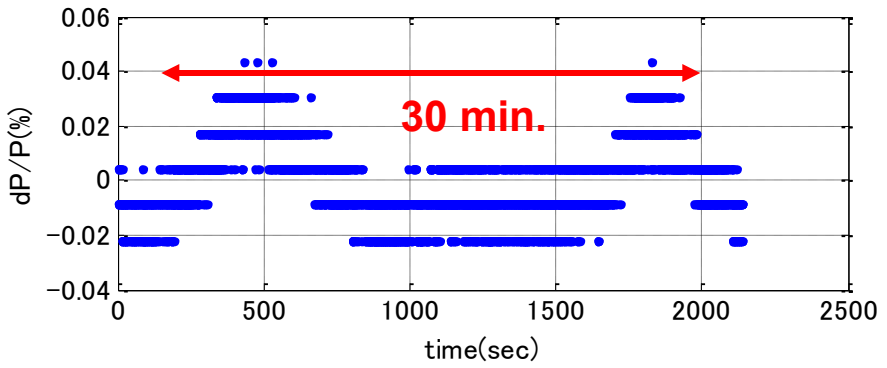






beam energy stability: ~0.01%rms

T. Miura



µTCA AMC Board (Board 2)

Common mother board with board 1

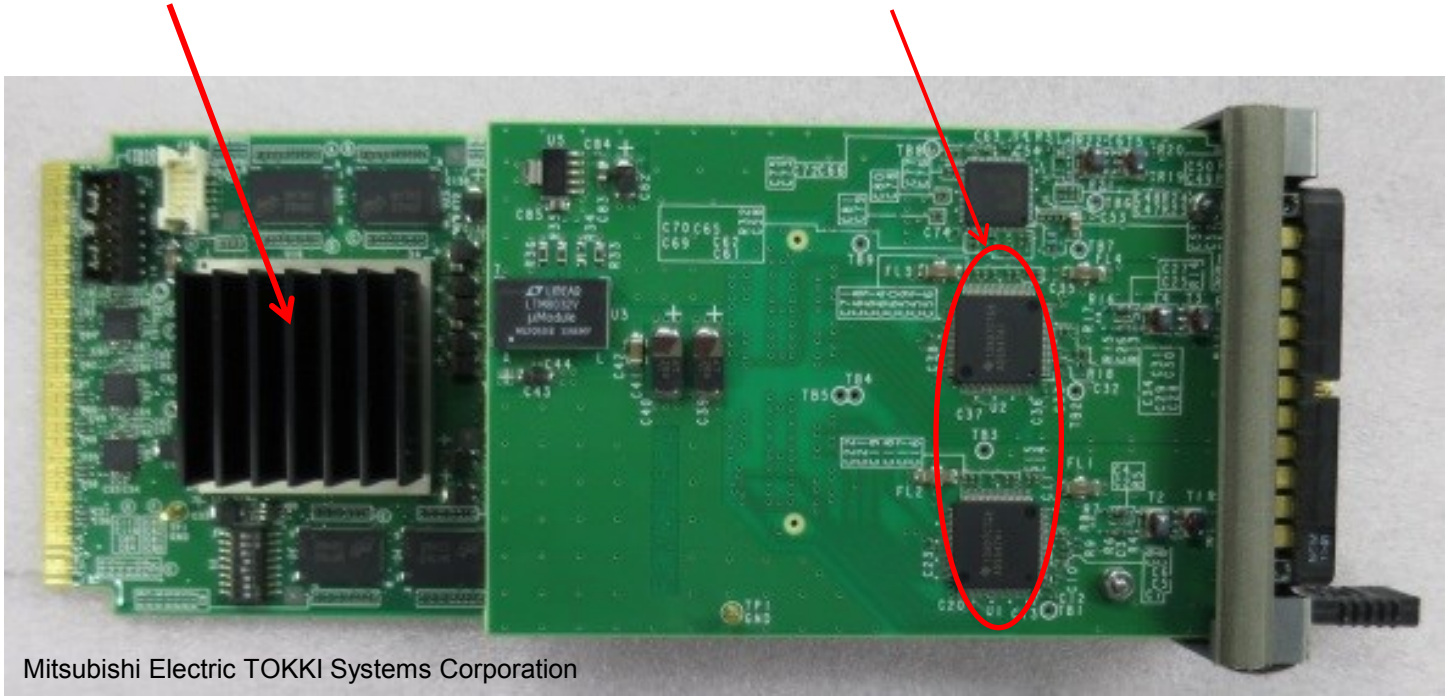
Motherboard

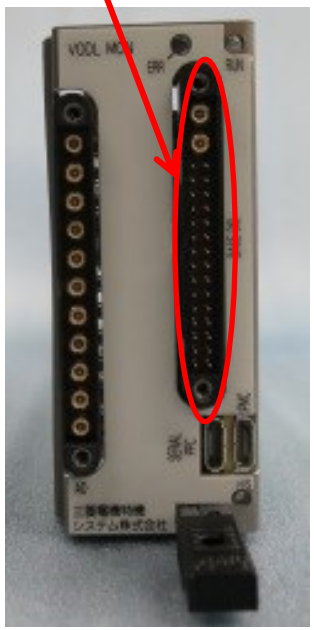
FPGA Virtex 5 FX
Linux installed on PowerPC
→ *EPICS-IOC*

One daughter board

2 fast (400 MSPS) 14-bit ADCs

Digital I/O





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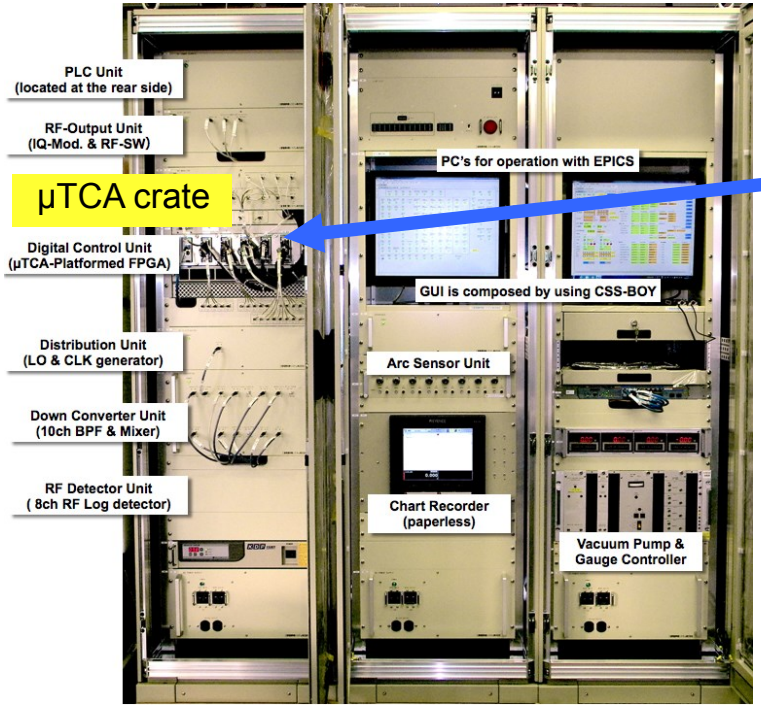
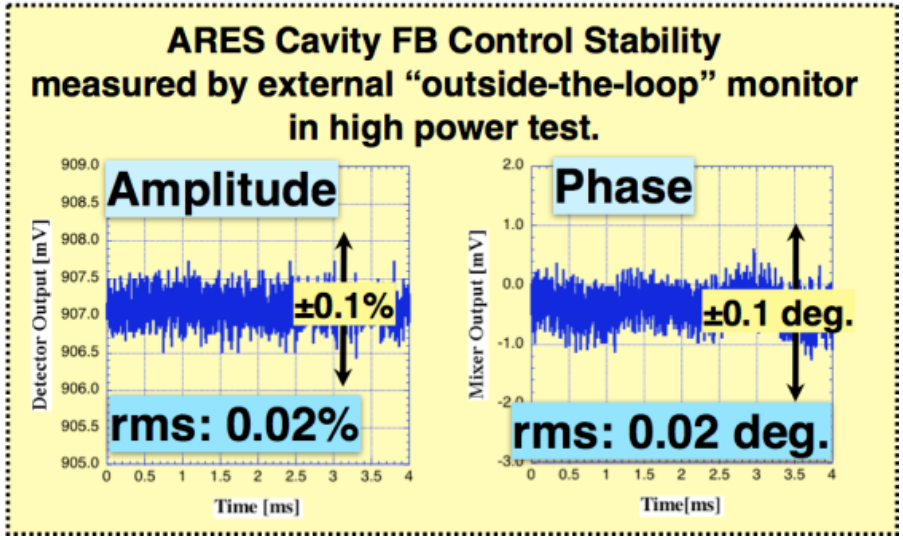
Board 1 at SuperKEKB

New LLRF system for one klystron



Mitsubishi Electric TOKKI Systems Corporation

T. Kobayashi

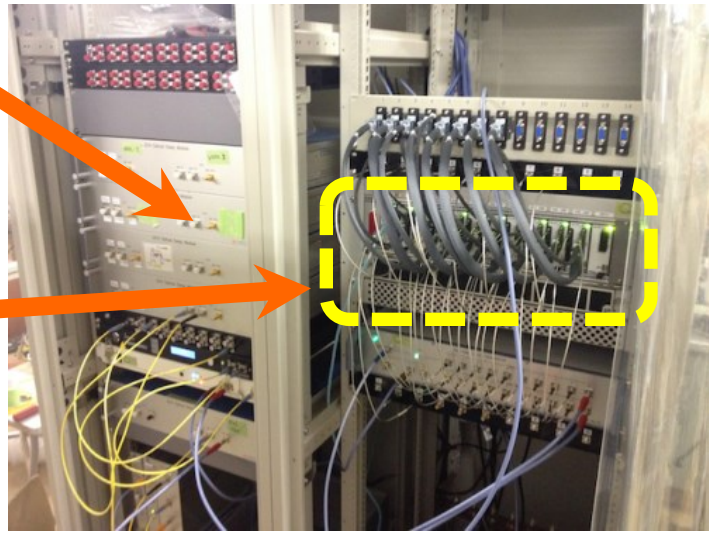


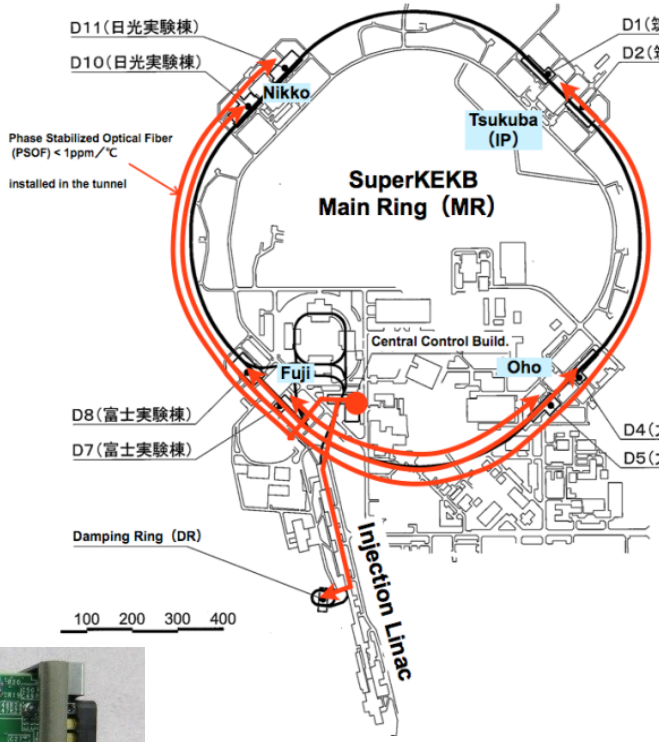
- **Common hardware for both of ARES (NC) & SC Cavity**

Board 2 at SuperKEKB

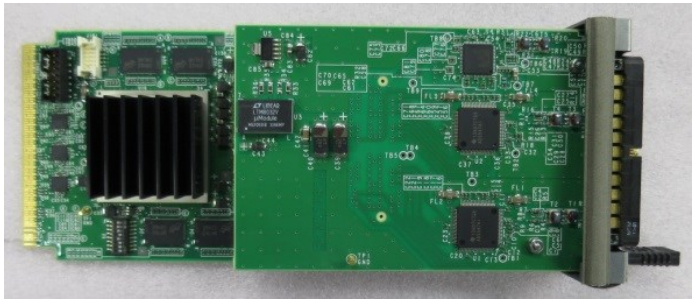
Optical delay stabilization of the RF reference distribution

- Variable Optical Delay Lines (VODLs) for 8 transmissions
- µTCA-platformed FPGAs for the control of the variable optical delay





Phases (delays) of 509-MHz RF are detected by direct sampling at 212 MHz



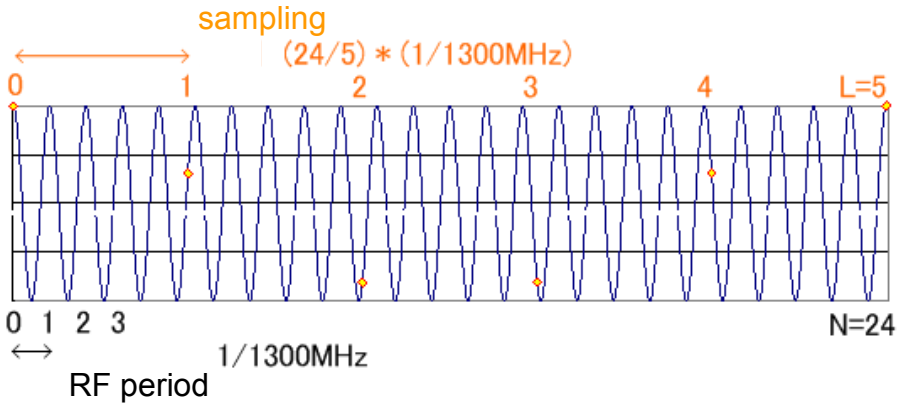
T. Kobayashi

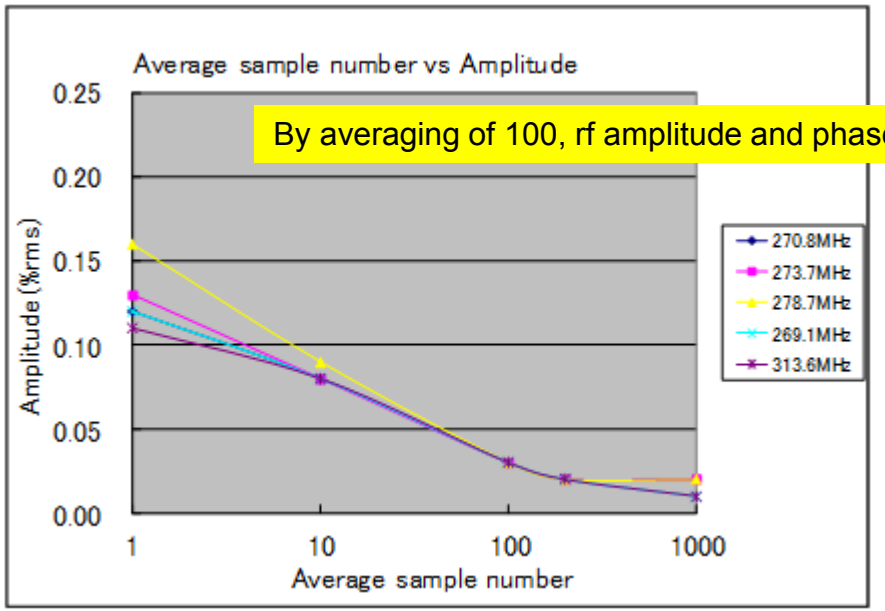
Short term stability (time jitter) : ~0.1 ps (rms)
Long term stability (pk-pk) : ±0.1° @508.9MHz = ±0.55 ps
(achieved by the optical delay control)

μTCA AMC Board (Board 2) :direct sampling

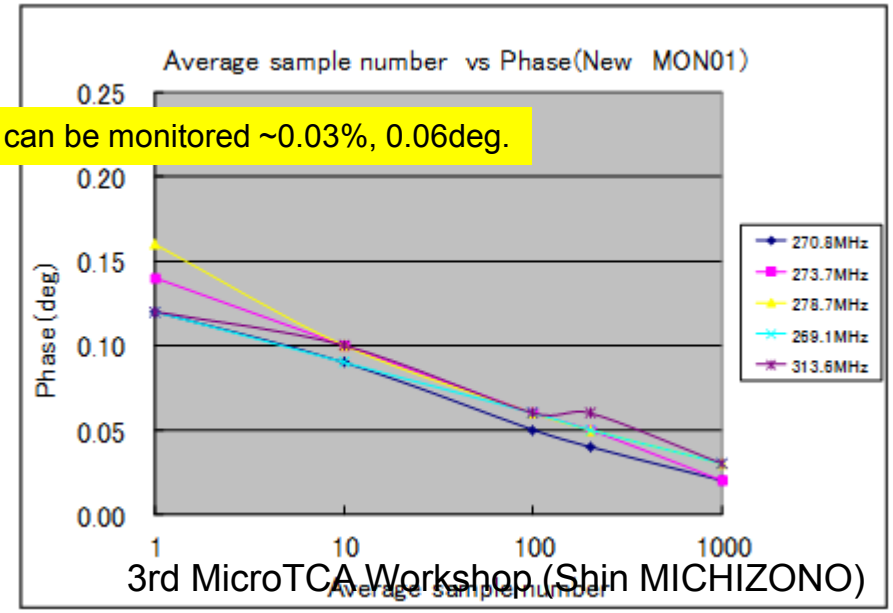
Undersampling procedure for direct sampling.
This will be installed at cERL.

No.	Clock [MHz]	RATE	L Data cycle	N RF cycle
1	270.8	1300* 5/24	5	24
2	273.7	1300* 4/19	4	19
3	278.6	1300* 3/14	3	14
4	269.0	1300* 6/29	6	29
5	313.8	1300* 7/29	7	29





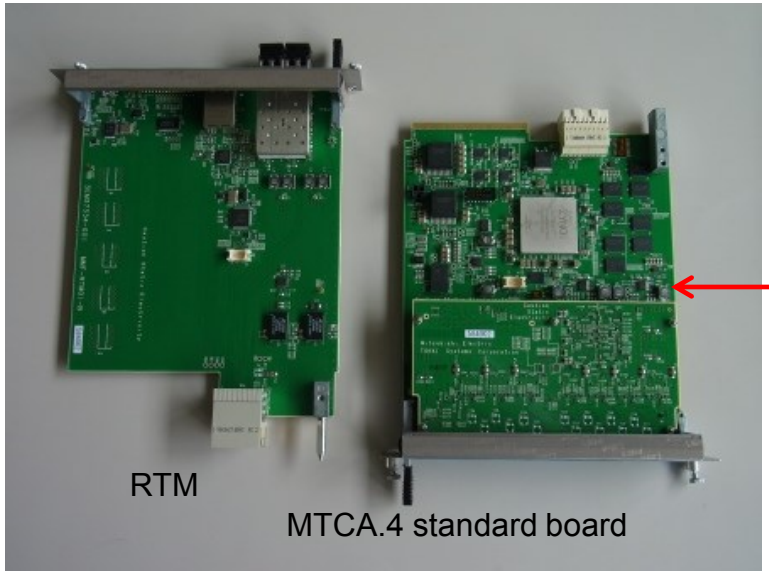
By averaging of 100, rf amplitude and phase can be monitored ~0.03%, 0.06deg.

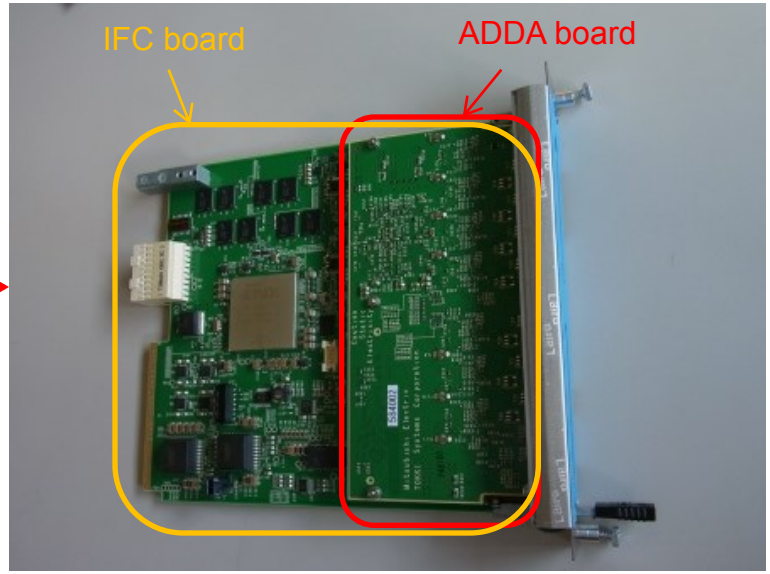


MTCA.4 Standard Boards (Board 3)

Digital LLRF control boards for STF-2

- MTCA.4 standard board
  - mother board:Zynq-7000 FPGA (XC7Z045): Linux installed on ARM (EPICS-IOC), two FMCs
  - FMC (HPC) ADDA board (double width):
    14ch ADCs (AD9650, 16bit), 2ch DACs (AD9783, 16bit)
  - RTM module:RJ-45 connector, 14ch DIO connectors
    2ch SFP connectors (Data communication between boards)





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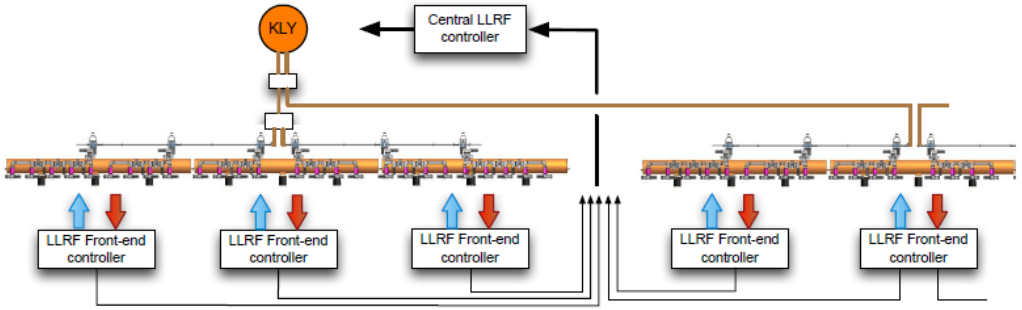
MTCA.4 Standard Boards at STF-2

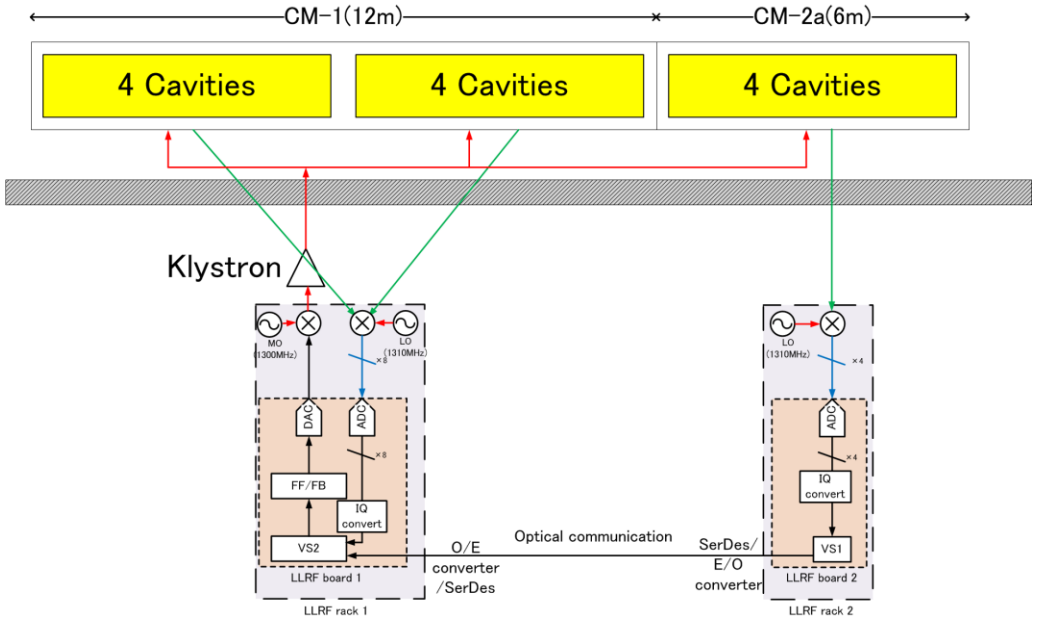
LLRF system in ILC-TDR (39 cavities per klystron)

RF: 1.3 GHz pulsed (5 Hz)



- Each front-end controller computes partial cavity-field vector-sums and sends those to the central LLRF controller
- The central LLRF controller performs the total vector-sum calculation and feedback/feedforward operation

LLRF system for STF-2



- At STF-2 two digital LLRF boards connected by optical communication will be configured for operation

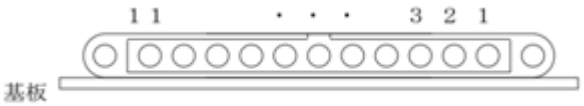
→ minimal configuration of an ILC LLRF system

Summary

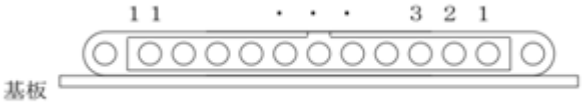
- We have developed uTCA and MTCA.4 boards for mainly LLRF control.
  - Digital FB control (board 1)
  - Direct sampling (board 2)
  - MTCA.4 with 14ch AD board (board 3)

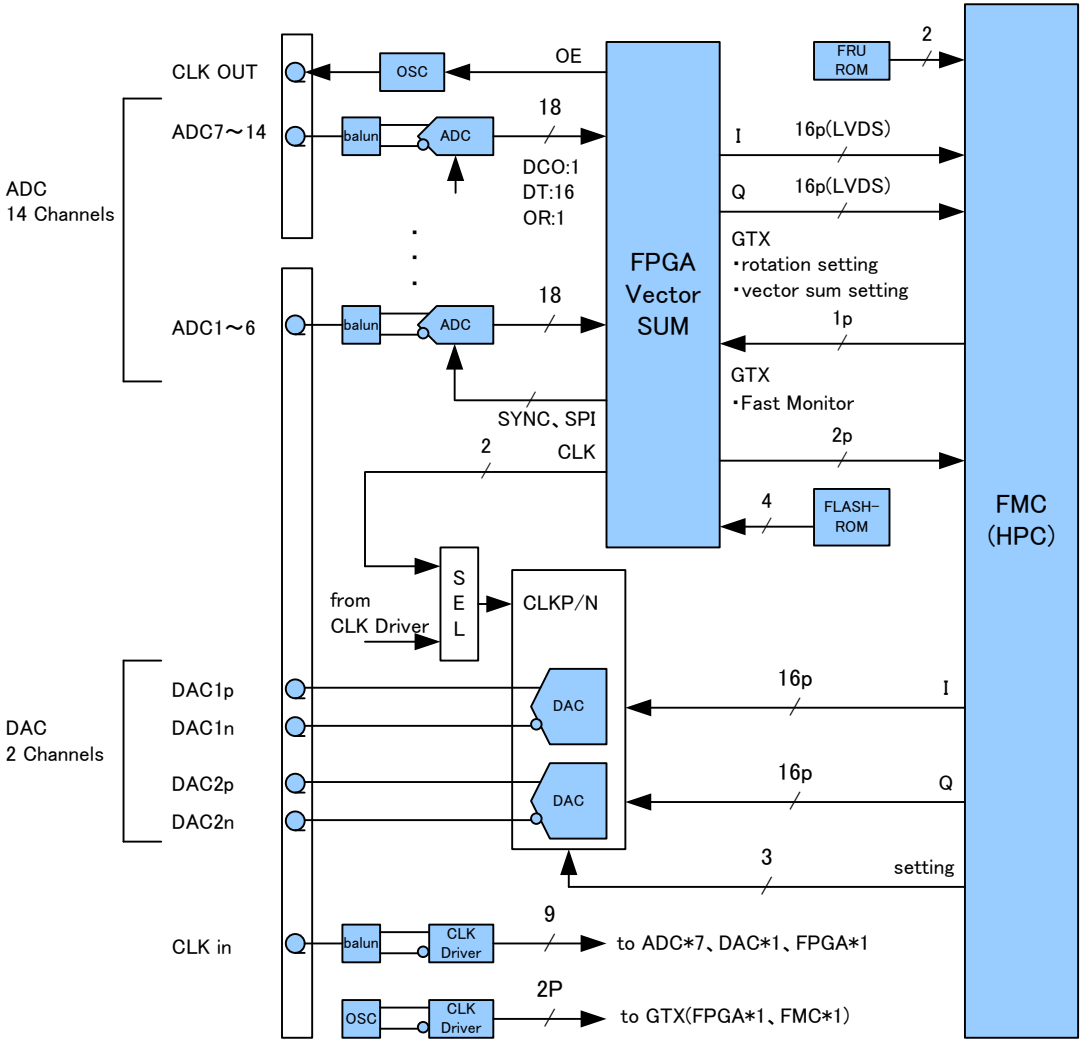
- Typical performance of the LLRF system is ~0.02%rms, 0.02deg. rms and these satisfy the LLRF requirements.

AD DA FMC



AD：AD9650BCPZ-105 （ADI）
DA:AD9783BCPZ （ADI）
FPGA：XC6SLX150T-3FG676C
Analog input output Connector：
221D00F26-0011-1400CMM （nicomatic）

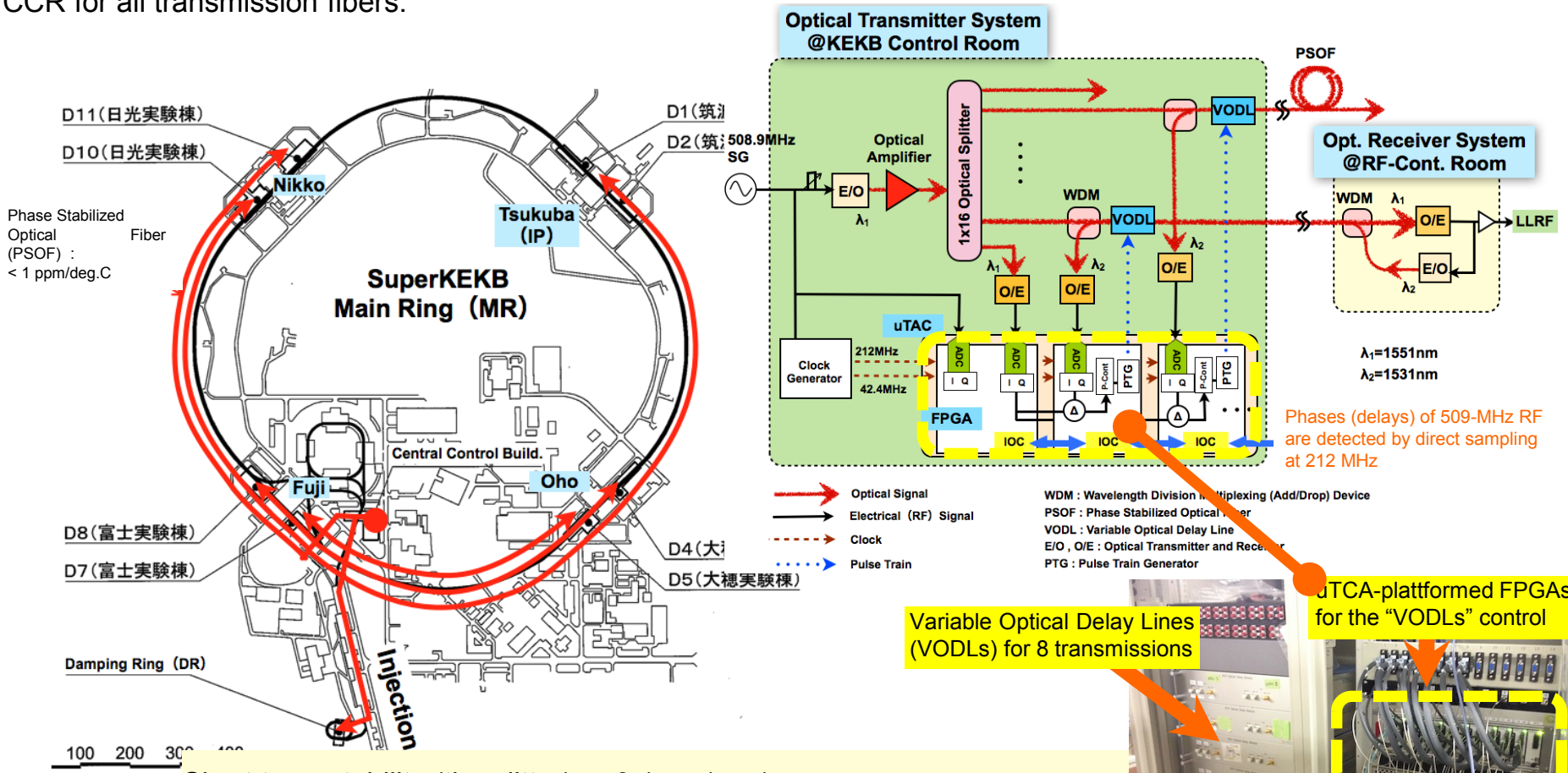




Board 2 for Optical Delay Stabilization of RF Reference Distribution for SueprKEKB

T. Kobayashi, et al.

- RF reference signal is optically distributed into 8 sections by means of “Star” topology configuration from the central control room (CCR).
- “Phase Stabilized Optical Fiber”, which has quite small thermal coefficient, is adapted : < 1ppm/°C (5 ps/km//°C)
- Furthermore, for thermal drift compensation, variable optical delay lines (VODLs) are controlled by uTCA-FPGAs at CCR for all transmission fibers.



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