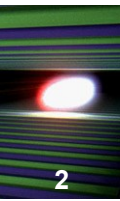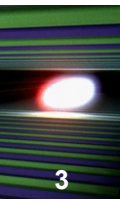# MicroTCA.4-based Timing System used at XFEL and FLASH/FLASH2

Agenda

- x2timer parameters
- Hardware implementation
  - External timing adapter (ETA)
  - Timing system setup
  - Drift compensation daughterboard
  - Rear Transition Module Types
- Software implementation
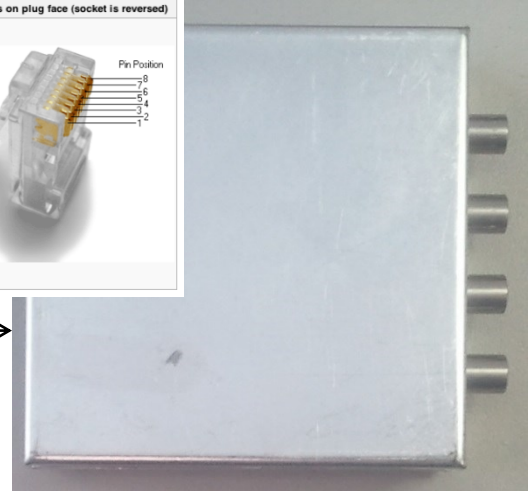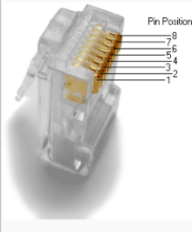- Setup in FLASH
- Setup in XFEL - outlook

x2timer parameters

- double-width AMC
  - receives/transmits 1 - 1.3GHz optical timing signal
  - Trigger/bunch pattern/FPGA clocks outputs via
    - → 3x RJ45 front connectors (2 triggers per connector)
      - LVDS signal level / TTL with external hardware
    - → 8x on µTCA backplane (MLVDS bus on port 17-21)
    - → 9x on optional RTM – LVDS & TTL level
  - Low jitter clock output via
    - → 3x RJ45 front connectors
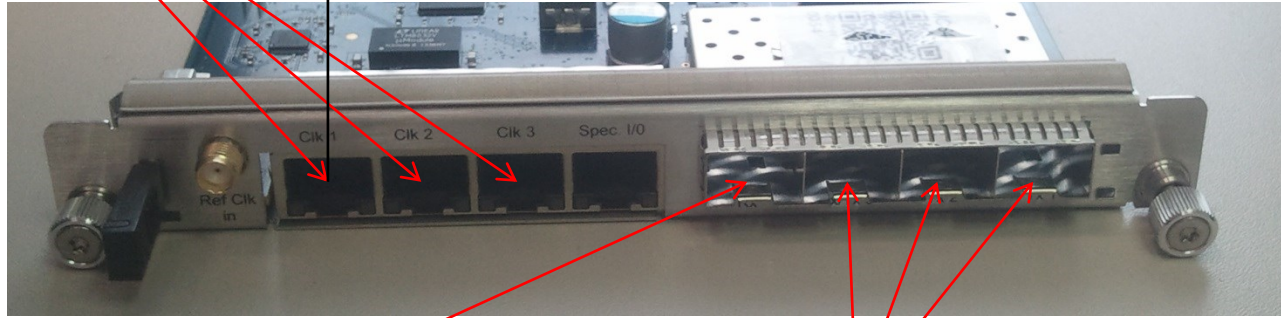   - → TCLKA/TCLKB and crosspoint switch on MCH

External timing adapter
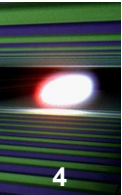
Pin	T568A Pair	T568B Pair	Wire	T568A Color	T568B Color	Pins on plug face (socket is reversed)
1	3	2	tip	white/green stripe	white/orange stripe	
2	3	2	ring	green solid	orange solid	
3	2	3	tip	white/orange stripe	white/green stripe	
4	1	1	ring	blue solid	blue solid	
5	1	1	tip	white/blue stripe	white/blue stripe	
6	2	3	ring	orange solid	green solid	
7	4	4	tip	white/brown stripe	white/brown stripe	
8	4	4	ring	brown solid	brown solid	

Clock or Trigger (Pin 1, 2)
5 Volt (Pin 3)
Clock or Trigger (Pin 4, 5)
GND (Pin 6)
Clock or Trigger (Pin 7, 8)
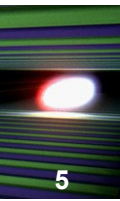
3x LVDS:
2x Trigger
1x clock

TTL:
Trigger
Trigger
clock

AMC

Input from Timing Master

Output to other Timing Receivers

Timing system setup

- Star topology
- One timing master, synchronized by Master Oscillator
  - Also connected to machine protection system
- Master oscillator clock is recovered on each receiver
- No limitation in no. of receivers
  - each receiver can forward signal to another system
- Timing information is (de-)coded in onboard FPGA
  - System keeps running even when CPU/network fails
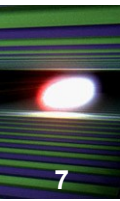- Receivers can be added/removed during runtime

Hardware implementation
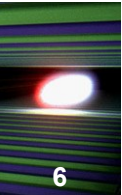
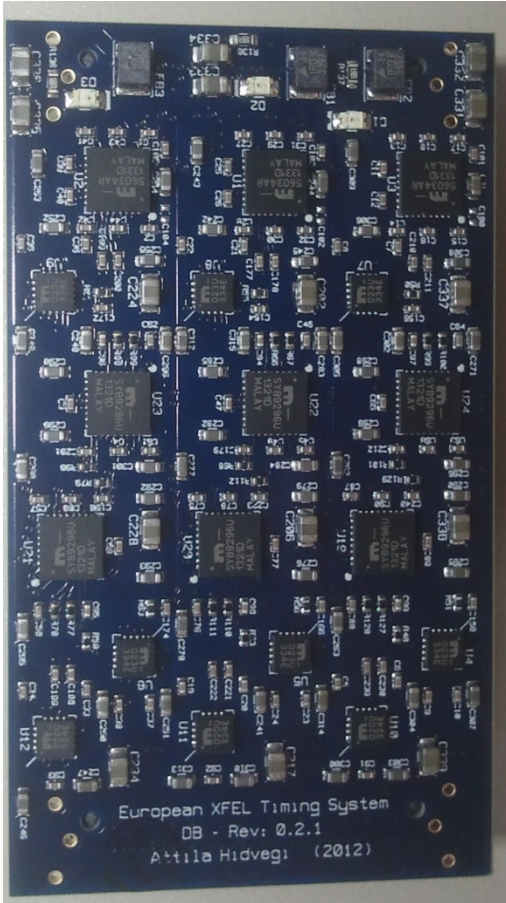## Rear Transition Module

AMC
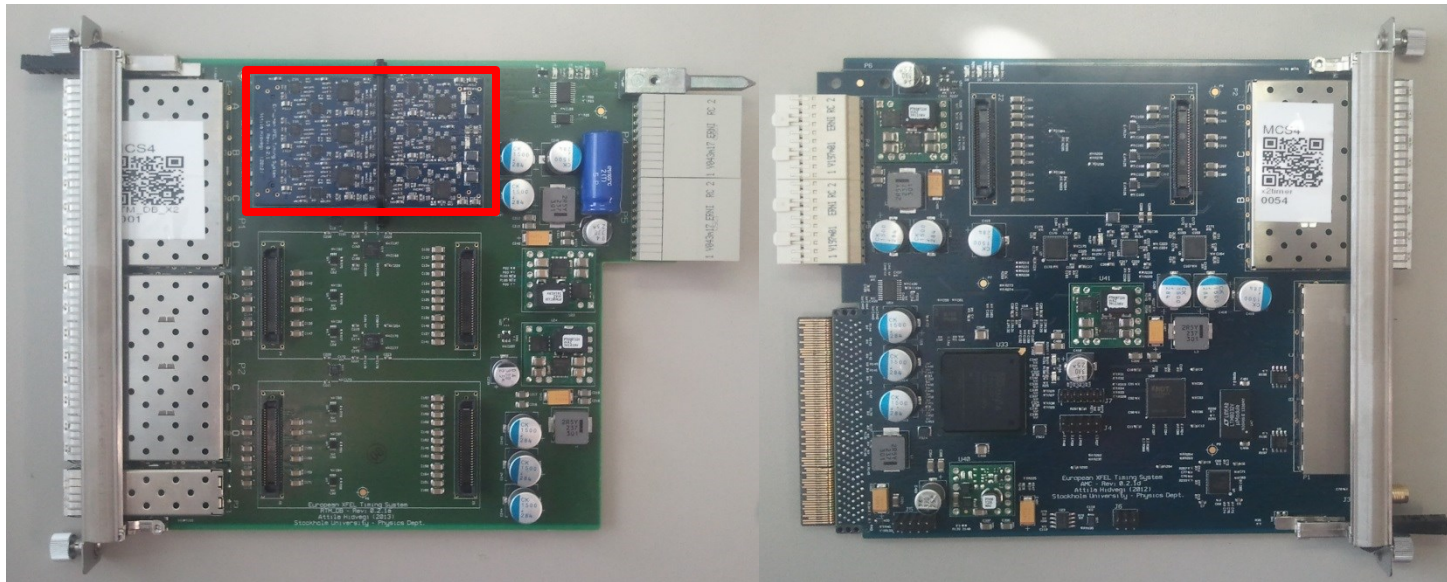
Hardware design @ Physics Department of Stockholm University

Drift compensation daughterboard

- Addon board for AMC and transmitter RTM
  - 3 channels, each controlled by seperate microcontroller
  - Programmable via HPM.1
- Measure phase difference between MO clock and looped signal
- Increase / decrease delay by some picoseconds to keep phase stable (long-term phase drift below 80ps peak-peak)
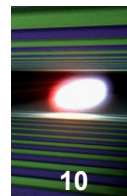
Rear transition module types
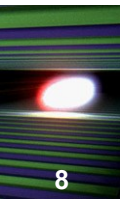
- ## Type 1: daughter-board RTM (available)
  - Up to 9 * output of optical timing signal for other systems, cable length and drift compensated per output channel
- ## Type 2: TTL Trigger RTM (in production)
  - Up to 9 * TTL level trigger output on LEMO connector
  - 2 * high-precision output with rise-/fall-delay in steps of 100ps
- ## Type 3: optical Trigger RTM (under development)
  - Up to 9 * optical trigger output on ST connector

Software implementation
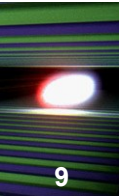
- Each crate contains one CPU AMC

- x2timer server running on that CPU

- One server can manage several x2timer AMCs via PCIe

- Configurable remotely via DOOCS / Ethernet
  - FPGA firmware upgrade also possble via PCIe

- x2timer hardware generates CPU interrupts that may be used for other parts of the system, e.g. sampling of ADC channel, data aquisition, etc.

Software implementation

Configuration of x2timer - 2

Figure: x2_trigger_channel.xml FLASH.DIAG/TIMER/LASER1/FRONT.TRG1

Trigger Channel — LASER1/FRONT.TRG1

Channel description: gate for 25kHz camera trigger

Input Source Select: Trigger del. or imm.
2. Source Select: Front Ch 1
Output Source Select: Width output

- FPGA clock 1 — 54.17 MHz
- FPGA clock 2 — 54.17 MHz
- Bunch pattern 1
- Bunch pattern 2

- Backplane Ch. 1...8
- RTM Ch. 1...9
- Front Ch. 1...6

- Fast Data/Clock
- UART 115kbaud
- Global Sync
- OR
- AND
- FF — Gate
- Ch. out intern to "2. source"

Trigger No.: 166
Delay: 338000 * 9.23ns = 3,1296265ms
Width: 86400 * 9.23 ns = 799,9992µs
Fine Delay: 0 * 923ps = 0 s

x2timer setup in FLASH/FLASH2

x2timer setup in XFEL