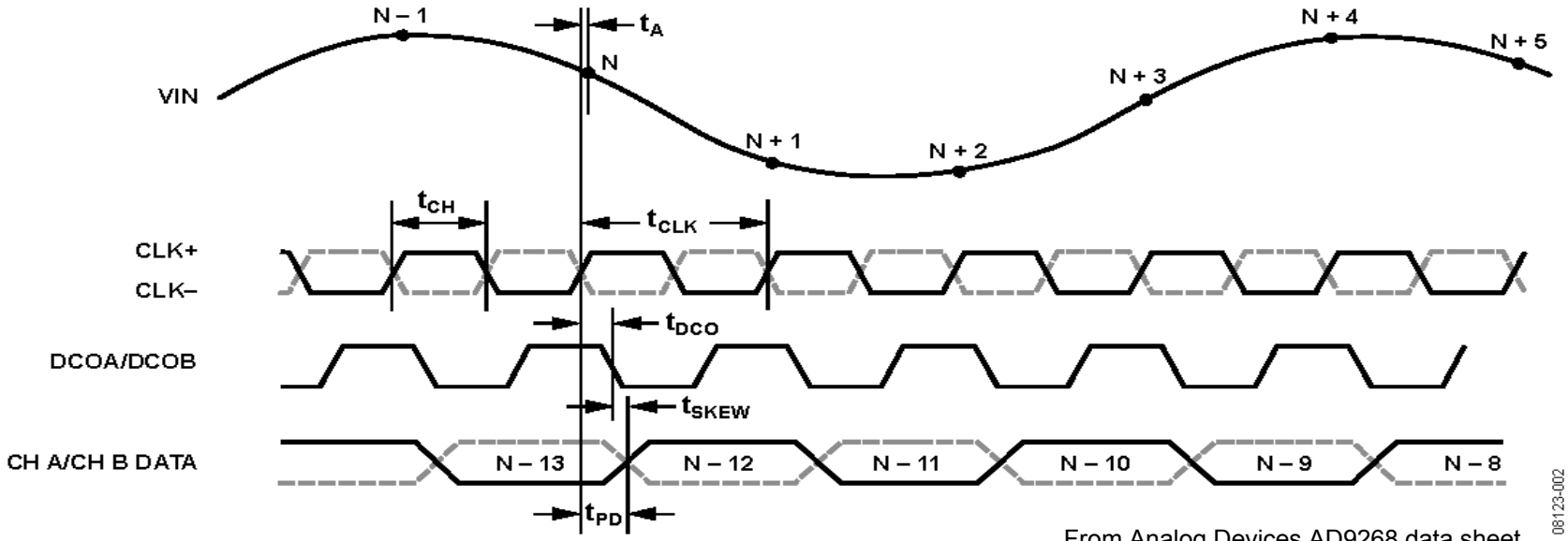
MTCA Digitizers and RTMs, Downconversion versus Direct Sampling

Dr. Matthias Kirsch

Direct Sampling
Digitizer „Scope without Screen“



From Analog Devices AD9268 data sheet

- One sample/clock
- Pipelining

Direct Sampling

Niquist-Shannon Sampling Theorem

Vladimir Kotelnikov (1933)

A signal with bandwidth f_{max} has to be sampled at least with $f_{sam} = 2 \times f_{max}$

to allow for signal reconstruction from the sampled digitized values.

→ Downconversion in RF applications

Downconversion

Mixer

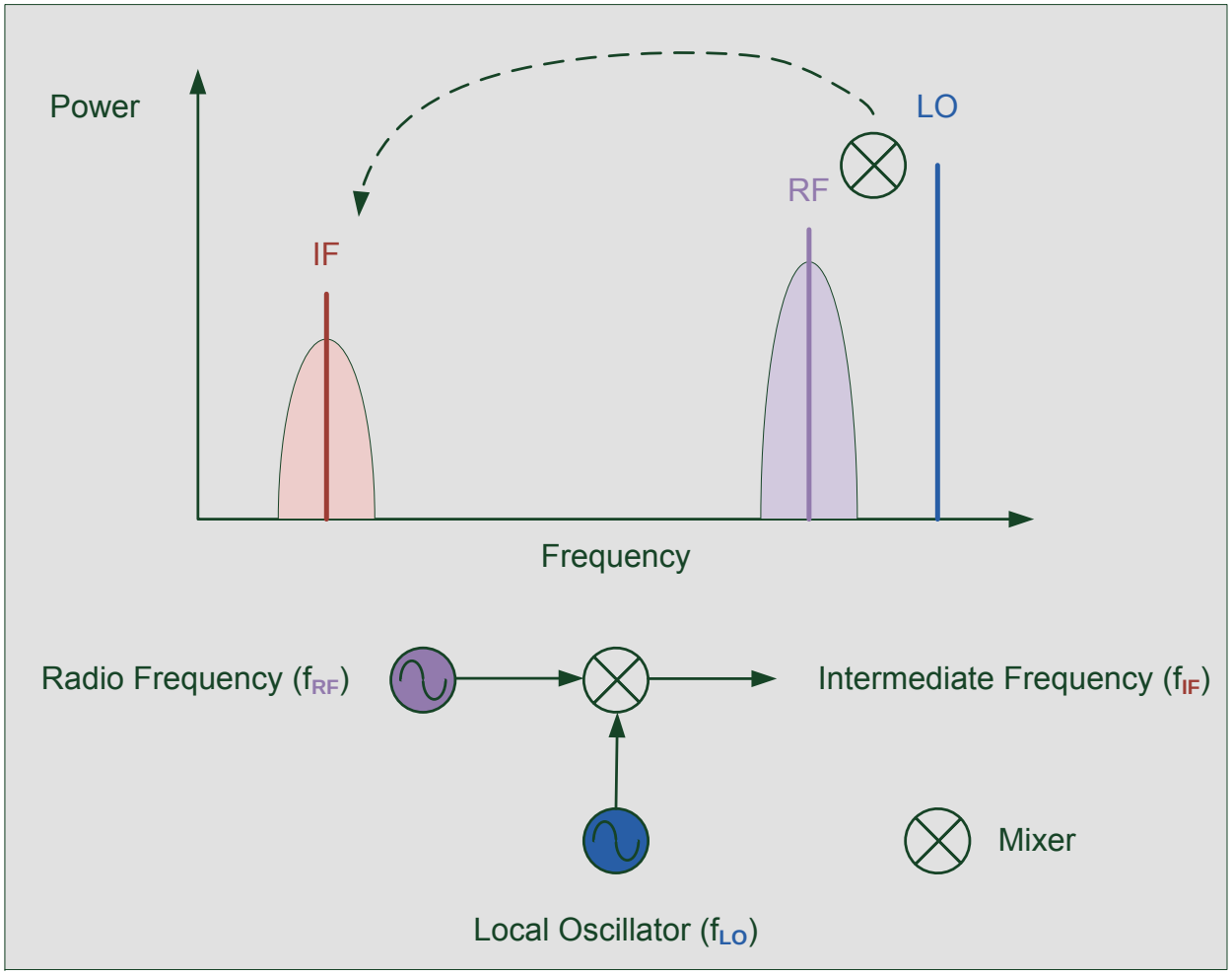
$f_{out} = f_{in1} \pm f_{in2}$

$f_{IF} = f_{LO} \pm f_{RF}$

Downconversion

$f_{IF} < f_{RF}$

$f_{IF} = | f_{LO} - f_{RF} |$



Applications

Direct Sampling

Arbitrary Analog Signals.

Detectors, Medical, Automotive, …

Downconversion

Sinusoidal continuous wave (CW) or square wave signals.

RF, Radar, Radio Astronomy, …

Sampling Speed vs. Power Consumption and Chip Price

Sampling Rate	Resolution	Mfg	Wattage per Channel	Price per Channel
125 MSPS	16-bit	ADI	375 mW	50 EUR
250 MSPS	16-bit	TI	820 mW	90 EUR
1 GSPS	14-bit	ADI	1650 mW	250 EUR
1.6 GSPS	12-bit	TI	1940 mW	800 EUR

What do I use?

Tradeoff between

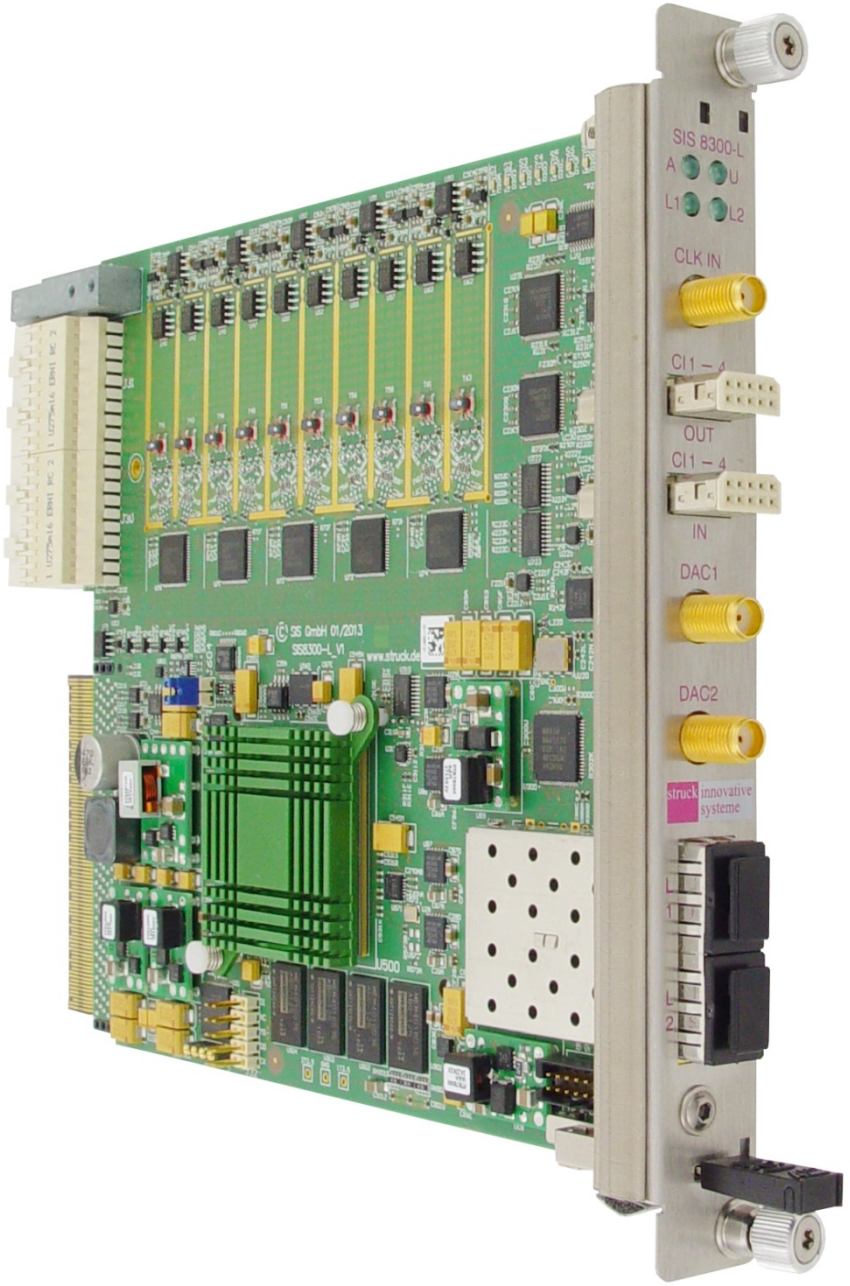
- Cost per channel
- Power consumption
- Available Conversion Speed/Resolution
- Required computing power to extract information from digitized signal
- CW or non CW signal
- …

SIS8300-L2 Digitizer Properties

- MTCA.4
- 4 lane PCI Express
- 10 channels 125 MS/s 16-bit ADC
- 10 MS/s to 125 MS/s per channel
- AC and DC input stage
- two 250 MS/s 16-bit DACs for fast feedback implementation
- high precision, flexible clock distribution logic
- Internal, front panel, RTM and backplane clock sources
- Programmable delay of twin ADC groups
- Gigabit Link Port implementation to backplane
- Double SFP cage for high speed system interconnects
- XC6VLX130T-2FFG1156C FPGA
- 4 x 4 GBit DDR3 Sample Memory
- additional point to point links over backplane
- In field firmware upgrade
- DESY MMC1.0

SIS8300-L/L2


© SIS GmbH 08/2014
SIS8300-L2_V1
www.struck.de


SIS 8300-L
A
U
L1
L2
CLK IN
CI1 – 4
OUT
CI1 – 4
IN
DAC1
DAC2
struck innovative systeme
© SIS GmbH 01/2013
SIS8300-L_V1
www.struck.de

Two Direct Sampling RTMs

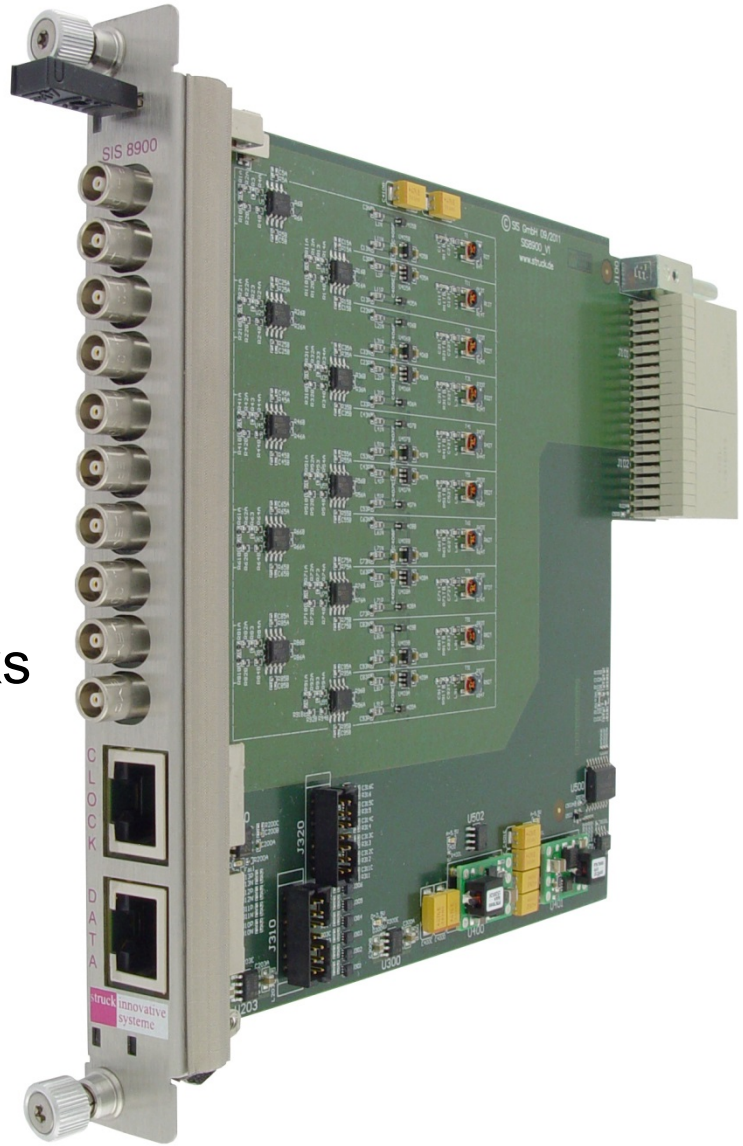
- SIS8900
- DS8VM1

Two Downconversion RTMs

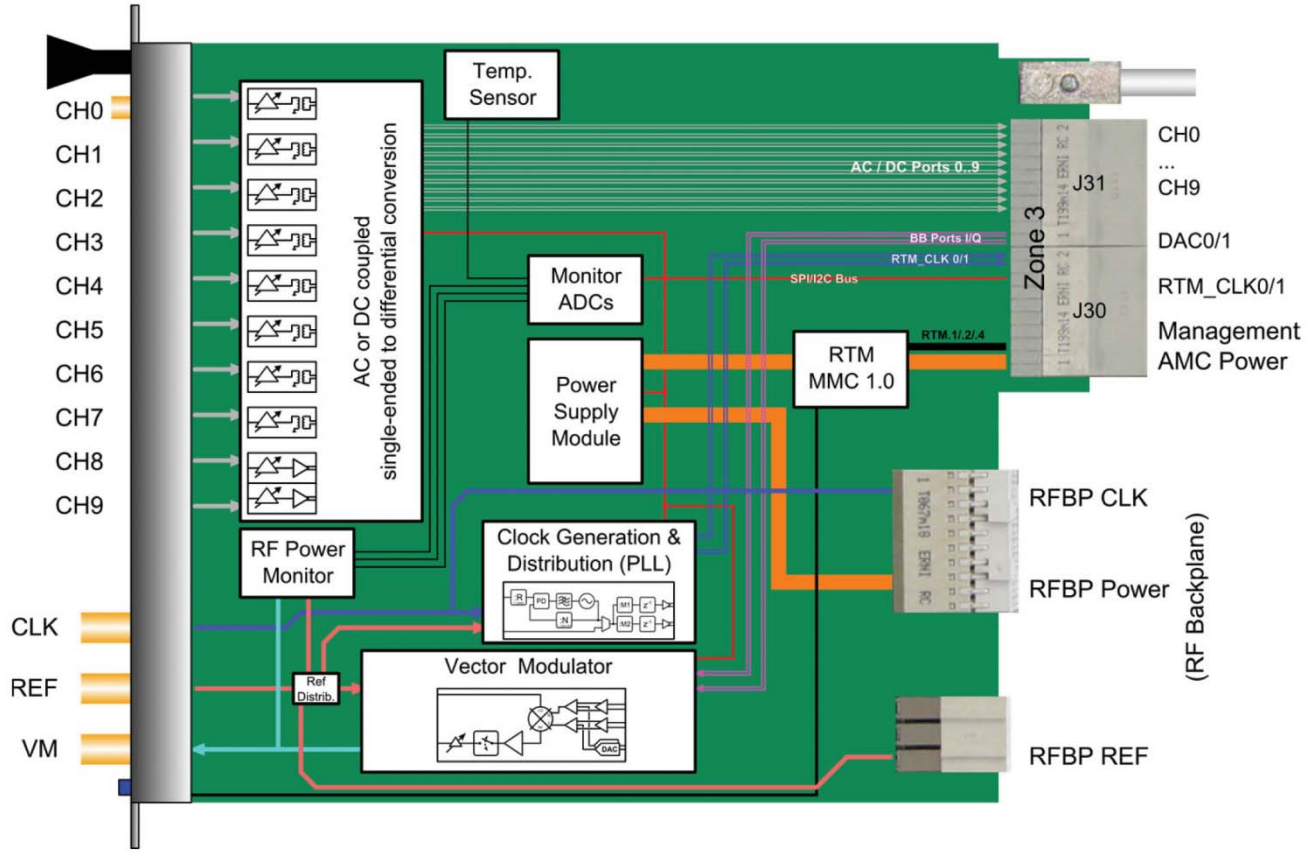
- DWC8300/DWC10
- DWC8VM1

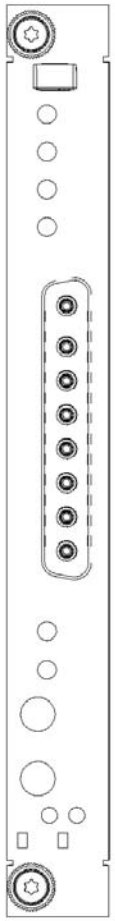
SIS8900 Single Ended Input RTM

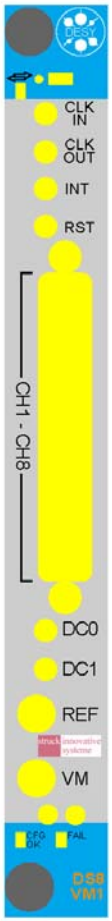
- 10 LEMO 00 connectors (FBM option)
- 50 Ohm input impedance
- -1 V,...,+1 V default input range
- analog signals can be routed to AC and DC input stage
- RJ45 jack for RTM clocks
- RJ45 jack for Digital I/O
- +5V, 250 mA power option for RJ45 jacks
- two metric on board pin headers for 6 LVDS input/output signals each



DS8VM1 Direct Sampling/ Vector Modulator RTM







- First R11 preseries batch in production

Under license of DESY

DWC8300/DWC10 Downconverter RTM

- 10 channel downconverter
- 700 MHz to 4 GHz
- FP and RF backplane

- R11 volume production

DWC8VM1 Downconverter/ Vector Modulator RTM

- 8 channel downconverter
- one channel vector modulator
- 700 MHz to 4 GHz
- R11 700, 1300 and 3000 MHz shipped,
- first R12 batch in production

Application Examples

Direct Sampling

100 Pixel Germanium Detector Readout
Petra III SIS8300-L/DRTM-DS10

Downconversion

XFEL Low Level Radio Frequency

SIS8300-L2S/DWC8300

SIS8325 250 MSPS 16-bit Digitizer (Helmholtz Validation fund project)

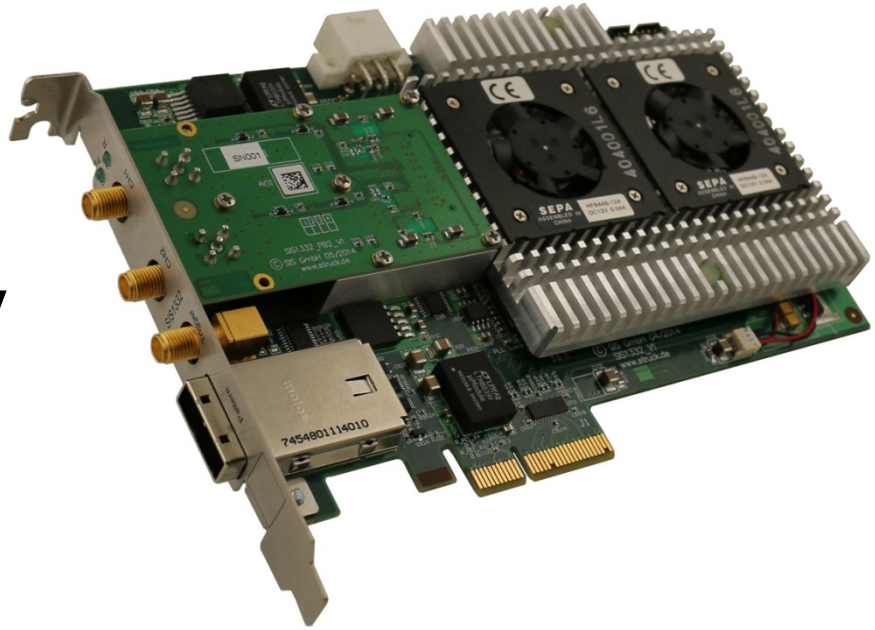
- TI ADS42LB69IRGC based
- Low clock jitter optimization
- Preseries end of Q1 2015 (postponed amid SIS8300L2 developments)
-

Applications

- BPM
- n/Gamma
- SiPM

Possible New GSPS Developments I (SIS8332)

- Port of SIS1332 PCI Express Card to MTCA
- 2 channels 1.6 GSPS 12-bit or
- 1 channel 3.2 GSPS 12-bit
- TI ADC12D1600RF based
- XC6VLX240T-2FFG1156C
- 4 Lane PCI Express
- 2 x 2 GByte DDR3 Memory



Possible New GSPS Developments II (SIS8310)

- 4-8 channels 1 GSPS 14-bit
- ADI AD9680 based (JESD204B)
- 10.8 vs 9.4 ENOB (vs TI 12-bit)
- FPGA Candidate: XCKU035 FGG1156
- 4 Lane PCI Express Gen 3
- DDR4 Memory/Hybrid Memory Cube?

Conclusion

In General

Ever increasing ADC performance as well as in digitization speed as in resolution

MTCA Related

More options for the MTCA community to base readout and controls systems on

Questions/Discussion

GL ISO 9001
GL Systems Certification