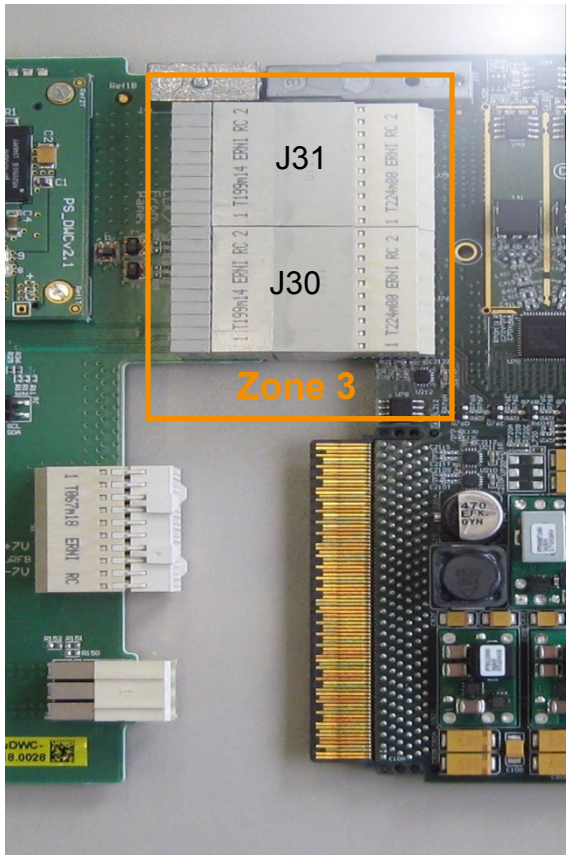
3rd MTCA Workshop for Industry and Research



Ratified Zone 3 classes to achieve enhanced AMC – RTM modularity

Dr. Frank Ludwig
for the LLRF Team
Hamburg, 10.12.2014

HELMHOLTZ GEMEINSCHAFT

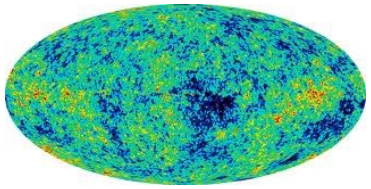
DESY

Motivation

FIL

> MTCA.4 – at the beginning → Idea of AMC – RTM pair

Problems:



- AMCs and RTMs do not fit together from different vendors
- Different life cycles for AMCs (digital signal processing) and RTMs (analog signal conditioning)
- Not all companies / labs have good digital and analog experts

> MTCA.4 – today → after 3 years class concept

... more than 25 different board types are class compatible ...

vadatech THE POWER OF VISION
IC INTERFACE CONCEPT ADVANCED ELECTRONIC SOLUTIONS
eicSys GmbH Embedded Integrated Control Systems
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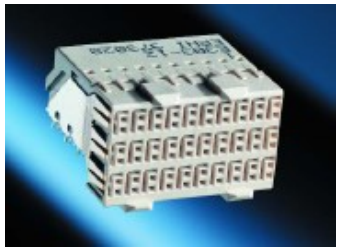
TEWS TECHNOLOGIES
IOxOS TECHNOLOGIES RELIABILITY BY DESIGN
SLAC NATIONAL ACCELERATOR LABORATORY
CAENels Gear For Science
SINTEC Microwave Systems GmbH

. . . and more boards will be compatible . . .

Zone 3 Class Concept in MTCA.4

- Class A1 mainly for analog signal transmission over Zone 3
- Class D1.x for digital signal transmission over Zone 3
- Class concept to be open for future signal types

- Requires
  - AMC FPGA module based,
  - 2 ADF 30 pair (Mid-size) connectors
  - Class A1 and D1.x needs not to be compatible



- Supports
  - LVDS, LVCMOS, OC, CML, analog differential
  - Digital signals (single-, diff.-ended, bi-directional)
  - Analog signals
  - High-speed links
  - non-FPGA low-jitter clock signals
  - non-FPGA signals with fixed direction
  - ps-stable timing signals

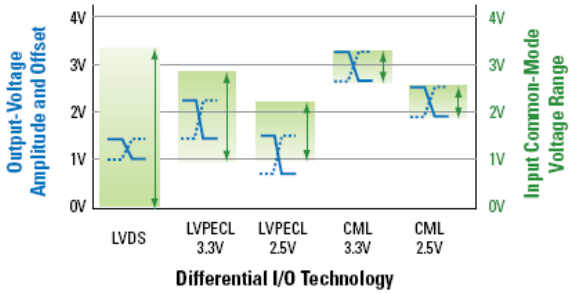


Figure 4-8. Differential Technologies

Ratified Zone 3 Class Recommendations http://mtca.desy.de/

Home | Community | Components | Support | Resources | Events | News | Contact

Zone 3 Pin Assignment Recommendation

The Zone 3 connector in the MTCA.4 standard connects the Advanced-Mezzanine Card (AMC) module and the Rear-Transition Module (RTM). MTCA.4 defines the management on the Zone 3 connector and provides enough freedom to the designers to use an application-specific pin assignment for an AMC and RTM pair.

To improve the compatibility and modularity of AMC and RTM boards we present a classification recommendation of the Zone 3 connector pin assignment for the MTCA.4 standard for different classes of applications. This implies a zone description, electrical specification, electrical protection sequence, electronic keying and grounding and shielding options.

in process to PICMG →

Class A1 Zone 3 Pin Assignment Recommendation for Analog Applications for AMC/RTM Boards in the MTCA.4 standard (Release Rev.A.4 - 26/08/2014 approved by the BoF Group 1)

→

Class D1.x Zone 3 Pin Assignment Recommendation for Digital Applications for AMC/RTM Boards in the MTCA.4 standard (Release Rev.A.3 - 21/03/2013 approved by the BoF Group 1)

To guarantee and maintain the AMC and RTM compatibility of previous, existing and future products only minor changes of released classes can be requested to the BoF Group 1 convener. The introduction of new fields of classes is supported by the BoF Group 1, contact person is the convener.

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Latest News

1 November 2014
The 3rd MicroTCA workshop for industry and research will take place from 10th to 11th December 2014 in Hamburg, Germany. More ...

08 April 2014
New offer from DESY for MMC Starter Kits. More ...

20 December 2013
2nd MTCA Workshop at DESY achieves record numbers of participants and industry. More ...

Class A1 (Analog signal transmission)

- ZONE 3 DESCRIPTION
- ZONE 3 PIN ASSIGNMENT
- ZONE 3 ELECTRICAL SPECIFICATION
- ZONE 3 QUIESCENT SIGNAL CONDITIONS
- ZONE 3 TERMINATION FOR UNUSED FUNCTIONS
- ZONE 3 SEQUENCE OF SIGNAL OCCUPATION
- REVISION CHANGES AND HISTORY

Deutsches Elektronen-Synchrotron
Ein Forschungszentrum der Helmholtz-Gemeinschaft

http://mtca.desy.de

Class A1

Zone 3 Connector Pin Assignment Recommendation for Analog Applications for AMC/µRTM Boards in the MTCA.4 standard

FEATURES

MTCA.4 management zone:
- Power, I²C, optional JTag support

Analog signal transmission zone:
- 10 channel AC-coupled differential input signals
- 10 channel DC-coupled differential input signals
- 5 channel DC-coupled differential output signals

Digital clock signal transmission zone:
- 6 AC-coupled differential inputs for low-jitter clock signals

User signal transmission zone:
- 6-12 LVDS inputs / outputs for user-configuration
- Optional 3 LVDS outputs with fixed output direction
- Optional high-speed link

Zone shielding:
- Supports ground shielding between zones

APPLICATIONS

- AMC / µRTM board design in MTCA.4 standard
- High-precision multi-channel analog-to-digital converters
- High-speed multi-channel analog-to-digital converters
- Multi-channel high-frequency down/up-converters
- Multi-channel sensor readout and output
- Analog signal conditioning boards
- Low-jitter clock signal sampling and clock recovery

GENERAL DESCRIPTION

This Class A1 pin assignment definition of the Zone 3 connector in the MTCA.4 standard is a recommendation mainly for AMC and µRTM boards transferring analog signals over the Zone 3 connector. This analog class is designed for two three row ADF Zone 3 connectors and AMC modules having an FPGA. The main goal is to classify the undefined Zone 3 pin assignment for applications to achieve a high compatibility between AMC and µRTM boards.

This Class A1 pin assignment requires a common µRTM management implementation to make AMC and µRTM boards compatible. Appropriate management interface templates for this Class are available on http://mtca.desy.de.

AMC ZONE 3 CONNECTOR PIN ASSIGNMENT RECOMMENDATION

Class A1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
FPGA / Standard Gbit-Link		3	D0+ / SFP-CLK+	D0- / SFP-CLK-	D1+ / SFP-RX+	D1- /SFP-RX-	D2+ / SFP-TX+	D2- / SFP-TX-
FPGA User-configuration		4	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
FPGA / Digital fixed I/O		6	D9+ / AMC_TCLK+	D9- / AMC_TCLK-	D10+ / OUT0+	D10- / OUT0-	D11+ / OUT1+	D11- / OUT1-
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		8	RTM_CLK4+	RTM_CLK4-	RTM_CLK2+	RTM_CLK2-	RTM_CLK5+	RTM_CLK5+
		9	RTM_CLK0+	RTM_CLK0-	RTM_CLK3+	RTM_CLK3-	RTM_CLK1+	RTM_CLK1-
Shielding		10	gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	1	CH9_PA+	CH9_PA-	DAC0+	DAC0-	CH9_TF+	CH9_TF-
		2	CH8_TF+	CH8_TF-	gnd	gnd	CH8_PA+	CH8_PA-
		3	CH7 PA+	CH7 PA-	DAC1+	DAC1-	CH7 TF+	CH7 TF-
		4	CH6_TF+	CH6_TF-	gnd	gnd	CH6_PA+	CH6_PA-
		5	CH5 PA+	CH5 PA-	DAC2+	DAC2-	CH5 TF+	CH5 TF-
		6	CH4_TF+	CH4_TF-	gnd	gnd	CH4_PA+	CH4_PA-
		7	CH3_PA+	CH3_PA-	DAC3+	DAC3-	CH3_TF+	CH3_TF-
		8	CH2_TF+	CH2_TF-	gnd	gnd	CH2_PA+	CH2_PA-
		9	CH1_PA+	CH1_PA-	DAC4+	DAC4-	CH1_TF+	CH1_TF-
		10	CH0_TF+	CH0_TF-	gnd	gnd	CH0_PA+	CH0_PA-

Table 1 : Pin assignment of Class A1, AMC side view

ZONE DESCRIPTION

As depicted in Table 1, the zones in the analog Class A1 consists of a management zone, user zone, digital clock zone and a zone for analog differential signals. The signal placement and filling sequence is done such, that the most sensitive signals have to be filled-up from connector (J31 row 10) to (J30 row 3) and signals emitting high distortions filled-up vice versa.

The management zone (J30 row 1-2) is reserved for the µRTM management in the MTCA.4 standard. The user zone (J30 row 3-6) houses input and output signals in LVDS, CMOS or open collector (OC) level, which can be used for general purpose, e.g. I²C communication for slow board diagnostics. To achieve a high compatibility between AMC and µRTM boards, these inputs and outputs should be programmable in direction and signal type, preferable by an FPGA located on the AMC side.

Rev.A.4, 26/08/2014

Class A1 (Analog signal transmission)

> Zone 3 Pin Assignment (AMC side, Rev.A.4.):

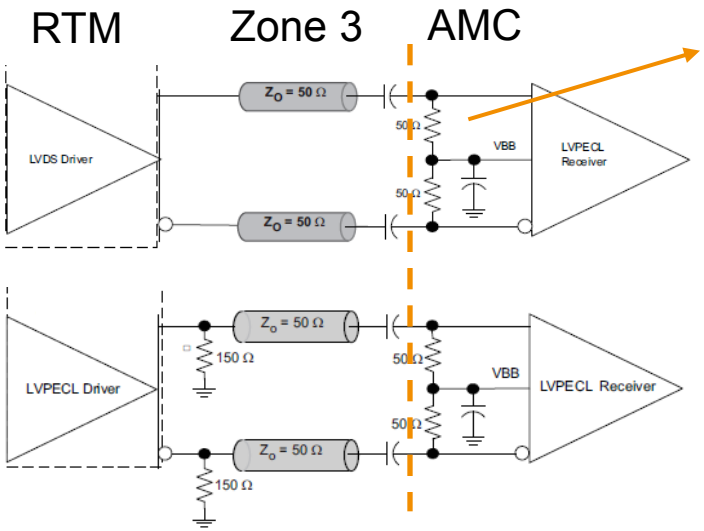
Class A1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
FPGA / Standard Gbit-Link		3	D0+ / SFP-CLK+	D0- / SFP-CLK-	D1+ / SFP-RX+	D1- /SFP-RX-	D2+ / SFP-TX+	D2- / SFP-TX-
FPGA User-configuration		4	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
FPGA / Digital fixed I/O		6	D9+ / AMC_TCLK+	D9- / AMC_TCLK-	D10+ / OUT0+	D10- / OUT0-	D11+ / OUT1+	D11- / OUT1-
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		8	RTM_CLK4+	RTM_CLK4-	RTM_CLK2+	RTM_CLK2-	RTM_CLK5+	RTM_CLK5+
		9	RTM_CLK0+	RTM_CLK0-	RTM_CLK3+	RTM_CLK3-	RTM_CLK1+	RTM_CLK1-
Shielding		10	gnd	gnd	gnd	gnd	gnd	gnd
Analog signals	J31	1	CH9_PA+	CH9_PA-	DAC0+	DAC0-	CH9_TF+	CH9_TF-
		2	CH8_TF+	CH8_TF-	gnd	gnd	CH8_PA+	CH8_PA-
		3	CH7_PA+	CH7_PA-	DAC1+	DAC1-	CH7_TF+	CH7_TF-
		4	CH6_TF+	CH6_TF-	gnd	gnd	CH6_PA+	CH6_PA-
		5	CH5_PA+	CH5_PA-	DAC2+	DAC2-	CH5_TF+	CH5_TF-
		6	CH4_TF+	CH4_TF-	gnd	gnd	CH4_PA+	CH4_PA-
		7	CH3_PA+	CH3_PA-	DAC3+	DAC3-	CH3_TF+	CH3_TF-
		8	CH2_TF+	CH2_TF-	gnd	gnd	CH2_PA+	CH2_PA-
		9	CH1_PA+	CH1_PA-	DAC4+	DAC4-	CH1_TF+	CH1_TF-
		10	CH0_TF+	CH0_TF-	gnd	gnd	CH0_PA+	CH0_PA-

- MTCA.4 management
- 10 analog AC-coupled differential inputs
- 10 analog DC-coupled differential inputs
- 5 analog DC-coupled differential outputs
- 6 LVDS inputs for low-jitter clock signals
- 6 LVDS inputs / outputs
- 3 LDVS fixed outputs (non FPGA driven)
- Dual high-speed link support

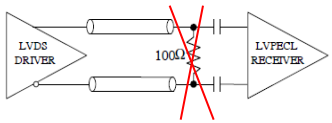
Class A1 (Analog signal transmission)

- Low jitter clocks termination (AMC side, Rev.A.4.):

Class A1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
FPGA / Standard Gbit-Link		3	LVDS/LVCMOS/OC-I/O or LVDS-I	LVDS/LVCMOS/OC-I/O or LVDS-I	LVDS/LVCMOS/OC-I/O or CML-I	LVDS/LVCMOS/OC-I/O or CML-I	LVDS/LVCMOS/OC-I/O or CML-O	LVDS/LVCMOS/OC-I/O or CML-O
FPGA User-configuration		4	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
		5	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
FPGA / Digital fixed I/O		6	LVDS/LVCMOS/OC-I/O or LDVS-O	LVDS/LVCMOS/OC-I/O or LDVS-O	LVDS/LVCMOS/OC-I/O or LDVS-O	LVDS/LVCMOS/OC-I/O or LDVS-O	LVDS/LVCMOS/OC-I/O or LDVS-O	LVDS/LVCMOS/OC-I/O or LDVS-O
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs		8	Differential AC-coupled, ±350mV...±1V / I, 100Ω		Differential AC-coupled, ±350mV...±1V / I, 100Ω		Differential AC-coupled, ±350mV...±1V / I, 100Ω	
		9	Differential AC-coupled, ±350mV...±1V / I, 100Ω		Differential AC-coupled, ±350mV...±1V / I, 100Ω		Differential AC-coupled, ±350mV...±1V / I, 100Ω	
Shielding		10	gnd	gnd	gnd	gnd	gnd	gnd
	J31	1	Differential 0 - ±1V / I, 100Ω		Differential 0 - ±20mA / 0 - ±1V / O, 100Ω		Differential 0 - ±1V / I, 100Ω	
		2	Differential 0 - ±1V / I, 100Ω		gnd	gnd		
		3	Differential 0 - ±1V / I, 100Ω					



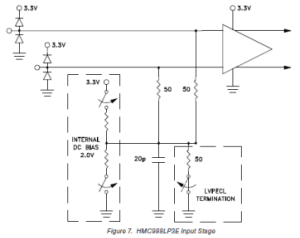
- Termination and level adjustment <u>after</u> AC-coupling at the „end“.



e.g. on-chip termination ...

HMC988LP3E

Hittite MICROWAVE CORPORATION



Class A1 (Analog signal transmission)

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> Introdution of subclasses A1.0, A1.0C, A1.1CO (AMC side, Rev.A.4.):

- A simple E-keying via Class IDs requires a class for all boards -> backward compatibility

- Notation: „A1.x“ – x number of GTPs (SFP)
  „C“ – Clock option (AMC_TCLK)
  „O“ – Output option (OUT0,1)

- Optional: Covering subclasses via assembly options (AMC: 1 Class in the FRU, RTM: may be more)

Subclass A1.0			a	b	c	d	e	f
Pin-assignment								
FPGA	J30	3	D0+	D0-	D1+	D1	D2+	D2-
FPGA User-configuration		4	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
FPGA		6	D9+	D9-	D10+	D10-	D11+	D11-
Electrical specification								
FPGA	J30	3	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
FPGA User-configuration		4	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
		5	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
FPGA		6	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O

Subclass A1.0C			a	b	c	d	e	f
Pin-assignment								
FPGA	J30	3	D0+	D0-	D1+	D1	D2+	D2-
FPGA User-configuration		4	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
FPGA / Digital fixed I/O		6	AMC_TCLK+	AMC_TCLK-	D10+	D10-	D11+	D11-
Electrical specification								
FPGA	J30	3	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
FPGA User-configuration		4	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
		5	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
FPGA / Digital fixed I/O		6	LVDS - O	LVDS - O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O

Subclass A1.1CO			a	b	c	d	e	f
Pin-assignment								
Standard Gbit-Link	J30	3	SFP-CLK+	SFP-CLK-	SFP-RX+	SFP-RX-	SFP-TX+	SFP-TX-
FPGA User-configuration		4	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
Digital fixed I/O		6	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
Electrical specification								
Standard Gbit-Link	J30	3	LVDS-I	LVDS-I	CML-I	CML-I	CML-O	CML-O
FPGA User-configuration		4	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
		5	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O	LVDS/LVCMOS/OC-I/O
Digital fixed I/O		6	LDVS-O	LDVS-O	LDVS-O	LDVS-O	LDVS-O	LDVS-O

Class A1 (Analog signal transmission)

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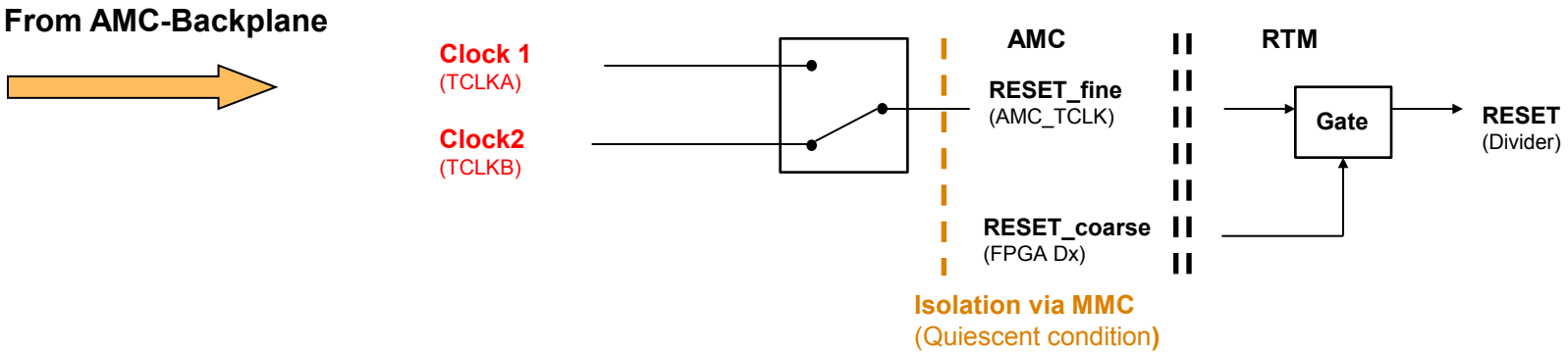
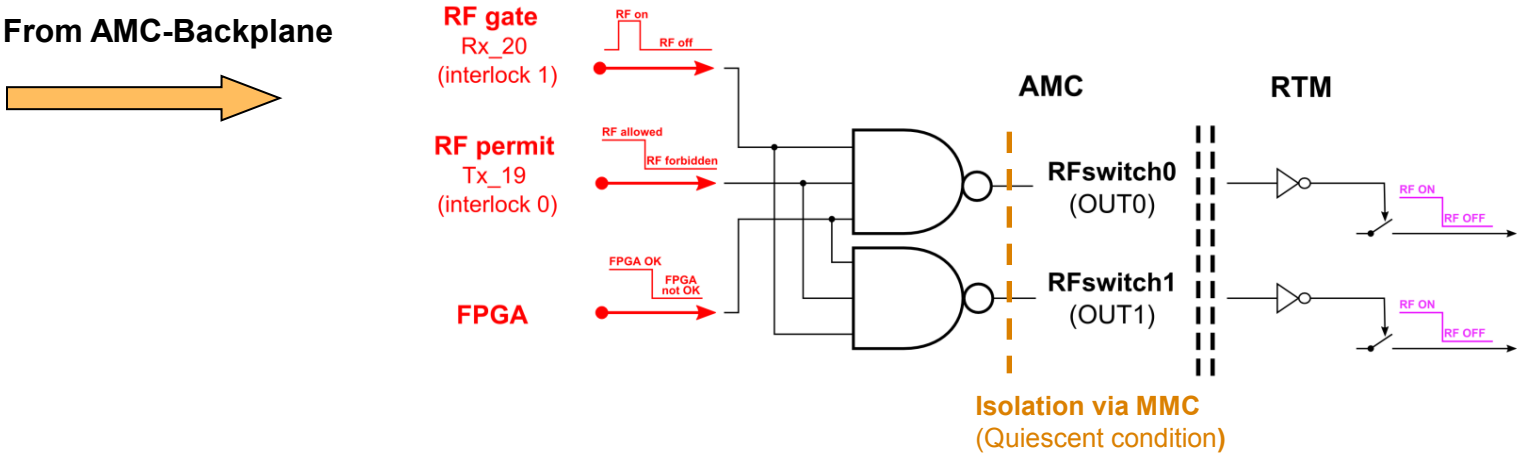
Examples : AMC_TCLK (non-FPGA driven)



Examples : OUT0, OUT1 (non-FPGA driven)



Class D1.0 (Digital signal transmission)

> Zone 3 Pin Assignment (AMC side, Rev.A.3.):

Class D1.0 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5	P30_IO+ / CC *	P30_IO- / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+ / CC *	P30_IO- / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User -configuration	J31	1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		4	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		5	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		6	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		7	P31_IO+ / CC*	P31_IO- / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		8	P31_IO+ / CC*	P31_IO- / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		9	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		10	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-

D1.0 Subclass :

- MTCA.4 management
- 48 LVDS inputs / outputs

(+) High compatibility, also to existing boards

(-) No High-speed link support
(-) No support of low-jitter clocks
(-) No support of non-FPGA output signals

Class D1.1 (Digital signal transmission)

> Zone 3 Pin Assignment (AMC side, Rev.A.3.):

Class D1.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5	P30_IO+ / CC *	P30_IO- / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+ / CC *	P30_IO- / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User Configuaration	J31	1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		4	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		5	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		6	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		7	P31_IO+ / CC*	P31_IO- / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		8	P31_IO+ / CC*	P31_IO- / CC*	P31_IO+	P31_IO-	P31_IO+	P31_IO-
Standard Gbit-Links		9	GTP0-1_CLK_IN+	GTP0-1_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-1_CLK_OUT+	GTP0-1_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

D1.1 Subclass :

- MTCA.4 management
- 42 LVDS inputs / outputs
- 2 High-speed links
- 2 LVDS signals for low-jitter clocks
- 4 LVDS outputs

( ) Moderate compatibility

(+) High-speed link support

(+) Support of low-jitter clocks

(+) Support of non-FPGA output signals

Class D1.2 (Digital signal transmission)

> Zone 3 Pin Assignment (AMC side, Rev.A.3.):

Class D1.2 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+ / CC *	P30_IO+ / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User Configuaration	J31	1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		3	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		4	P31_IO+ / CC	P31_IO- / CC	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		5	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
		6	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+ / CC	P31_IO- / CC
Standard Gbit-Links		7	P31_IO+ / CC*	P31_IO- / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8	P31_IO+ / CC*	P31_IO- / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9	GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

D1.2 Subclass :

- MTCA.4 management
- 38 LVDS inputs / outputs
- 4 High-speed links
- 2 LVDS signals for low-jitter clocks
- 4 LVDS outputs

( ) Moderate compatibility

(+) High-speed link support

(+) Support of low-jitter clocks

(+) Support of non-FPGA output signals

Class D1.3 (Digital signal transmission)

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> Zone 3 Pin Assignment (AMC side, Rev.A.3.):

Class D1.3 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
User -configuration		5	P30_IO+ / CC *	P30_IO- / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		6	P30_IO+ / CC *	P30_IO- / CC *	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		7	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		8	P30_IO+	P30_IO-	P30_IO+	P30_IO-	P30_IO+ / CC	P30_IO+ / CC
		9	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
		10	P30_IO+ / CC*	P30_IO+ / CC*	P30_IO+	P30_IO-	P30_IO+	P30_IO-
User Configuaration	J31	1	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
		2	P31_IO+	P31_IO-	P31_IO+	P31_IO-	P31_IO+	P31_IO-
Standard Gbit-Links		3	P31_IO+ / CC	P31_IO- / CC	GTP7_RX+	GTP7_RX-	GTP7_TX+	GTP7_TX-
		4	P31_IO+ / CC	P31_IO- / CC	GTP6_RX+	GTP6_RX-	GTP6_TX+	GTP6_TX-
		5	GTP4-7_CLK_IN+	GTP4-7_CLK_IN-	GTP5_RX+	GTP5_RX-	GTP5_TX+	GTP5_TX-
		6	GTP4-7_CLK_OUT+	GTP4-7_CLK_OUT-	GTP4_RX+	GTP4_RX-	GTP4_TX+	GTP4_TX-
		7	P31_IO+ / CC*	P31_IO- / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8	P31_IO+ / CC*	P31_IO- / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9	GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

D1.3 Subclass :

- MTCA.4 management
- 28 LVDS inputs / outputs
- 8 High-speed links
- 2 LVDS signals for low-jitter clocks
- 4 LVDS outputs

( ) Moderate compatibility

(+) High-speed link support

(+) Support of low-jitter clocks

(+) Support of non-FPGA output signals

Class D1.4 (Digital signal transmission)

> Zone 3 Pin Assignment (AMC side, Rev.A.3.):

Class D1.4 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Digital clocks fixed I/O		3	AMC_CLK1+	AMC_CLK1-	RTM_CLK1+	RTM_CLK1-	OUT2+	OUT2-
		4	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
Standard Gbit-Links		5	P30_IO+ / CC *	P30_IO+ / CC *	GTP15_RX+	GTP15_RX-	GTP15_TX+	GTP15_TX-
		6	P30_IO+ / CC *	P30_IO+ / CC *	GTP14_RX+	GTP14_RX-	GTP14_TX+	GTP14_TX-
		7	GTP12-15_CLK_IN+	GTP12-15_CLK_IN-	GTP13_RX+	GTP13_RX-	GTP13_TX+	GTP13_TX-
		8	GTP12-15_CLK_OUT+	GTP12-15_CLK_OUT-	GTP12_RX+	GTP12_RX-	GTP12_TX+	GTP12_TX-
		9	P30_IO+ / CC*	P30_IO+ / CC*	GTP11_RX+	GTP11_RX-	GTP11_TX+	GTP11_TX-
		10	P30_IO+ / CC*	P30_IO+ / CC*	GTP10_RX+	GTP10_RX-	GTP10_TX+	GTP10_TX-
Standard Gbit-Links	J31	1	GTP8-11_CLK_IN+	GTP8-11_CLK_IN-	GTP9_RX+	GTP9_RX-	GTP9_TX+	GTP9_TX-
		2	GTP8-11_CLK_OUT+	GTP8-11_CLK_OUT-	GTP8_RX+	GTP8_RX-	GTP8_TX+	GTP8_TX-
		3	P31_IO+ / CC	P31_IO- / CC	GTP7_RX+	GTP7_RX-	GTP7_TX+	GTP7_TX-
		4	P31_IO+ / CC	P31_IO- / CC	GTP6_RX+	GTP6_RX-	GTP6_TX+	GTP6_TX-
		5	GTP4-7_CLK_IN+	GTP4-7_CLK_IN-	GTP5_RX+	GTP5_RX-	GTP5_TX+	GTP5_TX-
		6	GTP4-7_CLK_OUT+	GTP4-7_CLK_OUT-	GTP4_RX+	GTP4_RX-	GTP4_TX+	GTP4_TX-
		7	P31_IO+ / CC*	P31_IO- / CC*	GTP3_RX+	GTP3_RX-	GTP3_TX+	GTP3_TX-
		8	P31_IO+ / CC*	P31_IO- / CC*	GTP2_RX+	GTP2_RX-	GTP2_TX+	GTP2_TX-
		9	GTP0-3_CLK_IN+	GTP0-3_CLK_IN-	GTP1_RX+	GTP1_RX-	GTP1_TX+	GTP1_TX-
		10	GTP0-3_CLK_OUT+	GTP0-3_CLK_OUT-	GTP0_RX+	GTP0_RX-	GTP0_TX+	GTP0_TX-

D1.4 Subclass :

- MTCA.4 management
- 16 LVDS inputs / outputs
- 16 High-speed links
- 2 LVDS signals for low-jitter clocks
- 4 LVDS outputs

( ) Moderate compatibility

(+) High-speed link support

(+) Support of low-jitter clocks

(+) Support of non-FPGA output signals

Class A2.1 (Analog signal transmission – 32 ADCs)

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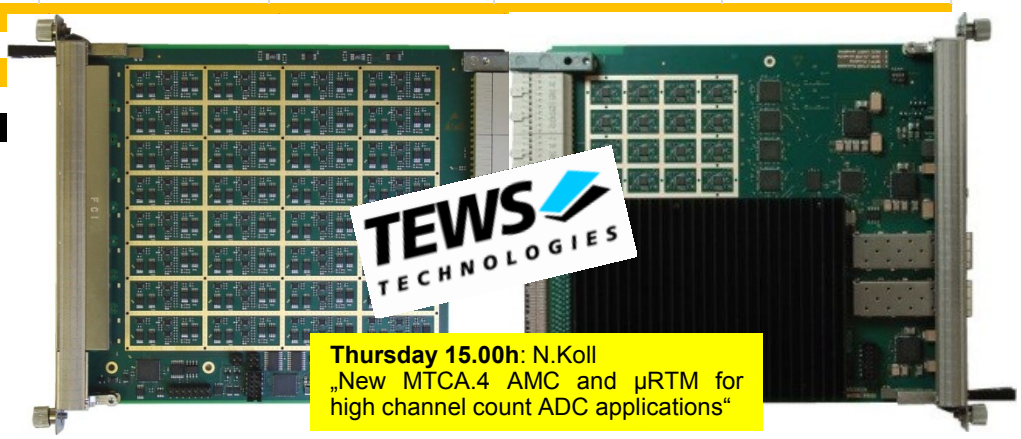
> Zone 3 Pin Assignment (AMC side, Rev.A.1.):

NEW!

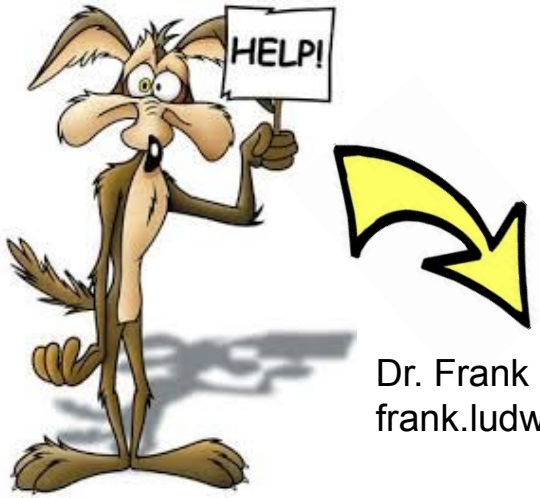
Class A2.1 / Zone			a	b	c	d	e	f
MTCA.4 management	J30	1	PWRA1	PWRB1	PS#	SDA	TCK	TDO
		2	PWRA2	PWRB2	MP	SCL	TDI	TMS
Standard Gbit-Link		3	SFP-CLK+	SFP-CLK-	SFP-RX+	SFP-RX-	SFP-TX+	SFP-TX-
User-configuration		4	D3+	D3-	D4+	D4-	D5+	D5-
		5	D6+	D6-	D7+	D7-	D8+	D8-
Digital fixed I/O		6	AMC_TCLK+	AMC_TCLK-	OUT0+	OUT0-	OUT1+	OUT1-
Shielding		7	gnd	gnd	gnd	gnd	gnd	gnd
Digital clock inputs / Analog Signals		8	AMC_CLK0+	AMC_CLK0-	DAC3+	DAC3-	DAC2+	DAC2-
		9	RTM_CLK0+	RTM_CLK0-	DAC1+	DAC1-	DAC0+	DAC0-
		10	RTM_CLK1+	RTM_CLK1-	CH31+	CH31-	CH30+	CH30-
Analog signals	J31	1	CH29+	CH29-	CH28+	CH28-	CH27+	CH27-
		2	CH26+	CH26-	CH25+	CH25-	CH24+	CH24-
		3	CH23+	CH23-	CH22+	CH22-	CH21+	CH21-
		4	CH20+	CH20-	CH19+	CH19-	CH18+	CH18-
		5	CH17+	CH17-	CH16+	CH16-	CH15+	CH15-
		6	CH14+	CH14-	CH13+	CH13-	CH12+	CH12-
		7	CH11+	CH11-				
		8	CH8+	CH8-				
		9	CH5+	CH5-				
		10	CH2+	CH2-				

- TAMC532 (32 Channel ADC)
- TRTM532 (32 Channel Shaper)



Thursday 15.00h: N.Koll
„New MTCA.4 AMC and µRTM for high channel count ADC applications“

Wishlist . . .



Dr. Frank Ludwig
frank.ludwig@desy.de

Thanks for your attention!

MTCA.4 : Electrical Protection during RTM Insertion

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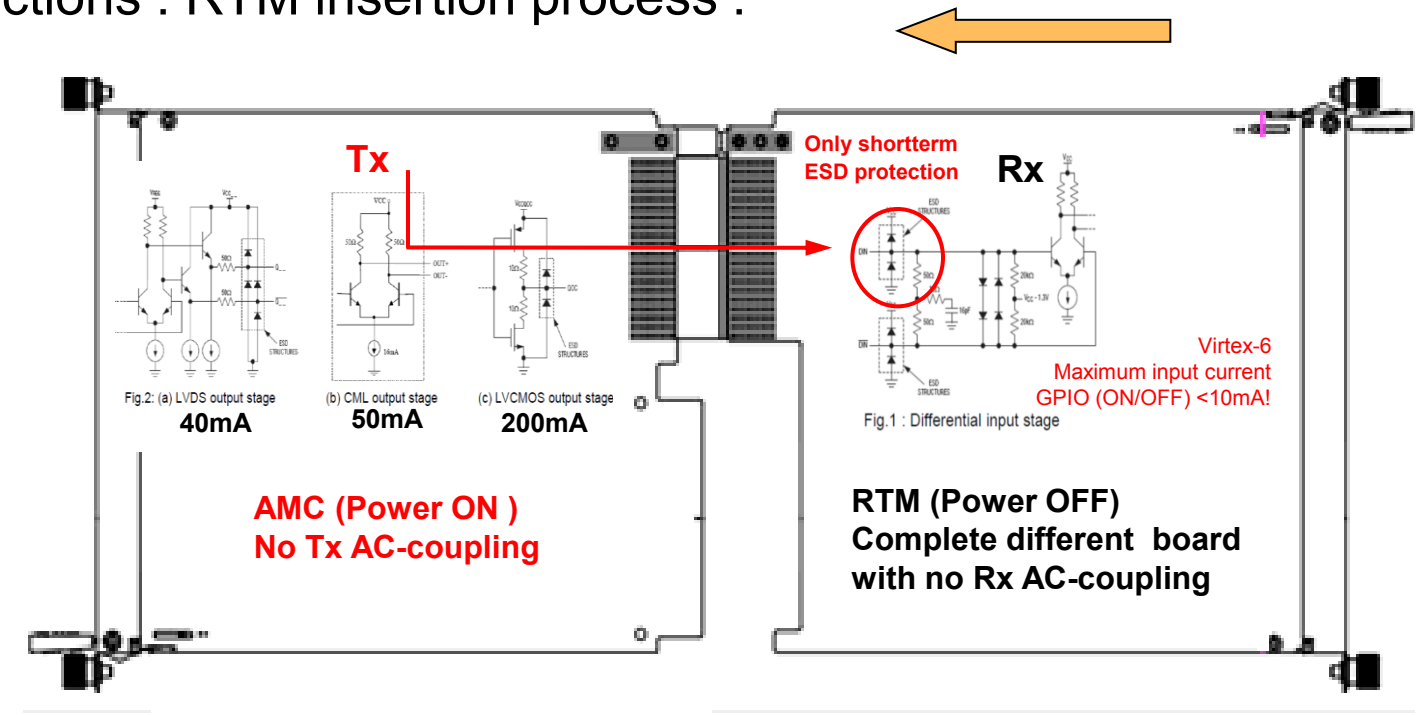
- Quiesce actions : RTM insertion process :



- Class A1, Class D1.2 → GTP Tx AC-coupling over Zone 3 is a must.

	7	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
	8	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA	Disabling via FPGA
Standard Gbit-Links	9			Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled
	10	Disabling via Buffer	Disabling via Buffer	Idle state, RTM AC-coupled	Idle state, RTM AC-coupled	Idle state, AMC AC-coupled	Idle state, AMC AC-coupled