MicroTCA.4 Event Receiver for MRF Timing System

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MicroTCA.4 Learning Curve

- Lots of documentation split around in various specifications: ATCA, AMC, mTCA, mTCA.4, etc.
- MMC – Module Management Controller
  - Study of MMC implementations
  - Many commercial providers, both high and low priced
  - DESY implementation
- Electrical interface simple, not too many pins required
- Most difficult platform to design on (so far)
  - MMC needs to run before you get main power to your board
  - FRU information has to be correct
  - Remaining uncertainties about responsibilities
- Development system is unpredictable
  - Not all boards always detected by MCH – PCIe link down
  - Sometimes need to reboot CPU and/or MCH or power cycle
  - Issues with Xilinx Vivado tools and USB programming dongle
  - Issues with Atmel Studio and programming dongle

MicroTCA.4 Event Receiver Status

- Project started in 2013, has been a lower priority project and subject to delays because of “other work”
- mTCA.4 development starter kit ordered in mid. 2013, delivery in late 2013 due to power supply issues
- Learned about DESY MMC implementation at ICALEPCS ´13 from Kay Rehlich
- Prototype layout “almost ready” one year ago
- New ideas from last mTCA workshop in Dec. 2013
- Prototype hardware April 2014
- MMC code from DESY in May 2014, in ~1 week prototype was powered up in crate
- Problems getting PCIe link up in June, resolved in 1 week with help of Vollrath Dirksen (N.A.T.)
- Due to limited time resources no progress for several months
- Now both Event Receiver and Event Generator code ported
- BRAM corruption issue detected – wrong power supply for BRAMs
  - New PCB required

MicroTCA.4 Hardware Considerations

Initial target to build functional prototype to serve as both Event Receiver and Event Generator

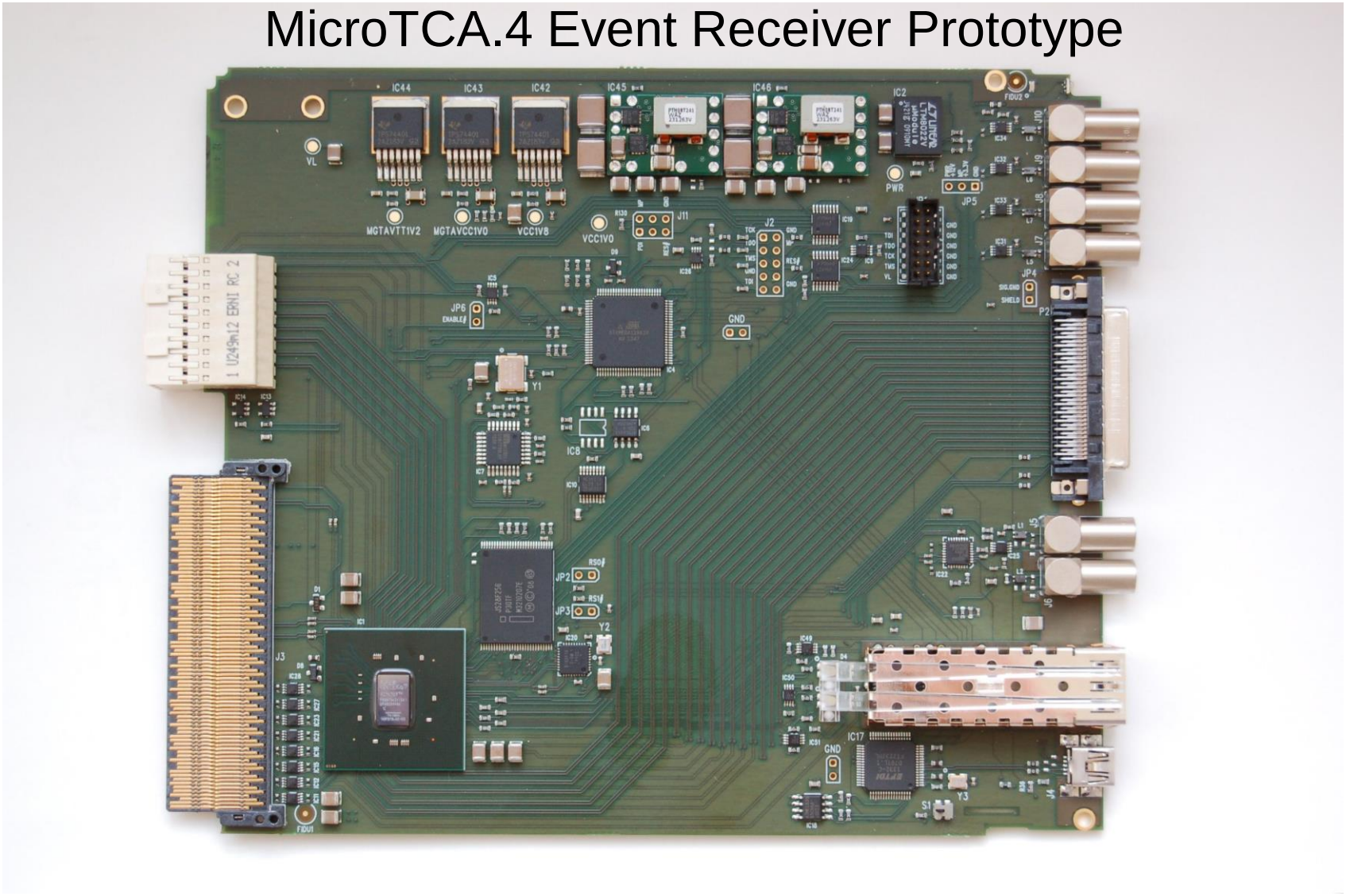
- Xilinx Kintex-7 XC7K70T FPGA was chosen based on experiments with KC705 evaluation module
- Atmel XMEGA128A1 as MMC (supported by DESY MMC software)
- Factory programming through USB (no special adapters/dongles)
- Headers for development dongles
  - Xilinx FPGA cable header
  - Atmel PDI header
- FTDI FT2232HL dual serial port / JTAG USB interface
  - Not supported by Xilinx / Atmel
  - However supported by xc3sprog (http://xc3sprog.sourceforge.net)
  - JTAG programming of Xilinx FPGAs works!
  - Atmel XMEGA128A1 flash programming works!
  - Serial interface to MMC

➢ Not all of these goal were reached

MicroTCA.4 EVR Hardware Features

- Xilinx Kintex-7 XC7K70T FPGA chosen
- Atmel XMEGA128A1 as MMC (supported by DESY MMC software)
- 4 LVTTL Outputs (LEMO)
- 2 TTL inputs
- microSCSI connector for IFB-300 Interface Box with Universal I/O modules
- mTCA.4 backplane 8 bussed & 4 PTP lines usable
- Support for rear I/O
- Unfortunately front panel space not usable for Universal I/O

MicroTCA.4 Event Receiver Prototype



MicroTCA.4 Issues - MMC

MMC software from DESY

- Hardware and software were changed during the process quite much, however pins are easy to remap in Atmel Studio projects
- Easy to get running
- Limited/missing documentation
- Unclear responsibilities between MCH / MMC
- Board is running but if values are out of range who is responsible to take action?

MicroTCA.4 Issues – PCI Express

PCI Express endpoint in FPGA

+ simplifies PCI design
+ reduces component count
- Increases design implementation time, currently ~15-20 min synthesis and implementation time for Event Receiver design using Xilinx Vivado
- Requires booting of CPU to get working, hot swap issues

MicroTCA.4 Event Receiver – Future Plans

- Need to roll out new PCB version
- Rear I/O
  - Request for at least TTL level outputs
  - mTCA.4 mechanics does not allow using pluggable Universal I/O modules
  - Aware of “standard” for RTMs
  - Is there a digital COTS I/O RTM available with TTL/other type of I/O
- How to support RF backplane?

MRF Timing System – Future Plans

- Support higher Frame rate > 125 MHz
- Need to implement fiber delay drift compensation
- Incompatibilities with existing products

MicroTCA.4 – Summary
What I want to talk about this week

- Backplane bussed/PTP signals. Anyone using these?
  - Cannot be directly connected to FPGA
  - How are you driving these signals?
- Rear I/O
  - Request for at least TTL level outputs
  - mTCA.4 mechanics does not allow using pluggable Universal I/O modules
- RF backplane
- PCIe hot-plug, can I avoid rebooting after reloading the FPGA?
- MMC responsibilities, temperature monitoring, voltage monitoring
- Testing: what do I need to test?
- Is there a mailing list or forum for mTCA.4 developers? Suggestion: something similar to EPICS tech-talk mailing list would make mTCA.4 more popular easier to get started with – mtca help exists, how about making this “open”?