MTCA White Rabbit Timing Receiver for FAIR

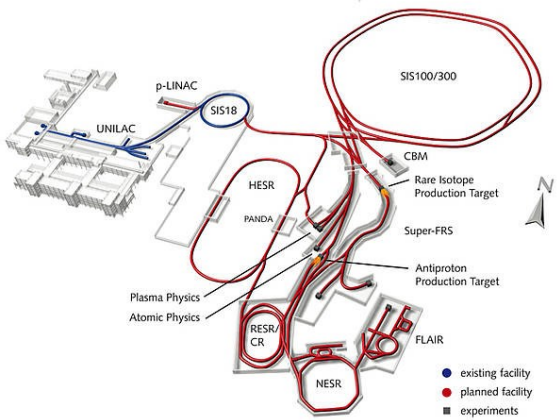
Marko Mehle

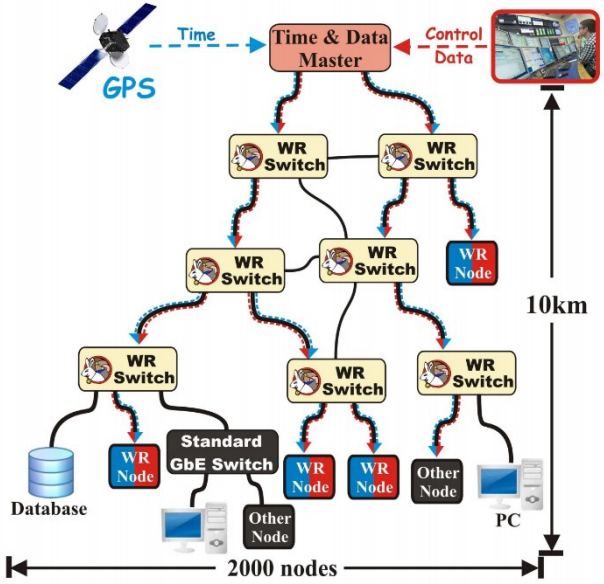
(on behalf of Rok Tavčar and Tom Slejko)

marko.mehle@cosylab.com

FAIR

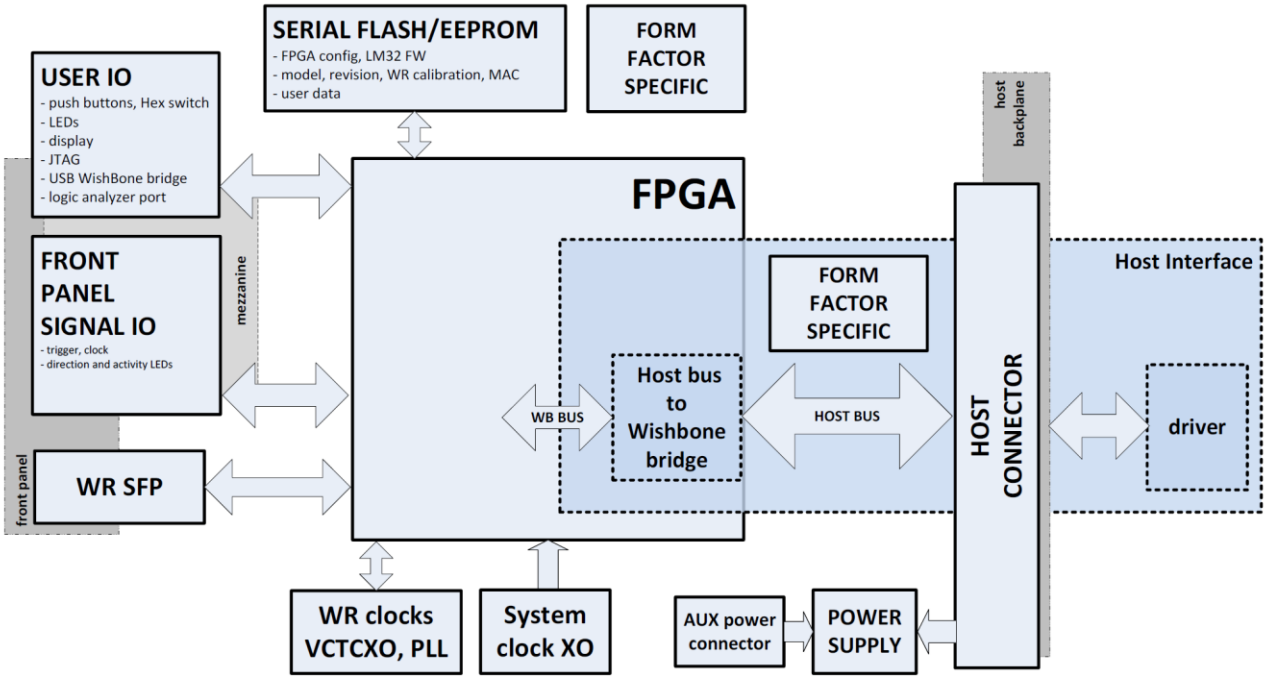
- Facility for Antiproton and Ion Research at GSI in Darmstadt, Germany.
- Accelerator complex consisting of many accelerators (SIS18, SIS100/300, RESR, HESR)
- Parallel execution of different beam production chains.
- White Rabbit (WR) network used as the general timing system.
- WR networks are based on the notion of absolute time.
- Gigabit-Ethernet, IEEE1588-2008 (PTP), precise knowledge of the link delay and Synchronous Ethernet.
- Time synchronization is achieved by adjusting the clock phase (125 MHz carrier) and offset (UTC).





FAIR Timing Receiver

- Clock and time synchronization with a Clock Master according to the WR specifications.
- Record arrival time of a digital pulse in front panel IO.
- Generate a digital pulse or a pulse sequence at a given time.
- Generate clock signals with a given frequency and phase.
- Generate specified interrupts on the host at given times.



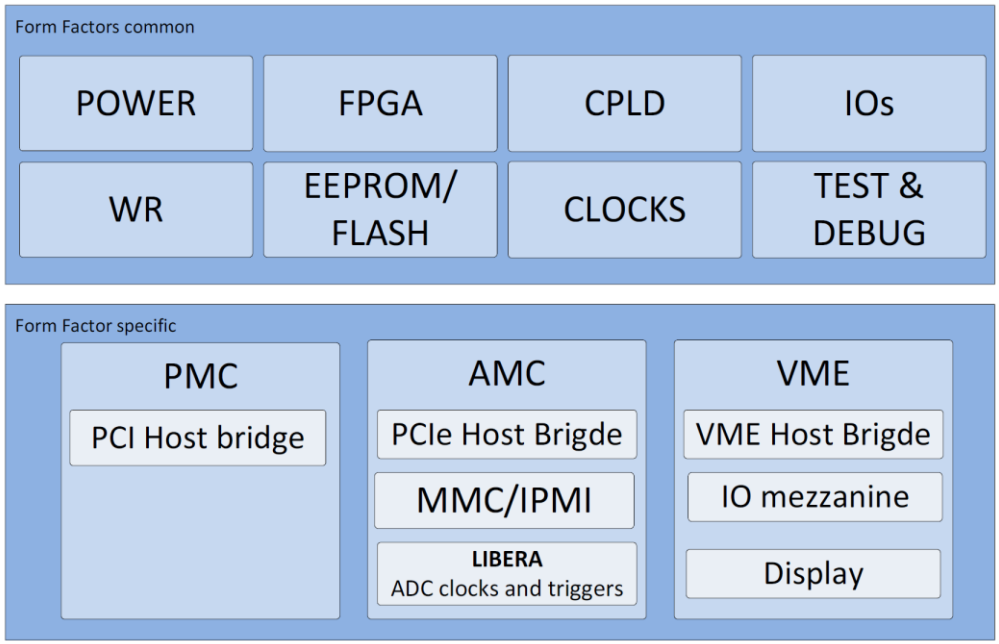
FAIR Timing Receiver

COSYLAB

- 3 form factors: PMC, AMC and VME64x.

Common to all FF:

- Altera ARRIA V GX FPGA and CPLD
- White Rabbit
- I/O and Clocks

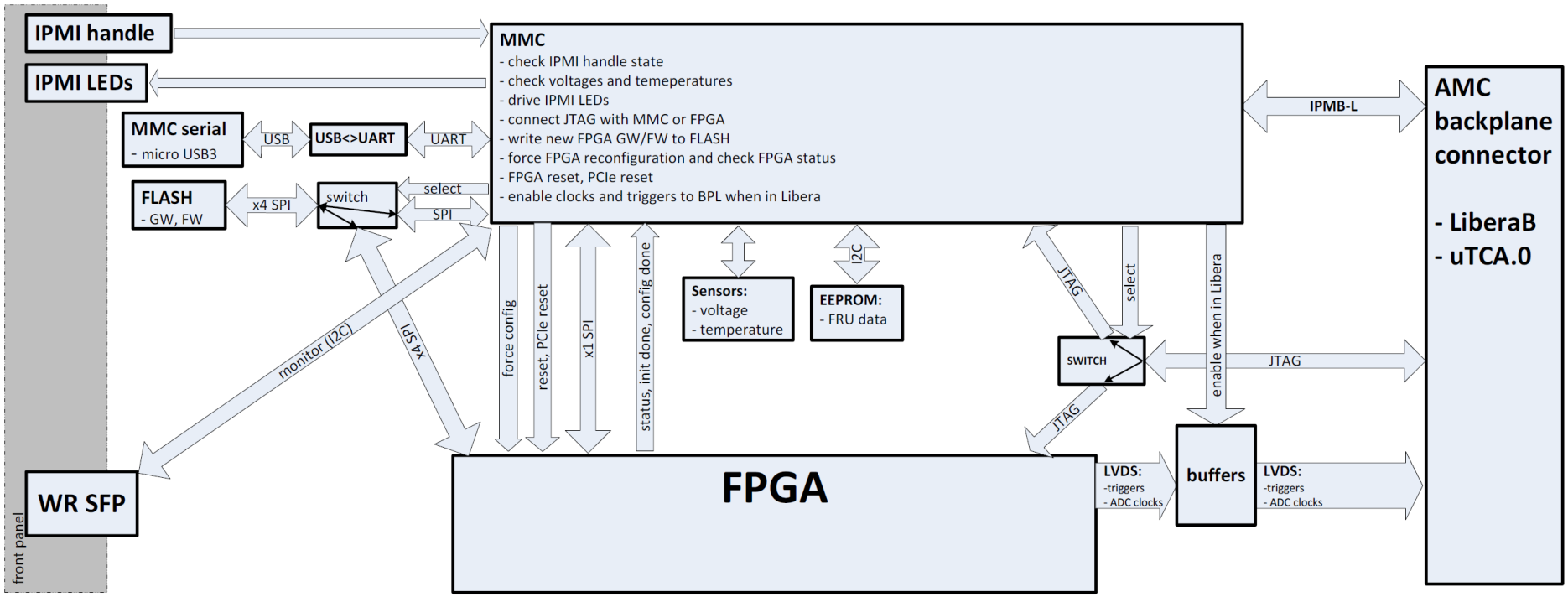


FF Specific:

- Connection to the host bus
- Platform-specific requirements on the host bus controllers (such as MMC/IPMI on AMC)
- Special clocks and triggers on the AMC form factor for the Libera platform.
- Mezzanine option for IOs.
- Display on front panel (but the display connector is on all form factors).

AMC WR receiver

- NXP LPC2136 microcontroller for MMC
- EEPROM for storing FRU data
- The PCIe Host bus bridge implemented in FPGA
- PORT 4 in Fat Pipe as PCI Express, Lane 0
- 5 LEMO connectors for Bidirectional digital IOs



MMC Implementation

- Monitor board temperature and on-board voltages
- Support hot-swap operation as defined in the AMC.0 specification
- Support e-Keying, as described in the AMC.0 specification
- Store FRU information, sensor records, and e-Keying data using an external EEPROM
- Comply with the IPMI Controller Firmware Upgrade specification
- Support firmware rollback using an external flash
- Control on-board HOT SWAP, Out Of Service, and OK LEDs

MMC Implementation (planned)

- Control the JTAG switch to connect JTAG signals from backplane to MMC (default) or FPGA/CPLD JTAG chain
- Force FPGA reconfiguration to factory FW by low pulse on FPGA's nCONFIG pin
- Monitor FPGA configuration status pins (nSTATUS, CONF_DONE, INIT_DONE)
- Control access to SPI FLASH, by FPGA or MMC
- Provide FW configuration writing to SPI FW memory
- Monitor WR SFP directly (e.g. temperature)

MMC firmware

- A MMC firmware is being developed at Cosylab, currently solving interoperability issues.
- Based on Core IPM open source solution.
- Free RTOS used as scheduler.
- Core IPM original source was reduced. Event loop removed. Main functions remained:
  - IPMB-L decoder
  - IPMI functions (sensor data record)
  - PICMG standard: FRU data parsing, managed FRU state transitions, P2P connectivity record, port state commands (set port state, get port state).

Libera B compatibility

- Libera B is a MTCA based platform by Instrumentation Technologies. Compatible with MTCA.0.
- Trigger lines are connected to the Libera B backplane, enabled by the MMC/MCH
- Compatibility not yet implemented in MMC firmware. Two ideas:
  - To define a new port in the PTP connectivity record
  - Define a Libera specific custom IPMI command

Upgrade to MTCA.4

- A switch, controlled by the MMC would be necessary to change the backplane between Libera and MTCA.4 modes.
- Due to signal quality requirements in Libera, this kind of switch could not be afforded.
- Current design compatible with MTCA.0 and Libera B.
- Backplane ADC clocks only used in Libera B, enabled by the MMC.
- In the future it would be possible to upgrade the design and make it compatible with MTCA.4.
- MMC would somehow need to know the platform: either asking the MCH or being set manually.

Remarks / Conclusions

- Hardware in design stage, schematics are being prepared.
- MMC software currently under test.
- Open IPM core was too big for our use case and it has to be modified. There were some bugs.
- Resulting MMC SW is a spinoff of the Core IPM based on Free RTOS.
- Differences between MCH‘s: NAT more strict, Advantech more tolerant.
- There are differences between MCH‘s on the FRU state machines
- Many months of effort were required to adapt the MMC software and to make it compatible with both MCH‘s. Our recommendation: use „off-the-shelf“ solutions whenever possible.

THANK YOU!

Marko Mehle

COSYLAB

Web: www.cosylab.com

Your [illegible] Control System Partner