DESY MMC V1.0

Standardized Solution of Management Controller for MTCA.4

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Progress on MMC V1.00
Management Controller for MTCA.4
Hamburg, 11.12.2014

HELMHOLTZ ASSOCIATION

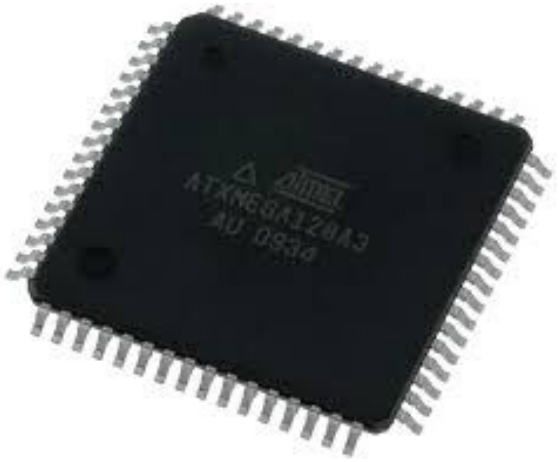
Lodz University of Technology

DMCS

DESY

Introduction

- Agenda:
  - Repetition of MMC features
  - Improvements in 2014
  - Demonstration

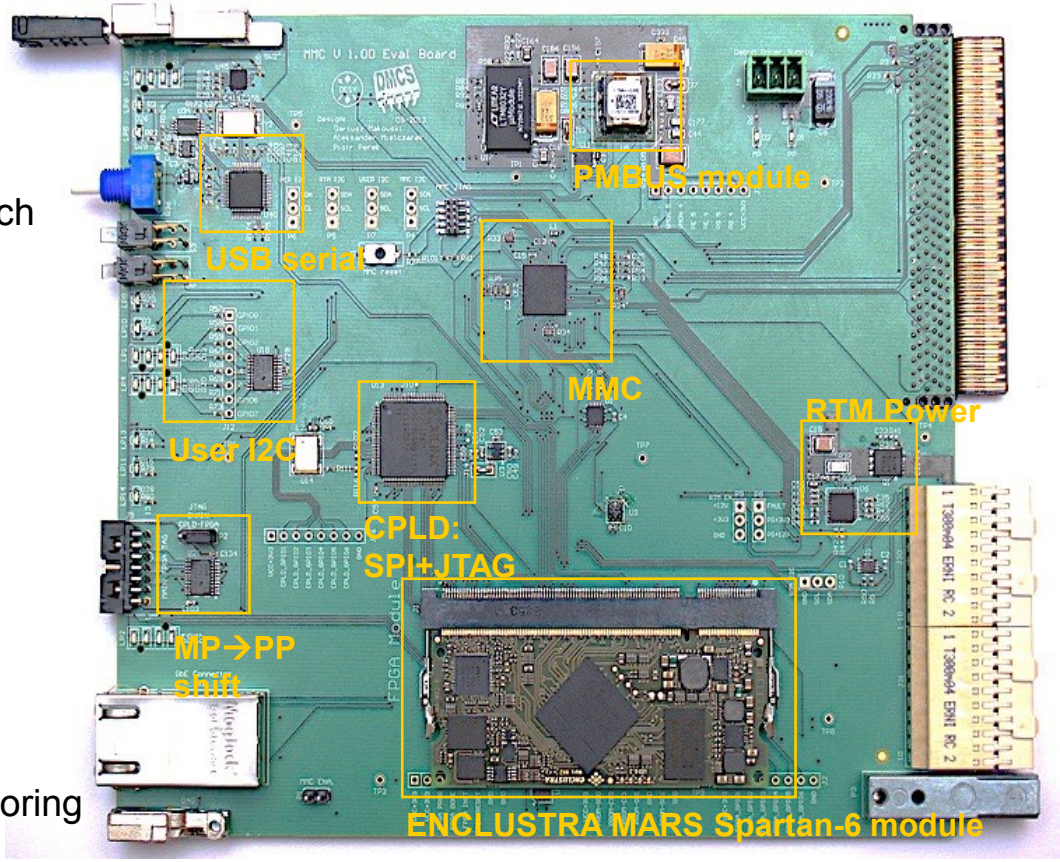


- DESY MMC V1.0 is a set of hardware and software building blocks, created by DESY and its partners
- Management is the most difficult part, almost all interoperability issues are based on management
- Idea: Create one proven feature-rich standard solution and share it with the partners
- Bases on Atmel ATxmega128A1
- Over 5 man-years of design work put into it
- Great improvements during the last year

Overview of Building Blocks – Starter Kit

Commonly used Blocks

- IPMI Communication
  - Intensively tested with NAT and Vadatech
- Power Management
  - Sequencing and safety shutdown
- FPGA Management
  - DONE, INIT, PROG, RESET over IPMI
- HPM.1 MMC and FPGA upgrade
  - Redundant SPI Flashes
- RTM Management
  - RTM Inrush current control
  - Temperature, voltage and current monitoring



Design: Dariusz Makowski, DMCS

- CPLD for JTAG and Flash Control (optional!)
  - Allows to program “dead board”; Redundant Flash selection
- Debug UART
- PMBUS control

Progress

State of Last Year: “Basic” functionality (Development Version)

- IPMI Communication
- Power Management, Temperature Monitoring
- FPGA Management
- Static CPLD for JTAG and Flash Control
- AMC FRU generator

Great Improvements in 2014 (25.000 lines of code added)

- Architecture change: Full separation IPMI/user logic
- Vadatech compatibility: IW25, IW26
- HPM.1 Support (8KB Boot loader) → MMC, SPI
- MMC and CPLD register control with IPMItool
- Temperature Events (Fan speed increase)
- Automation tools (program.bat, bin2hpm)

Reference Customers

- DESY MMC V1.00 is running on DESY Boards
  - DAMC-FMC20, DAMC-FMC25, DAMC-TCK7
- In 2014 we won partners – very good feedback
  - CAENels
  - Michigan State University
  - NRF Korea
  - *Micro-Research Finland*
  - *Interface Concept*
  - In negotiation with SLAC
- Success story: Struck SIS8300L2
  - Spend two days together for MMC schematic change
  - Spend one day for Code-Porting
  - Full set of new features: Remote MMC and Flash Upgrade, redundant FPGA Flash Memories, RTM inrush current control, Temperature Alerts, FPGA and RTM supervision

CAENels Gear For Science

MICHIGAN STATE UNIVERSITY

NRF National Research Foundation of Korea

Micro-Research Finland Oy

IC INTERFACE CONCEPT

struck innovative systeme

Demonstration

- Sensor Information
- HPM file generation
- IPMI Upgrade
- Production Programming

Bin2hpm – in Bitfile mode

```
D:bin2hpm llrf_ctrl_sis8300l_acc1_r908.bit /bit /compress
BIN-to-HPM file converter. Version: 1.0
Written by Michael Fenner (C) DESY 2014;
with compression based on VPackBits (C) Michael Dipperstein (LGPL) and
with MD5 algorithm from Alexander Peslyak (public domain)

Reading file                    : llrf_ctrl_sis8300l_acc1_r908.bit
File Lengh is                   : 5465076 bytes
Bit File mode. Header check ok.
a-Section detected. Design info : ENT_SIS8300L_TOP.ncd;UserID=0xFFFFFFFF
b-Section detected. Part name   : 6vlx130tff1156
c-Section detected. File date   : 2014/11/27
d-Section detected. File time   : 01:58:26
e-Section detected. Image size  : 0x0053638C (5336KB)
BIT header sucessfully parsed.
Generating HPM header...
Device ID                       : 0x00
Manufacturer ID                 : 0x000000
Product ID                      : 0x0000
Time value                      : 0x54886D64
Component ID                    : 0x01
Firmware revision               : 0x0000
Firmware revision auxilary information          : 0x00000000
Generating header checksum                      : 0xF0
Generating upgrade action checksum (prepare)    : 0xFE
Generating upgrade action checksum (upload)     : 0xFD
Information: Output will be compressed with RLE
Reading 5464972 Bytes from file...
Largest RLE block is            : 128 bytes
Compression Ratio is            : 32.9%
16-bit Checksum of data is      : 0xBDB3.
Begin of data stream is         : 9EFF810004BB1122004486FF04AA995566208100...
End of data stream is           : 00208100022000000020810000208100022000000.
Testing MD5 checksum            : E5546C065678FBF39CE2CC5FC2F8F32A
Output data length is           : 1796463 bytes
Overhead (header+MD5) size is   : 99 bytes
Writing file                    : llrf_ctrl_sis8300l_acc1_r908.rle.hpm
Bytes actually written          : 1796463
All done.
```

Demonstration

```
PICMG HPM.1 Upgrade Agent 1.0.2:

-------Target Information-------
Device Id          : 0x0
Device Revision    : 0x80
Product Id         : 0x0002
Manufacturer Id    : 0x053f (Unknown (0x53F))


---------------------------------
|ID | Name      |    Versions   |
|   |           | Active| Backup|
---------------------------------
| 0 |MMCV100 HPM|  2.00 | --.-- |
---------------------------------
```

```
mskcpuhvf1@mskcpuhvf1:~$ ipmitool -H mskmchhvf1 -P "" -t 0x76 hpm upgrade SIS8300L2.hpm

PICMG HPM.1 Upgrade Agent 1.0.2:

Validating firmware image integrity...OK
Performing preparation stage...OK

Performing upgrade stage:

-------------------------------------------------------------------------------
|ID | Name      |    Versions           |    Upload Progress  | Upload| Image |
|   |           | Active| Backup| File  |0%       50%     100%| Time  | Size  |
|---|-----------|-------|-------|-------||----+----+----+----||-------|-------|
| 0 |MMCV100 HPM|  2.00 | --.-- |  0.01 ||...................|| 00.33 | 18cec |
-------------------------------------------------------------------------------

Firmware upgrade procedure successful
```

show_sensorinfo

```
nat> show_sensorinfo 9
Sensor Information for FRU 9 / AMC5
=================================================================
  #   SDRType  Sensor Entity Inst  Value   State    Name
-----------------------------------------------------------------
  0   MDevLoc           0xc1  0x65                 SIS8300L2 AMC
  0   Full     0xf2     0xc1  0x65  0x01           Hot Swap
  1   Full     Voltage  0xc1  0x65  12.1 V    ok    12V PP
  2   Full     Voltage  0xc1  0x65  3.30 V    ok    3.3V MP
  3   Full     Voltage  0xc1  0x65  0.97 V    ok    1.0V CORE
  4   Full     Voltage  0xc1  0x65  2.48 V    ok    2.5V
  5   Full     Voltage  0xc1  0x65  1.80 V    ok    1.8V
  6   Full     Voltage  0xc1  0x65  1.49 V    ok    1.5V DDR3
  7   Full     Current  0xc1  0x65  0.240 A   ok    RTM PP Current
  8   Full     Current  0xc1  0x65  0.017 A   ok    RTM MP Current
  9   Full     Temp     0xc1  0x65  35.5 C    ok    Inlet
 10   Full     Temp     0xc1  0x65  39.5 C    ok    Outlet
 11   Full     Temp     0xc1  0x65  47.0 C    ok    Middle
 12   Full     Temp     0xc1  0x65  40.0 C    ok    FPGA PCB
 13   Full     Temp     0xc1  0x65  49.0 C    ok    FPGA DIE
 14   Compact  0x0b     0xc1  0x65  0x00           0x00  FPGA Done
 15   Compact  0x0b     0xc1  0x65  0x00           0x00  FPGA Init
 16   Compact  0x0b     0xc1  0x65  0x00           0x00  RTM OC Fault
 17   Compact  0x0b     0xc1  0x65  0x00           0x00  ID:0004A3D16829
-----------------------------------------------------------------
nat> SEL: 1970/01/01 01:40:00 alive
```

Licensing

- Licensor needs so sign an NDA and a Software License Agreement
- Free of Charge for collaboration projects
- Licensing Items
  - Altium Designer Files as Templates for AMC and RTM
  - C Source Code
  - AMC FRU Generator
  - Command-Line HPM Generator