TAMC532

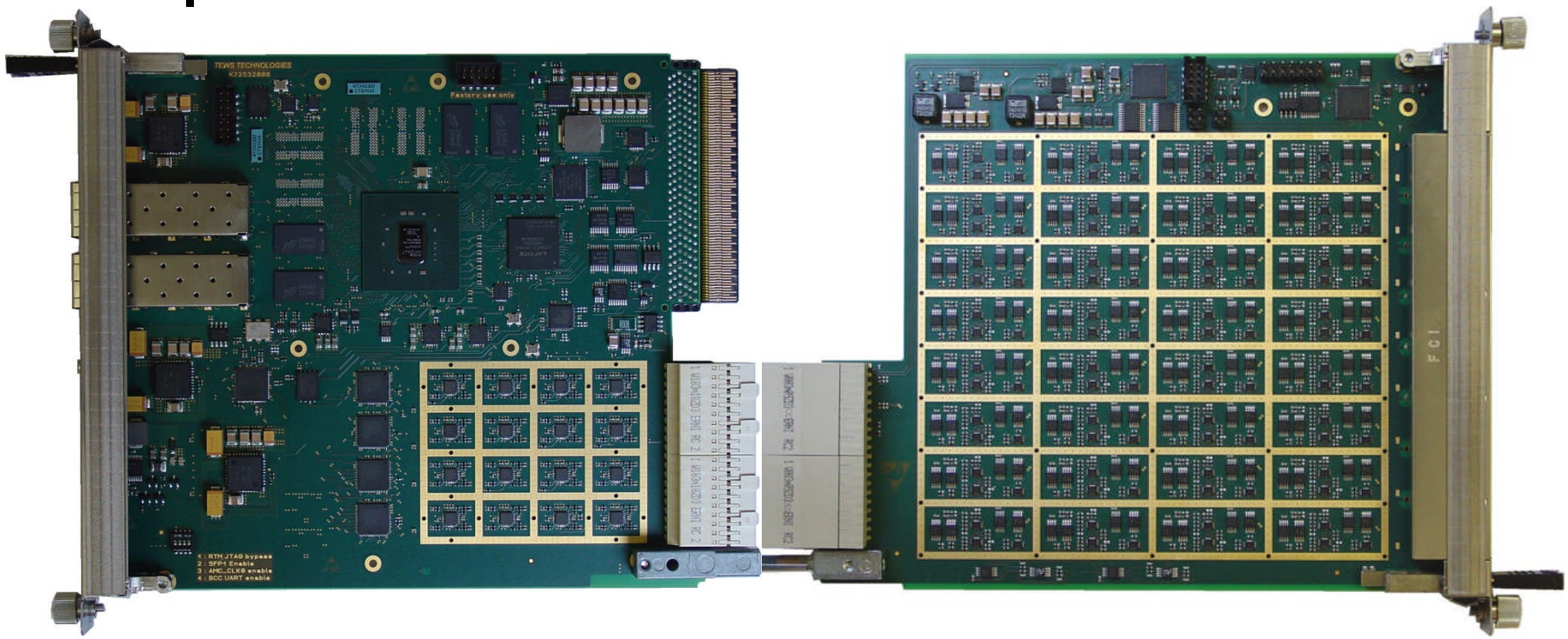
32 x
12 Bit ADC @ 75Msps

Company Background

TEWS TECHNOLOGIES is a leading solutions provider of embedded I/O and CPU products based on open architecture standards (i.e. IndustryPack, PMC, XMC, CompactPCI, standard PCI, PCIe, VME, AMC, and FMC).

Our modular hardware designs are coupled with extensive software drivers and support for major real-time and server operating systems (i.e. VxWorks, Windows, Linux, Integrity, QNX)

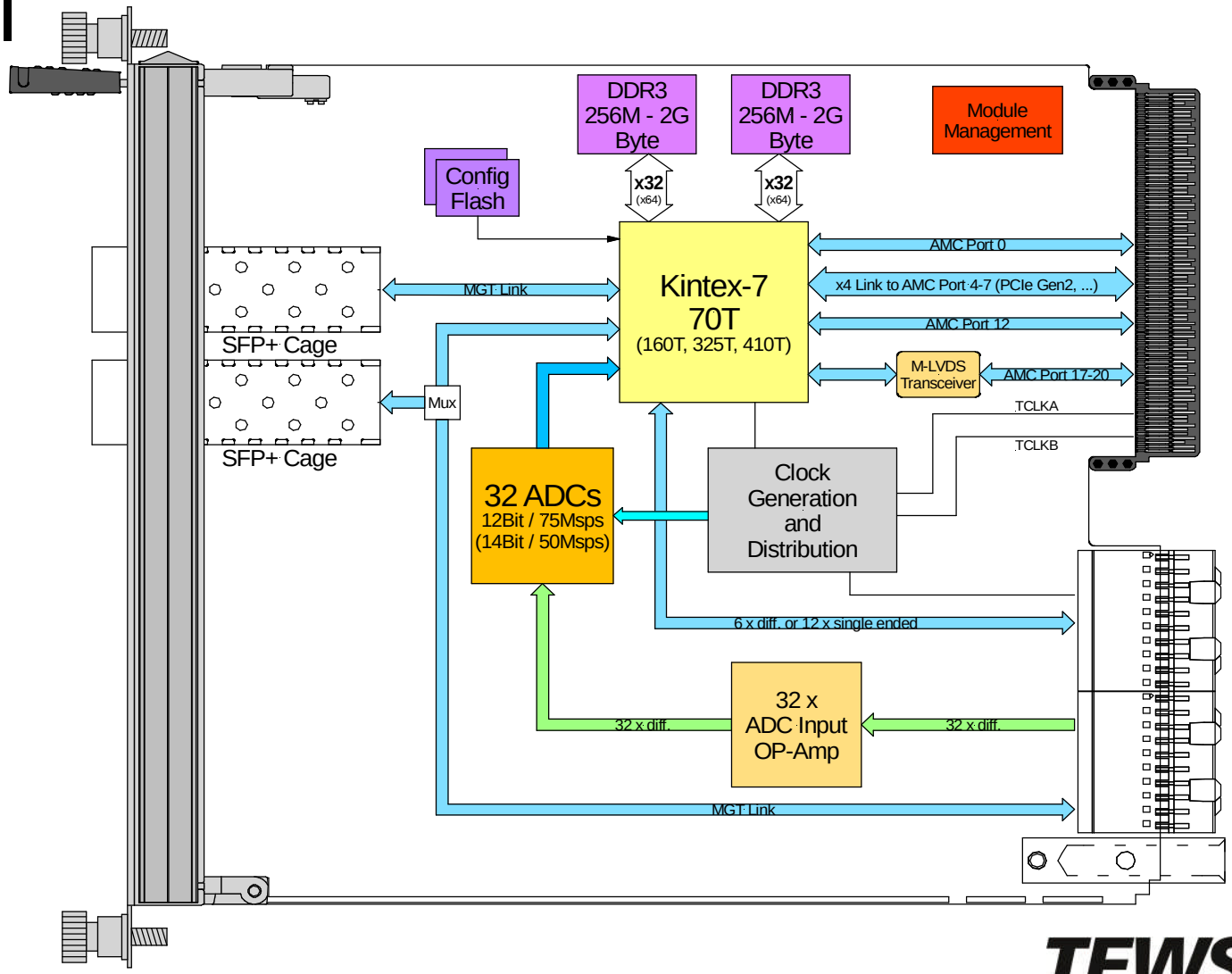
Product Photo



TAMC532 **TAMC532-TM**

(Developed within Helmholtz Validation Fund)

TAMC532 Block Diagram

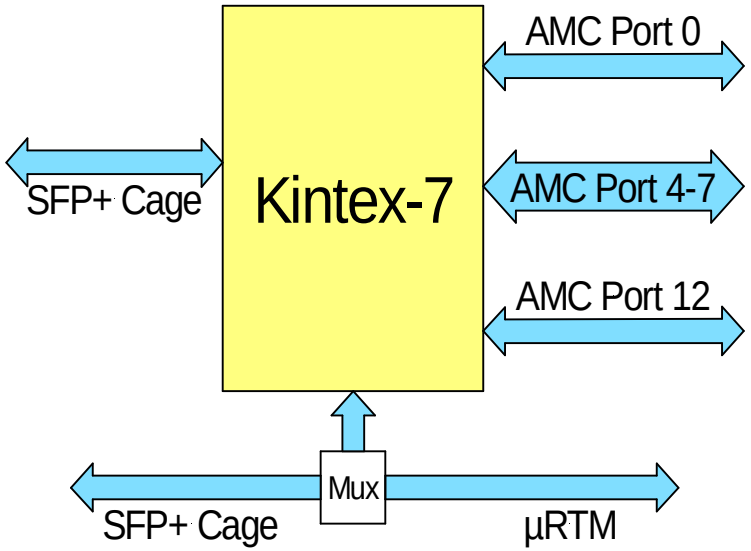


FPGA

- Kintex 7
  - 8 Multi-Gigabit Transceiver
    - 6.6Gb/s (optional up to 12.5Gb/s)
  - PCIe Gen 2 Interface
    - Endpoint or Root Port
  - 70k (optional up to 410k Logic Cells)

- Redundant Configuration Flash
  - 2 x 128MBit SPI-Flash
  - Field Update via MMC
  - User Access

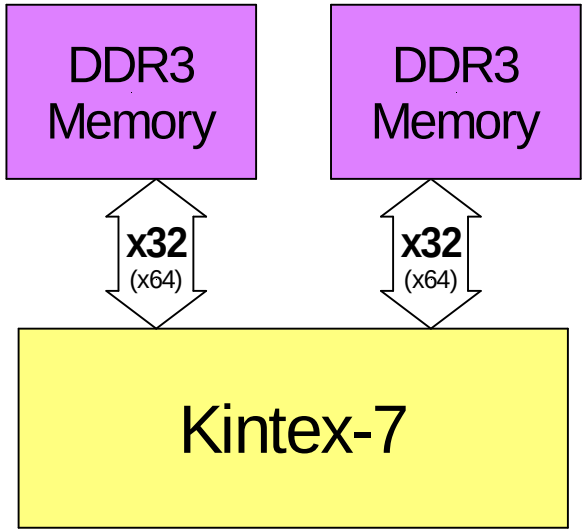
FPGA Fabric Interconnects



- AMC Port 0
  - (e.g. Gigabit Ethernet)
- AMC Port [7:4]
  - (e.g. x4 PCI-Express Gen 2)
- AMC Port 12
- SFP+ Cage in AMC Bezel
- µRTM or 2nd SFP+ Cage (software controlled)

DDR3 Memory

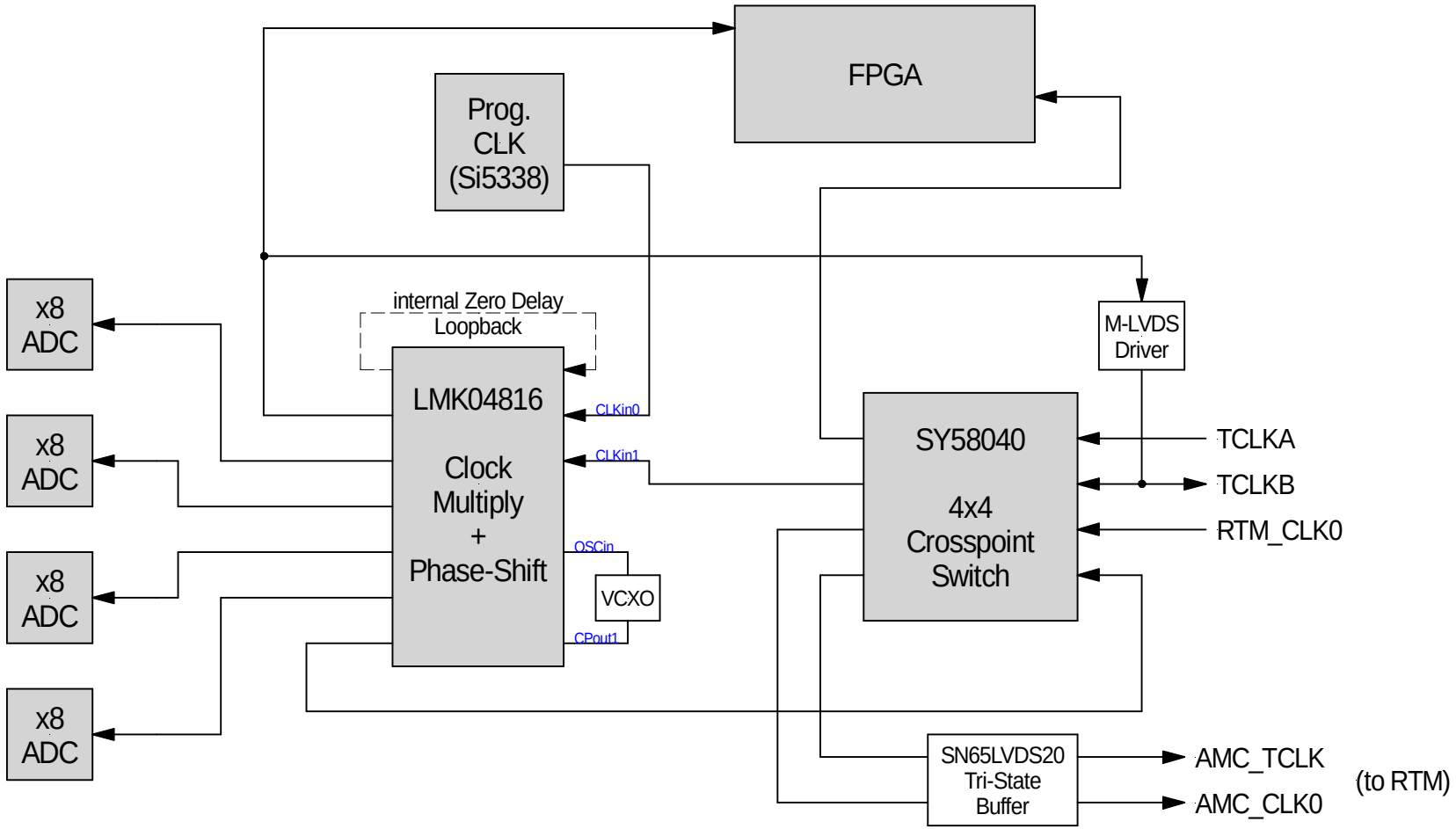
- Two independent banks
  - allow double buffering or doubling the data rate
- 32 Bit data bus width / bank (optional 64 Bit)
- 800Mb/s – 1600Mb/s line rate
- 256MByte – 2GByte / bank



4 x Octal ADC

- Resolution:
  - 12 or 14 Bit (assembly option)
- max. Sample Rate
  - 75 Msps @ 12 Bit
  - 50 Msps @ 14 bit
- Analog Inputs:
  - DC-coupled with on-board ADC-driver
  - Input voltage Range according to Class A2.1
    - ±1V differential @ 0V common-mode voltage
- Zone 3 pin assignment
  - According to Zone 3 Recommendation Class A2.1

ADC Clocking --- Block Diagram



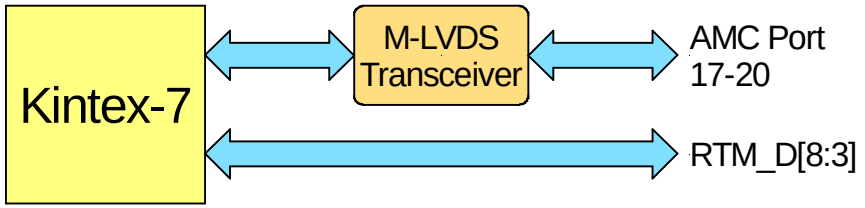
ADC Clocking --- Facts

- Clock Inputs:
  - TCLKA + B
  - µRTM CLK0
  - On-Board generated Clock
- Input frequency range:
  - 10kHz – 100MHz
- Clock Up- and Downscaling
- ADC Clock Phase Shift
  - 522 steps of ½ PLL freq. (app. 200ps / step)
- ADC Clock Delay
  - up to 475ps (25ps steps)
- Zero-Delay operation
- Bypass-Mode
- Clock Outputs:
  - TCLKB
  - AMC_TCLK
  - AMC_CLK0

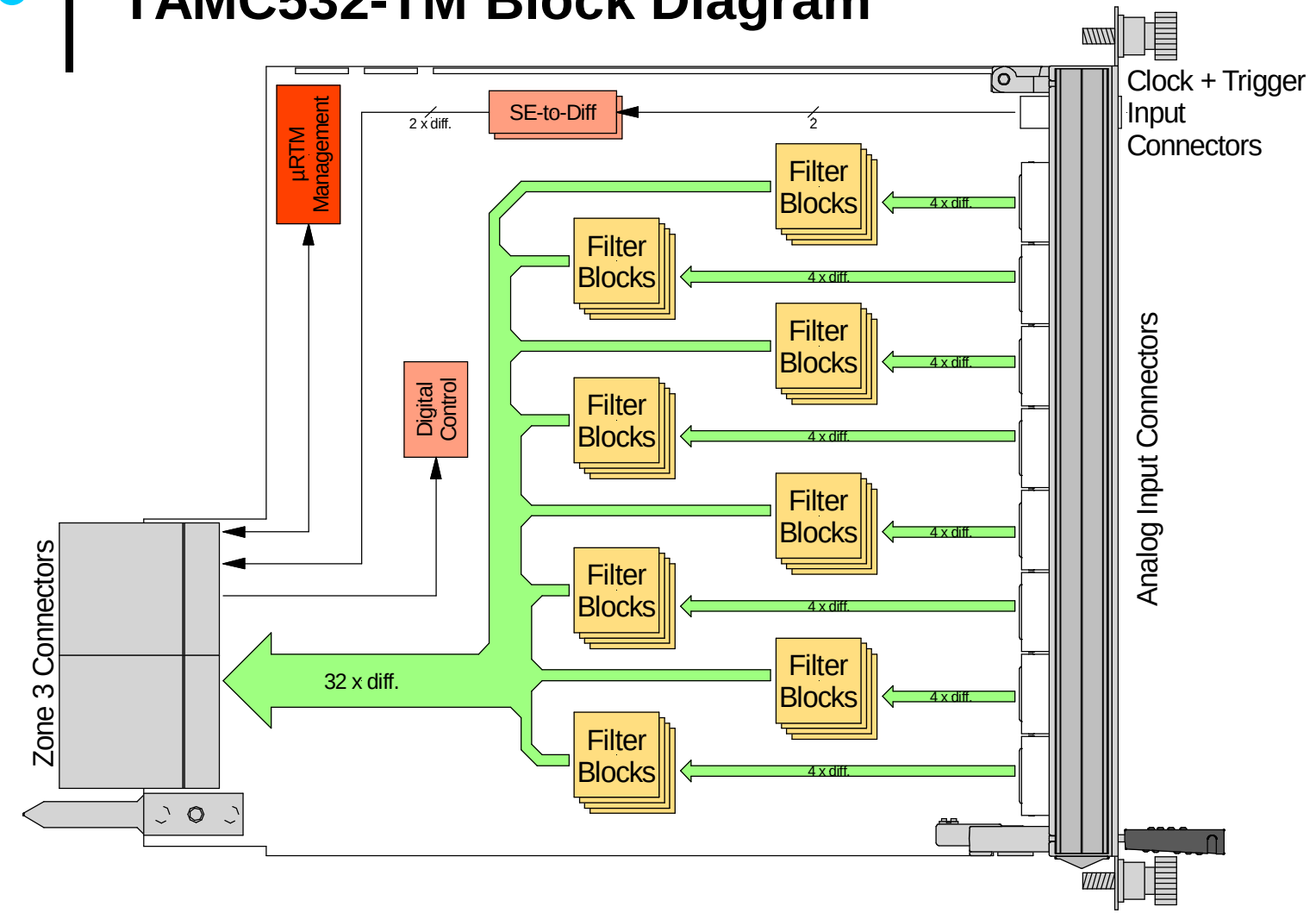
Trigger

- 8 Trigger from AMC-Backplane
  - AMC Port [20:17] via MLVDS-Transceivers
    - each Trigger can be Input or Output
    - additional NAND connection of Tx[19] and Rx[20] to Zone 3 OUT0 and OUT1

- Up to 6 Trigger from RTM
  - Zone 3 D[8:3] have direct connection to FPGA
  - 2.5V IO-Voltage



TAMC532-TM Block Diagram



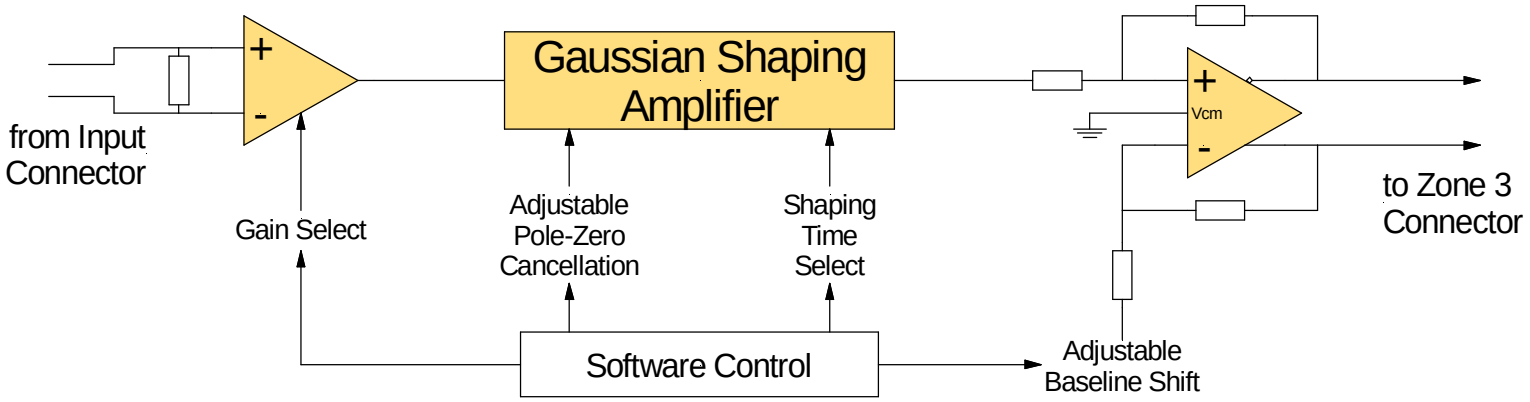
Inputs

- 32 x Analog Input
  - RJ45 Input Connectors
    - cheap cables
    - easy cable field tailoring
  - Differential
  - up to ±1V differential input voltage
  - up to ±3V common mode voltage

- 1 x Clock + 1 x Trigger Input
  - MMCX Connectors
  - single-ended

Filter Block (32x)

- Gain selection
  - 1, 2, 5 or 10
- Adjustable Pole-Zero Cancellation
- Gaussian Shaping Amplifier with selectable shaping time
  - 10µs, 1µs, 100ns
- Adjustable Baseline-Shift
- Zone 3 pin assignment according to Class A2.1



Clock / Trigger + Control

- single ended clock input
  - single-ended to differential conversion
  - connected to Zone 3 RTM_CLK0±
- single ended trigger input
  - single-ended to differential conversion
  - connected to Zone 3 D[8]±
- digital Control from the AMC
  - Gain, pole-zero cancellation, Shaper time and baseline shift are all controlled via one I^2C interface
  - IO-Voltage selectable as 1.5V, 1.8V, 2.5V or 3.3V

Management

- Zone 3 pin assignment according to Class A2.1
- µRTM Management according to Class A2.1
- Optional management implementation via microcontroller
  - allows adaption to nearly any MMC
  - IPMI-controlled D[8:3] IO-Voltage possible

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