3rd MicroTCA Workshop for Industry and Research

Report of Contributions

https://indico.desy.de/e/mtcaws2014

Contribution ID: **0** Type: **not specified**

MTCA.4 Platform Configurations

Wednesday 10 December 2014 14:45 (15 minutes)

The range of COTS products available in MicroTCA and MTCA.4 has grown rapidly over the last few years. This presentation shows how this provides users with flexibility in system configurations, from very dense processing platforms to distributed control and monitoring systems.

Primary author: Mr SHEARER, Ian (VadaTech Ltd)

Presenter: Mr SHEARER, Ian (VadaTech Ltd)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **1** Type: **not specified**

Open Hardware MTCA development at Creotech Instruments SA and WUT

Wednesday 10 December 2014 17:00 (15 minutes)

Since a few years Creotech Instruments develops complex MTCA-based systems based on Open Hardware approach. We want to share with experience gained with OHWR business model and introduce new products.

Primary author: Dr KASPROWICZ, Grzegorz Kasprowicz (Warsaw University of Technology / Creotech Instruments SA)

Co-author: Mr KIEPIELA, Marcin (Creotech Instruments SA)

Presenter: Dr KASPROWICZ, Grzegorz Kasprowicz (Warsaw University of Technology / Creotech Instruments SA)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **2** Type: **not specified**

1000W MTCA.4 Low Noise Power Supply

Thursday 11 December 2014 11:15 (15 minutes)

The WIENER 1000W Low Noise MTCA.4 Power Supply will be presented including the latest improvements.

Primary author: Mr BERNER, Thomas (WIENER Plein + Baus GmbH)

Presenter: Mr BERNER, Thomas (WIENER Plein + Baus GmbH)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **3** Type: **not specified**

Performance evaluation of RF-Backplane option for MTCA.4 system

Wednesday 10 December 2014 14:00 (15 minutes)

RF-Backplane is an RTM backplane for MTCA.4 based LLRF system. Prototype implementation was designed for upcoming European XFEL accelerator to distribute CLK and analog RF signals (up to 6GHz) between uRTM/eRTM modules. Precision regulation of the RF fields performed by LLRF system forces high signal integrity demands on these RF and CLK distribution networks. Therefore one of the multiple aspects of R&D process was optimization of connector-PCB interfaces by employing 3D full-wave EM field solver. Laboratory test results confirmed, that the performance of RF signal transmission over RF-Backplane is comparable to the distribution by a network of RF coaxial cables.
The entire development effort has led to excellent performance in terms of reflection coefficients, insertion losses, channel-to-channel cross-talks and high phase stability over temperature. This talk covers performance evaluation of the designed RF-Backplane v3.2 prototype.

Primary author: Mr LEŚNIAK, Tomasz (Warsaw University of Technology, ISE)

Co-authors: Dr LEWANDOWSKI, Arkadiusz (Warsaw University of Technology, ISE); Dr LUDWIG, Frank (DESY); Dr SCHLARB, Holger (DESY); Dr CZUBA, Krzysztof (Warsaw University of Technology, ISE)

Presenter: Mr LEŚNIAK, Tomasz (Warsaw University of Technology, ISE)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **4** Type: **not specified**

GND Modelling of MTCA.4 Crates

Wednesday 10 December 2014 13:30 (15 minutes)

In MTCA.4 systems sensitive analogue and aggressive digital signals have to be handled on one board or one AMC/RTM combination. The open MTCA architecture with plugged in modules designed by multiple designers for multiple purposes creates additional noise on the sensitive analogue signals. In the DC and low frequency range this EMC problem is dominated by conductive coupling especially within the GND System. By modelling the GND of a complete MTCA shelf the impact of single components on the system can be simulated. The biggest simulation effort is caused by the models of the GND planes in the backplane and the modules. Different approaches are discussed to handle the well-known effort/accuracy relation of simulation models. As layout data for off the shelf modules often are not available the only practicable way is usually the modelling by measurement data.

Primary author: Dr IBOWSKI, Heinz-Hartmut (b1-ES GmbH)

Co-author: GANSS, Rudi (b1-ES GmbH)

Presenter: Dr IBOWSKI, Heinz-Hartmut (b1-ES GmbH)

Session Classification: Standard

Track Classification: Standard

Contribution ID: **5** Type: **not specified**

An MTCA White Rabbit Timing Receiver for FAIR

Wednesday 10 December 2014 17:45 (15 minutes)

The FAIR facility involves a long chain of accelerators which need to be tightly synchronized. This is achieved by using by using a timing system based on White Rabbit (WR). FAIR Timing Receiver Nodes (FTRNs) are part of the FAIR General Machine Timing System. FTRNs receive and decode
broadcasted network messages in real time.

One of the form factors to be used in the facility will be the MTCA platform, therefore a WR timing receiver module had to be developed for it. The card format is a Single-Width Mid-Height AMC, and it is based on the Altera ARRIA V FPGA for the main functionality. The MMC was
implemented using a NXP LPC2136 microcontroller.

Since the FAIR facility will also use the i-Tech Libera Platform B, the White Rabbit timing receiver card was designed to be compliant with this platform. The MMC firmware development was
based on the Open Source coreIPM management architecture and the FreeRTOS operating system. Besides the standard functionality defined by the PICMG specification, the MMC must support a series of custom commands that allow it to fit either into an MTCA.0 or a Libera B system.

Primary author: Mr MEHLE, Marko (Cosylab)

Presenter: Mr MEHLE, Marko (Cosylab)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **6** Type: **not specified**

A demonstration of a mTCA.4 crate used as a high precision data acquisition and control system with optical PCIe Gen.3 up-link.

Wednesday 10 December 2014 14:30 (15 minutes)

The talk will contain an architecture of a MTCA.4 crate, including an advance backplane for the usage of an extreme precise timing and clock distribution. The crate, including the MCH with the optical PCI-e Gen.3 uplink, the fiber optic cable and the receiving PC board as a unit will be part of a live demonstration.

Summary

With the new precise timing module as part of the new ELMA MCH, the operator can use the slot, which was occupied with the ordinary timing module, for other options.
The connection of MTCA.4 crates with the PC world through fiber optics will open new possibilities in the research environment

Primary author: Mr SALTUKLAR, Aksel (ELMA)

Presenter: Mr SALTUKLAR, Aksel (ELMA)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **7** Type: **not specified**

Test-Stand for High-Performance FPGA Computing Module

Thursday 11 December 2014 17:30 (15 minutes)

The European-XFEL project requires a powerful computing module for the Low-Level RF system. The processing power will be provided by CM045 module delivered by Vadatech –a fruit of successful commercialization of DAMC_TCK7 module developed for DESY by DMCS. About 100 boards will be ordered and will have to be carefully evaluated before installation in the accelerator tunnel. Manual testing of every important component on each board would be enormous task. In order to boost the effectivity and reduce risk of missing any important problem a semi-automated Test-Stand was proposed.
The test-stand suite is composed of two FPGA firmwares and a set of Python scripts. The test suite verifies operation of the power supplies, FPGA, CPLD, MMC, all the memories and fast data links. Finally a PDF report is generated for each tested module. The presentation will provide more details on how the solution is implemented and how it parts are interfacing together.

Primary author: Mr MIELCZAREK, Aleksander (Lodz University of Technology)

Co-author: Dr MAKOWSKI, Dariusz (Lodz University of Technology)

Presenter: Mr MIELCZAREK, Aleksander (Lodz University of Technology)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **8** Type: **not specified**

Standardized Solution for Management Controller for MTCA.4

Thursday 11 December 2014 10:15 (15 minutes)

The MTCA standard provides advanced management, monitoring and diagnostics functionalities. The hardware management is based on the extended Intelligent Platform Management Interface (IPMI) protocol, that was initially developed for the supervision of complex computers operation. The Module Management Controller (MMC) is required on each card installed in the MTCA chassis to provide IPMI functions.
The commercially available implementations of MMC are expensive and do not provide the complete set of functions required for specific High Energy Physics applications.
The authors decided to develop a unified solution of a management controller dedicated for AMC and RTM cards, that is fully compliant with AMC and MTCA.4 standards.
The MMC v1.00 solution is a dedicated management of AMC and RTM modules. The framework is based on the Atmel ATxmega microcontroller and can be fully customized by a hardware developer or used as a drop-in-module without any modifications. The implementation was verified with various AMC and RTM modules developed at DESY.
The presentation discusses the functionality of the MMC v1.00 solution.

Primary authors: Dr MAKOWSKI, Dariusz (Lodz University of Technology, DMCS); Mr FENNER, Michael (Deutsches Elektronen Synchrotron)

Presenter: Mr FENNER, Michael (Deutsches Elektronen Synchrotron)

Session Classification: Software for MicroTCA.4

Track Classification: Software for MTCA.4

Contribution ID: **9** Type: **not specified**

128 Gbps PCIe link for data acquisition with MTCA.4

Wednesday 10 December 2014 14:15 (15 minutes)

Data acquisition and processing systems used in modern physics produce large amount of data. A good example is the image acquisition system, that collects data from megapixel digital cameras. The image acquisition system, composed of ten 1 megapixel cameras, can easily produce the 100 gigabit data stream. The data acquisition and processing system requires a powerful interface to transfer such an enormous data steam.
The PCIe standard, initially developed for Personal Computers, allows transferring data with throughput reaching 128 gbps (PCIe x16, gen. 3) or even more. The interface provides a high-throughput low-latency data transmission and therefore makes possible to use a high-performance CPU blade that collects and processes data provided by the MTCA.4 based acquisition system.

In this talk, we will present the first results for the data throughput measurement for a MTCA.4-based data acquisition system that transfers data to an external CPU blade via the PCIe x16 cooper link.

Primary author: Dr MAKOWSKI, Dariusz (Lodz University of Technology, DMCS)

Presenter: Dr MAKOWSKI, Dariusz (Lodz University of Technology, DMCS)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **10** Type: **not specified**

MTCA.4 based LLRF system using direct sampling method

Thursday 11 December 2014 17:15 (15 minutes)

This contribution describes the design of an MTCA.4-based Rear Transition Module suited for direct sampling of signals in a bandwidth of 5-700 MHz.
The RTM is fully compliant with the DESY Analog class A1 recommendation and features RF backplane support. The board consists of 8 feed-through channels(AC or DC coupled), 1 vector modulator channel and a low-noise clock generation and distribution circuit. Additional features include 6 precise temperature sensors and input power measurement. The card was designed to be used in direct sampling based LLRF control system. The module was tested at the ELBE facility at HZDR. It was used in a direct sampling LLRF control system regulating a 260 MHz normal conducting buncher cavity. The system diagram and test results will be presented.

Primary author: Mr GRZEGRZÓŁKA, Maciek (ISE Warsaw University of Technology)

Co-authors: Dr SCHMIDT, Christian (DESY, Hamburg); Dr BÜTTIG, Harmut (HZDR, Dresden); Mr RUTKOWSKI, Igor (ISE Warsaw University of Technology); Dr HOFFMANN, Matthias (DESY, Hamburg); KUNTZSCH, Michael (HZDR, Dresden); RYBANIEC, Radosław (ISE Warsaw University of Technology); SCHURIG, Rico (HZDR, Dresden); BUTKOWSKI, Łukasz (DESY, Hamburg)

Presenter: Mr GRZEGRZÓŁKA, Maciek (ISE Warsaw University of Technology)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **12** Type: **not specified**

High voltage piezo driver RTM and its application

Thursday 11 December 2014 11:45 (15 minutes)

A MicroTCA.4 (MTCA.4) compliant Piezo Driver (DRTM-PZT4) has been developed to drive piezoelectric-based actuators used in accelerator instrumentation applications. More specifically, it is used for synchronization of pulsed lasers, stabilization of fiber links, piezo based motor driver control and superconducting cavities fine tuning. This paper briefly presents the designed system requirements and discusses the main hardware components and their latest improvements. The results of the designed hardware usage for various application are summarized.

Primary author: Dr PRZYGODA, Konrad (DESY)

Presenter: Dr PRZYGODA, Konrad (DESY)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **13** Type: **not specified**

Precision regulation for SRF cavities using MTCA.4

Thursday 11 December 2014 16:45 (15 minutes)

The stable and reproducible generation of a high average brilliance photon beam at Free Electron Lasers requires a high-precision radio frequency regulation of the accelerating fields inside the cavities. ELBE (Electron Linac for beams with high Brilliance and low Emittance) is a multi-purpose radiation source at HZDR (Helmholtz-Zentrum Dresden-Rossendorf). The LLRF system controls two normal conducting buncher cavities (one operating at 260 MHz and one at 1300 GHz), a superconducting gun cavity and 4 super conducting TESLA-type accelerating cavities. Field detection resolution was improved and measurement results are presented. The system's architecture and possible future system developments are discussed.

Primary author: Mr RUTKOWSKI, Igor (ISE, Warsaw University of Technology)

Co-authors: Dr SCHMIDT, Christian (DESY); Dr BÜTTIG, Hartmut (HZDR); Dr HOFFMANN, Matthias (DESY); Mr KUNTZSCH, Michael (HZDR); Mr RYBANIEC, Radosław (ISE, Warsaw University of Technology); Mr SCHURIG, Rico (HZDR); Mr BUTKOWSKI, Łukasz (DESY)

Presenter: Mr RUTKOWSKI, Igor (ISE, Warsaw University of Technology)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **14** Type: **not specified**

Status of MTCA Driver Development at DESY in Zeuthen

Thursday 11 December 2014 09:00 (15 minutes)

Micro Telecommunications Computing Architecture (MicroTCA) is the new generation system, which should allow more stable and reliable control of the accelerator facilities such as FLASH at DESY and the European XFEL. The photo injector test facility at DESY, Zeuthen site (PITZ) is optimizing the electron source for the European XFEL. The MicroTCA system is also planned to be used at PITZ in order to have hardware/software configuration of different subsystems (RF system, interlock system, etc.) as close as possible to the European XFEL. At PITZ, it is not always possible to find the driver for MicroTCA devices, especially for homemade devices and sometimes additional work should be performed (special drivers have to be written) to adapt the system for PITZ. One of the examples is the PITZ timing system, where specific functionalities like bitwise writing, several register accesses in atomic manner, interrupt handling etc. are needed to handle the device. In general the aim is to have a driver that is able to handle different MicroTCA devices without slowing down the overall performance. Such a driver was developed at DESY-Zeuthen and is already in use for the PITZ timing devices. Some of frequently used functionalities are generalized for this driver. In addition the driver offers the hardware developer functionalities for debugging during hardware development stage. Adding new functionality for handling more devices and making optimizations are in progress. Using driver stacking makes possible to create specific drivers by adding only specific functionality required for each specific device, if it is not possible to handle the devices with specific functionalities. Some investigations have been done to select good synchronization mechanism for concurrent access to device registers. So far implemented functionalities like read and/or write arbitrary amount of data, bitwise writing arbitrary amount of bits from arbitrary number of registers etc. and ongoing implementation will be presented.

Primary author: Dr KALANTARYAN, Davit (DESY)

Presenter: Dr KALANTARYAN, Davit (DESY)

Session Classification: Software for MicroTCA.4

Track Classification: Software for MTCA.4

Contribution ID: **15** Type: **not specified**

Key Parts of the new RTM backplane in MicroTCA.4

Wednesday 10 December 2014 11:45 (15 minutes)

Learn the key parts to get RTM backplane running in a MTCA.4 systems:

- rear transition module for MCH with connection to RTM backplane
- rear power module connected to RTM backplane
- management of the rear power modules
- management of µRTMs connected to front AMCs
- management of µRTMs connected to front AMCs and RTM backplane
- management of eRTMs with only connection to RTM backplane

Summary

Desy and industrial partners extend MicroTCA.4 by integrating a RTM backplane behind the MTCA backplane. In the PICMG MTCA.4 hardware workgroup the mechanics and management extensions are prepared for standardization.

This presentation shows how

- the needed differential power i.e. +7,-7 Volt is produced and connected to the RTM backplane
- to manage this power and how e-keying is implemented
- to manage beside the µRTMs with optional RF connector also the eRTMs (eRTMs are not connected to any front AMC)
- how to manage a minimal configuration with just one eRTM but no additional power

After listening to this presentation you will have a status update of the standardization of RF in MTCA.4 in the PICMG hardware working group and about the available hard- and software components.

Primary author: Mr DIRKSEN, Vollrath (N.A.T. GmbH)

Presenter: Mr DIRKSEN, Vollrath (N.A.T. GmbH)

Session Classification: Standard

Track Classification: Standard

Contribution ID: **16** Type: **not specified**

MTCA.4 PCIexpress Uplinks - optical and copper

Thursday 11 December 2014 11:00 (15 minutes)

Up to 16 PCIexpress lanes inside and outside of a MTCA.4 system are demanded in application with high data throughput, low latency and huge computing requirements.

This presentation presents how to upgrade existing MTCA.4 systems

inside the system with

- 16 PCIexpress lanes to the local root complex as rear module behind the MCH

at the front-side with

- 16 lanes of optical PCIexpress uplinks (128 Gb/s)
- two times 8 lanes of optical PCIexpress uplinks (each 64 Gb/s)
- daisy chain with 8 lanes of optical PCIexpress uplinks multiple MTCA.4 systems (64 Gb/s)

at the backside-side with

- 16 lanes of electrical PCIexpress uplinks (128 Gb/s)

On new MicroTCA.4 system with new backplanes also a 16 PCIexpress port can be routed to one AMC slot.

Summary

Existing standard MTCA.4 system have only 4 PCIexpress lanes per AMC slot, which can become a bottleneck if only one CPU has to process data coming from up to 11 AMCs populated with high performance FPGAs DMAing data directly into the memory of the CPU.

If PCIexpress clustering with up to 6 PCIexpress cluster cannot be used due to the impossibility to distribute data to different CPUs, a bigger data path to the main CPU is needed.

If the AMC CPUs are not powerful enough and/or an GbE and 10 GbE interface creates too much latency, a high speed optical or copper PCIexpress path to a powerful external computer is needed.

In this presentation available solutions to upgrade existing MTCA.4 system with up to 16 PCI-express lanes to the local CPU and/or to external computers via high performance, low latency PCIexpress uplinks are shown.

Primary author: Mr DIRKSEN, Vollrath (N.A.T. GmbH)

Presenter: Mr DIRKSEN, Vollrath (N.A.T. GmbH)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **17** Type: **not specified**

Versatile Frame Grabber Card for MTCA.4

Thursday 11 December 2014 11:30 (15 minutes)

Fast evolution of visible and infrared-light digital cameras was observed within last ten years. The cameras providing images with the megapixel resolution are useful diagnostic tools applied in various experiments of modern physics.
Dedicated protocols were developed for transferring megapixel images in complex physics experiments. Camera Link and CoaXPress interfaces assure both a high bandwidth and high reliability, and therefore they are commonly used in physics.
A frame grabber providing a suitable interface to cameras, synchronization, memory and processing power is required for the image acquisition.
In this talk we will present a versatile frame grabber card with Camera Link and CoaXPress interfaces dedicated for MTCA.4 systems. The module acquires images from maximum 4 cameras and delivers resources and synchronization required for further image processing. The module was optimized to provide a high performance but it is still a cost effective solution.

Primary author: Mr DANYCH, Remigiusz (AIES Sp. z o.o.)

Presenter: Mr DANYCH, Remigiusz (AIES Sp. z o.o.)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **18** Type: **not specified**

Easy Power Redundancy and Load Sharing Configuration of MTCA.4 system

Wednesday 10 December 2014 15:00 (15 minutes)

12 slot MTCA.4 chassis offer 2, 4 or more power module sides. Each application demands a different power configuration.

This presentation describes load sharing, 1+1 and n+1 redundancy and a combination of load sharing and redundancy power configuration. The new and available graphical tool Power Configuration Manager (PCM) is introduced. Just by some mouse clicks the needed power configuration can be set and saved in the MTCA backplane FRU.

Summary

Redundancy and load sharing of power modules gets more and more important for system designers. The new PCM (Power Configuration Manager) in NATview makes power configuration save and quick.

NATview can be used to scan, monitor and change the various resources of a MicroTCA system. NATview is a Java application and runs with any operating system.

Other NATview options are FRU Editor, Backplane Viewer, HPM update, MCH Scanner, System Dump and Event Log.

Primary author: Mr DIRKSEN, Vollrath (N.A.T. GmbH)

Presenter: Mr DIRKSEN, Vollrath (N.A.T. GmbH)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **20** Type: **not specified**

Rapid Firmware Prototyping with Matlab/Simulink for MicroTCA.4

Thursday 11 December 2014 09:15 (15 minutes)

The new MicroTCA.4 hardware platform facilitates control of complex system with a large number of actuators and sensors. However, the number of available devices and their complexity makes it increasingly difficult to simulate and implement a controller design. The usual work flow includes simulating the system behavior, building and testing a controller in the simulation and, finally, translating it to a hardware-description language and building the firmware. This requires expertise on both topics, the simulation and controller design as well as the HDL development, which usually means dividing the work between application engineers and FPGA programmers.

The Xillinx System Generator Toolbox for Matlab Simulink allows the application engineer to use a model based approach to design the application and precisely simulate the final behavior e.g. taking the fixed point representation of numbers into account. The new toolbox developed at DESY complements System Generator and allows the user to add and simulate board specific interfaces and generate the VHDL code and netlists that reflect the design for a specific AMC with possible FMC and RTM extensions. This contribution will demonstrate the capabilities of this toolbox and show the simplicity of building a small control application from scratch.

Primary authors: Mr MICHAEL, Heuer (DESY); Mr PREDKI, Pawel (TUL / DMCS)

Presenter: Mr PREDKI, Pawel (TUL / DMCS)

Session Classification: Software for MicroTCA.4

Track Classification: Software for MTCA.4

Contribution ID: **21** Type: **not specified**

SLAC National Accelerator Laboratory MicroTCA.4 Collaboration

Wednesday 10 December 2014 16:45 (15 minutes)

SLAC National Accelerator Laboratory has two microTCA collaborations with other laboratories. These collaborations are to developed BPM systems with European Spallation Source (ESS) and Pohang Accelerator Laboratory (PAL). The ESS collaboration is designing a new Rear Transition Module (RTM) that can be used as a BPM interface and as a LLRF interface for a development system. The PAL collaboration is designing a stripline BPM system for the LINAC for the XFEL project. This consists of 145 ADC and RTMs all packaged into 17 microTCA crates that consists of power modules.

Summary

Work Funded though CRADA 13-219C and WFO 13-197.A4

Primary author: YOUNG, A (SLAC)

Co-authors: JANSSON, A (ESS); JOHANSSON, A (Lund University); KIM, C (PAL); XU, C (SLAC); HASSANZADEGAN, H (ESS); KANG, Heung-Sik (PAL); OLSEN, J (SLAC); ZENG, R (ESS); HOOBLER, S (SLAC); STRAUMANN, T (SLAC)

Presenter: YOUNG, A (SLAC)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **22** Type: **not specified**

MicroTCA.4-based BPM and orbit feedback systems at Sirius

Thursday 11 December 2014 17:00 (15 minutes)

Sirius, a new ultra-low emittance (0.28 nm.rad) synchrotron light source, is currently under development at the Brazilian Synchrotron Light Laboratory (LNLS). Sirius's beam position monitor (BPM) and fast orbit feedback (FOFB) systems will adopt MicroTCA.4 infrastructure for its electronics and communication.

Sirius's most stringent BPM specification is the electron beam position monitoring noise over a 0.1 Hz - 1 kHz bandwidth, which should be less than 80 nm RMS. Together with an overall loop latency of less than 50 us throughout 500 meters of storage ring's circumference and proper subsystems' response bandwidth, this specification will make it possible to reach a closed-loop 0 dB crossover frequency of 1 kHz, at least doubling the performance of present day similar systems.

The position data from all BPMs in the MicroTCA.4 crate must be sent to FPGA-based boards called FOFB processors, which will distribute electron and photon BPM data to all other FOFB processors located in other crates and calculate orbit correction setpoints to be sent to the steering magnets' power supplies. All data transmission in this system is latency critical, therefore the system topology must be carefully chosen to avoid limitations on day-zero and future performance. This presentation will show the work already done for the BPM electronics as well as the proposed system architectures for reaching low-latency data transmission in a MicroTCA.4-based system.

Primary author: Mr BRUNO, Gustavo (LNLS)

Co-authors: Mr TAVARES, Daniel (LNLS); Mr RUSSO, Lucas (LNLS); Mr BARON, Rafael (LNLS); Mr MARQUES, Sergio (LNLS)

Presenter: Mr BRUNO, Gustavo (LNLS)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **23** Type: **not specified**

EMI Tests in MTCA.4

Wednesday 10 December 2014 13:45 (15 minutes)

EMI problems in MTCA.4 system can degrade the whole system accuracy. An AMC board called DAMC-EMI board was developed at DESY to easily identify the conductive mode EMI problems in MTCA.4 system. Now a new revision (R1.1) of the board has been developed. A selected measurement results which show some of the EMI problems in MTCA.4 systems are presented.

Primary author: Dr OWCZAREK, Tomasz (Warsaw University of Technology, ISE)

Presenter: Dr OWCZAREK, Tomasz (Warsaw University of Technology, ISE)

Session Classification: Standard

Track Classification: Standard

Contribution ID: **25** Type: **not specified**

MicroTCA.4-based Timing System used at XFEL and FLASH/FLASH2

Wednesday 10 December 2014 17:15 (15 minutes)

At XFEL accelerator almost 150 MicroTCA crates will be synchronized with a picosecond stable timing signal.
An overview of this timing system based on MicroTCA.4 technology, responsible for triggering components like lasers, kickers, etc in XFEL and FLASH accelerator will be given. The presentation will give a look into design of hardware, drift and length compensated signal distribution, user interface configuration and into the current setup in different facilities at DESY.

Primary author: STECHMANN, Christoph (DESY)

Presenter: STECHMANN, Christoph (DESY)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **26** Type: **not specified**

Conceptual Design of LCLS II BPM System on MicroTCA.4

Thursday 11 December 2014 14:15 (15 minutes)

SLAC National Accelerator Laboratory is building the LCLS II facility. It is a 1MW superconducting Free Electron Laser (FEL) facility capable of producing soft and hard x-rays. There will be about 300 different kinds of Beam Position Monitors (BPM) installed at the LCLS II facility. We have come up with the conceptual design for stripline, button, L-band cavity, and X-band cavity BPM electronics. The BPM controls system will use the MicroTCA (Micro Telecommunication Computing Architecture) for physics platform that consists of a 125MSPS ADC module and 250MSPS ADC module. This paper will discuss the conceptual design of the RTM electronics, system architecture, and preliminary calculation results.

Primary author: Mr XU, Chengcheng (SLAC National Accelerator Laboratory)

Co-authors: Mr YOUNG, Andrew (SLAC National Accelerator Laboratory); Mr OLSEN, Jeff (SLAC National Accelerator Laboratory); Ms HOOBLER, Sonya (SLAC National Accelerator Laboratory); Mr STRAUMANN, Till (SLAC National Accelerator Laboratory)

Presenter: Mr XU, Chengcheng (SLAC National Accelerator Laboratory)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **27** Type: **not specified**

W7-X Dispersion Interferometer's Current Signal Processing and Future Bayesian Model Based Data Analysis

Thursday 11 December 2014 10:00 (15 minutes)

The dispersion interferometer (DI) diagnostic, which can be used to measure line integrated electron density, currently performs data acquisition and signal processing with an FPGA embedded on the SIS8300-L board. This W7-X interferometer is being developed to calculate a real time estimation of the line integrated electron density, store raw data and transmit processed signal for control purposes via a real-time network. This diagnostic has a complex non-linear signal model involving arccosine ambiguity that has to be estimated to obtain the parameter of interest. The complexity of the model, required assumptions and final estimation of the uncertainty motivates to address alternatives using other methods. The use of Bayesian probability theory and forward modeling would achieve a purely mathematical model reaching a more informed estimation of a value and a rigorous determination of its uncertainty. This technique has been typically used for post processing. A real-time processing implementation is needed and still missing. Possible approaches are the use of on an FPGA (Field Programmable Gate Array) or a Hardware/Software combination which can make use of efficient backplane communications of the current platform the DI is currently using. If achieved, the approach could be useful for diverse applications generating signals for control systems or determining required parameters. This projects reach includes improvement of data integration and signal processing on smart systems or other platforms that have incoming data from several peripherals, in the way some diagnostics are integrated using Bayesian graphical models.

Primary author: Mr TRIMIÑO MORA, Humberto (Max-Planck Institut für Plasmaphysik)

Presenter: Mr TRIMIÑO MORA, Humberto (Max-Planck Institut für Plasmaphysik)

Session Classification: Software for MicroTCA.4

Track Classification: Software for MTCA.4

Contribution ID: **28** Type: **not specified**

Architecture and main features of the Virtex-7 MTCA.4 carrier IC-FEP-TCAa and its 1.6 GSPS 4 channel FMC

Wednesday 10 December 2014 15:15 (15 minutes)

This presentation will explain the architecture and the main features of the Virtex-7 MTCA.4 carrier (IC-FEP-TCAa)and the four channel 1.6 GSPS ADC FMC (IC-ADC-FMCc) developed in cooperation with DESY.

Primary author: Mr WASTIAUX, Thierry (Interface Concept)

Presenter: Mr WASTIAUX, Thierry (Interface Concept)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **29** Type: **not specified**

uTCA and MTCA.4 hardware used at KEK

Wednesday 10 December 2014 16:15 (15 minutes)

We have been developed micro-TCA boards for LLRF controls. Multi AD/DA board has been used at cERL (test facilities for electron recovery linac), STF (superconducting rf test facility) and super KEKB. The board is controlled by EPICS on the FPGA (Virtex5-FX). Recently, we have also developed MTCA.4 board for multi-cavity control. I will also report this board.

Primary author: Dr MICHIZONO, Shinichiro (KEK)

Presenter: Dr MICHIZONO, Shinichiro (KEK)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **30** Type: **not specified**

A MicroTCA Power Module Test Pad and a short status report on the MTCA evaluation project at CERN

Wednesday 10 December 2014 16:30 (15 minutes)

MicroTCA is a candidate platform for the upgrade of the Large Hadron Collider (LHC) experiments at CERN. The CERN PH-ESE group launched in 2011 the µTCA evaluation project whose aim is to perform technical evaluations and provide support for selected components. Products tested are shelves, MicroTCA Carrier Hubs (MCH) and power modules (PM). The project includes the electrical evaluation of PMs, thermal characterization of shelves and IPMI functionality tests. The electrical evaluations of PMs include static and dynamic regulation tests, efficiency and power factor measurements, ripple and noise characterization as well as an overcurrent protection test. In order to evaluate the power modules on a dedicated setup as well as to be able to perform all PM related tests in a systematic manner, a dedicated automatic PM test pad has been developed. It offers the possibility to check certain µTCA compliant functionalities as well as the possibility to evaluate the Power Module's EMI compliance that cannot easily be tested when the PM is installed in a µTCA shelf. The test bench includes software and hardware components that provide information about the PM under test and verify its compliance with the standard.

This presentation will give an overview on the PM test pad, its hardware and software implementation and the functionalities it offers. We will present details about the test procedure as well as results obtained. Moreover, this presentation will give a brief status update on the µTCA evaluation project currently being carried out in the CERN PH-ESE group.

Primary author: Mr MENDEZ, Julian (CERN)

Presenter: Mr MENDEZ, Julian (CERN)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **31** Type: **not specified**

Update on the MicroTCA.4 User Tool Kit (MTCA4U)

Thursday 11 December 2014 09:45 (15 minutes)

The main goal of the MicroTCA.4 User Tool Kit (MTCA4U) is to facilitate the development of control applications with MicroTCA.4. It provides a universal PCIexpress driver, a C++ library for accessing the MicroTCA devices and tools for interfacing the control system. We report on the new features which have been established, for example command line tools and python bindings which allow easy scripting. Especially the control system adapter is important because it facilitates the integration of control and feedback algorithms into different software ecosystems. A lot of work has been invested into the code quality. MTCA4U is tested on a continuous integration server running a unit test suite with code coverage report, memory leak checks and a static code analysis.

Primary author: KILLENBERG, Martin (DESY)

Presenter: KILLENBERG, Martin (DESY)

Session Classification: Software for MicroTCA.4

Track Classification: Software for MTCA.4

Contribution ID: **32** Type: **not specified**

A universal PCI Express driver for MicroTCA.4

Thursday 11 December 2014 09:30 (15 minutes)

DESY is developing a universal, modular and expandable PCI Express driver for the use in MicroTCA.4 systems. In the last year the driver has seen many improvements. In collaboration with Cosylab, the performance of the Direct Memory Access has significantly been improved. Currently the driver is going through a full review to solve the remaining bugs, ensure stable hot-plug performance, improve the user interface and harden the driver
for production use.

We report on our experience with the modular driver concept for the developments for FLASH and the European XFEL, where it is being used for several years now.

Primary author: Mr PETROSYAN, Ludwig (DESY)

Presenter: Mr PETROSYAN, Ludwig (DESY)

Session Classification: Software for MicroTCA.4

Track Classification: Software for MTCA.4

Contribution ID: **33** Type: **not specified**

MTCA and PCI Express and PCI Express Hot Swap under Linux

Tuesday 9 December 2014 16:15 (45 minutes)

The MTCA use the PCI Express bus as a central bus of data transmissions.
The AMC module to be visible to the user application has to be enabled in PCI Express bus and right configured.

One of especially important features of this bus is a possibility of hot replacement of the devices without rebooting an operating system.
The PCI Express Hot-Swap service is being used relatively long. However, the MTCA system makes its own amendments into general architecture of the PCI Express Hot-Swap and in the methods and ways of use.

Our experience of the adjustment, starting and testing as well as use of the PCI Express Bus and PCI Express Hot-Swap in MTCA architecture will be presented.

Primary author: Mr PETROSYAN, Ludwig (DESY)

Presenter: Mr PETROSYAN, Ludwig (DESY)

Session Classification: Tutorials by experts

Contribution ID: **34** Type: **not specified**

Towards a Standard Hardware API and a Standard Device Model

Wednesday 10 December 2014 11:15 (15 minutes)

To interface with the outside world, many devices provide some control registers which can be accessed via a field bus. Introducing a standardised set of registers will allow one to use the same software tools for many board. They can for instance have a common driver or user space library. The PICMG software working group is currently working on an implementation recommendation guideline called Standard Hardware API, with the goal to improve the interoperability and compatibility of boards from different labs and vendors.

On the higher software level devices often represent themselves either as random access devices to an address range or as streaming devices. A Standard Device Model will allow one to access these functionalities through a uniform interface, abstracting the access details of the actual hardware. The PICMG software working group is preparing an implementation recommendation guideline for such a model and will provide use case reference implementations.

The talk on behalf of the Software Working Group presents the ideas and design concepts of these PICMG recommendations.

Primary author: PICMG, Software Working Group (DESY)

Presenter: Mr STRAUMANN, Till (SLAC National Accelerator Laboratory)

Session Classification: Standard

Track Classification: Standard

Contribution ID: **35** Type: **not specified**

FLASH2/XFEL machine protection system, experience

Thursday 11 December 2014 16:15 (15 minutes)

Reliability, flexibility, scalability and timeliness are only a few functional requirements a machine protection system (MPS) is permanently confronted with. This presentation tries to show how the newly developed µTCA-based MPS for FLASH2 and XFEL tries to fulfill these requirements with reasonable effort. The chosen hardware, the MPS-internal fiber optical communication topology, the multitude of alarm providing systems, and the cooperation concept with the µTCA-based timing system are shown.

Primary authors: Mr JAEGER, Juergen M. (DESY); Mr STAACK, Martin (DESY); Mr KARSTENSEN, Sven (DESY)

Co-author: Mr KUNZE, Robert (DESY)

Presenter: Mr JAEGER, Juergen M. (DESY)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **36** Type: **not specified**

MTCA.4 Products and Solutions for accelerators at CAEN ELS

Thursday 11 December 2014 14:45 (15 minutes)

An overview of CAEN ELS products related to the MTCA.4 standard will be introduced. The HV-PANDA multi-channel High-Voltage power supply module, the FMC-Pico-1M4 quad-channel low-current measurement front-end that can be used in conjunction with the DAMC-FMC25 board for quadrature BPM applications and the dual/quad channel SPF+ FMC modules will be presented as self-developed or distributed and supported solutions.

Primary author: BRAIDOTTI, Enrico (CAEN ELS d.o.o)

Co-author: FARINA, Simone (CAEN ELS d.o.o)

Presenter: BRAIDOTTI, Enrico (CAEN ELS d.o.o)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **38** Type: **not specified**

New MTCA.4 AMC and µRTM for high channel count ADC applications

Thursday 11 December 2014 15:00 (15 minutes)

This talk presents the TAMC532, an MTCA.4 compliant AMC and its companion µRTM TAMC532-TM for high channel count analog to digital conversion applications, developed within HVF.
The TAMC532 provides 32 ADCs with 12 or 14 Bit resolution. Depending on the resolution, sample rates up to 75 Msps are possible.
A powerful clock distribution allows using the TAMC532 in nearly any clocking scheme required by the application.
A Kintex-7 FPGA provides the ability to transfer ADC data via x4 PCI-Express Gen 2 or two SFP+ interfaces. In addition, on-board DDR3 memory allows to store ADC data for subsequent readout.
The ADCs analog inputs connect to a µRTM via Zone 3 with a pin assignment according to Class A2.1.
Signal conditioning and analog input connectors are located on the µRTM, allowing easy adaption to different user requirements.
The TAMC532-TM is a µRTM according to Class 2.1, and holds an adjustable gaussian shaping amplifier for each of the 32 input channels.

Primary author: Mr KOLL, Niels (TEWS Technologies)

Presenter: Mr KOLL, Niels (TEWS Technologies)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **39** Type: **not specified**

Status of MicroTCA at DESY and XFEL

Wednesday 10 December 2014 16:00 (15 minutes)

FLASH is running reliably 24/7 in user operations since a few month with 20 MicroTCA crates. First installations are available for the European XFEL as well. During the next months this installation will grow to about 200 crates. Both facilities are equipped with commercial of-the-shelf products and with in-house designs. The talk will give an overview of the installations and the status of the board designs.

Primary author: Mr REHLICH, Kay

Presenter: Mr REHLICH, Kay

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **40** Type: **not specified**

MicroTCA.4 Event Receiver for MRF Timing System

Wednesday 10 December 2014 17:30 (15 minutes)

A native MicroTCA.4 prototype of an event receiver for the MRF timing system has been developed. This presentation will discuss lessons learned during the development process and provide a brief look at the future enhancements of the MRF timing system.

Primary author: Mr PIETARINEN, Jukka

Presenter: Mr PIETARINEN, Jukka

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **42** Type: **not specified**

PICMG Hardware and Software Group Updates

Wednesday 10 December 2014 11:00 (15 minutes)

The PICMG xTCA for Physics Technical Committees were approved in May 2009 so now have been operating for over five years. The major work of the PICMG MTCA.4 hardware extensions to MTCA.0, "MicroTCA Enhancements for Rear I/O and Precision Timing", was approved in September 2011, a short time for such an extensive undertaking. This standard seems now firmly established in several labs and supporting industries. In addition software guideline tasks drafted in2009 have continued to develop slowly until a year ago. Thanks to new volunteers joining after an appeal at MTCAWS 2013, three new guidelines are very close to submittal to PICMG for approval. The hardware standard has also advanced further to include an auxiliary RTM backplane invented by the DESY XFEL team for use specifically in the Low Level RF system, but with potential applicability to many different applications; as well as protective covers for both sides of AMCs and RTMs. The status and roadmaps for these emerging standards and guidelines will be described. As new applications discover other imaginative uses for MTCA.4, the Committees anticipate fruitful work will continue well into 2015.

Primary author: LARSEN, Raymond (IC Division, SLAC)

Presenter: LARSEN, Raymond (IC Division, SLAC)

Session Classification: Standard

Track Classification: Standard

Contribution ID: **43** Type: **not specified**

eicSys activities for MTCA.4 Technology

Thursday 11 December 2014 15:30 (15 minutes)

Review of eicSys activities for MTCA.4
Technology Presentation of existing Boards in License from DESY Presentation of existing Boards in own development.
Upcoming new developments of MTCA.4 Boards, FMC´s and Systems. First application plans for MTCA.4 in industry projects.
Roadmap for developments.

Primary author: Mr FIX, Friedrich (eicSys GmBH)

Presenter: Mr FIX, Friedrich (eicSys GmBH)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **44** Type: **not specified**

Ratified ZONE 3 classes to achieve enhanced AMC-RTM modularity

Wednesday 10 December 2014 11:30 (15 minutes)

To enhance the compatibility and modularity of AMC and RTM boards, board manufacturers should follow the ZONE3 classes for analog or digital applications. The ZONE3 classes are in the ratification process of the PICMG consortium. For having a simple E-keying based on class identifiers and to guarantee the backward compatibility of existing boards, subclasses in the analog class were introduced and presented here with helpful examples.

Primary author: Dr LUDWIG, Frank (DESY)

Presenter: Dr LUDWIG, Frank (DESY)

Session Classification: Standard

Track Classification: Standard

Contribution ID: **45** Type: **not specified**

Future High-Speed ADC and DAC Developments, Trends and Technology Advances

Thursday 11 December 2014 13:30 (45 minutes)

High speed data converter technology has seen break-troughs in terms of performance and functionality in the past 10 years. Some key applications have been driving the development of leading edge data converter technology:
o The wireless broadband broad-band revolution, starting with GSM as a voice-only service till the late 1990s, evolving to EDGE and Multi-carrier GSM, then followed by WCDMA and quickly by LTE thereafter with tremendous increases in requirements on dynamic range, bandwidth and as well foot-print with the introduction of MIMO antenna systems. Now 5G as the next future generation is already on the horizon and expected to present new challenges.
o Wide-spread adoption of sophisticated medical imaging systems like ultra-sound, MRI or CT scanners. Massive beam-forming and desire for detecting smallest features to create accurate 2D and 3D representations of the human body's inside are key characteristics.
o Introduction of high-density phased array approaches for example in radar systems drives the need for accurate synchronization of very complex, often distributed systems allowing to quickly scan large areas with static antennas instead of previously used rotating antennas.
o Ultimately, the aim to create true Software Defined Radios (SDRs), capable of operating at virtually every frequency and with every wave form, is calling for a revolution in radio architectures and thus motivating the use direct sampling technology, eliminating frequency conversion stages and frequency specific components.

Now that some of the underlying drivers have become clear, the quest for ever more data converter performance is on and we'll take a look at the challenges involved specifically for data converters:
o Wider bandwidth and the need to detect ever smaller signals are pushing dynamic performance & sample rate of data converters. We will look at trends for those and what factors are limiting ultimate performance.
o Innovative architectures can help boost performance and move closer to the ideal performance and we'll introduce some recent advances.

Spot light on interfaces: The evolution from CMOS to LVDS to JESD204B has enabled step functions in interface throughput and density
o Synchronization for complex large array systems presents a challenge. JESD204B was defined with that in mind and introduces that capability as a standard feature.
o Enabling remote concepts: Usage of a serialized digital link allows to route sample over wider distances, back planes and even over fiber.
o Latency becomes deterministic: Aligning the sampling instant of individual elements in distributed systems becomes easier, but how is overall system latency managed?

Where will we go next?

Primary author: FEULNER, Matthias (Texas Instruments Deutschland GmbH)

Presenter: FEULNER, Matthias (Texas Instruments Deutschland GmbH)

Contribution ID: **46** Type: **not specified**

MTCA Digitizers and RTMs, Downconversion versus Direct Sampling

Thursday 11 December 2014 15:15 (15 minutes)

Enhancements of the SIS8300 10 channel 125 MSPS 16-bit AMC digitzer resulting in the SIS8300-L2 design will be presented.
The status of the 250 MSPS 16-bit SIS8325 MTCA.4 digitizer will be addressed. Both the SIS8300 family and the SIS8325 can be used with Downconverter and direct sampling RTMs to cover a range of frequencies and applications.
Possible future developments comprise a 1.6/3.2 GSPS 12-bit and a 1 GSPS 14-bit design for high speed direct sampling for current transformer readout and a variety other applications.

Primary author: Dr KIRSCH, Matthias (Struck)

Presenter: Dr KIRSCH, Matthias (Struck)

Session Classification: New Products

Track Classification: New products and updates

Contribution ID: **47** Type: **not specified**

Welcome to DESY

Wednesday 10 December 2014 10:00 (15 minutes)

Primary author: Prof. DOSCH, Helmut (DESY)

Presenter: Prof. DOSCH, Helmut (DESY)

Session Classification: Welcome

Contribution ID: **48** Type: **not specified**

Helmholtz Validation Fund Results and Perspectives

Wednesday 10 December 2014 10:15 (15 minutes)

Presenter: Dr SCHLARB, Holger (DESY)

Session Classification: Welcome

Contribution ID: **49** Type: **not specified**

PICMG activities, new and future standards

Wednesday 10 December 2014 10:30 (30 minutes)

PICMG activities, new and future standards

Primary author: PAVLAT, Joe

Presenter: PAVLAT, Joe

Contribution ID: **50** Type: **not specified**

MicroTCA.4 Tutorial Basics

Tuesday 9 December 2014 14:00 (45 minutes)

MicroTCA.4 Tutorial Basics

Primary author: Mr MANN, Dietmar (PENTAIR)

Presenter: Mr MANN, Dietmar (PENTAIR)

Session Classification: Tutorials by experts

Contribution ID: **51** Type: **not specified**

MicroTCA Management

Tuesday 9 December 2014 14:45 (45 minutes)

High availability, serviceability and reliability are among the most desirable features of control systems in modern High-Energy Physics (HEPs) and other big-scale scientific experiments. One of the recent developments that have influenced this field was the emergence of the xTCA standards (Advanced and Micro-Telecommunications Computing Architecture). The standards developed for telecommunication industry have been successfully applied in other domains such as accelerator control systems. The Intelligent Platform Management Interface (IPMI) with PICMG extension was applied in xTCA to enhance the availability of the system and simplify hardware diagnostics. The IPMI standard was initially developed to manage computer systems and monitor its operation. In case of xTCA, it provides useful features for shelf management, monitoring of crucial parameters, like: temperature, voltages, supply currents and fan speed. The system manages power, cooling and interconnect resource in the shelf via e-keying mechanism. The tutorial introduce the basics of hardware platform management in MTCA systems. The presentation provides information concerning IPMI basics with PICMG extension and hardware required for shelf management. Finally, the example implementation of Management Controller for Advanced Mezzanine Card (MMC) and Rear Transition Module (RMC) will be presented.

Primary author: Dr MAKOWSKI, Dariusz (DMCS)

Presenter: Dr MAKOWSKI, Dariusz (DMCS)

Session Classification: Tutorials by experts

Contribution ID: **53** Type: **not specified**

Closing remarks

Thursday 11 December 2014 17:45 (15 minutes)

Presenter: Dr SCHLARB, Holger (DESY)

Contribution ID: **54** Type: **not specified**

DESY Board Development Stage and Licensing

Thursday 11 December 2014 16:30 (15 minutes)

During the last year, DESY has nearly finished the design of all digital and analog boards for the XFEL Low-Level-RF system. The boards with the widest application fields are being licensed to industry, so they are available for customers outside of DESY - either in industry or in other research facilities. This is a new approach that DESY follows. It helps sharing our experience and knowledge with partners, saves our customers development efforts and gives us the ability to buy our boards of-the-shelf. We benefit from the fact that our partners do board programming and testing. Additionally, our licensees often get better prices for the expensive components, especially for ICs such as FPGAs.
Currently 3rd parties can purchase over ten different newly designed AMC cards. On the high-end side of our digital portfolio we offer DAMC-TCK7, a Kindex-7 based AMC card for high-end computing and transmission tasks which is now available from Vadatech under the name CM045. A mid-range digital signal processing board with a Virtex-5 and two FMC slots is the DAMC-FMC25, which is now available from CAENels. On the price-sensitive end we offer the Spartan-6 based dual FMC carrier DAMC-FMC20, which is marketed under the Eicsys Name EAMC-FMC500. In the analog field, our Downconverter DRTM-DWC10, our Downconverter-Vector-Modulator DRTM-DWC8VM1 and our feed through Board DRTM-DS8VM1 are available from Struck Innovative Systems. More information about our products including MMC Starter Kit, Piezo drivers, FMC cards and many more can be found at http://mtca.desy.de.

Primary author: Mr FENNER, Michael (DESY)

Presenter: Mr FENNER, Michael (DESY)

Session Classification: Applications in research facilities

Track Classification: Applications in research facilities

Contribution ID: **55** Type: **not specified**

Tutorial about MicroTCA.4

Tuesday 9 December 2014 15:30 (45 minutes)

Tutorial about MicroTCA.4

Primary author: DIRKSEN, Vollrath (N.A.T. GmbH)

Presenter: DIRKSEN, Vollrath (N.A.T. GmbH)

Session Classification: Tutorials by experts

Contribution ID: **56** Type: **not specified**

Simulation of High Speed Interfaces with Ansys Software

Thursday 11 December 2014 14:30 (15 minutes)

An Introduction to Ansys simulation software for Signal Integrity is presented. A PCI Express 8 GT/s Channel example is shown. Analysis and post processing in frequency domain is shown in the SIwave tool. Also, time domain specification in the tool HFSS SI is mentioned.

Primary author: Mr FOCHO, Atte Formum (Ansys Germany)

Presenter: Mr FOCHO, Atte Formum (Ansys Germany)

Session Classification: New Products