Project Specification
Project Name: CHESS-1

Test Chip: CMOS (HV/HR) Evaluation for Strip Sensors-1

Version: V 0.1

Abstract

This document lists the target specifications for the test chip, which will be fabricated and tested in order to evaluate the basic device performance of HV-CMOS technologies for use as a silicon strip sensor. Two representative foundries will be used.

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Revision History			
Rev. No.	***Date***	***Pages***	***Description of Changes***

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1 SCOPE

This document describes the details of the target specification for a test chip, which will be fabricated in order to evaluate the basic device properties of HV-CMOS technologies for use as silicon strip sensors in place of the traditional planar silicon strip sensors. The test chip will be made up of several different types of test structures, each designed to test certain characteristics of the technologies. For each type of test structure, several variations of device features will be included, for example variations in the length and fill factor of the individual pixel area. The expectation is that two foundries will be sampled and some technology specific differences will be made to the designs to match the requirements of each foundry's technology.

2 Foundries

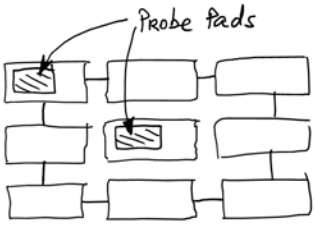
Two foundries will be targeted at this time based upon the current understanding of the available technologies and their appropriateness for strip sensors. The two technologies are Tower-Jazz TJ180 and Austrian Micro Systems AMS-H35.

3 Test Structure Types and Their Specifications

The test chip will be comprised of five different types of test structures. Each is described below along with their specifications and variations.

3.1 Passive Pixel Arrays

There will be groups of 3 x 3 pixels arranged in a rectangular array such that the eight outer pixels are electrically tied together and connected to a single probe pad. The inner pixel will be connected to a separate probe pad. An example is shown in Figure 3.1.1. This will allow direct measurements of the charge collection characteristics and pixel capacitance independent of any built-in amplifier circuitry. About 40% of the top pixel surface should have no metallization to allow laser injection measurements.



{Need to include pad positions and sizes in figure or another table.}

Figure 3.1.1 Layout of Typical Passive Pixel Array

3.1.1 Passive Pixel Array Specifications

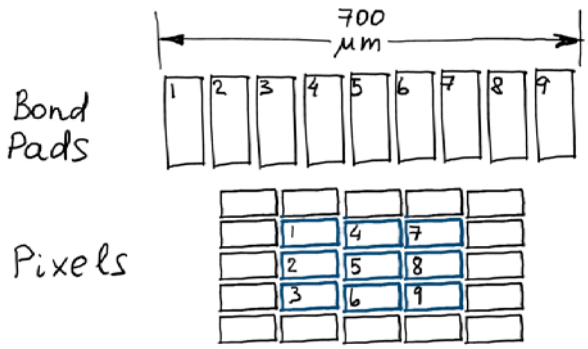
The passive pixel arrays will have the following specifications. For each set of specifications, ? arrays will be included.

Table 3.1.1 Spatial Specifications for Passive Pixel Arrays

PPA #	Pixel Dimensions	Fill Factor	??	??
PPA01	37 µm x 100 µm	50%		
PPA02	37 µm x 100 µm	90%		
PPA03	37 µm x 200 µm	50%		
PPA04	37 µm x 200 µm	90%		
PPA05	37 µm x 400 µm	50%		
PPA06	37 µm x 400 µm	90%		
PPA07	37 µm x 800 µm	50%		
PPA08	37 µm x 800 µm	90%		

3.2 Active Pixel Arrays

There will be groups of 5 x 5 pixels arranged in a rectangular array. Each pixel will include a fast amplifier circuit, which may not be representative of the amplifiers to be used in the actual CMOS strip sensors but is very fast to allow evaluation of the time structure of the collected charge. The power consumption of this amplifier is not a concern. The 16 outer ring of pixels are electrically ties together and connected to a single bond pad. The inner 9 pixels will be each connected to separate bond pads. An example of such a pixel array and the associated bond pads is shown in Figure 3.2.1.



{Need to include pad positions and sizes in figure or another table.}

Figure 3.2.1 Layout of Typical Active Pixel Array

3.2.1 Active Pixel Array Specifications

The active pixel arrays will have the following spatial specifications. For each set of specifications, ? arrays will be included.

Table 3.2.1 Active Pixel Array Spatial Specifications

APA #	Pixel Dimensions	Fill Factor	??	??
APA1	37 µm x 100 µm	50%		
APA2	37 µm x 100 µm	90%		
APA3	37 µm x 200 µm	50%		
APA1	37 µm x 200 µm	90%		
APA2	37 µm x 400 µm	50%		
APA3	37 µm x 400 µm	90%		

APA2	37 μm x 800 μm	50%		
APA3	37 μm x 800 μm	90%		

The amplifier circuit included in each pixel will have the following electrical specifications:

Table 3.2.2 Fast Amplifier Specifications

Risetime	<= 10 ns
Noise	<50 e-
Gain	Roughly 1000 mV/fC ?
??	

3.3 Isolated Fast Amplifier

An isolated example of the fast amplifier circuit used with the active pixel arrays will be included with an input and out pad. This is to separately test the characteristics of the amplifier in order to separate its characteristics and their evolution with radiation from that of the passive pixel sensors. ? copies of this amplifier will be included. {Do we need a picture with a pad layout?}

3.3.1 Isolated Fast Amplifier Specifications

Substantially the same as what is used for Active pixel array in section 3.2 .

3.4 Isolated Realistic Amplifier

Two types of realistic amplifiers should be included:

- An amplifier with “tuning knobs”, such as bias current, which can be used to find the technology limits with respect to noise, rise time, and power consumption when no special techniques are used to limit the rise time.
- An amplifier with additional timewalk correction scheme designed to improve the time resolution.

Properties

3.5 Array of individual transistors, resistors and capacitors

In order to evaluate the characteristics of individual components of each technology, which will be important for further improvements to the active circuitry to be employed in the final CMOS sensor, an array of transistors, resistors and capacitors will be included.

The pad layout is to copy one already developed by CERN for such purposes. This will allow the use of a probe card already designed and in existence at CERN to test all the devices in this array.

3.5.1 Specifications for Array of Individual Device Structures

Table 3.5.1 Individual Device Properties

Transistors	
Resistors	
Capacitors	

4 Top Level Chip Layout

The layout of the overall chip showing the locations of each type of test structure is shown in Figure 4.1.

Some of the active and passive pixel arrays are located near the edge of the structure to allow edge-TCT measurements of the depletion region.

Figure 4.1: Top View of the Full Chip

5 References