High Resolution Si Pixel Technologies Developed for Charged Particle Tracking in Subatomic Physics

Marc Winter (IPHC-Strasbourg)

contributions: **V.Re (CMOS sensors / INFN-Pavia), L.Andricek (DEPFET / MPI-Munich), M.Demarteau (3D sensors / FNAL-Chicago)**

▷ **More information on Web-site of VERTEX-08, TWEPP-08 & PIXEL-08 workshops**

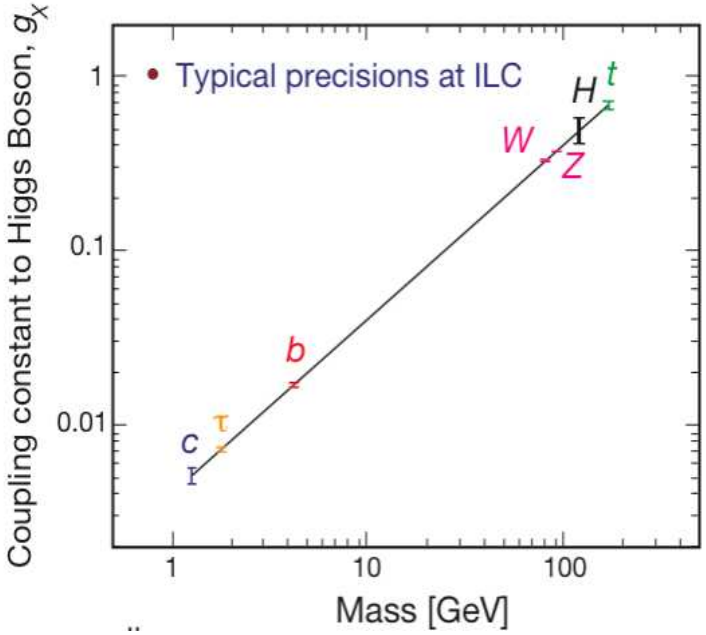
OUTLINE

- *Generic experimental requirements driving SC pixel R&D*
  - *Constraints from physics goals*
  - *Constraints from running conditions*
- *Pixel technologies optimised for read-out speed and radiation tolerance constraints*
  - *Hybrid pixel sensors*
  - *3D sensors*
- *Pixel technologies optimised for spatial resolution and material budget*
  - *CMOS sensors (1st & 2nd generation)*
  - *CCDs*
  - *DEPFETs*
- *The emergence of 3D (quasi-)monolithic pixel sensors*
- *Conclusion – Perspectives*

Fundamental Questions of HEP driving Pixel R&D

- **The physics potential of numerous experimental programmes in subatomic physics depends on performances achievable with SC pixel arrays**
  - *colliders for Particle Physics (PP) : LHC ⟼ SuperLHC ; ILC ⟼ CLIC ; SuperB factory*
  - *Heavy Ion Collisions (HIC) : RHIC ⟼ (s)LHC ; FAIR*

- **High precision pixel detectors are essential for :**
  - ▷ **Discoveries** *(≡ 1st evidence of particle or phenomenon) :*
    - *Higgs boson*
    - *non-standard particles (SUSY part., extra gauge bosons, ...)*
    - *collective phenomena in HIC*
  - ▷ **Characterisation** *(≡ study underlying dynamics: quantum nb, forces) :*
    - *particle properties : ⁂ Higgs couplings to W, Z, q, l, γ,*
      ⁂ strength of non-standard particle decays
    - *production properties : charmed mesons produced in HI collisions*



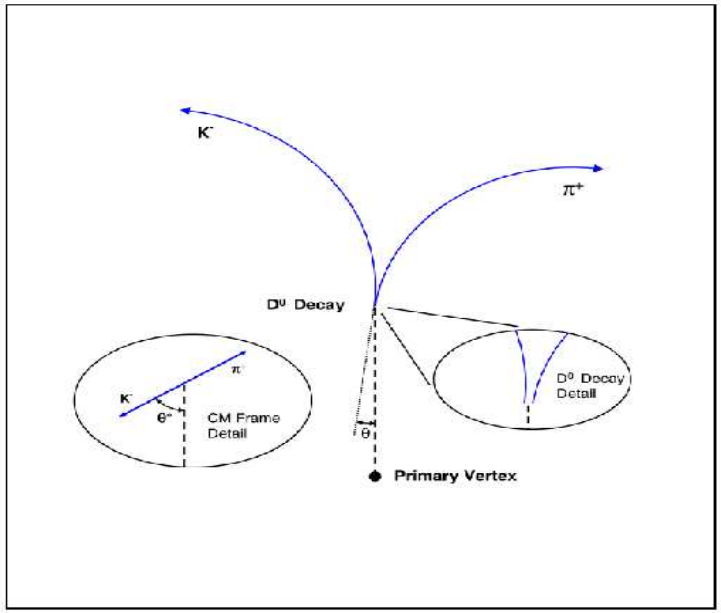
Access to short Lived Particle Decays

Main challenge : identify c quark and $\tau^{\pm}$ lepton jets

↪ *lifetime* $\sim O(10^{-12})$ *s* $\Rightarrow$ $\beta\gamma c\tau \sim 100\ \mu m$

$\Rightarrow$ *particles decay inside vacuum pipe in which beams circulate*

$\Rightarrow$ *recontruct origin of decay products*

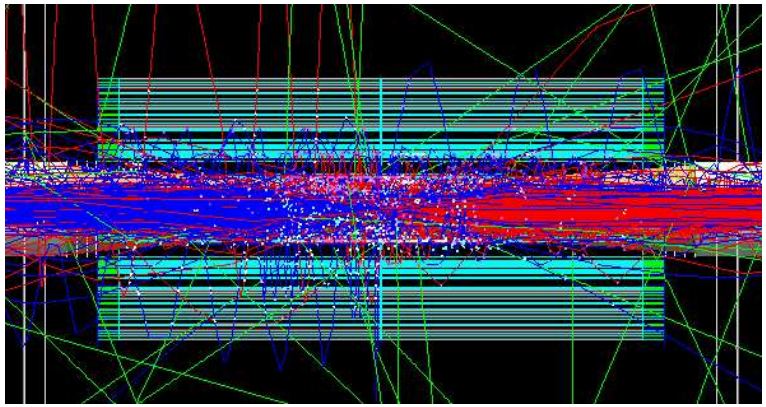


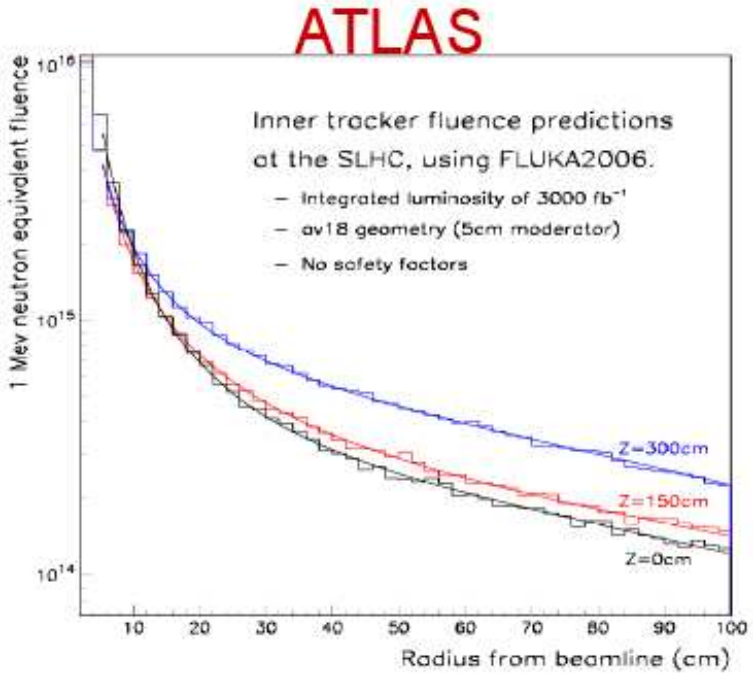
$\Rightarrow$ **Experimental trend :** *pixellised detectors installed very close to the beam interaction region*

▷ **Minimal distance limitations :**

- *beam pipe radius*
- *beam associated backgrounds*
- *density of particles produced at the IP*

▷ **Consequences on occupancy and radiation level**





Optimising = Compromising

Conflict between physics performance driven parameters and running condition contraints :

- *Physics performance : spatial resolution and material budget (+ distance to IR)*
- *Running conditions : read-out speed and radiation tolerance*
- *Moreover :*
  - ⁂ *limitations from maximum power dissipation compatible with running conditions and material budget*
  - ⁂ *limitations from highest data flow acceptable by DAS*

⇛ **Ultimate performance on all specifications cannot be reached** $\underline{simultaneously}$

▷ **each facility & expt requires dedicated optimisation :**

(≡ hierarchy between physics requirements and running constraints)

▷ **there is no single technology best suited to all applications**

- ⁂ *explore various technological options*
- ⁂ *motivation for continuous R&D (optimum is strongly time dependent)*

Balance between Physics & Running Constraints

Physics performance driven :

- *thin (potentially undepleted) sensitive volume*
- *ILC* ↘ *RHIC* ↘ *CLIC, SuperB, FAIR*
- *CMOS sensors, CCDs, DEPFETs*

Running conditions driven :

- *"thick" depleted sensitive volume*
- *LHC* ↗ *SLHC*
- *Hybrid pixel sensors, 3D sensors*

Future : 3D integrated pixel devices (see also talk of Ch. De La Taille)

⇒ *reduce the gap between the two main optimisation options*

Pixel Technologies Adapted to Harsh Running Conditions :

- *pp collisions : LHC* $\rightarrowtail$ *SuperLHC*
- *HI collisions : RHIC, LHC, FAIR*

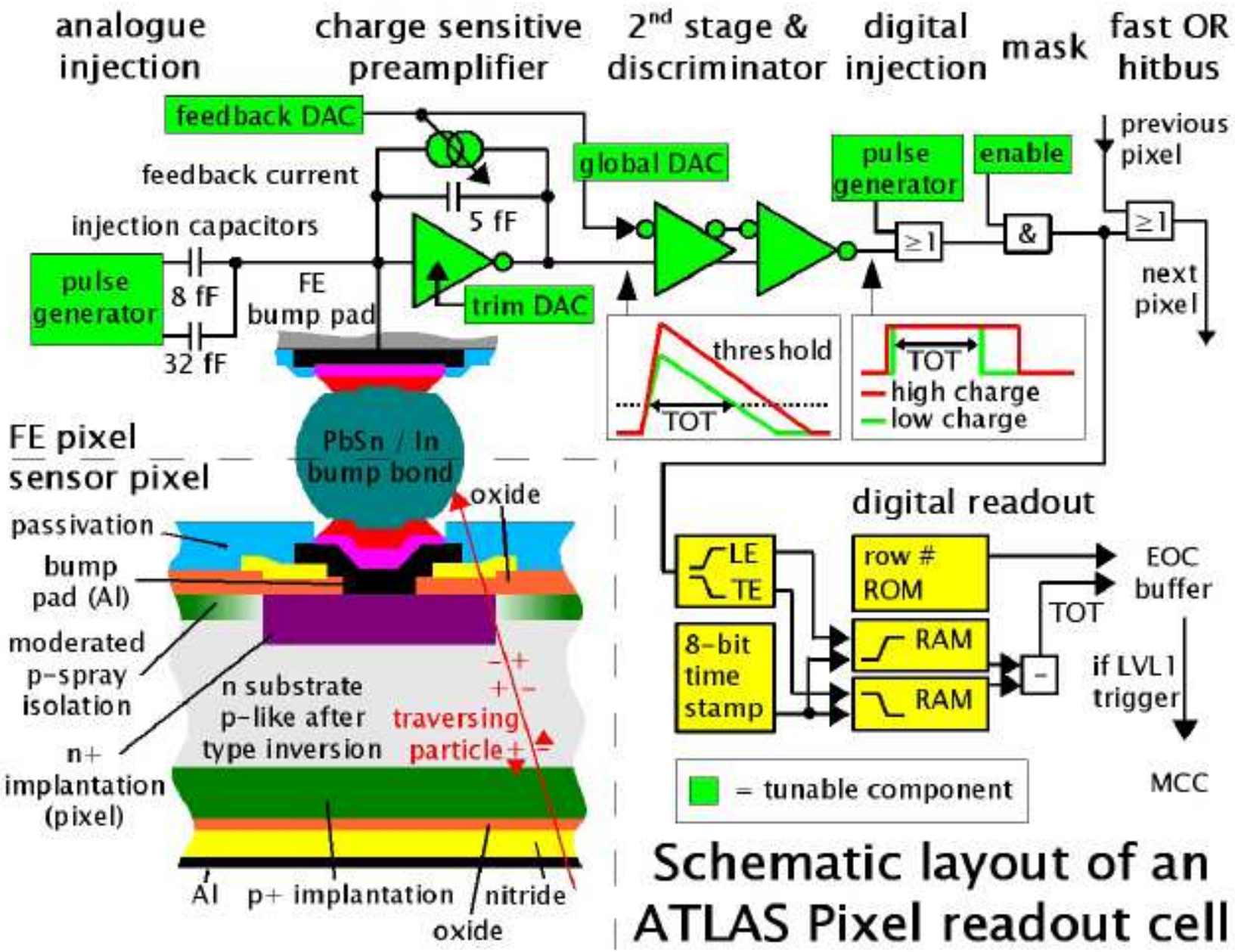
Typical LHC Requirements

Ex: ATLAS pixel requirements *(G.Gaycken - Vertex-08)*

- *Bunch spacing : 25 ns*
- *Radiation hardness : 500 kGy, 10^{15} n_{eq}/cm^2 (life time)*
- *Coverage in pseudo rapidity : $\eta \geq 2.5$ with 3 pixel hits*
- *Occupancy/BX $>$ 0.17 hits per 320 pixel (column pair) for L = 10^{34} $cm^{-2} \cdot s^{-1}$*
- *Efficiency $>$ 98 %*

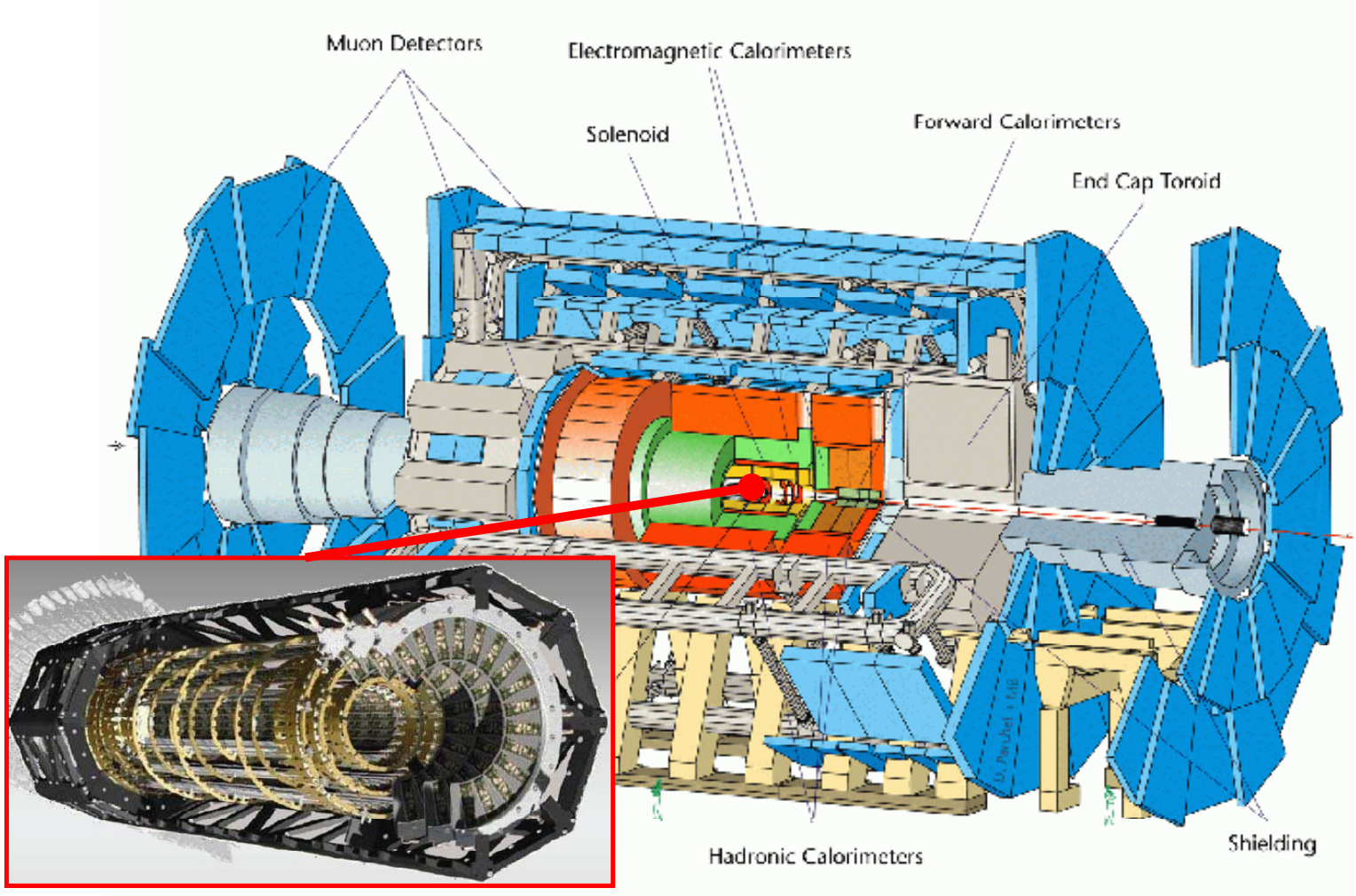
$\Rrightarrow$ **Main detector features :**

- *Pixel dimensions : 50x400 μm^2 (ATLAS) , 100x150 μm^2 (CMS) $\Rightarrow$ $\sigma_{sp}^{transv} \sim$ 10–15 μm*
- *Inner radius : $\sim$ 4–5 cm*
- *Power dissipation : $\gtrsim$ 0.5 W / cm^2*
- *Layer material budget : $\sim$ 1–2 % X_0*
- *Total surfaces covered with pixels : up to 1.8 m^2*
- *Number of Pixels : several 10^7*



Schematic layout of an ATLAS Pixel readout cell

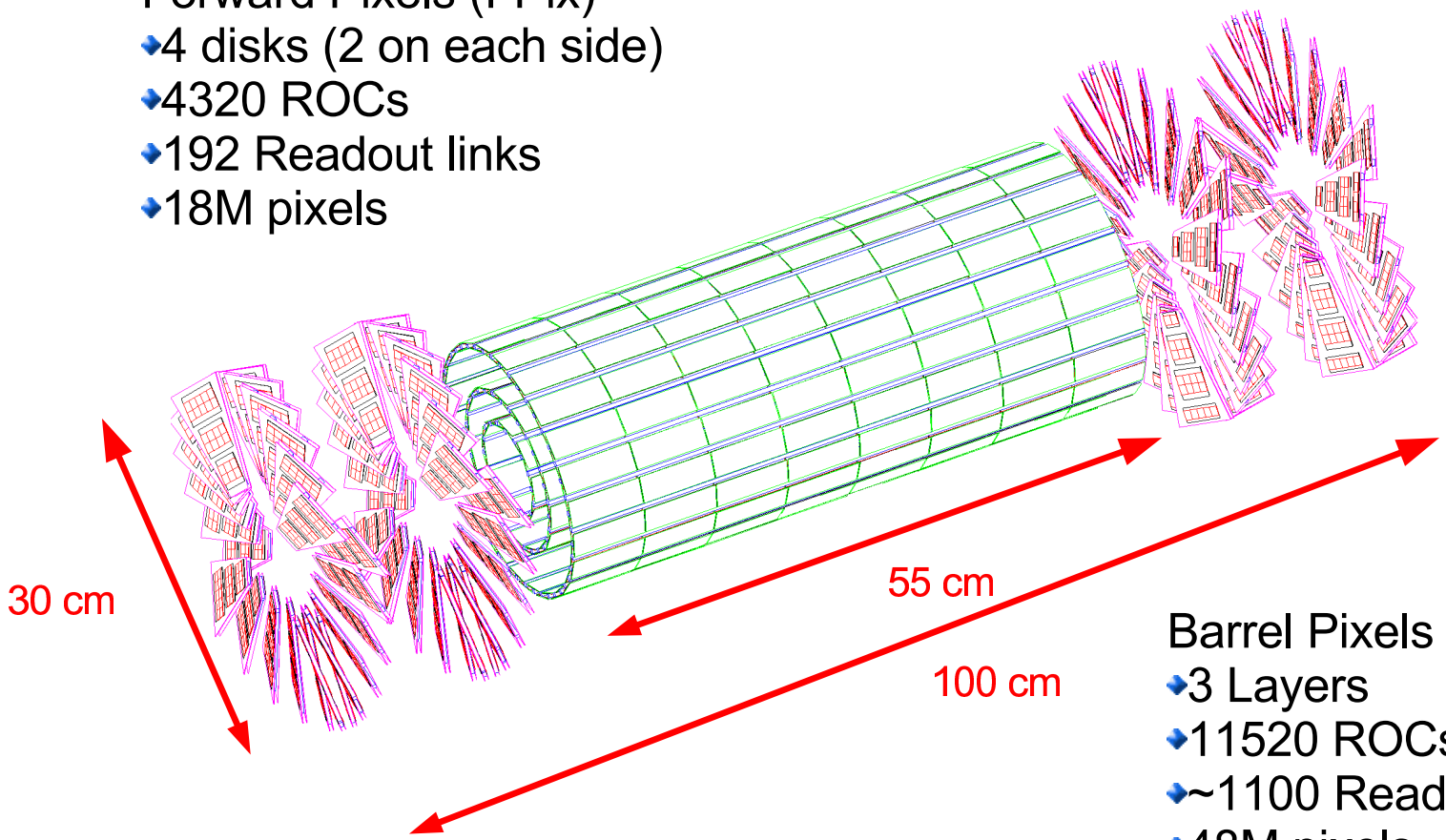
A Toroidal LHC ApparatuS



CMS Pixel Detector

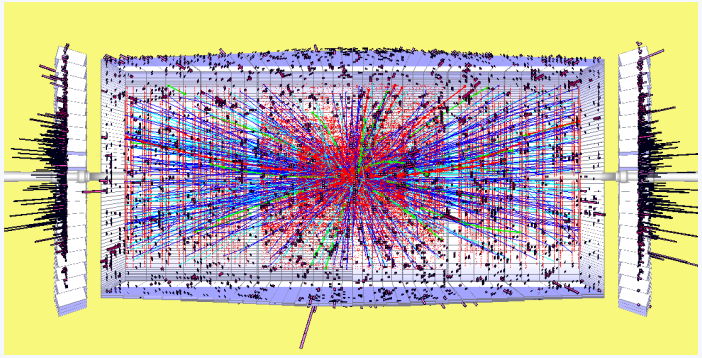
Total of about 66M pixels

Forward Pixels (FPix)
- 4 disks (2 on each side)
- 4320 ROCs
- 192 Readout links
- 18M pixels

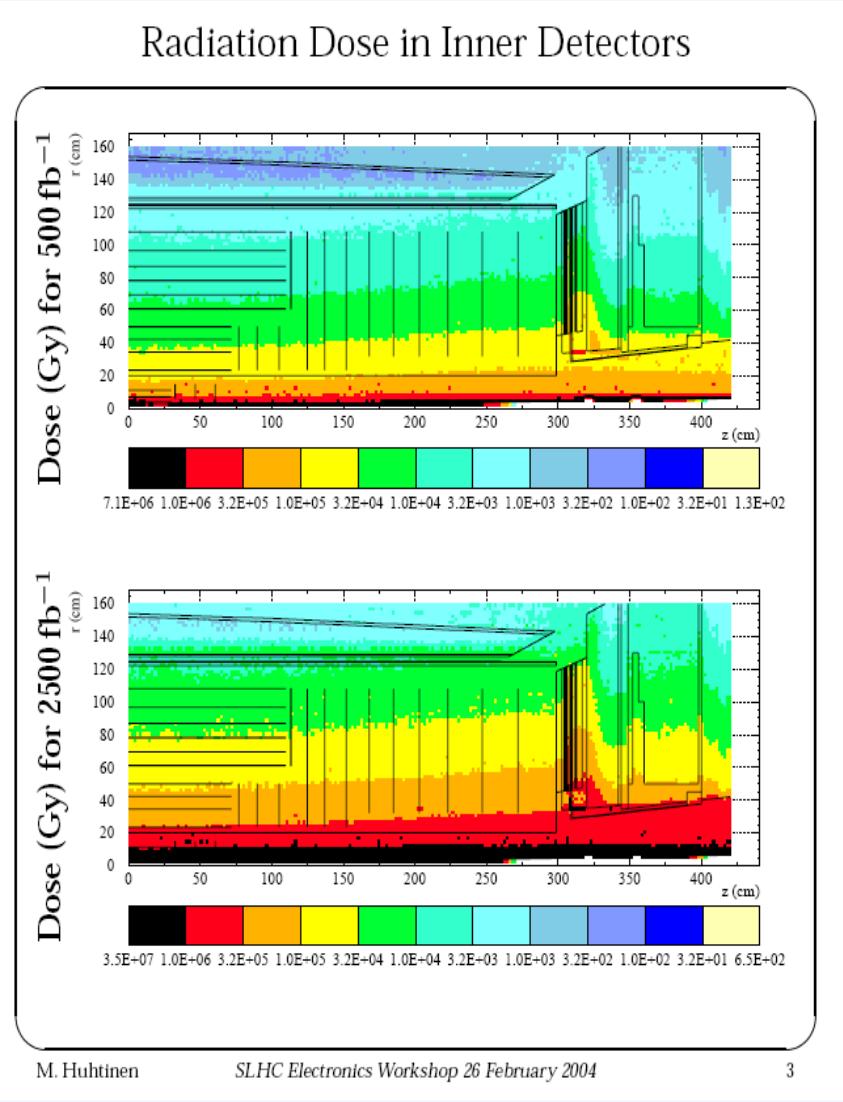


Barrel Pixels (BPix)
- 3 Layers
- 11520 ROCs
- ~1100 Readout links
- 48M pixels

What are the conditions at sLHC?



- 300 – 400 pile-up events at start of spill (unless luminosity levelling)
- Want to survive at least 3000 fb^{-1} data taking
- B-layer at 37 mm:
  - ~30 tracks per cm^{-2} per bunch crossing
  - >10^{16} 1 MeV n-equivalent non-ionising
  - Few 10s of MGray



SLHC : Several Technological Solutions under Study

Improvement/evolution of hybrid pixel sensors :

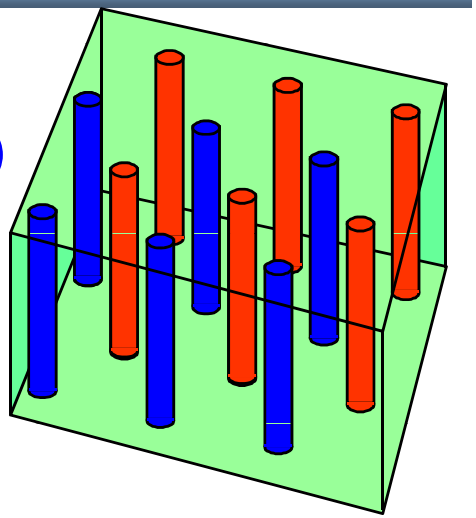
- *Smaller CMOS feature size ⇒ more compact FE μcircuits*
  - *⇒ smaller pixels ⇒ occupancy*
- *Improved sensitive volume radiation hardness*
- *Larger nb of pixels ⇒ power dissipation is an issue !*

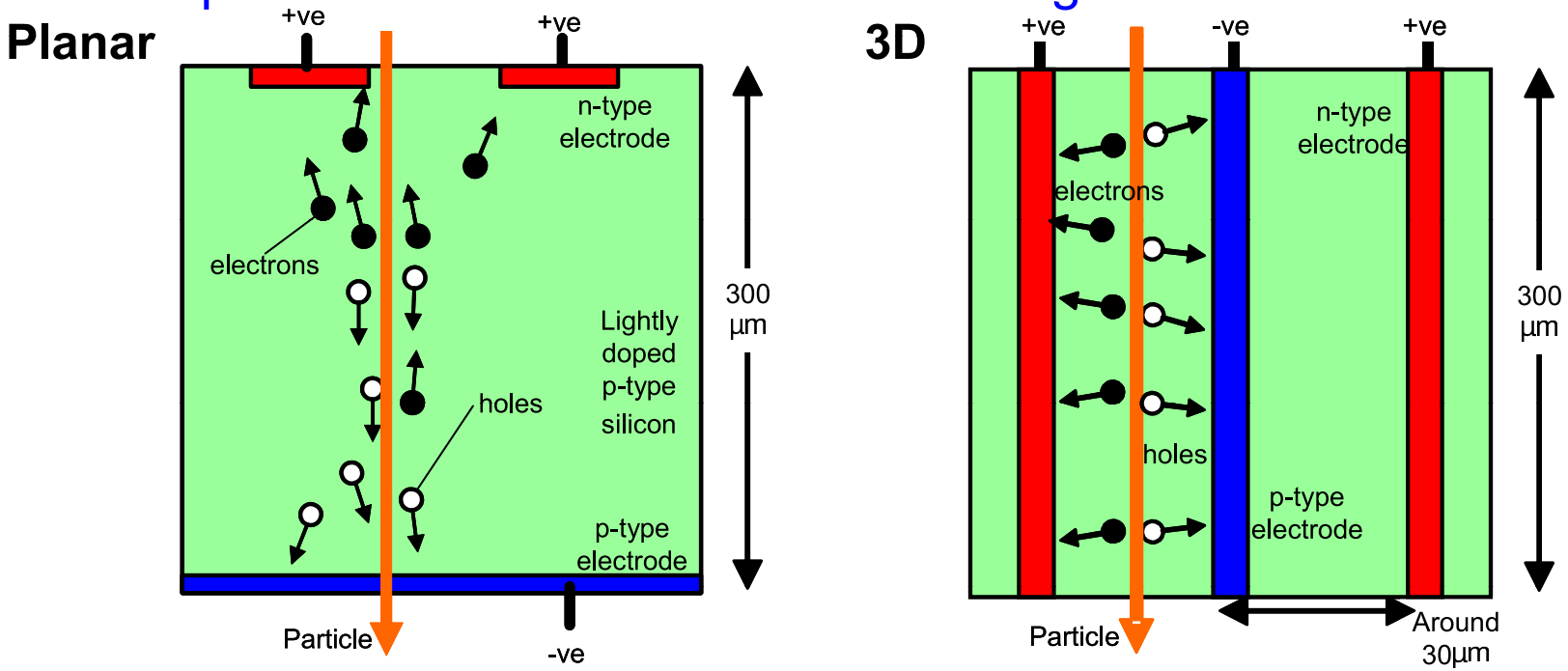
⇒ Alternatives to hybrid pixels :

- *Particularly in fashion : 3D sensors*
- *Others : 3D integrated devices (see talk of Ch. de la Taille), ...*

3D Detector Structure

- Array of electrode columns passing through substrate
- Electrode spacing << wafer thickness (e.g. 30μm:300μm)
- Benefits
  - $V_{depletion} \propto$ (Electrode spacing)^2
  - Collection time $\propto$ Electrode spacing
  - Reduced charge sharing
- More complicated fabrication - micromachining



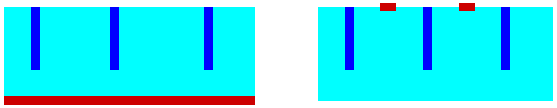


Concept, Types

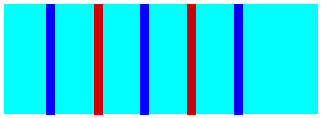
- Invented in 1997 - S. Parker, C. Kenney, J. Segal *Nucl. Instr. Meth. A*, vol. 395, 328, 1997
  - First produced in 1999 - Stanford Nanofabrication facility
- Recent development: R&D towards experimental use
  - Improvements in micromachining make larger-scale, reliable production more feasible
  - Simplified structure: Double Sided, G. Pellegrini et al.

    IEEE Trans. Nucl. Sci, vol. 54, no. 4, Aug. 2007
    Nucl. Instr. Meth. A, vol. 592 (1), July 2008
  - Application: radiation-hard detectors for Super-LHC, Synchrotrons

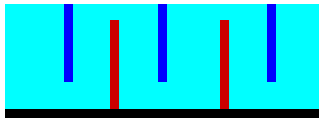
Single Sided Single Type Columns (semi-3D)



Single Sided Double Type Columns (classic 3D)

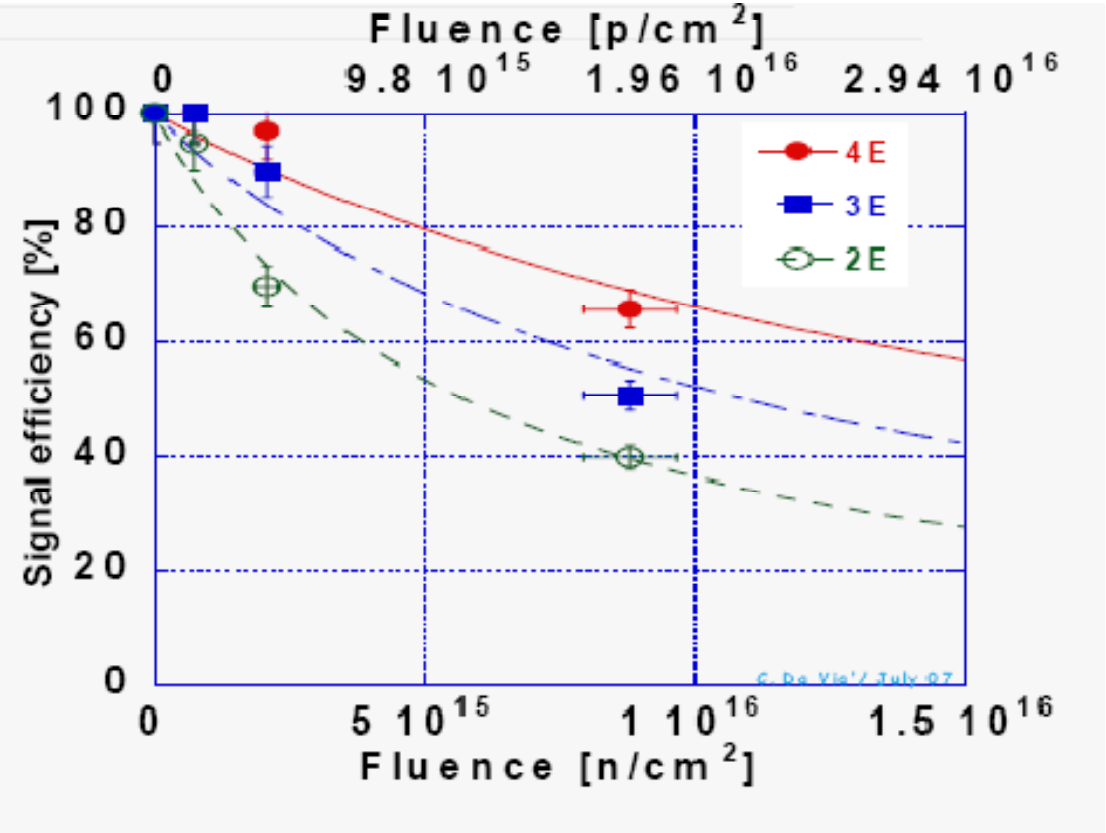


Double Sided Double Type Columns (new 3D)



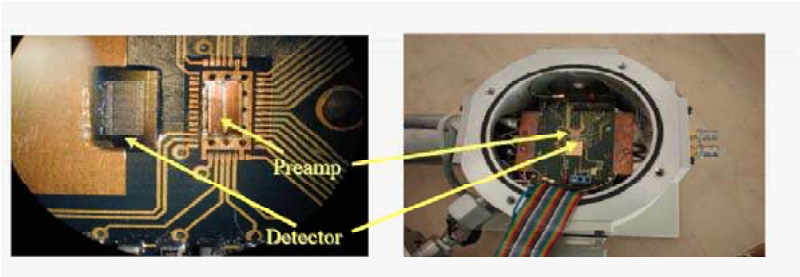
Hawaii/Stanford/Manchester cont..

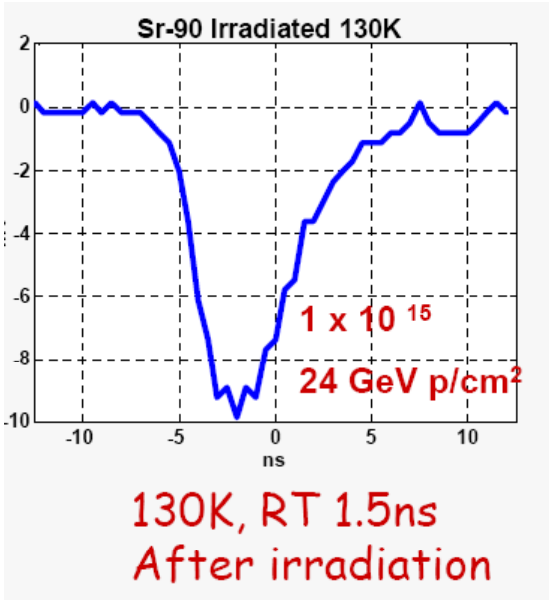
Stanford fabricated devices



- Most advanced radiation results
- Results for different pixel configurations

- Fast timing applications
- FP220 in ATLAS trigger

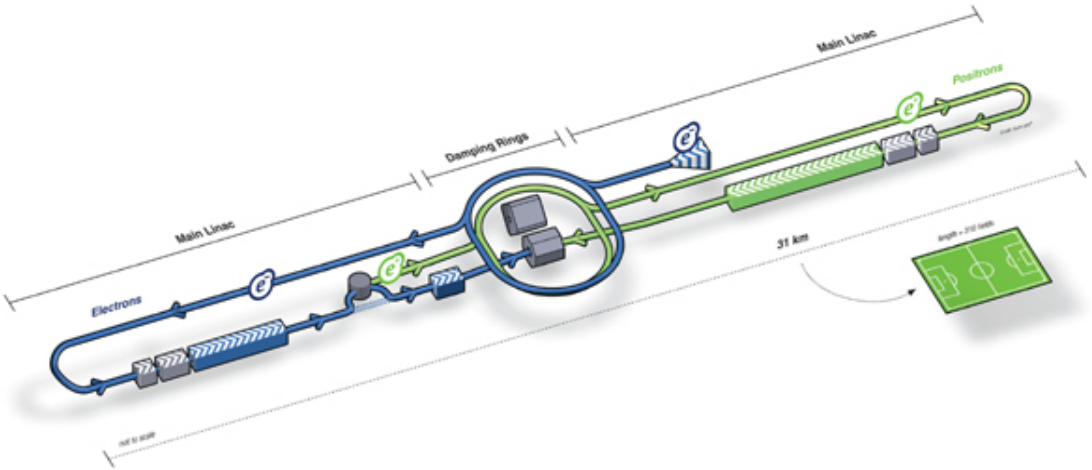


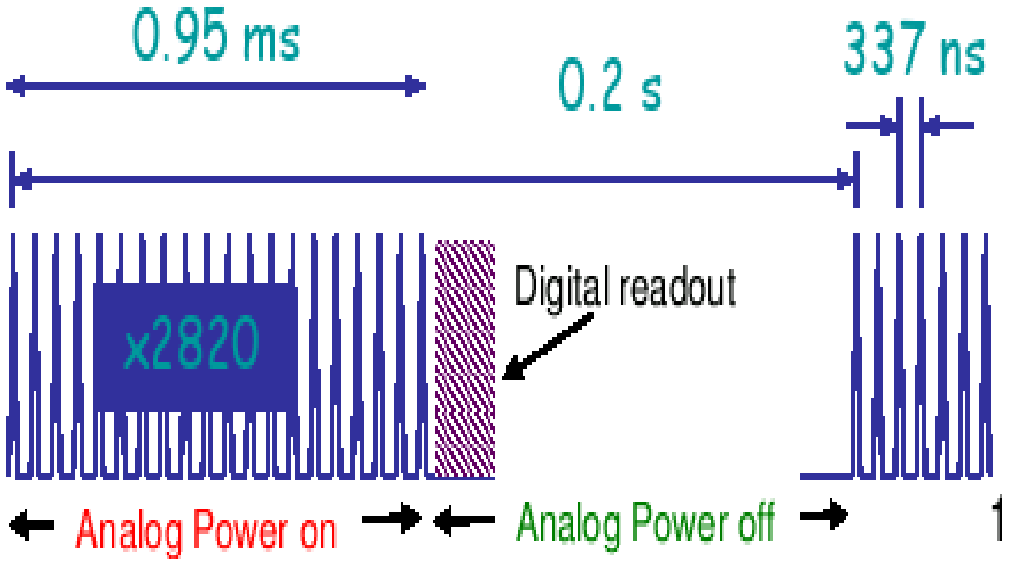


Pixel Technologies Driven by Physics Performance

- *e^+e^- collisions : ILC $\rightarrowtail$ CLIC , SuperB Factory*
- *HI collisions : RHIC, FAIR*

- **ILC ≡ next large scale accelerator after LHC :** e^+e^- *linear collider with c.m. energy up to 1 TeV*
  - ▷ *Physics programme expected/hoped to start* $\gtrsim$ *2020*
  - ▷ *Emphasis on spatial resolution and material budget rather than on speed and radiation tolerance*
    ($\gtrsim$ *2 orders of magnitude below LHC)*
  - ▷ *ILC time structure includes 5,* $\sim$ *1 ms long, "trains" made of* $\sim$ *3000 bunch crossings / second*
    $\longmapsto$ *only a few contain relevant Physics info. but all contain large amounts of Background* $\longmapsto$ *remove them !*





Typical Requirements for an ILC Vertex Detector

Material budget is a major concern ▷ mandatory to ensure necessary impact resolution at low transverse momentum ($\lesssim$ 1 GeV/c) $\longmapsto$ jet flavors and electrical charge

$\Rrightarrow$ **hybdrid pixel sensors used at LHC excluded**

- *very thin sensors : thickness $\longmapsto$ 50 μm Si*
- *very light mechanical supports : $<$ 0.1 % X_0*
- *very low material servicing (low power sensors $\longmapsto$ modest cooling)*

▷▷▷ **Goal :** *$\sim$ 0.1 % X_0 for complete ladder*

Excellent spatial resolution :

- *single point resolution $\sim$ 2–3 μm*
- *double hit separation $\lesssim$ 40 μm*
- *inner radius $\sim$ 12-15 mm !*
- *total active surface $<$ 1 m^2*

Accelerator	a (μm)	b ($\mu m \cdot GeV$)
LEP	25	70
SLD	8	33
LHC	12	70
RHIC-II	13	19
ILC	< 5	< 10

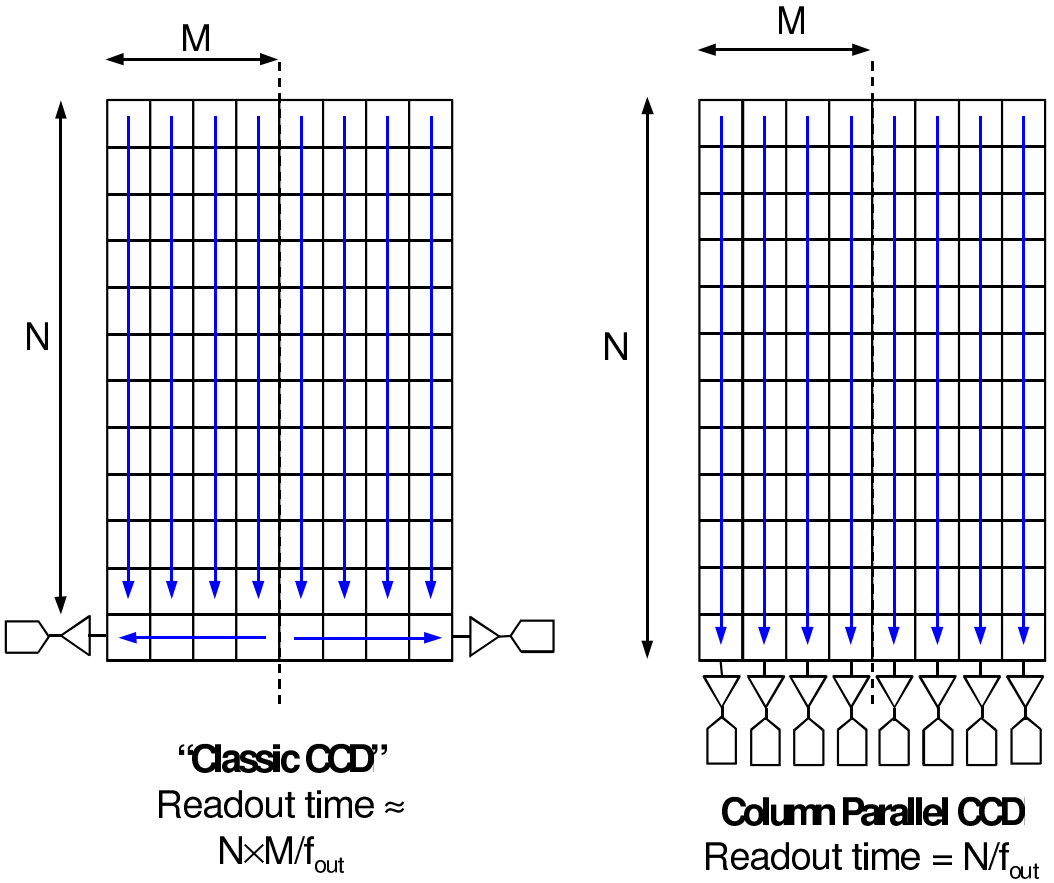
▷▷▷ **Constraints mainly driven by σ_{ip} = a $\oplus$ b/p·sin$^{3/2}\theta$**

Several alternative pixel technologies & read-out architectures under devt

- *sensing technologies : CCDs, CMOS sensors, DEPFETs, (SoI)*
- *continuous versus delayed read-out (inbetween bunch trains)*

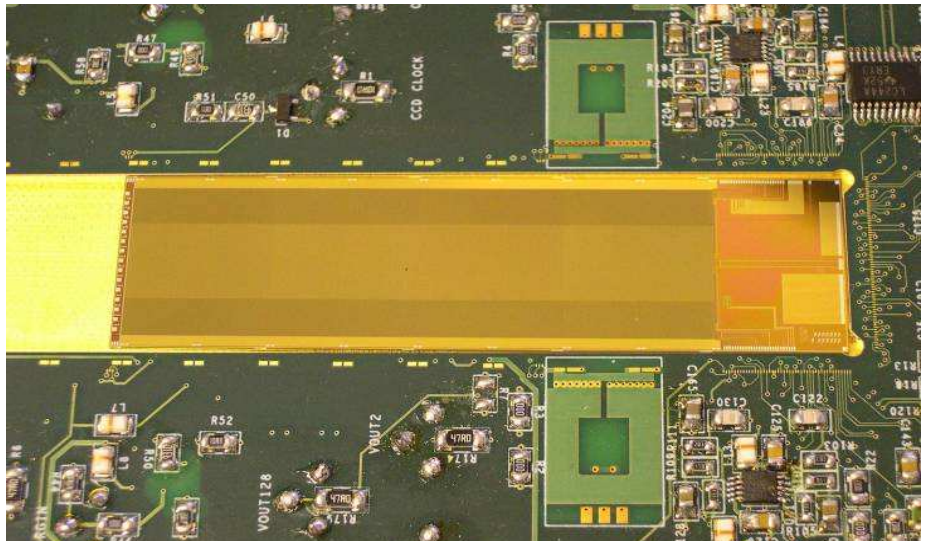
CPCCD

- LCFI proposes: a two phase column parallel CCD sensor
- Simple idea: readout a vector instead of a matrix
- Readout time shortened by orders of magnitude



"Classic CCD"
Readout time ≈ $N \times M / f_{out}$

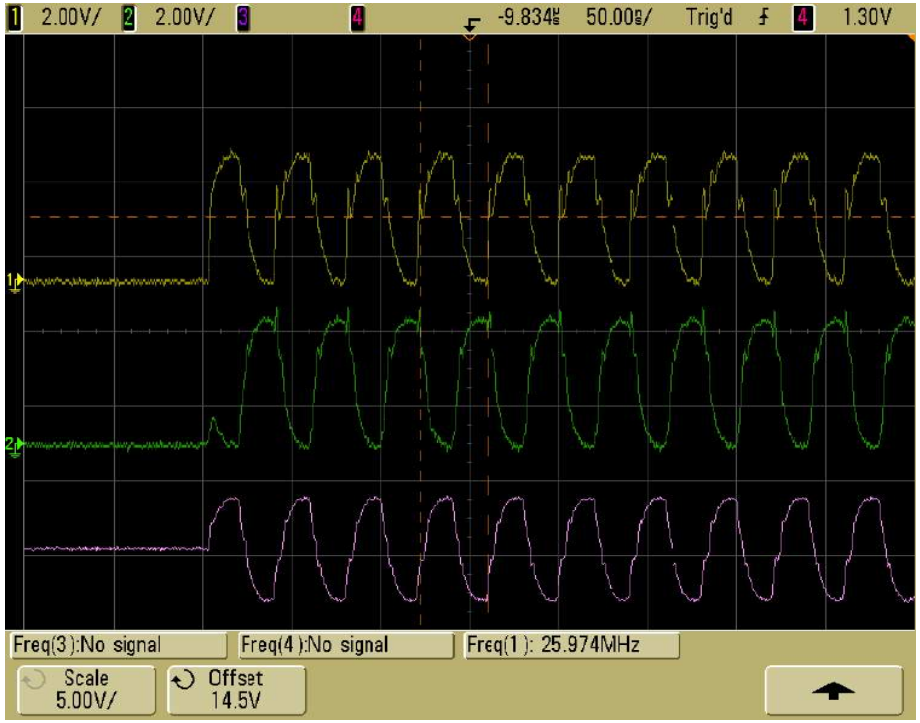
Column Parallel CCD
Readout time = N / f_{out}



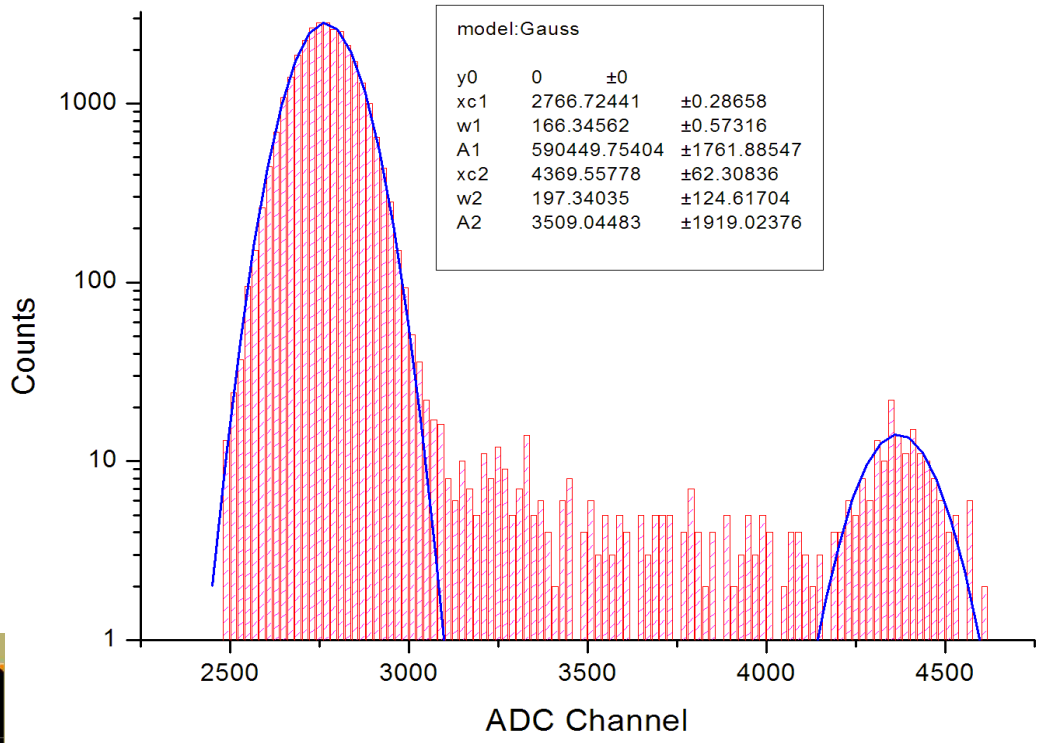
- **Readout still challenging - 50MHz clock for 50mm sensor**
- **Fast clocking implies heating and power dissipation**

Proof of Principle

- Detected Fe^{55} 5.9keV X-rays
- Noise analysis: 180e^-(34°C), 65e^-(-40°C)
- Working on noise reduction



R. Gao, A. Nomerotski

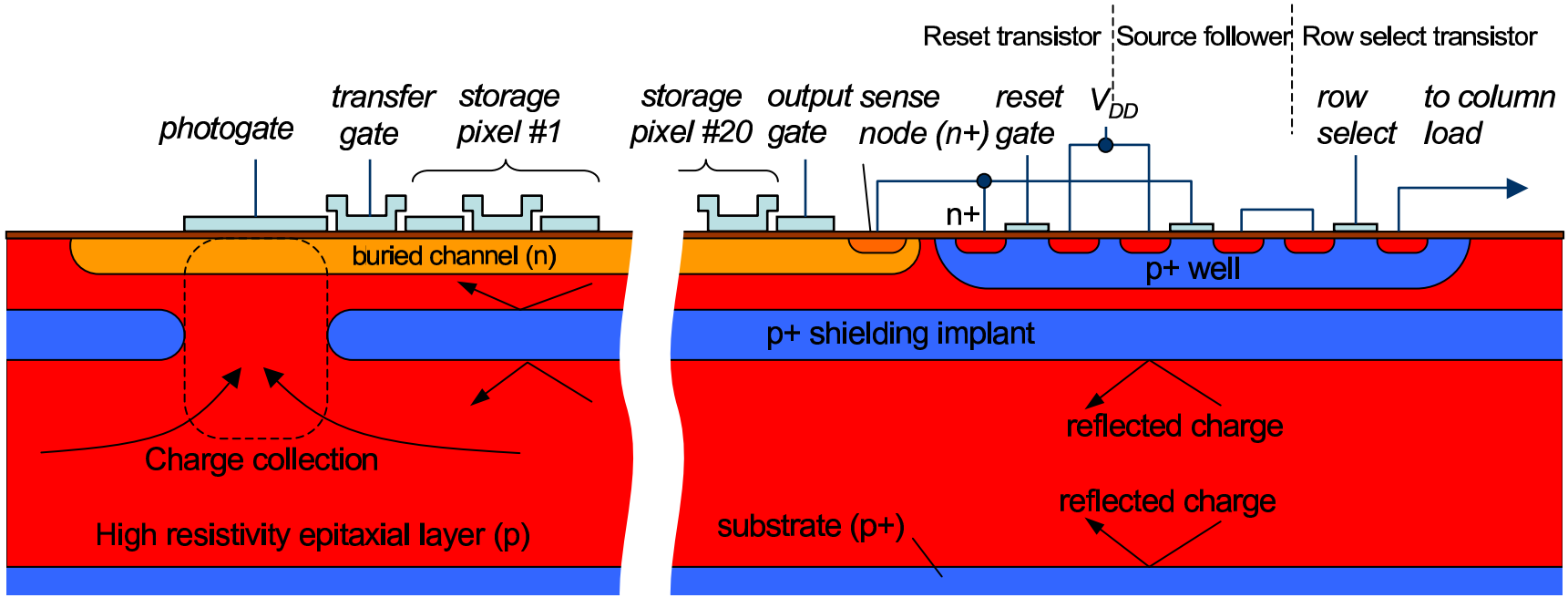


Y. Banda, E. Devetak B.Jeffery, A. Nomerotski

- Studying various possibilities for driving CPCCD:
  - IC Drive
  - Transformer
- Current driver chip - 25MHz

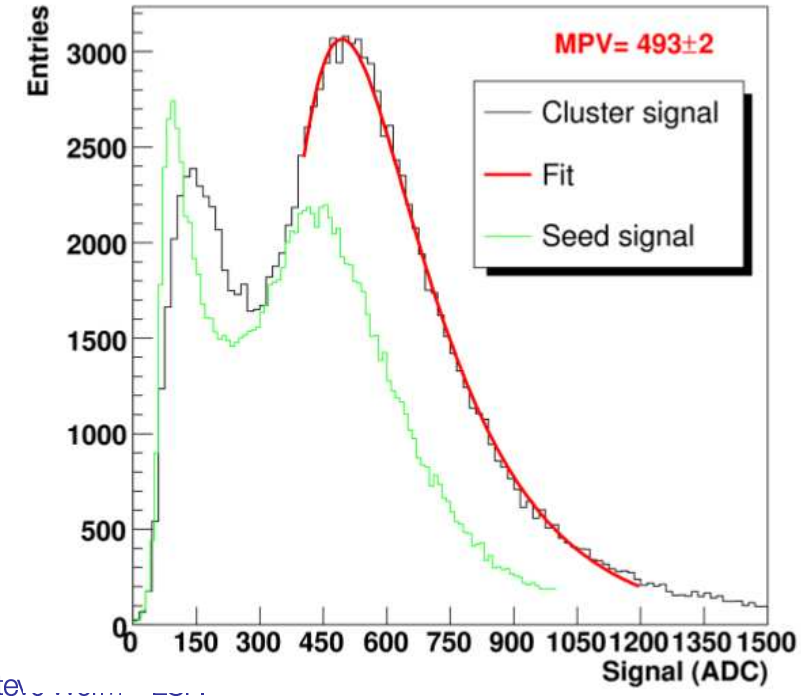
In-Situ Storage Image Sensor

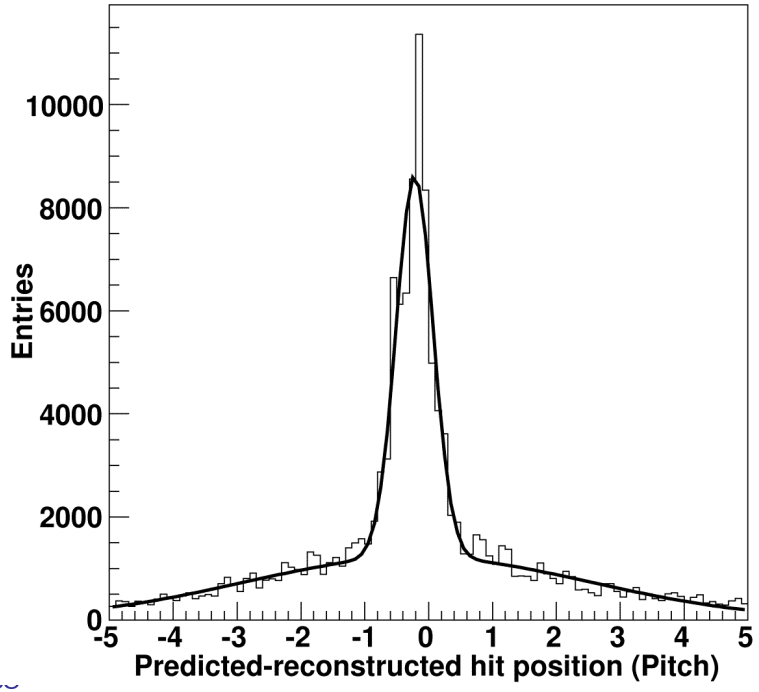
- ISIS Sensor details:
  - CCD-like charge storage cells in MAPS pixel, CMOS or CCD technology
  - p+ shielding implant (or epi) forms reflective barrier
  - Designed for “burst” imaging (*see* Prof. Etoh http://hydraulics.web.infoseek.co.jp)
- Operational Details
  - Charge collected at photogate
  - During active period charge is periodically shifted into short CCD register
  - During readout period charge is moved to output gate and ADC



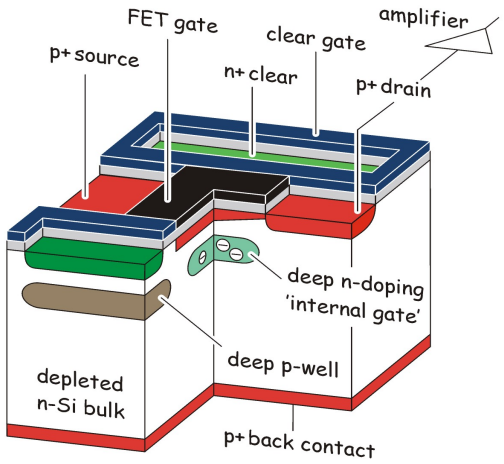
ISIS1 Test Beam: Resolution and Cluster

- Cluster Charge
  - Hits clear: most probable = 3.9 ke-
  - Peak structure caused by: noise, charge spreading over many pixels, charge lost to output structures
- Tracking Resolution
  - Using sensors 0,1,3; calculate distance to hit in sensor 2
  - Subtract effect of multiple scattering
  - Corrected resolution in “y” (short pixel direction) = 9.4±0.2 μm.
  - Negligible charge sharing in “x”



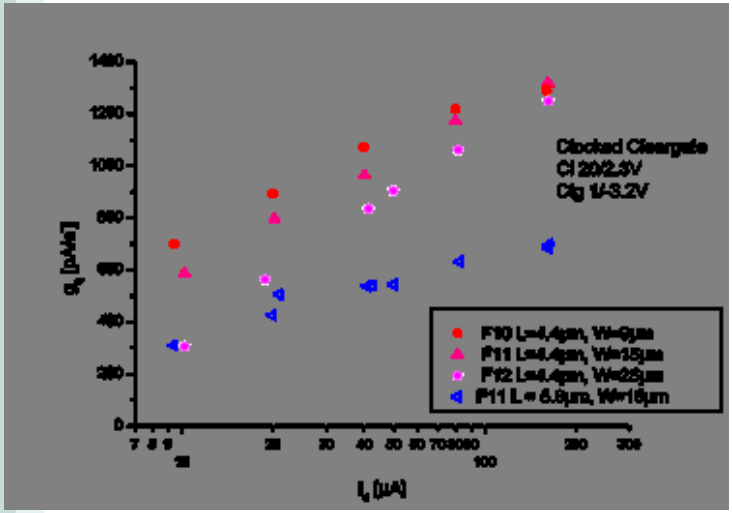


DEPFET Pixel Cell



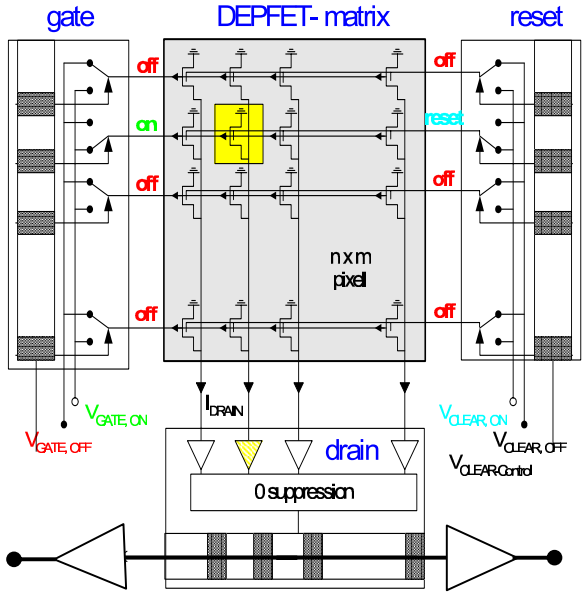
Depleted P-channel FET

- fully depleted sensitive volume
  - fast signal rise time (~ns), small cluster szie
- internal amplification
  - large signal, even for thin devices
  - charge-to-current conversion:
    $g_q = dI_d/dq$ = 0.5 - 1 nA/electron (latest production)
    scales with gate length
- Charge collection in "off" state, read out on demand
  - potentially low power device



- special technology, currently only available at the MPI Semiconductor Laboratory (MPI HLL)
- future developments:
  - improve technology for large wafer scale (Φ=150mm) sensors
  - main applications:
    - X-ray Astronomy (BepiColumbo, SimbolX, IXO)
    - Vertex Detetor at SuperBelle
    - candidate for the VXD at ILC and for the XFEL ....

DEPFET Array - different ways for read-out



1. Row wise read-out ("rolling shutter") → ILC VXD and SuperBelle

- select row with external gate, read current, clear DEPFET, read current again → the difference is the signal (row wise CDS)

Advantage

- Low power consumption → low material!
- No advanced interconnection technologies needed

Disadvantage

- two different types of auxiliary ASICs needed
- for high frame rates very little time per row

Design goal at SuperBelle: 10MHz frame rate → 80ns row rate

2. Hybrid-pixel-like approach: one amp. and ADC per pixel

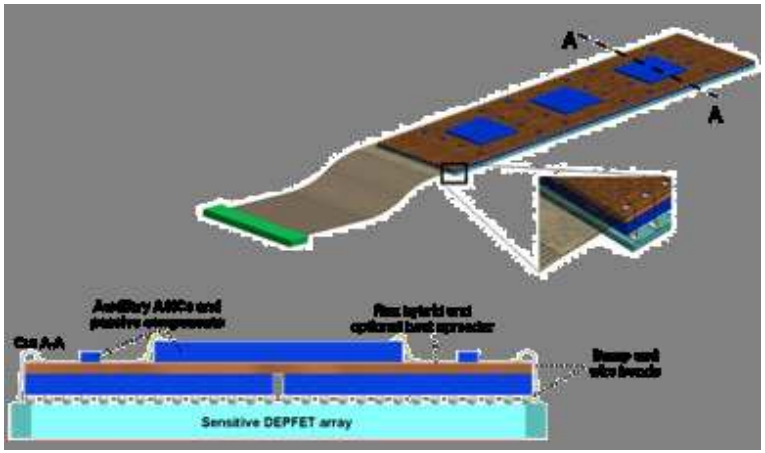
Advantage

- parallel processing of the pixels → higher frame rates with low noise

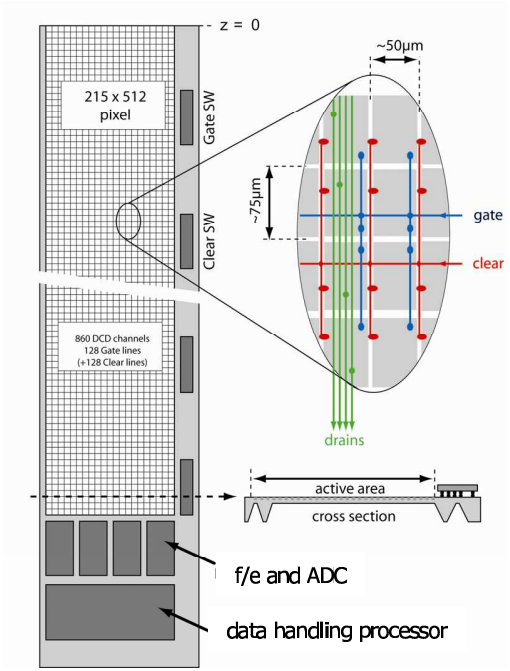
Disadvantage

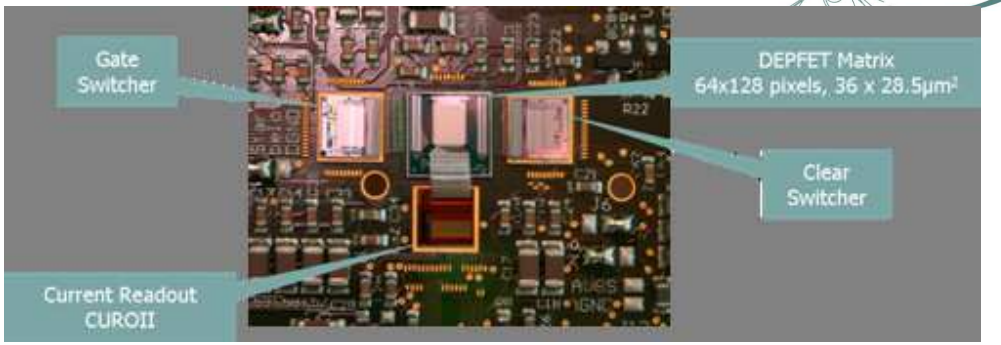
- more challenging interconnection
- higher power consumption

Foreseen the focal plane at the **XFEL**



- SuperBelle Concept (very similar to ILC VXD!!)





Prototype system achievements:

- thick (!) DEPFETs (450µm), CURO and Switcher
- test beam @ CERN:
  - S/N≈140 @ 450 µm ←→ goal S/N ≈ 20-40 @ 50 µm
  - sample-clear-sample 320 ns ←→ goal 80 ns
  - s.p. res. ≈ 1 µm @ 450 µm ←→ goal ≈ 10 µm @ 50 µm
- radiation tolerance up to 8 Mrad and ~10^{12} n_{eq}/cm^2 tested with single pixel structures and mini matrices
- New DCD r/o chip with integrated ADC tested and functional

Next steps - very(!) briefly:

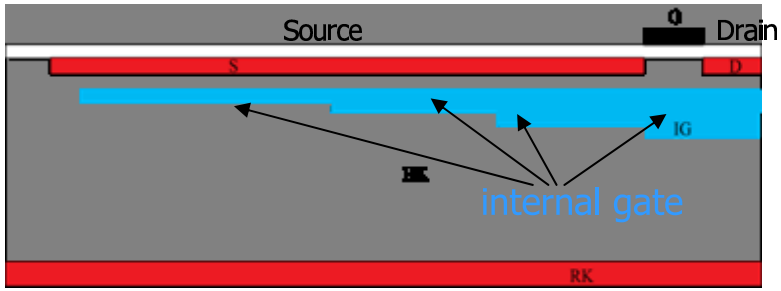
- Production of thin wafer scale DEPFET arrays in 2009
- Final SuperBelle Sensors 1.15x7.25 cm^2 (L1) in 2011
- 0.14% X_0 (incl. frame, chips, bumps)

XFEL: DEPFETs with Signal Compression

mpi halbleiterlabor

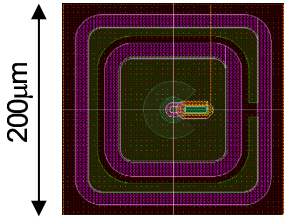
Challenges at XFEL

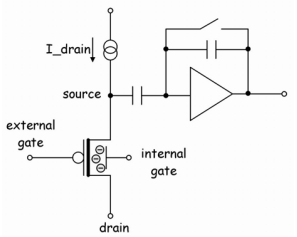
-: high dynamic range up to 10^3 photon/pix/bunch (10keV)
-: fast read out (5MHz frame rate)
-: .... and many more!



DEPFETs for the XFEL

-: 200 x 200 µm², 1024x1024 pixel in the focal plane
-: Bump bonded f/e, 5Mhz frame rate
-: read out noise <50 e^- rms
-: single photon resolution
-: quantum efficiency >0.8 from 0.3 to 12 keV photons



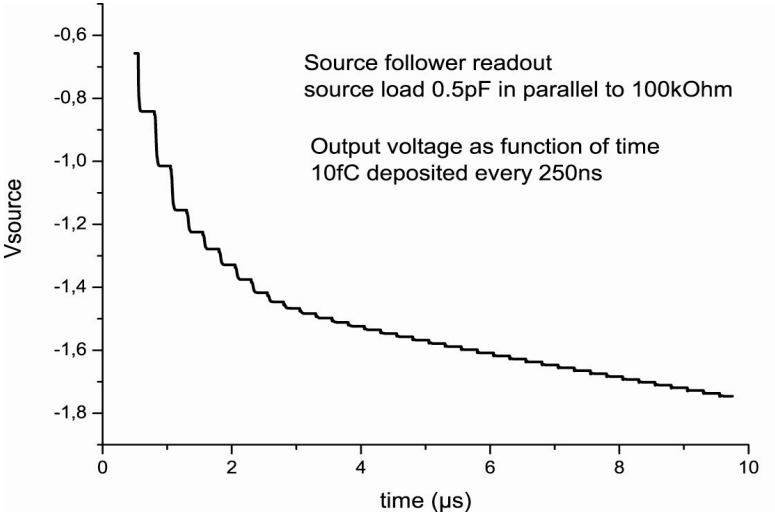


Signal compression by shaping of the internal gate:

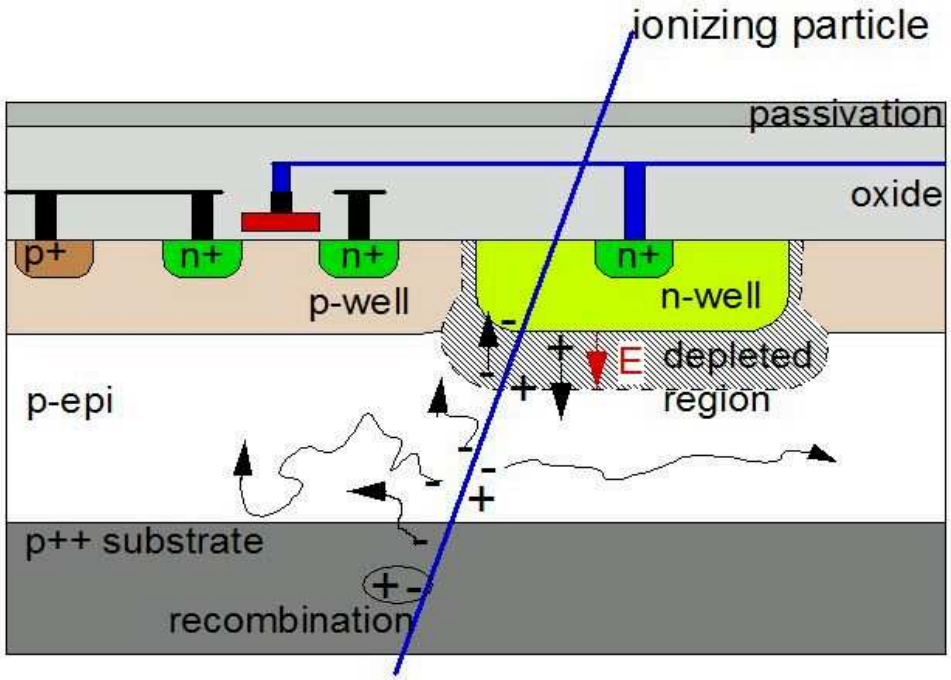
-: The internal gate extends into the region below the source

-: Small signals assemble below the channel, being fully effective in steering the transistor current

-: Large signals spill over into the region below the source. They are less effective in steering the transistor current.



CMOS Sensors: Main Features



p-type low-resistivity Si hosting n-type "charge collectors"

- *signal created in epitaxial layer (low doping):*

  $Q \sim 80$ *e-h /* $\mu m \mapsto$ *signal* $\lesssim 1000\ e^-$
- *charge sensing through n-well/p-epi junction*
- *excess carriers propagate (thermally) to diode*

  with help of reflection on boundaries

  with p-well and substrate (high doping)

Specific advantages of CMOS sensors:

◇ *Signal processing* μ*circuits integrated on sensor substrate (system-on-chip)* $\mapsto$ *compact, flexible*

◇ *Sensitive volume (*$\sim$ *epitaxial layer) is* $\sim$ *10–15* μm *thick* $\longrightarrow$ *thinning to* $\sim$ *30–40* μm *permitted*

◇ *Standard, massive production, fabrication technology* $\longrightarrow$ *cheap, fast turn-over*

◇ *Room temperature operation*

◇ Attractive balance between granularity, mat. budget, rad. tolerance, r.o. speed and power dissipation

⋈ *Very thin sensitive volume* $\rightarrowtail$ *impact on signal magnitude (mV !)*

⋈ *Sensitive volume almost undepleted* $\rightarrowtail$ *impact on radiation tolerance & speed*

⋈ *Commercial fabrication (parameters)* $\rightarrowtail$ *impact on sensing performances & radiation tolerance*

CMOS Sensors with Analog Output

- **Numerous MIMOSA chips tested on H.E. beams (SPS, DESY)**

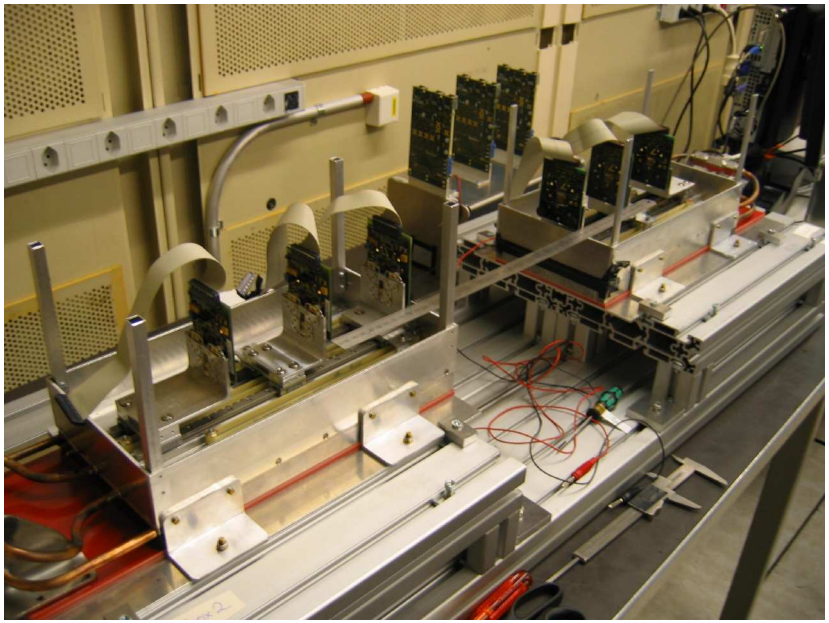
  ⇛ **validated for several short & mid-term applications :**

  - *$N \sim 10\ e^- \mapsto$ S/N $\gtrsim$ 20–30 (MPV)*

    ⇛ *$\epsilon_{det} \sim$ 99.5–99.9 % for fake rate $\lesssim 10^{-5}$*
  - *$T_{oper.} \gtrsim 40\ ^\circ C$*
  - *Spatial resolution exploits charge sharing between pixels:*

    $\sigma_{\mathbf{sp}} \sim$ 1 – 1.5 – 2 – 3 μm for 10 – 20 – 30 – 40 μm pitch
  - *Ionising radiation tolerance: $\gtrsim$ 1 MRad (10 keV X-Ray)*
  - *Non-Ionising radiation tolerance: $\sim O(10^{13})\ n_{eq}/cm^2$*
  - *Technology without epitaxy also performing well :*

    very high S/N but large clusters (hit separation $\searrow$)



  - *Macroscopic sensors used for particle tracking/vertexing (thinned to 50 μm)*

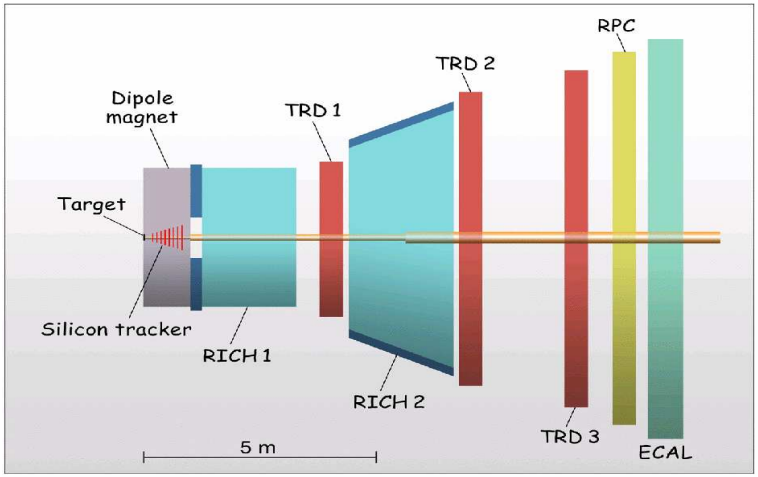
- **Sensors adapted to applications with $\lesssim 10^3$ frames/s :**

  ⇛ **several beam telescopes – ex: EUDET (EU-FP6) beam telescope**

- **column // sensor (70,000 pixels, 18 μm pitch) operationnal at 10 kfps**
  - *128 column of 576 pixels read-out in // with in-pixel Correl. Dble Sampling*
  - *each column terminated by discriminator*
  - *operated at CERN-SPS : N ∼10–13 e^- ENC $\longmapsto$ $\epsilon_{det} \gtrsim$ 99.8 %*
  - *Nov. '08 : reticle size (1152 columns) with integrated zero supp.*

- **STAR vertex detector at RHIC : 2 consecutive versions**
  - *2008/09 : 30 μm pitch with discriminated outputs ($\sigma_{sp} \sim 6\ \mu m$) and 640 μs r.o. time*
  - *2009/10 : 18 μm pitch with integrated zero suppression ($\sigma_{sp} < 4\ \mu m$) and $<$ 200 μs r.o. time*
  - ※ *$T_{op} \gtrsim 30^\circ C$ — $P_{diss} \sim 100$ mW/cm^2*

- **CBM vertex detector at FAIR: 2 steps**
  - *2011/12 (?) : $\lesssim$ 20 μm pitch with integrated zero suppression and $<$ 20 μs read-out time*
  - *$\gtrsim$ 201X ? : faster and more radiation tolerant sensors, likely based on 3D (=vertical) integration technologies*
  - ※ *Operation in vacuum*

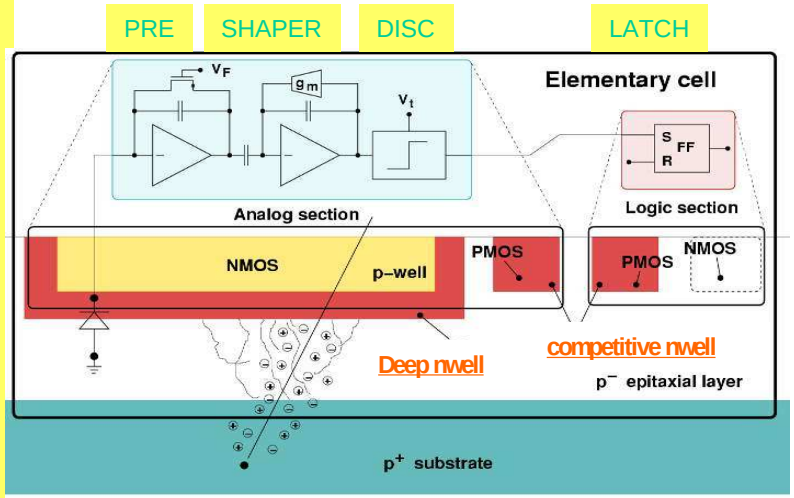


Deep NWell 130nm CMOS MAPS

- Rad-hard MAPS with data sparsification and high rate capability (self-triggering pixel design, in-pixel comparator, in-pixel time stamping and sparsification logic)
  - Deep N-Well (DNW) as collecting electrode
  - Classical pixel analog processing with charge-sensitive preamplifier

    Gain independent of the sensor capacitance collecting electrode can be extended and include NMOS of the analog section
  - Area of the "competitive" nwells housing PMOSFETs inside the pixel kept to a minimum. Fill factor = DNW/total n-well area ~90% in the prototype test structures
- **Pros:** With 100-nm scale CMOS, integration of advanced analog and digital functions at the pixel level (as in hybrid pixels), rad-hard electronics
- **Cons:** possible limitations in pixel pitch (go to more scaled CMOS, but higher cost, only binary readout) and detection efficiency (pixel layout critical, deep P-well option?)

SLIM5, ILC – INFN & Italian Universities

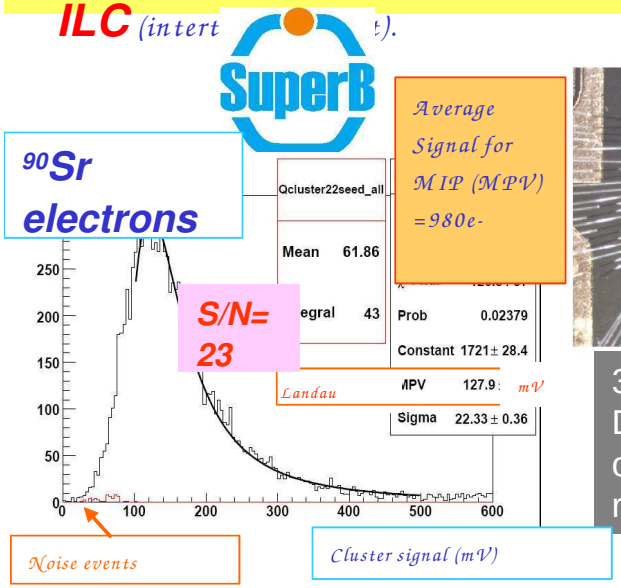


- 2004-2006: Proof of principle achieved with the first prototypes in a 130 nm triple well CMOS process
- 2007-2009: Full size MAPS sensors and detector modules, beam tests

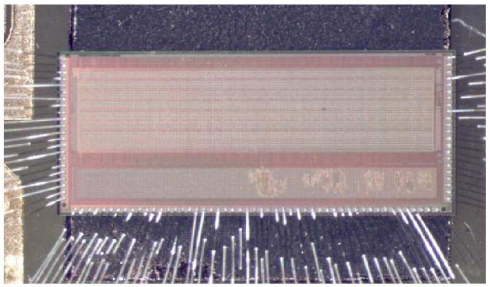
Experimental results and plans

- Performed successful tests of a **first generation of Deep N-Well CMOS MAPS with in-pixel sparsification and time stamping**.

- **Sensors with different sparsified readout architectures and pixel pitches** are being optimized for operation at a **Super B–Factory** (large background, equivalent to a continuous beam operation) and at **ILC** (intert[illegible]).



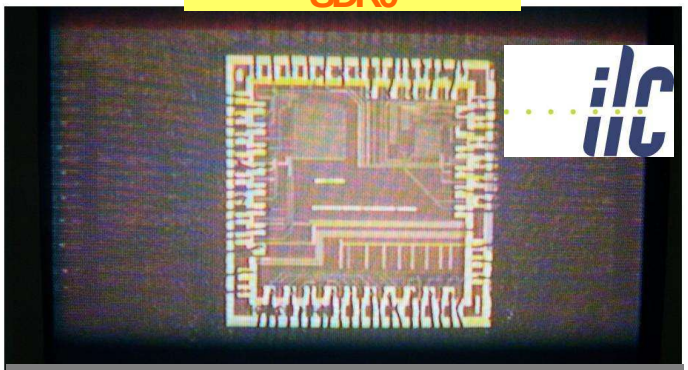
APSEL4D



32x128 matrix.
Data Driven, continuously operating sparsified readout

50x50 um pitch

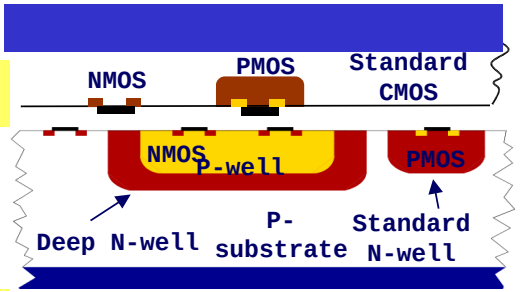
SDR0



16x16 matrix, Intertrain sparsified readout

25x25 um pitch

- **DNW MAPS are evolving towards vertical integration**. A design with a 2 tier structure (sensor& analog tier + digital tier) is pursued to improve performance (smaller pitch, higher efficiency, increased pixel functionalities)



Vertex2008, S…, Sweden (… 08) 2

SOI

. Activity started as
one of KEK detector R&D proje… 5

. Sensor size is limited by reticle s… 21 x 21 mm²)
20μm x 20μm : 128 x 128
gap in the acceptance

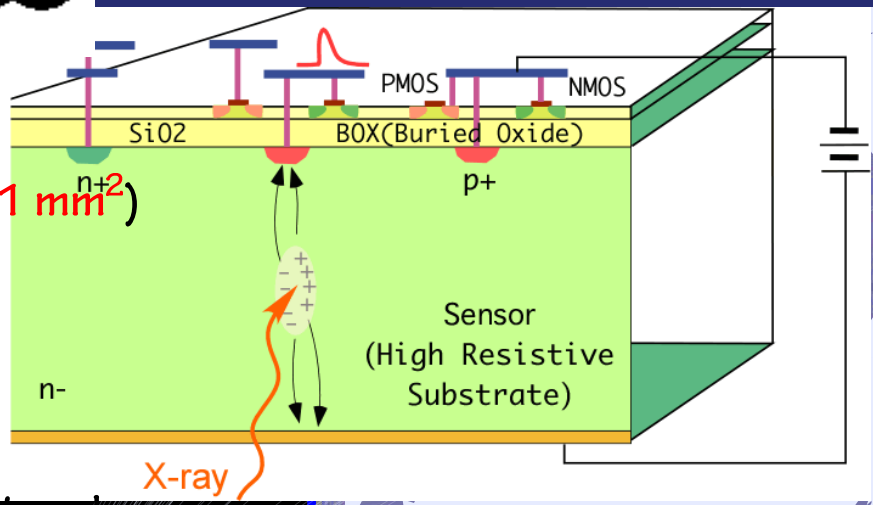
rad-hard (deep 0.2 μm technology)
tested > 30 MRad
…sh of 50-100μm has bee…
…silicon process

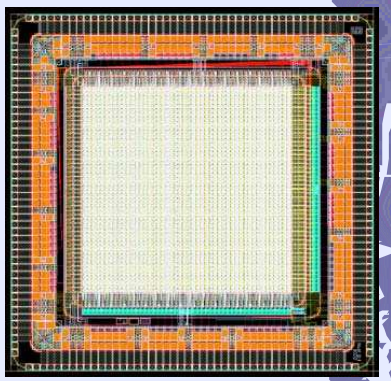
<= 50 μm

. Sig… proces…ed by the …OS circuit
Complex rad-hard circuit can be made
DEPFET/CAP type readoout is also possible

10kHz trigger rate ???

. R&D in progress
Evaluation of Belle PIXEL chip will start soon
(pixel-shaper-discrimi… …al pipeline)

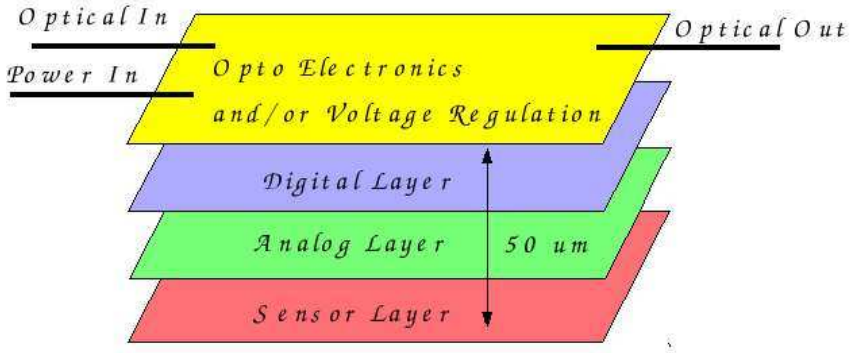




Vertical Integration – 3D

- A 3D device is a chip comprised of 2 or more layers of semiconductor devices which have been thinned, bonded, and interconnected to form a monolithic circuit

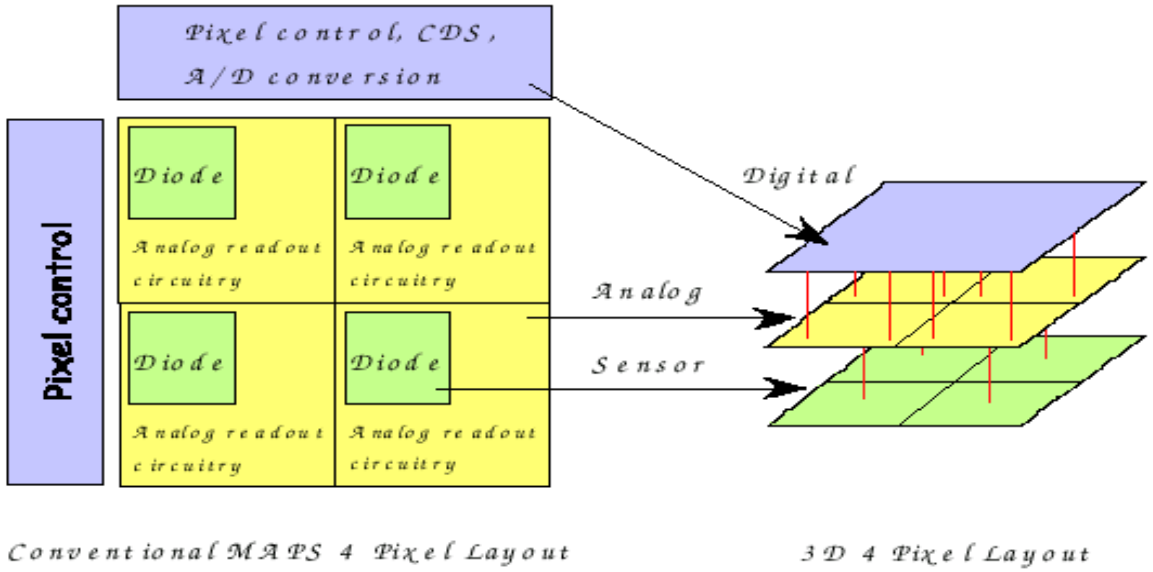
- Advantages of 3D
  - Increased circuit density due to multiple tiers of electronics
  - Fully active sensor area
  - Independent control of substrate materials for each of the tiers
    - Process optimization for each layer
  - Ability to mate various technologies in a monolithic assembly

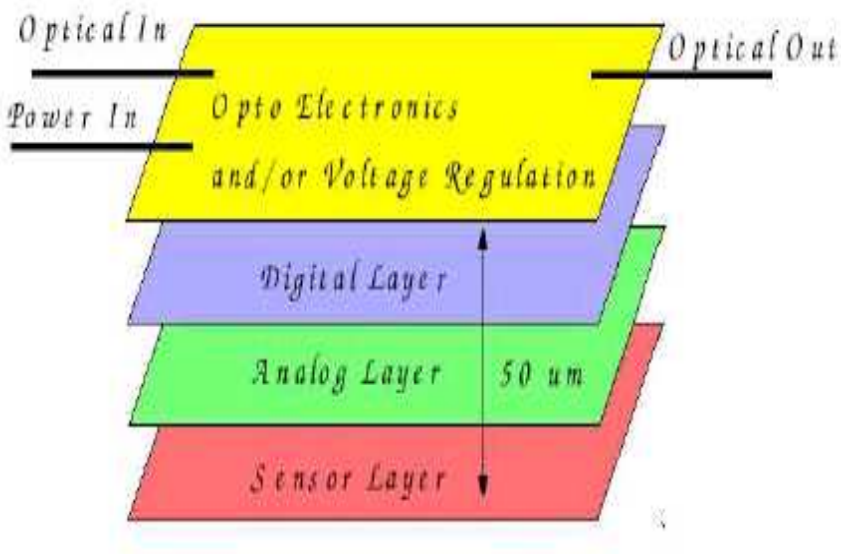


- Technology driven by industry
  - Reduce R, L, C for higher speed
  - Reduce chip I/O pads
  - Provide increased functionality
  - Reduce interconnect power, crosstalk

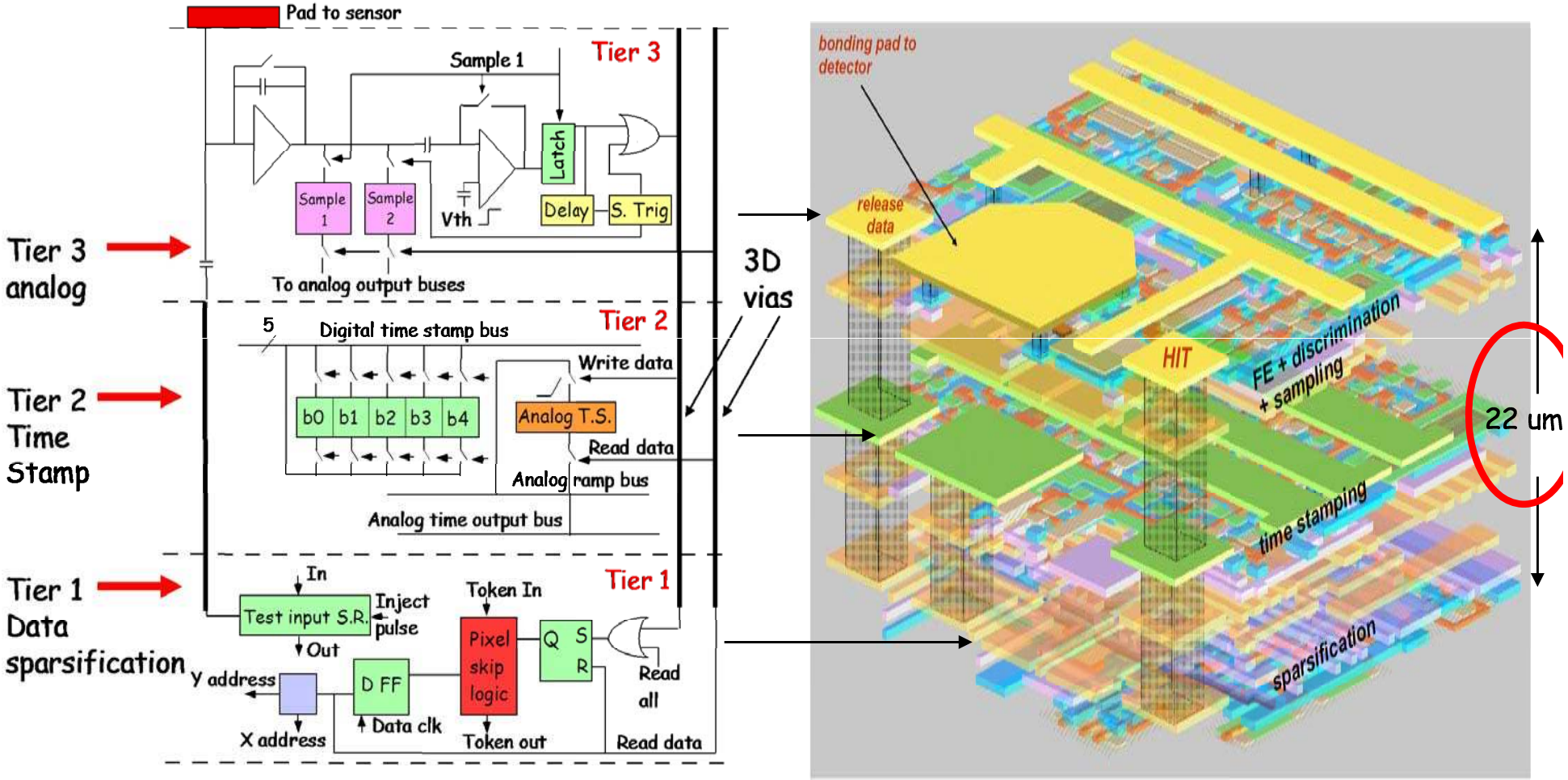
- Critical issue are:
  - Layer thinning to < 10 μm
  - Precision alignment (< 1 μm)
  - Bonding of the layers
  - Through-wafer via formation

- **3DIT are expected to be particularly beneficial for CMOS sensors :**
  - *combine different fab. processes*
  - *alleviate constraints on transistor type inside pixel*
- **Split signal collection and processing functionnalities :**
  - *Tier-1: charge collection system*
  - *Tier-2: analog signal processing*
  - *Tier-3: mixed and digital signal processing*
  - *Tier-4: data formatting (electro-optical conversion ?)*
- **Use best suited technology for each Tier :**
  - *Tier-1: epitaxy, deep N-well ?*
  - *Tier-2: analog, low leakage current, process (nb of metal layers)*
  - *Tier-3 & -4 : digital process (nb of metal layers), feature size ⟶ fast laser (VOCSEL) driver, etc.*





Three Tier Arrangement for VIP1 Pixel



ILC Projects in Tezzaron MPW

Convert MIT LL VIP2a design to the Tezzaron/Chartered process (VIP2b) - Fermilab

- CMOS design should be easier.
- Going from 3 layers in 0.18 um technology to 2 layers in 0.13 um technology could reduce pixel size below 20 um.
- Using the "via first" process at Chartered eliminates the wasted area needed for vias in the "via last" MIT LL process.
- Fabrication in the Chartered fully characterized process and models, along with standard cell libraries should lend itself to high yield.
- Because VIP2b is in a CMOS deep sub micron process, the design should be inherently more radiation hard.
  - Radiation tolerance of Chartered 0.13 um process is currently being studied by another group.

Convert 2D MAPS device design for ILC to 3D design where PMOS devices are placed on the tier without sensing diodes – Italy

CMOS pixels with one tier used as a sensitive volume and the second containing electronics. - France

SLHC Projects in Tezzaron MPW Run

Convert the current 0.25 um ATLAS pixel electronics to a 3D structure with separate analog and digital tiers in the Chartered 0.13 um process. – France [15]

Develop a 3D chip with 2 tiers of electronics to explore the advantages of 3D for the Super CMS pixel detector. - Fermilab

- Going from 1 layer of circuitry in a 0.25um process to 2 layers in a 0.13 um process can increase circuit density by a factor of 7.
- Circuit density can by traded for smaller pixel size.
- Features to consider for parallel processing
  - In pixel digitization
  - Large digital storage
  - Triggering capability
  - Sparsification
  - Reduction of peripheral circuitry

SUMMARY

SUMMARY

- **Numerous types of sensors & architectures currently developed for future vertex detectors**

  (several not mentioned in this talk)

  ↪ *R&D driving forces : ILC & SuperLHC (with benefits for HIC, SuperB factory, CLIC)*

- **CCDs and HPS were ± the only options for many years**

  ↪ *big landscape change under way*

- **Very promising emerging solution : 3D (vertical) Integration Technologies**

  ↪ *existing sensing technologies (CMOS sensors, DEPFETs, ... XR imaging ...)*

  obviously going to take big advantage of 3DIT

- **FNAL already well introduced in 3DIT (VIP-1 & -2 for ILC)**

  ⇛ *Next step : commercial run (Tezzaron-Chartered) in Spring '09*

  with Italian & French labs for ILC and SLHC

- **Coming 2 years expected to reveal numerous new results**

  ⇛ **Benefits for PS ? Common HEP-PS projects ?**