Interconnection technologies

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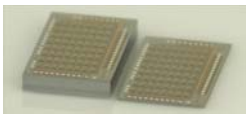
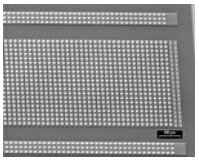
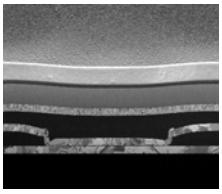
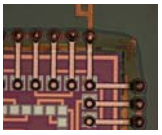
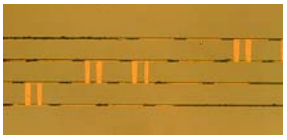
Overview:

- Technology enablers:
  - Substrate thinning
  - Assembly & bumping
  - Flex/stretch substrates
  - 3D integration & trade-offs
  - Custom analog design
- Detector systems examples
- Conclusions & outlook

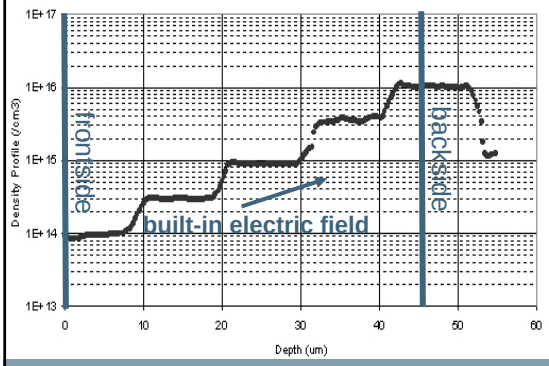



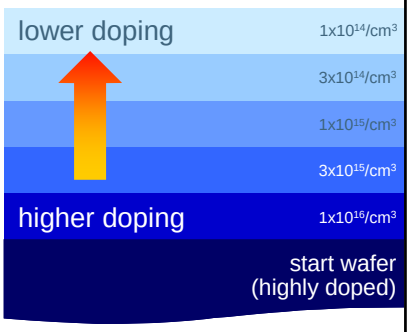





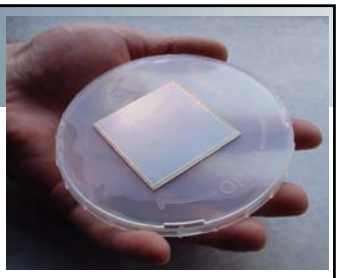
Technology enablers:
CMOS imagers performance enhancement

- growth of (up to 50 micron) thick epitaxial Si with **graded doping**
- aim: enhanced charge collection due to built-in electrical field, hence less cross-talk

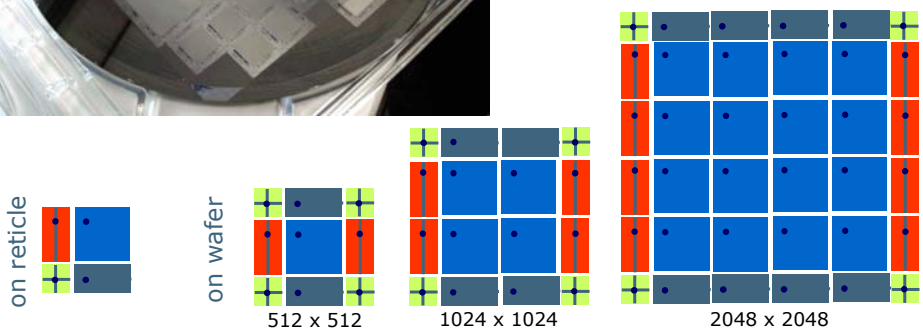




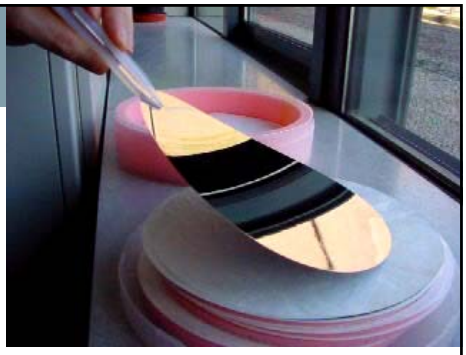
Technology enablers:
Stitching for large imagers



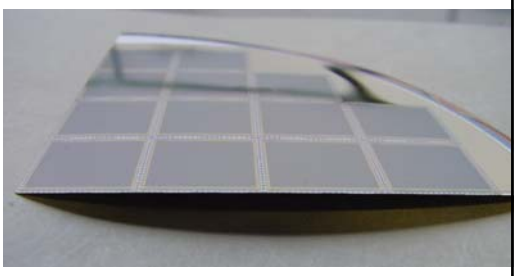
- Up to 5x5 cm² imagers realized on 200 mm Si wafers



Technology enablers:
Wafer thinning

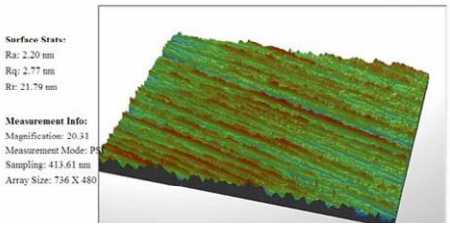


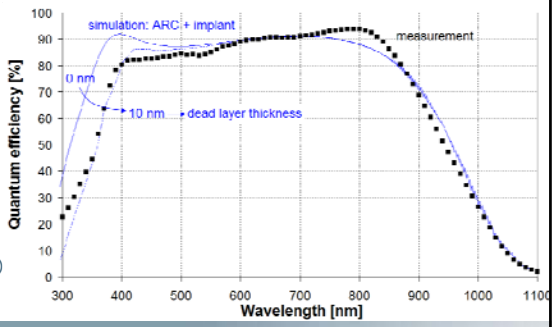
- Technology:
  - rough/fine grinding, dry/wet etch at wafer level
  - Si, glass, GaAs, …
  - critical: thinning damage, impact on devices
  - very thin wafers (< 100 um): use of carrier wafers and temporary (de-)bonding technology
- Features:
  - thinning down to 15 um
  - total thickness variation < 1 um
- Advantages/Applications:
  - thin (3D) integration
  - embedding in flexible substrates
  - backside illuminated imagers
  - ultra low X_0 -> tracking detectors



Technology enablers:
Backside illumination – backside passivation of (CMOS) imagers

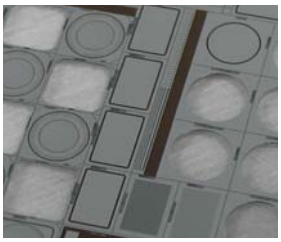
- Critical issues for backside illuminated imagers:
  - (thinning induced) damage at back side results in trapping of carriers, and therefore reduced quantum efficiency
- Solutions:
  - Ultra fine grinding :
    - Damage reduced to < 0.5 um
  - Damage removal techniques:
    - (Deep) Reactive Ion Etching
    - Wet etch (TMAH)
  - Backside surface passivation:
    - Low energy implantation
    - Laser annealing
- Results:
  - High charge collection (i.e. high QE in green/red
- However:
  - Surface passivation = thin dead layer
  - Impaires QE at wavelengths with (very) low penetration depths: e.g. (N)UV

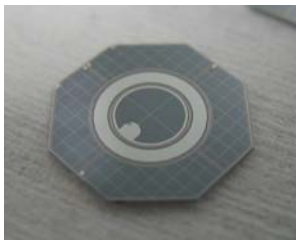


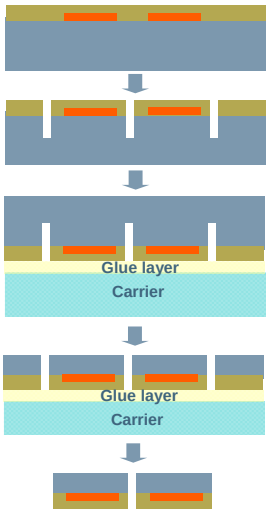


Technology enablers:
Dicing by grinding

- Process:
  - Front side trench + backside grinding
- Advantages:
  - Thin dicing lines
  - Less dicing damage:
    - enabling edgeless detectors
  - Non-rectangular die shape

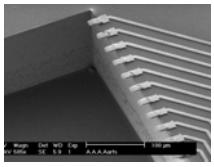


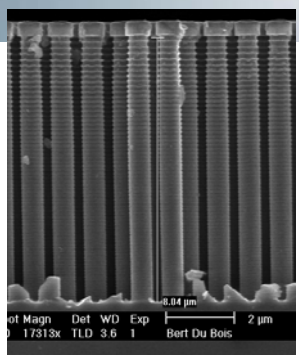


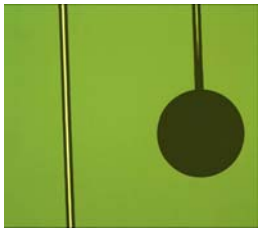


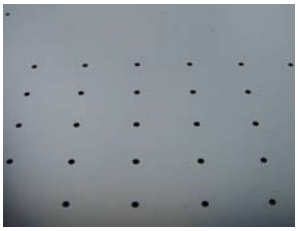
Technology enablers:
Si micromachining

- = etching Si to create (micro-) mechanical structures:
- Wet etching: KOH, TMAH, …
- Deep Reactive Ion Etching ('Bosch process'):
  - Allows to etch high aspect ratio structures
- Applications:
  - Through Si vias for 3D integration
  - Fluidic channels



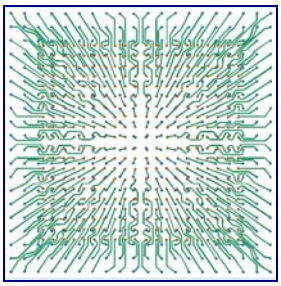


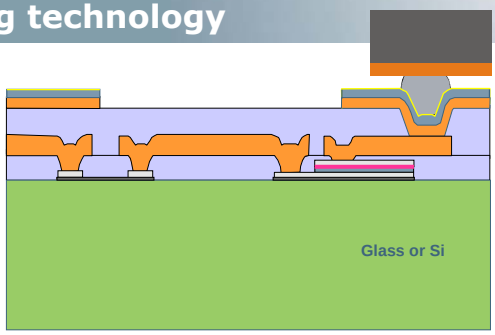


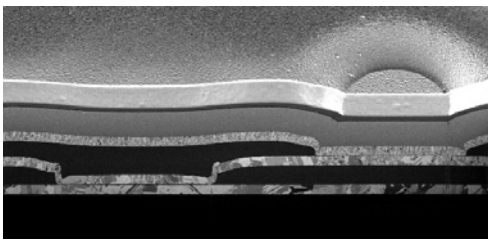


Technology enablers:
Wafer-Level Packaging technology

- Wafer-level-packaging technology:
  - multi-layer interconnect
  - Cu electroplating and dielectrics (BCB)
  - Linewidth: > 5 um lines/space
  - integrated passives: R, L, C
  - bump bonding compatible
- Applications:
  - redistribution of interconnects
  - RF-systems including antennas

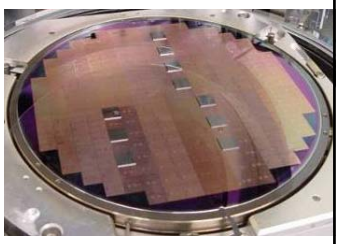


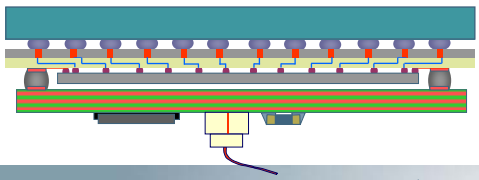




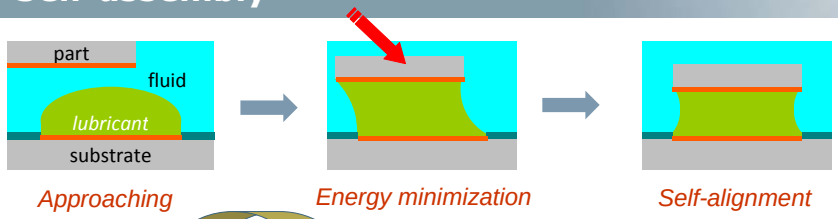
Technology enablers:
Hybrid assembly

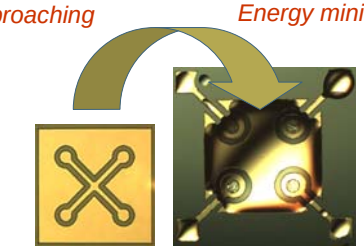
- Assembly at:
  - board or package level
  - (thin) wafer level
  - (thin) die level
- Using:
  - thermocompression bonding (e.g. Cu-Cu)
  - solder
  - (temporary) dielectric
- Limitations:
  - alignment accuracy
  - reliability issues (thermal expansion mismatch)
- Applications: smart heterogeneous systems:
  - 3D/2D integration

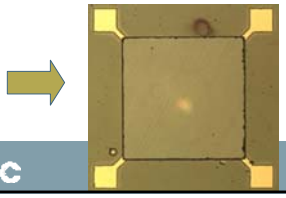




Technology enablers: Self-assembly





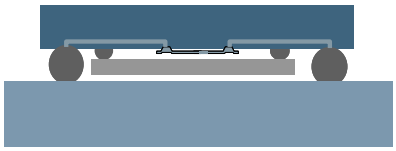


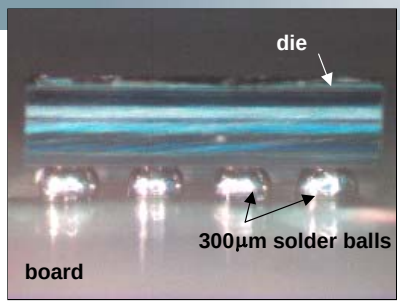
- Capillary self-assembly
- Advantages:
  - Parallel process = fast
  - Auto-alignement = sub-micron accuracy

LOW COST

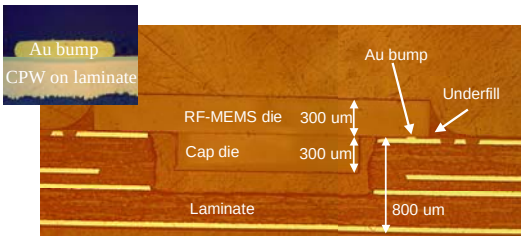
- Challenge:
  - Electrical interconnect

Technology enablers: Traditional bumping



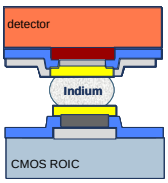


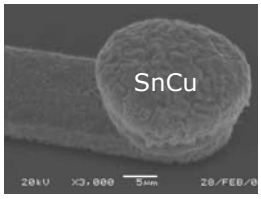
- Ball grid array (BGA):
  - Solder ball bumps:
  - Pitch ~ 300 um
- Au stud ball bumps:
  - Pitch ~ 100 um
  - High T and force
- Multiple bonding
- Underfill

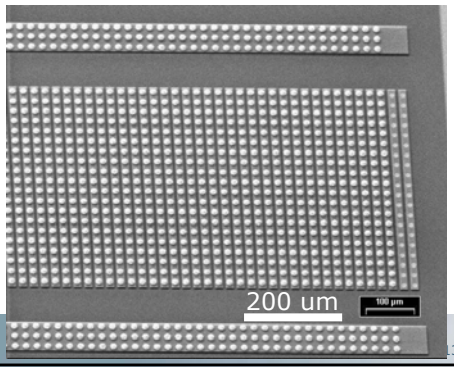


Technology enablers:
High density (micro-)bumping

- Technology:
  - (post-)processing Si, CMOS
  - under bump metallization (UBM)
  - solder (e.g. In, Sn, …) deposition using electroplating or evaporation
  - flip-chip bumping
- Features:
  - bump size ~ 10 um
  - pitch ~ 20 um
  - 1 Mpixel 2D arrays
- Applications:
  - hybrid interconnect between substrates of different technologies with low parasitics/microphonics
  - high density interconnect between imagers and read-out







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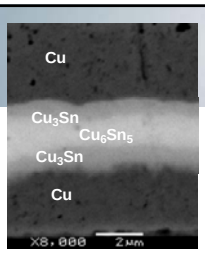
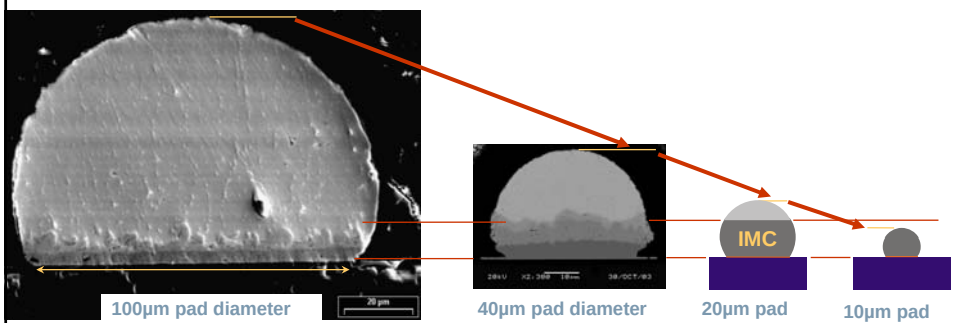
Technology enablers:
(Micro-)bumping



- Flip-chip interconnect scaling:
  - intermetallics formed by UBM solder interaction
  - smallest pitch: only intermetallic compounds
- Intermetallic bonding:
  - Advantage: have a higher melting point (and allow multiple layer stacking)
  - Disadvantage: multiple intermetallic compounds with variable reliability



100μm pad diameter
150-200μm bump pitch

40μm pad diameter
60μm bump pitch

20μm pad
40μm pitch

10μm pad
20μm pitch

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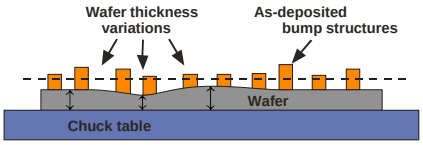
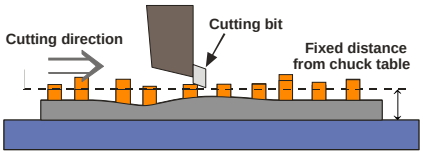
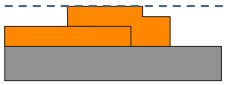
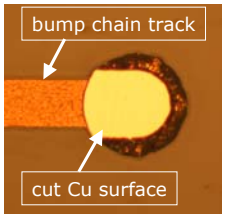
Technology enablers:
Fly cutting

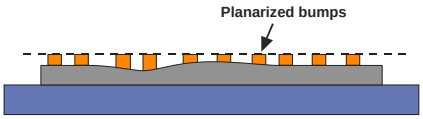
- Bump height differences are critical for interconnect yield
- Solution: fly cutting:
  - = surface planarization by diamond bit cutting
  - for soft materials: Cu, solder and/or polymer
  - Additional advantage: strong roughness reduction of bump surface





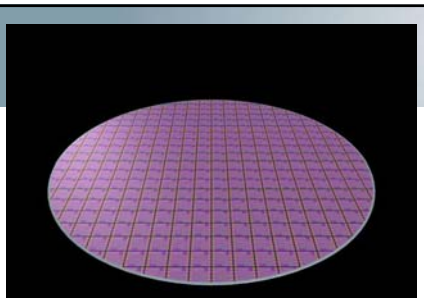


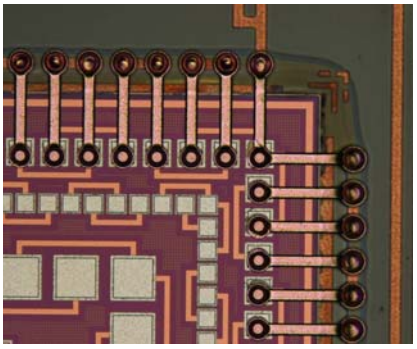


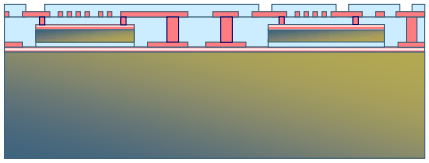


Technology enablers:
Ultra thin chip embedding

- Embedding:
  - using wafer-level and board-level technologies:
  - ~ 15 um thin dies and/or components
  - in BCB, Silicone, Polyimide dielectric
  - interconnect at bondpad level using (electroplated) Cu, Pt
  - board level: lamination/overmolding
  - wafer level: thin film technology
- Interconnect density:
  - demonstrated down to 40 um pitch

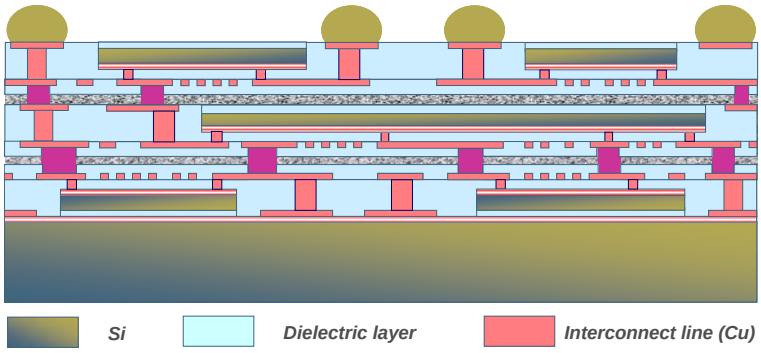






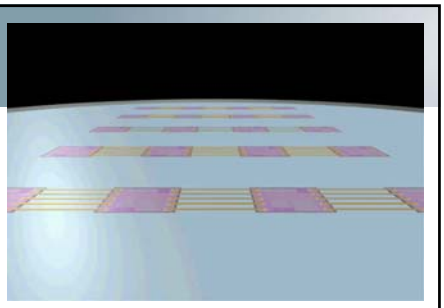
Technology enablers:
Multiple ultra thin chip embedding

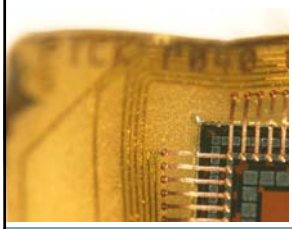
- development ongoing :
  - multiple layers of embedded thin dies
- enables 3D stacking of different die size

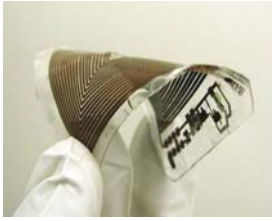


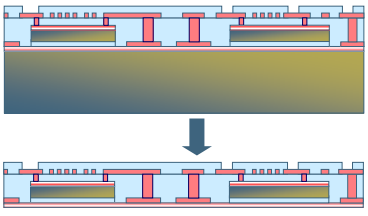
Technology enablers:
Embedding in flexible substrates

- = embedding flow in combination with sacrificial layer release
- application:
  - foldable tracker/imagers with minimal X_0



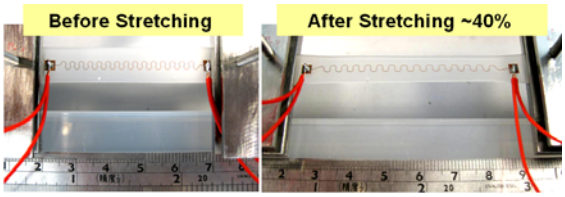


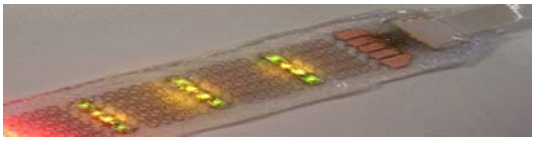


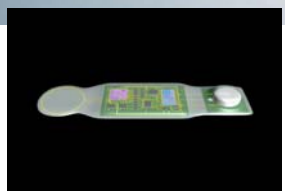


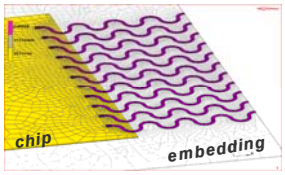
Technology enablers:
Embedding in stretchable substrates

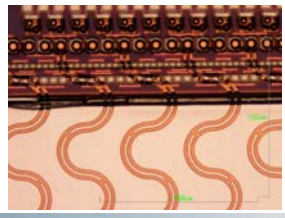
- Technology:
  - Silicone material easily deformable
  - Special design to allow stretchable (metal) interconnects
- Results:
  - Electrically yielding elongation up to 100% demonstrated





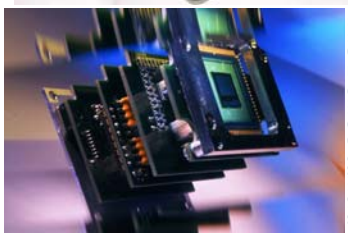






Technology enablers:
3D-System In a Package approach

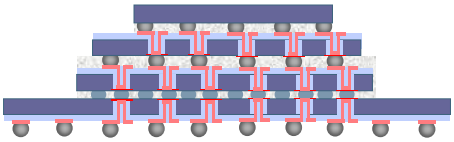
- Stacking of 2D-SIP "sub-systems"
  - each layer is an PCB with (packaged) dies and/or components
  - different assembly technologies can be used
  - interconnect density: 2-3/mm, 4-11/mm^2
- Advantages:
  - generic 3D technology
  - each layer is fully tested before final assembly
  - best yield and manufacturability
- Limitations :
  - relatively low 3D interconnectivity
  - lack of standardization of package sizes
- Application:
  - miniaturized detector systems
  - Heterogeneous integration of detectors, interposer, read-out, output drivers, cabling, …



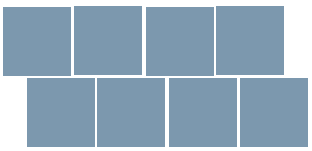
IRIS-2 CMOS camera

Technology enablers:
Post-processed 3D integration

- 3D interconnects:
  - realized at wafer level
  - Post-processing on fully processed wafers
- Technology:
  - Through Si via last approach
  - microbumping
- Interconnect pitch:
  - 50 – 100 um
- Advantages:
  - no interference with process of individual layers
- Limitations:
  - not the highest interconnect density
  - birthday cake limitation

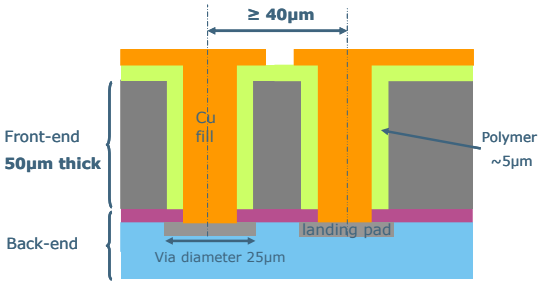


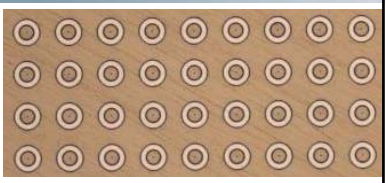
- Applications:
  - Vertical interconnects at bondpad level with low parasitics
  - Enables very thin smart 3D sensor/imager systems allowing tiling/full buttability with minimal non-sensitive detection area

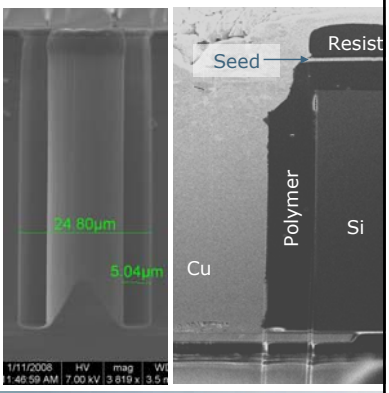


Technology enablers:
Post-processed 3D Through Si Vias

- = thinning first,
  then TSV processing from the back
- Design considerations:
  - Typical final substrate thickness = 50 um (= flexible !)
  - Landing pad to be designed at lowest metal

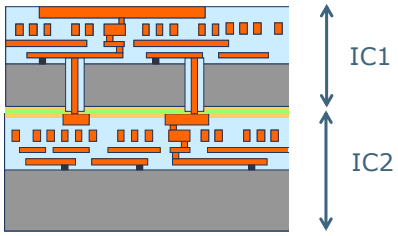






Technology enablers:
TSV processing during CMOS process

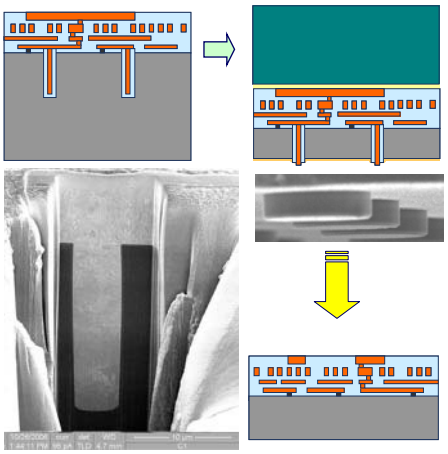
- Technology:
  - fabrication at device level, i.e. as a part of (CMOS) flow
  - after FEOL, before BEOL
  - will become established in advanced CMOS foundries (core partners, e.g. TSMC, Matsushita, Intel, Micron, …) participate in 3D IC work at IMEC
- Specifications:
  - Si thickness: 10 – 20 um
  - via diameter: 3 – 5 um
  - via pitch: 10 um
- Applications:
  - Pixel level interconnect
  - imager/processor/logic/memory stacking



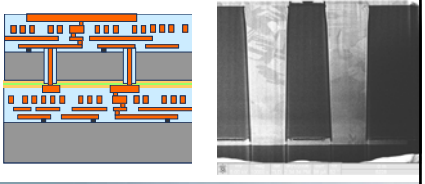
Technology enablers:
TSV processing during CMOS process

Via processing

Extreme thinning (on carrier)

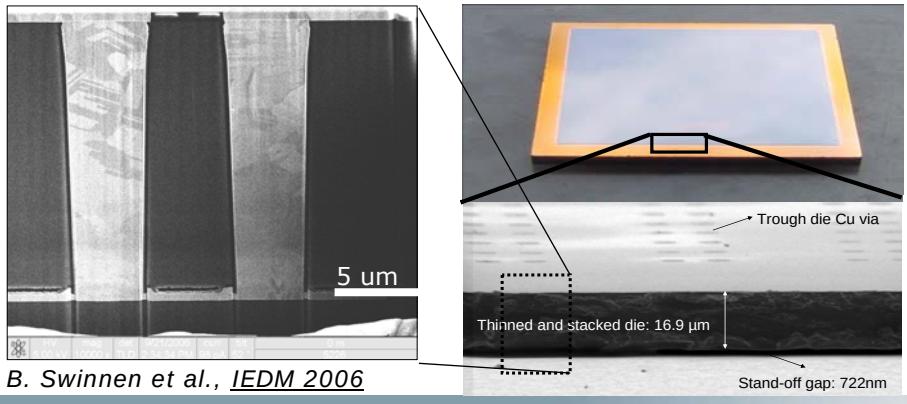


Mixed polymer and Cu-Cu thermocompression bonding



Technology enablers:
TSV processing during CMOS process

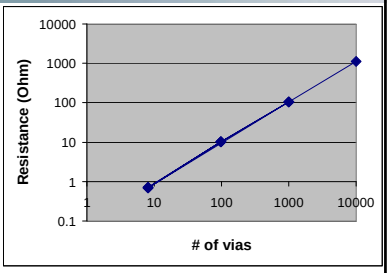
- Through Si vias:
  - Today: Pitch 10 micron, via diameter: 5 micron
  - Aspect ratio determines via diameter (thin dies = smaller interconnects)
  - Roadmap: via diameter 2 micron

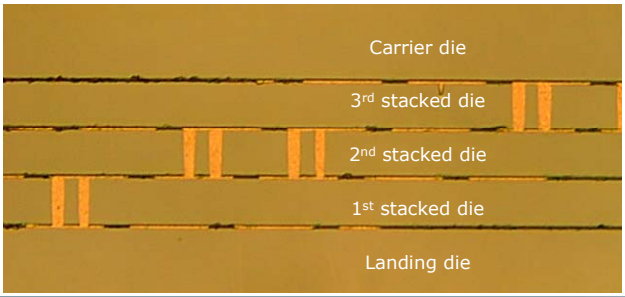


B. Swinnen et al., IEDM 2006

Technology enablers:
TSV processing during CMOS process

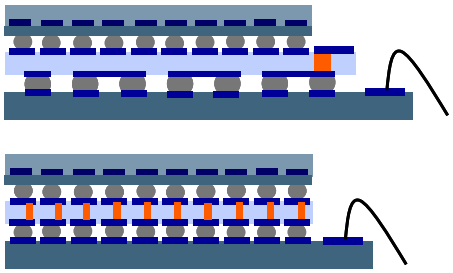
- Results
  - 10000 Cu vias in series yielding
  - via resistance ~ 30 mOhm
- 4-layer demonstrator realized





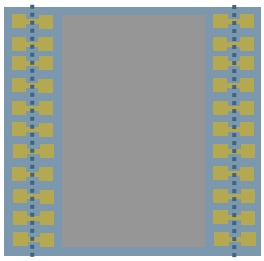
Technology enablers:
3D integration technology: trade-offs

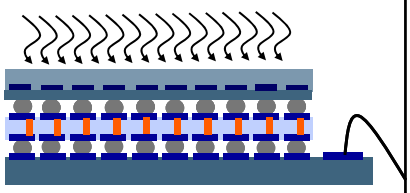
- Platform selection:
  - 3D stacking at package level (3D-SiP)
  - 3D stacking at wafer level:
    - During (CMOS) process
    - Post-process
- Required interconnect density:
  - Bondpad level:
    - ~ 50 um
  - Pixel level
    - ~ 10 um (or smaller)
    - Allows vertical pixel architecture



Technology enablers:
3D integration technology: considerations

- Known Good Die/testing considerations:
  - Probed bond pads are incompatible with bonding process
  - Solution (for die to wafer approach):
    - Special test pads outside final die
    - Removed by singulation
- Design for 3D:
  - For low energy/high stopping photons/particles:
    - Backside 'illuminated' imager on top
  - 1st layer: face to face bonding
  - What functionality on what layer (if multiple read-out layers)
  - Design software starting to appear

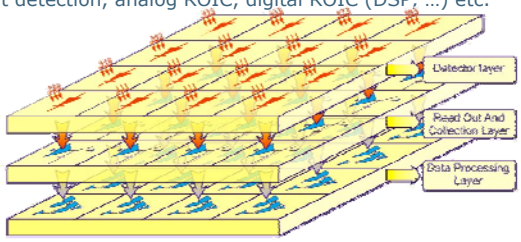




Technology enablers:
3D integration (imager) architecture

- Traditional: sensor + ROIC in 1 layer:
  - Disadvantage: limited detection area ~ efficiency and/or resolution (pitch)
- More advanced: hybrid integration of sensor-ROIC by face-to-face bumping:
  - Advantage: separate optimization of different layers

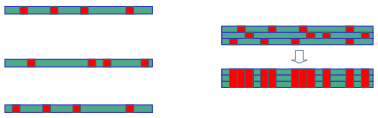
- Vertical pixel array: separate the different parts of the pixel electronics over the different layers
  - Enables better sensitivity and/or smaller pitch: (close to) 100% detection efficiency in (top) senor layer
  - Smart pixel: (extra) read-out electronics in the next layer(s)
  - Allows separate optimization of different layer (e.g. in different technologies): light detection, analog ROIC, digital ROIC (DSP, …) etc.



Technology enablers:
3D integration technology: yield trade-offs

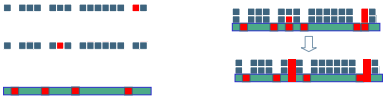
- Wafer-to-wafer vs. die-to-wafer assembly:
  - Compound yield issues with W2W
  - Yield loss due to the 'Known good die'-problem may easily exceed the processing cost for 3D stacking (!)
- D2W cost is lower than W2W stacking provided:
  - Testing allows to eliminate most bad die
  - Large die sizes always favor D2W stacking
  - Unequal die sizes always favor D2W stacking
- W2W cost is lower:
  - When testing of dies is not possible
  - For dies having very small area (<< 1 mm^2)
  - When there is interconnect redundancy (e.g. memory)

W2W assembly yield



$$Y_{3D-W2W} = Y_{2D}^{n} \cdot Y_{s}^{n-1}$$

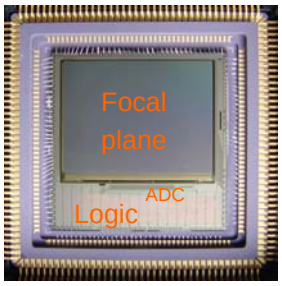
D2W assembly yield

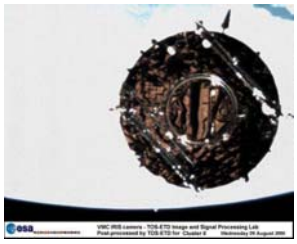


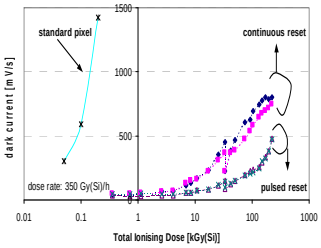
$$Y_{3D-D2W} = (1-(1-Y_{2D}) \cdot (1-F))^{n} \cdot Y_{s}^{n-1}$$

Design Enablers:
CMOS single-chip camera

- Flight Model IRIS3 single-chip camera:
  - nMOS pixel design with high fill factor
  - Single-chip camera: Digital logic (i.e. telemetry) and ADC on chip
  - Radiation-tolerant analog ROIC design: 2-3 orders of magnitude less sensitive to total dose



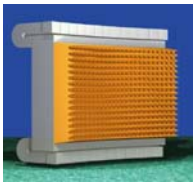


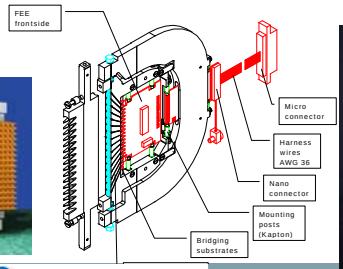


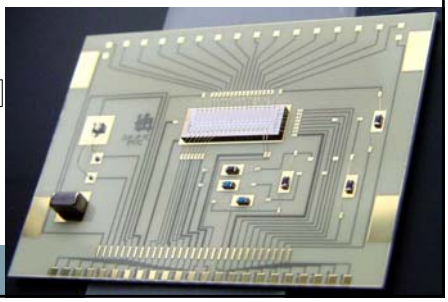
imec | OIP Sensor Systems | Fillfactory | esa

Design Enablers:
Custom analog design: cryogenic ROICs

- Analog design for 4 Kelvin operation:
  - special design to avoid anomalous behavior of standard CMOS < 20 K
- Example: PACS-CRE: ROIC for a far-infrared detector array
  - ~ 200 qualified assemblies delivered to ESA
  - Herschel satellite to be launched in 2008
  - very low noise: measures 10 fA – 100 pA
  - very low power consumption: 80 µW
  - irradiation tolerant @ 4 K



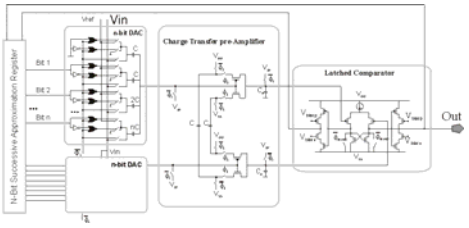


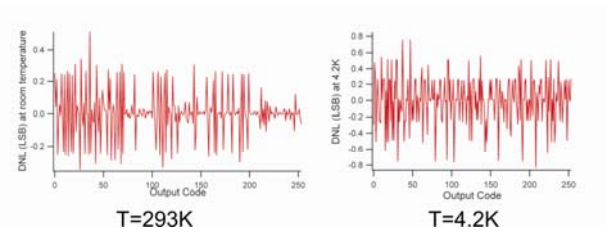


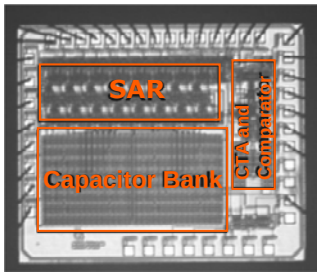
imec | esa

Design Enablers:
Custom analog design: CryoADC

- Successive Approximation ADC at Cryogenic T:
  - 8 bit resolution
  - implemented in 0.7µm AMIS CMOS
  - 350 uW power consumption
- Experiments show minor temperature dependance
- Aim: maintain signal integrity 4K – room temperature



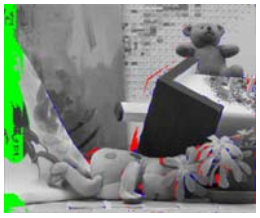




Y. Creten et al., ISSCC, 2007

Design Technology Competence:
Multi-view stereo matching and viewpoint interpolation

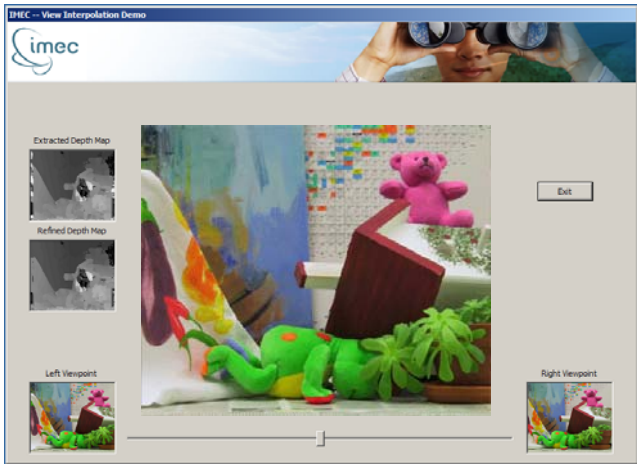
- (pseudo-)stereoscopic imaging using image processing
- Currently off-chip, could be implemented in a 3D stack



A

GeForce 7900 GPU
200 GFlops peak

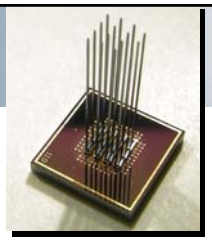
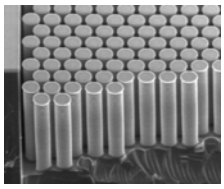
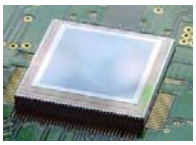
HDTV @ 20 fps
= 45 Mpixels/s

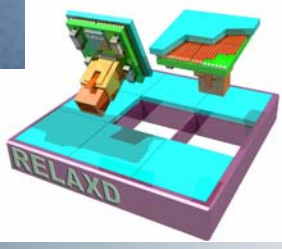


B

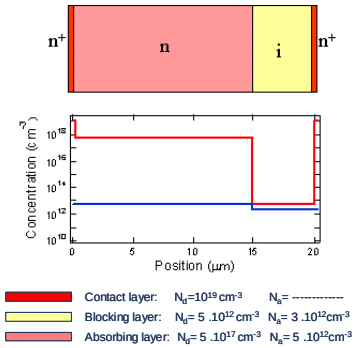
Overview:

- Technology enablers
- Detector systems examples:
  - far IR
  - TOF imaging
  - Backside illuminated CMOS
  - Endoscopy
  - (e)UV
  - X-ray
- Biomedical system examples:
  - Liquid chromatograph
  - Cochlear implant
  - Neural probing
- Conclusions & outlook

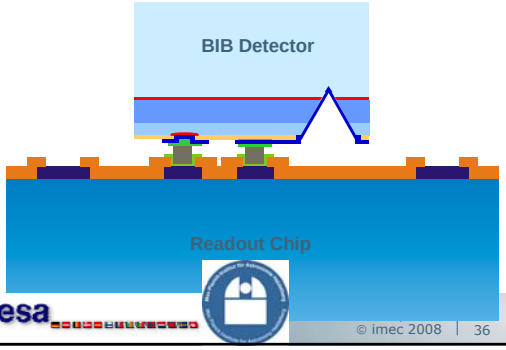






Detector systems:
Cryogenic BIB detector



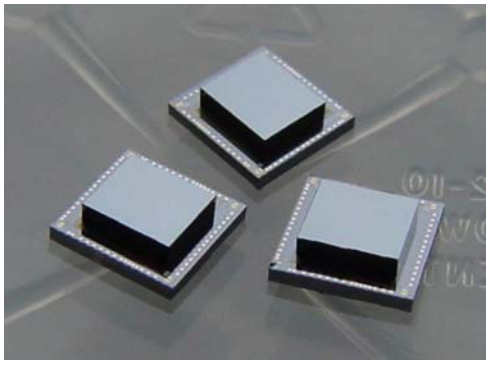
- Far IR detection: 6 – 18 um wavelength
- Si:As Blocked Impurity Band (BIB) detector array operating at 4 K
- Backside illuminated through high resistivity Si

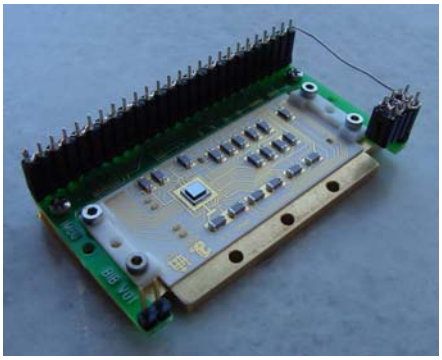


- Hybridization on cryogenic ROIC using In bumps

Detector systems:
Cryogenic BIB detector

- Linear array: 2x 88 pixels
- Pitch: 30 um
- Application:
  - DARWIN mission: search for exoplanets

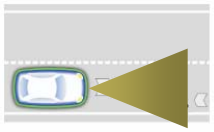


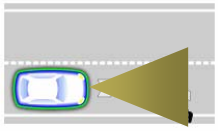


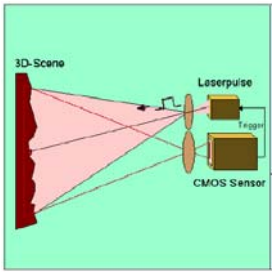
Detector systems:
3D Time-of-flight camera

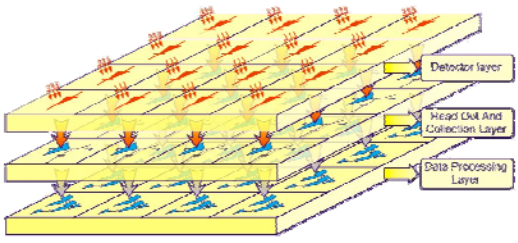
ADOSE

- **Automotive** ADAS application: object detection in front of car by time-of-flight imaging
- Requires fast and intelligent pixels in combination with high resolution
- 3D integration using TSVs per pixel allow for 'vertical' pixel



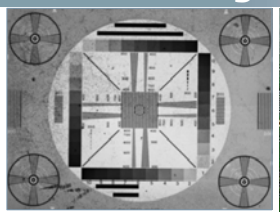


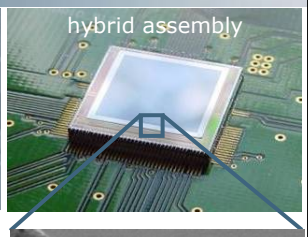


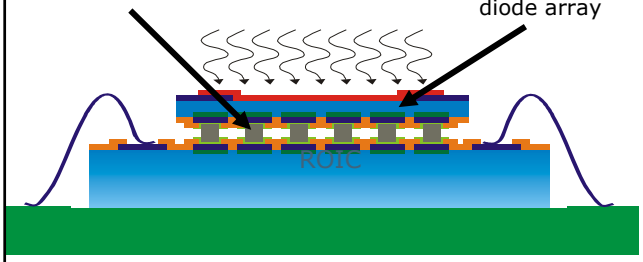


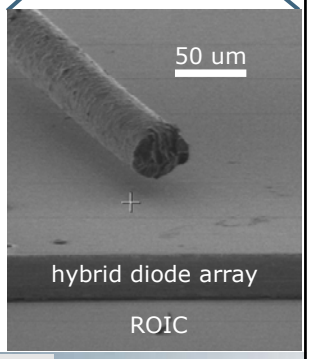
Detector systems:
Backside illuminated CMOS imager

- Specifications:
  - 22.5 um pitch
  - 1 – 4 Mpixel
  - thinned down to +/- 35 um
  - In bump yield ~ 99.95 %







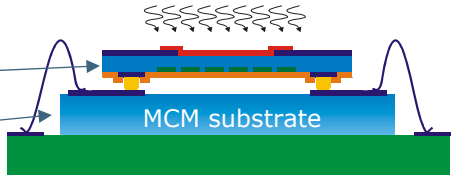


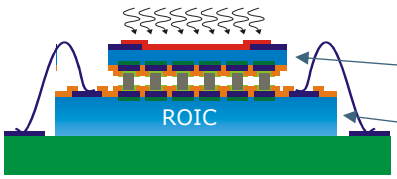
K. De Munck et al., IEDM 2006

System examples:
Backside illuminated CMOS imagers

Monolithic version

Backside thinned CMOS APS mounted on MCM substrate using Au stud bumps





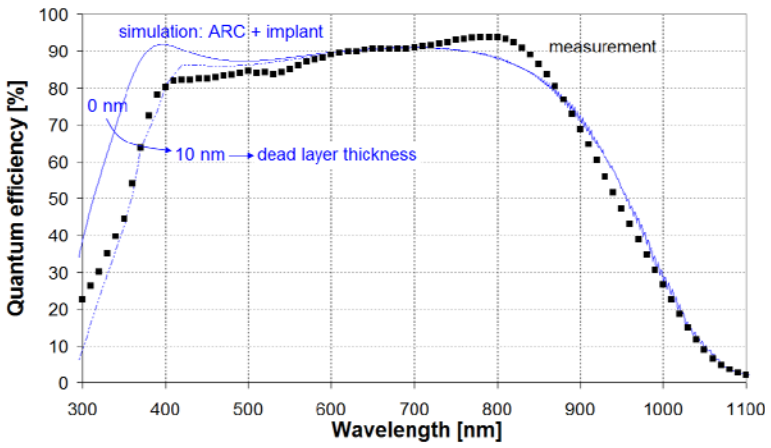
Hybrid version

Backside thinned diode array interconnected pixel-by pixel to CMOS ROIC by In bumps

- Process technology
  - Diode array: designed and manufactured @ IMEC 200 mm pilot line
  - Readout Circuit (hybrid) designed by FF/Cypress
  - CMOS manufactured @ XFAB UK foundry (0.35 um CMOS)
  - Thinning, post-processing, assembly, test @ IMEC

System examples:
Backside Illuminated CMOS Imagers

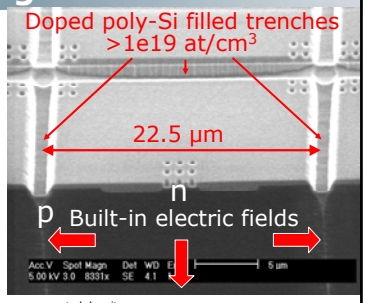
- Excellent QE of CMOS image sensor due to ARC and very shallow backside passivation:
  - > 80 % from 400 – 850 nm wavelength

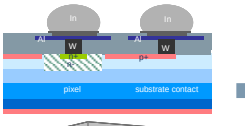


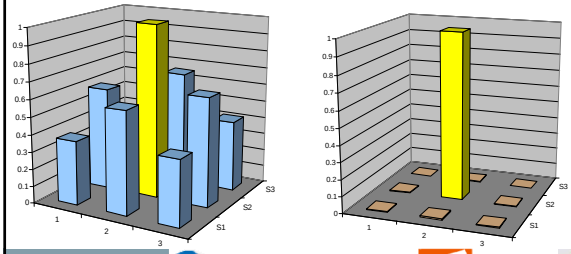
Detector systems:
Backside illuminated CMOS imager

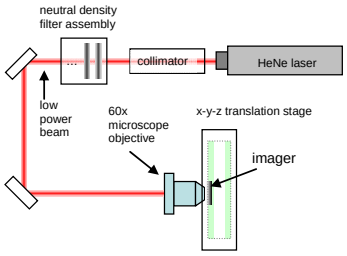
- Trenches along pixel boundaries processed in IMEC 200mm pilot-line

→ "zero" cross-talk between pixels



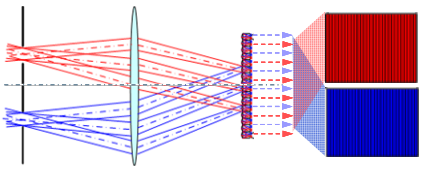


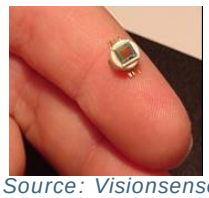




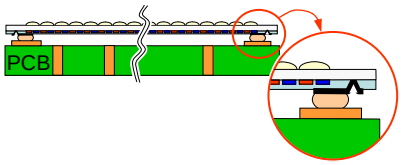
Ref.: K. Minoglou et al., IITC 2008

Detector systems:
Steroscopic endoscope camera



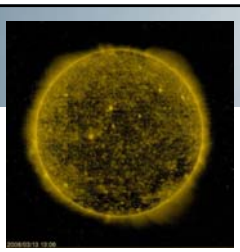


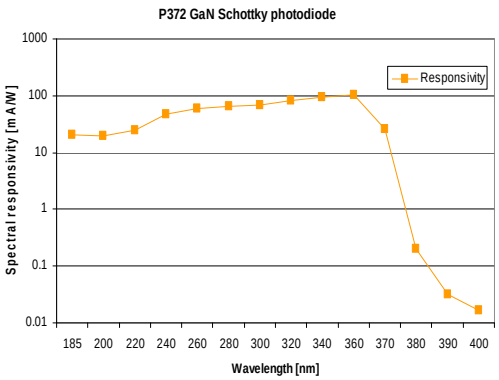
Source: Visionsense

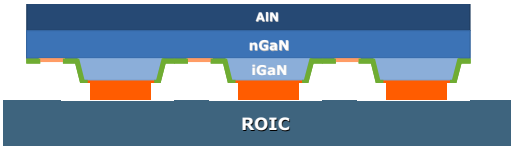


- Highly miniaturized stereoscopic imaging sensor for minimally invasive surgery
- Small area + high resolution require micron size pixels and advanced CMOS technology use
- Minimal area outside imaging sensor requires vertical integration using 3D TSV's

Detector systems:
BOLD: 2D (X)UV detection



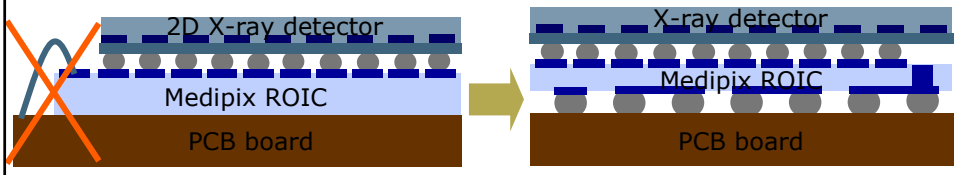




- Application: solar activity observation
- Large gap AlGaN Schottky or MSM diode detector
- Advantage over Si technology: intrinsically solar blind
- Backside illumination approach using wafer thinning, thin layer transfer, through Si optical access holes
- Hybridisation on 2D ROIC with 10 um pitch

Detector systems:
RelaxD: tilable X-ray imagers

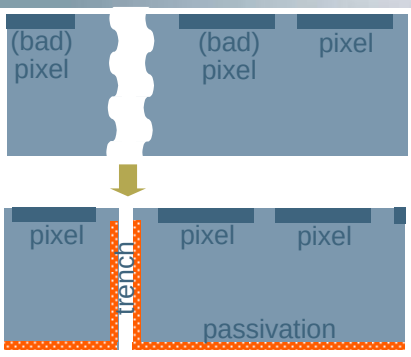
- Application: large area X-ray detection by tiling of imager modules
- Using Si X-ray detectors (Canberra) hybridized on Medipix ROICS (CERN)
- Issue: 'dead area' and hence loss of information at imager boundary due to:
  - wiring at > 1 side
- Solution:
  - Vertical electrical interconnections using 3D integration by using TSVs

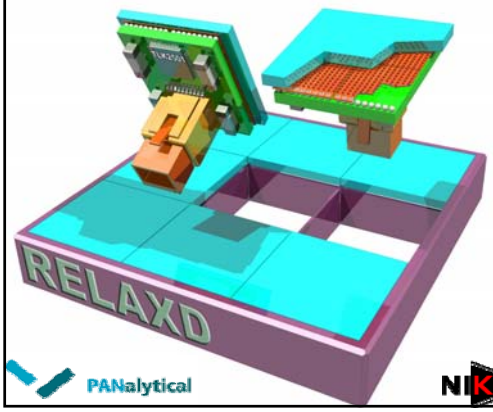


imec PANalytical NIKHEF CANBERRA AN AREVA COMPANY

Detector systems:
RelaxD: tilable X-ray imagers

- Issue: bad pixels at imager boundary due to damage by dicing
- Solution: edgeless detector concept:
  - Replace dicing by trench etching and proper passivation



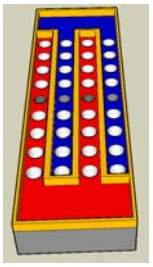


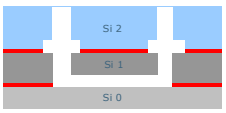
- Status:
  - 3D integration ongoing
  - minimal dead area by trench singulation and in situ passivation

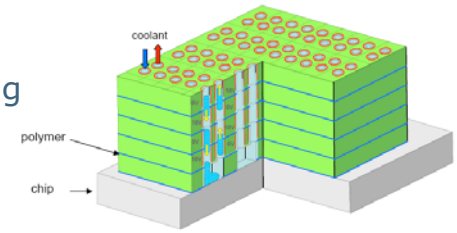
PANalytical NIKHEF CANBERRA AN AREVA COMPANY

Detector systems:
Efficient on-chip cooling

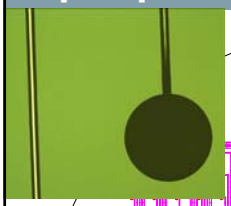
- Aim:
  - on-chip cooling of dies and 3D stacks
  - using micromachined channels and micropumps
- Concepts under study:
  - Droplet cooling
  - 2-phase cooling
- Thermal analysis by finite element modeling
- Technology:
  - DRIE
  - Wafer/die bonding

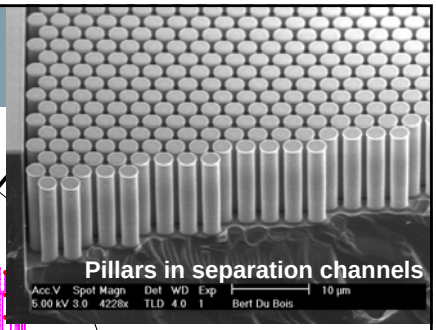






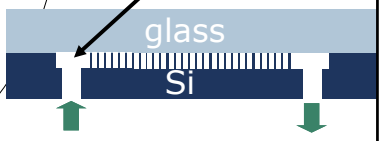
Biomedical systems:
Liquid phase chromatograph

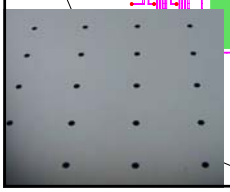




Supply channels

Through wafer holes

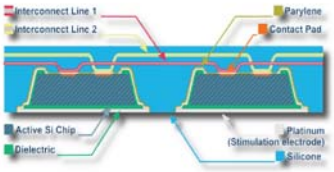




Deniz S. Tezcan et al., IEDM 2007

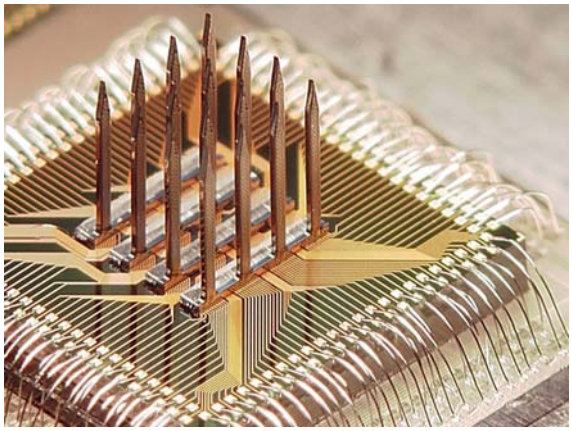
Biomedical systems:
Cochlear implant

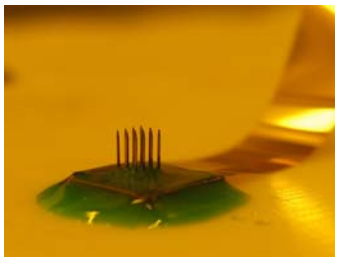
- Cochlear implants:
  - Stimulation electrodes in bended Silicone 'wire'
- 2 embodiments using wafer level flex embedding:
  - Passive electrodes = flexible Silicone substrates with Pt electrodes and interconnects
  - Active electrodes = embedding of active dies with Pt wires in thin Silicone carrier



Biomedical systems:
Neural probing and stimulation

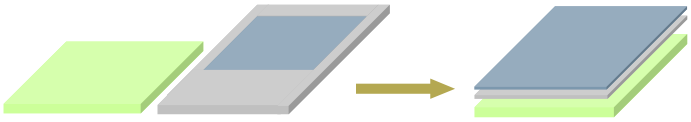
- '3D' matrix of electrodes for stimulation and recording of brain activity
- in-vivo testing ongoing





Conclusions & outlook I

- 2D flex-stretch and 3D integration technology are developing fast
- It will allow manufacturing of advanced detection systems:
  - highly **miniaturized**, i.e. compact imaging systems

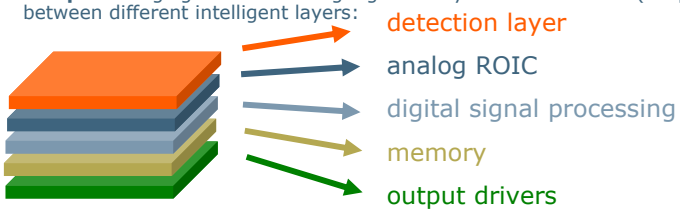


  - **tilable**, i.e. enabling large area detection with minimal non-sensitive area

  - **very thin**, e.g. **foldable** detector systems, for e.g. non-planar 4π detection, tracking detectors

Conclusions & outlook II

- High **sensitivity** by extreme thinning and backside illumination
- **3D integration technology** will allow manufacturing of **advanced detection systems**:
  - **complex** imaging detectors using high density 3D interconnects (≥1 per pixel) between different intelligent layers:



- Economical aspects:
  - (large) commercial foundries will offer 3D in (near) future
  - But: typically large volume
  - Solution: IMEC prototyping/small scale production "CMORE"

CMORE Process Environment

300 mm Facility : CMOS scaling

The 300mm cleanroom is a unique research facility that groups the world leading IC manufacterers, equipment suppliers and materials providers into a single research partnership.

NXP, Infineon, STMicroelectronics, Intel, Texas Instruments, Matsushita, Samsung, TSMC and **Micron** are core partners in this

200 mm Facility: CMORE

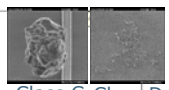
200 mm compatible cleanroom

- Silicon pilot line (24/7) for (0.13um, 90nm, 65nm CMOS processes)
- Advanced Packaging and Interconnect center and MEMS laboratories

→ **CMORE technology** offering **Multi Functional System-on-Chip** based on a 130 nm CMOS Technology Platform

IMEC's CMORE Initiative

Class A Class B



Class C Class D

- **CMORE**: ***From Concept to Production***
- Using IMEC's 200mm platform
  - advanced process tool set
  - FAB monitoring using a 130/90 nm CMOS baseline process
  - extensive Unit Process Library
  - integration methodology by development routes and dedicated teams
- Offering
  - Process transfer for large volume manufacturing
  - NEW – **Prototype and low volume production**
  - Testing, packaging and certification
  - Process & component build
  - Electronics & software design
  - Process & component design