**Project Specification**

**Project Name: CHESS-1**

**Test Chip: CMOS (HV/HR) Evaluation for Strip Sensors-1**

**Version: V 0.3**

***Abstract***

This document lists the target specifications for the test chip, which will be fabricated and tested in order to evaluate the basic device performance of HV/HR-CMOS technologies for use as a silicon strip sensor. Two representative foundries will be used.

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| ***Revision History*** | | | |
| ***Rev. No.*** | ***Date*** | ***Pages*** | ***Description of Changes*** |
| 0.0 | 2014/05/21 |  | Initial draft |
| 0.1 | 2014/05/22 |  |  |
| 0.2 | 2014/06/08 |  | Changed pixel width to 40 um.  Changed diode area fraction for the 2 technologies.  Added passive diode arrays with dummy transistors/amplifier for HV-CMOS.  Added large area array for CCE measurements.  Changed “fast amplifier” specs. |
| 0.3 | 2014/06/16 |  | A few typographical errors corrected.  The remaining open issues inserted into the spec in red |
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**Table of Contents**

# 1 SCOPE

This document describes the details of the target specification for a test chip, which will be fabricated in order to evaluate the basic device properties of HV-CMOS and HR-CMOS technologies for use as silicon strip sensors in place of the traditional planar silicon strip sensors. The test chip will be made up of several different types of test structures, each designed to test certain characteristics of the technologies. For each type of test structure, several variations of device features will be included, for example variations in the length and fill factor of the individual pixel areas. The expectation is that two foundries will be sampled and some technology specific differences will be made to the designs to match the requirements of each foundry’s technology.

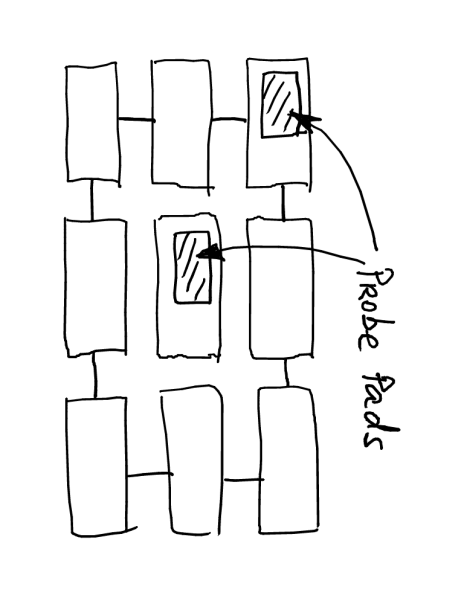
# 2 Foundries

Two foundries will be targeted at this time based upon the current understanding of the available technologies and their appropriateness for strip sensors. The two technologies are Tower-Jazz TJ180 and Austrian Micro Systems AMS-H35.

# 3 Test Structure Types and Their Specifications

The test chip will be comprised of six different types of test structures. Each is described below along with their specifications and variations.

## 3.1 Passive Pixel Arrays

For HV-CMOS technology, there will be groups of 3 x 3 pixels arranged in a rectangular array such that the eight outer pixels are electrically tied together and connected to a single probe pad. The inner pixel will be connected to a separate probe pad. An example is shown in Figure 3.1.1. This will allow direct measurements of the charge collection characteristics and pixel capacitance independent of any built-in amplifier circuitry. About 40% of the top pixel surface should have no metallization to allow laser injection measurements. Extra structures will be made with “dummy” disconnected transistors and amplifiers to evaluate their effect on the pixel capacitance.

**Figure 3.1.1 Layout of Typical Passive Pixel Array**

{Need to include pad positions and sizes in a figure. A common pad layout of two rows of 10 pads each has been proposed with pad size 90 m x 100 m, pitch of 125 m and a separation between the two rows of 250 m to fit the test structure. Is this acceptable?}

The HR-CMOS technology will feature much smaller diode area fractions and will need extra voltage buffers to evaluate the (smaller) capacitance. The array would be larger, about 16x16 pixels to avoid stray effects. No variation of diode area fraction is foreseen.

{What will be the connectivity of the 16 x 16 array? Which pixels are tied together and which have separate pads?}

{Will the common pad layout proposed for HV-CMOS work for the 16 x 16 array?}

### 3.1.1 Passive Pixel Array Specifications

The passive pixel arrays will have the following specifications. For each set of specifications, 1 array will be included.

**Table 3.1.1.A Spatial Specifications for Passive Pixel Arrays in HV-CMOS technology**

|  |  |  |  |
| --- | --- | --- | --- |
| PPA # | Pixel Dimensions | Diode Area Fraction | Extra circuitry |
| PPA01 | 40 m x 100 m | 30% |  |
| PPA02 | 40 m x 100 m | 60% |  |
| PPA03 | 40 m x 200 m | 30% |  |
| PPA04 | 40 m x 200 m | 60% |  |
| PPA05 | 40 m x 400 m | 30% |  |
| PPA06 | 40 m x 400 m | 60% |  |
| PPA07 | 40 m x 800 m | 30% |  |
| PPA08 | 40 m x 800 m | 60% |  |
| PPA09 | 40 m x 200 m | 60% | Disconnected transistors |
| PPA10 | 40 m x 200 m | 60% | Disconnected amplifier |

{Is the disconnected amplifier powered? What is its input connected to?}

{Does the disconnected transistor mean that the pixels just contain one transistor rather than a whole amplifier? What are its terminals connected to?}

**Table 3.1.1.B Spatial Specifications for Passive Pixel Arrays in HR-CMOS technology**

|  |  |  |
| --- | --- | --- |
| PPA # | Pixel Dimensions | Diode Area Fraction |
| PPA01 | 40 m x 100 m | Few % |
| PPA02 | 40 m x 200 m | Few % |
| PPA03 | 40 m x 400 m | Few % |
| PPA04 | 40 m x 800 m | Few % |

**Table 3.1.1.C Assignment of I/O pads for the test structures of both technologies.**

**{This table can be filled in later as long as there is a figure with pad layout.}**

## 3.2 Large Passive Array

To facilitate charge collection measurements with a source one would need a structure with relatively large area. To that effect, a 2x2 mm^2 area should be implemented as a passive diode array with common output from all pixels. The pixel size to be used is 40 m x 200 m.

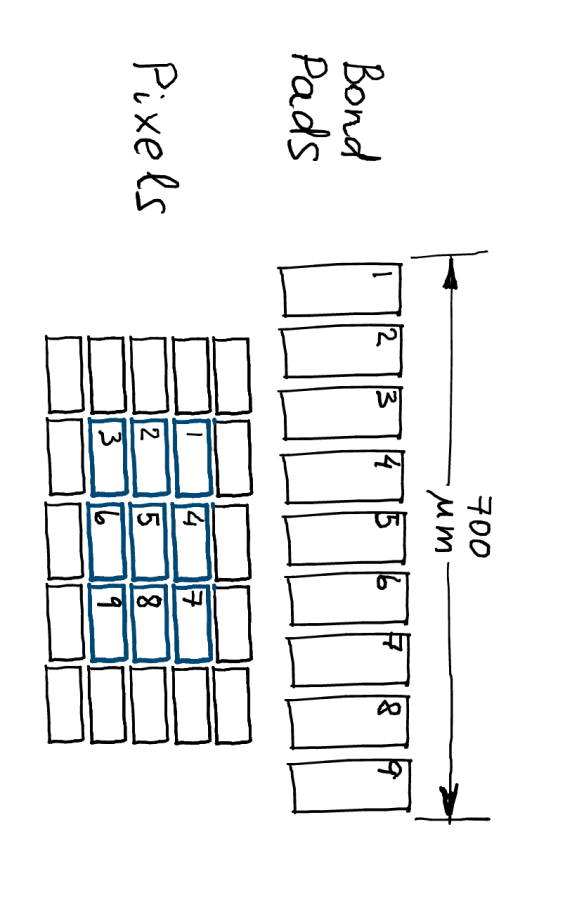
{What is the Diode Area Fraction for the HV-CMOS and HR-CMOS chips?}

{The common pad layout proposed above doesn’t work and we only need a few pads so a different pad layout figure is needed.}

## 3.3 Active Pixel Arrays

There will be groups of 5 x 5 pixels arranged in a rectangular array. Each pixel will include a fast amplifier circuit, which may not be representative of the amplifiers to be used in the actual CMOS strip sensors but is very fast to allow evaluation of the time structure of the collected charge. The power consumption of this amplifier is not a concern. The outer ring of 16 pixels are electrically tied together and connected to a single bond pad. The inner 9 pixels will be each connected to separate bond pads. An example of such a pixel array and the associated bond pads is shown in Figure 3.3.1.

{Does the HR-CMOS version also have 5x5 or something larger as was the case in 3.1?}



**Figure 3.3.1 Layout of Typical Active Pixel Array**

{Proposal for HV-CMOS chip is to use the same pad layout as in 3.1. Will this also work for the HR-CMOS chip?}

**Table 3.3.1 Assignment of I/O pads for the test structures of both technologies.**

**{This table can be filled in later as long as there is a figure with pad layout.}**

### 3.3.1 Active Pixel Array Specifications

The active pixel arrays will have the following spatial specifications. For each set of specifications, 1 array will be included.

**Table 3.3.1.A Active Pixel Array Spatial Specifications**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| APA # | Pixel Dimensions | Diode Area Fraction | ?? | ?? |
| APA1 | 40 m x 100 m | 30% |  |  |
| APA2 | 40 m x 100 m | 60% |  |  |
| APA3 | 40 m x 200 m | 30% |  |  |
| APA1 | 40 m x 200 m | 60% |  |  |
| APA2 | 40 m x 400 m | 30% |  |  |
| APA3 | 40 m x 400 m | 60% |  |  |
| APA2 | 40 m x 800 m | 30% |  |  |
| APA3 | 40 m x 800 m | 60% |  |  |

**Table 3.3.1.B Spatial Specifications for Passive Pixel Arrays in HR-CMOS technology**

|  |  |  |
| --- | --- | --- |
| PPA # | Pixel Dimensions | Diode Area Fraction |
| APA01 | 40 m x 100 m | Few % |
| APA02 | 40 m x 200 m | Few % |
| APA03 | 40 m x 400 m | Few % |
| APA04 | 40 m x 800 m | Few % |

It is preferable that the amplifier included in each pixel is fast enough to allow separation of drift and diffusion components of the charge collection. Due to the time constraints, the target speed is to be according to a “best effort” scenario. The amplifier circuit included in each pixel will have the following electrical specifications:

**Table 3.3.2 Fast Amplifier Specifications**

|  |  |
| --- | --- |
| Risetime | <= 30 ns (3 ) for HV-CMOS;  <= 100 ns for HR-CMOS |
| Noise | <50 e- |
| Gain | On the order of 500 mV/fC |
| ?? |  |

It is necessary that the inner 9 pixels have output routed to the probing pads for analog measurements. However, time-resolved digital readout can be additionally implemented if it does not interfere with the analog signals.

## 3.4 Isolated Fast Amplifier

An isolated example of the fast amplifier circuit used with the active pixel arrays will be included with an input and out pad. This is to separately test the characteristics of the amplifier in order to separate its characteristics and their evolution with radiation from that of the passive pixel sensors. ? copies of this amplifier will be included. {Do we need a picture with a pad layout?}

### 3.4.1 Isolated Fast Amplifier Specifications

Substantially the same as what is used for Active pixel array in section 3.2 .

## 3.5 Isolated Realistic Amplifier

Two types of realistic amplifiers should be included:

* An amplifier with “tuning knobs”, such as bias current, which can be used to find the technology limits with respect to noise, rise time, and power consumption when no special techniques are used to limit the rise time.
* An amplifier with additional timewalk correction scheme designed to improve the time resolution.

### 3.5.1 Isolated Realistic Amplifier Specifications

**Table 3.5.1 Realistic Amplifier Specifications**

|  |  |
| --- | --- |
|  |  |
|  |  |
|  |  |
|  |  |

## 3.6 Array of individual transistors, resistors and capacitors

In order to evaluate the characteristics of individual components of each technology, which will be important for further improvements to the active circuitry to be employed in the final CMOS sensor, an array of transistors, resistors and capacitors will be included.

The pad layout is to copy one already developed by CERN for such purposes. This will allow the use of a probe card already designed and in existence at CERN to test all the devices in this array.

{Where can we find the pad layout developed at CERN?}

# 3.6.1 Specifications for Array of Individual Device Structures

A list of transistor types and sizes, resistors and capacitors along with the pads they are connected to are listed in table 3.6.1.

**Table 3.6.1 Individual Device Properties**

|  |  |
| --- | --- |
| Transistors |  |
| Resistors |  |
| Capacitors |  |
|  |  |

# 4 Top Level Chip Layout

The layout of the overall chip showing the locations of each type of test structure is shown in Figure 4.1. {Likely not feasible now.}

Some of the active and passive pixel arrays are to be located near the edge of the design area to allow edge-TCT measurements of the depletion region.

**Figure 4.1: Top View of the Full Chip**

# 5 References