**Project Specification**

**Project Name: CHESS-1**

**Test Chip: CMOS (HV/HR) Evaluation for Strip Sensors-1**

**Version: V 0.5**

***Abstract***

This document lists the target specifications for the test chip, which will be fabricated and tested in order to evaluate the basic device performance of HV/HR-CMOS technologies for use as a silicon strip sensor. Two representative foundries will be used.

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| ***Prepared by:*** | ***Checked by:*** | ***Approved by:*** |

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| ***Revision History*** | | | |
| ***Rev. No.*** | ***Date*** | ***Pages*** | ***Description of Changes*** |
| 0.0 | 2014/05/21 |  | Initial draft |
| 0.1 | 2014/05/22 |  |  |
| 0.2 | 2014/06/08 |  | Changed pixel width to 40 um.  Changed diode area fraction for the 2 technologies.  Added passive diode arrays with dummy transistors/amplifier for HV-CMOS.  Added large area array for CCE measurements.  Changed “fast amplifier” specs. |
| 0.3 | 2014/06/16 |  | A few typographical errors corrected.  The remaining open issues inserted into the spec in red |
| 0.4 | 2014/06/17 |  | Add drawing of proposed pad layout.  Added titles for a few more needed tables, but table information yet to be included. |
| 0.5 | 2014/06/20 |  | Figures for pad layouts in Sections 3.1 and 3.3 are corrected. Shorter end pixels for arrays with pixel lengths > 400 m. A trial chip layout added in Figure 4.1. A few more details resolved. A few still unresolved in red. Questions from Ivan, Daniel & Alex inserted in green. |

**Table of Contents**

# 1 SCOPE

This document describes the details of the target specification for a test chip, which will be fabricated in order to evaluate the basic device properties of HV-CMOS and HR-CMOS technologies for use as silicon strip sensors in place of the traditional planar silicon strip sensors. The test chip will be made up of several different types of test structures, each designed to test certain characteristics of the technologies. For each type of test structure, several variations of device features will be included, for example variations in the length and fill factor of the individual pixel areas. The expectation is that two foundries will be sampled and some technology specific differences will be made to the designs to match the requirements of each foundry’s technology.

# 2 Foundries

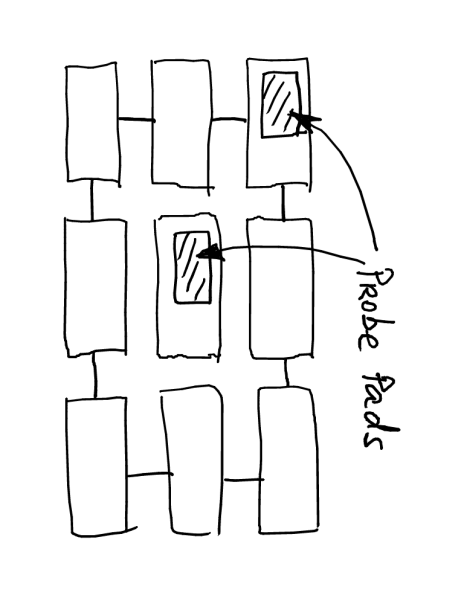
Two foundries will be targeted at this time based upon the current understanding of the available technologies and their appropriateness for strip sensors. The two technologies are Tower-Jazz TJ180 and Austrian Micro Systems AMS-H35.

# 3 Test Structure Types and Their Specifications

The test chip will be comprised of six different types of test structures. Each is described below along with their specifications and variations. {Daniel: Do we need a guard ring around each structure or around the whole chip?}

## 3.1 Passive Pixel Arrays

For HV-CMOS technology, there will be groups of 3 x 3 pixels arranged in a rectangular array such that the eight outer pixels are electrically tied together and connected to a single probe pad. The inner pixel will be connected to a separate probe pad. An example is shown in Figure 3.1.1. This will allow direct measurements of the charge collection characteristics and pixel capacitance independent of any built-in amplifier circuitry. About 40% of the top pixel surface should have no metallization to allow laser injection measurements. Extra structures will be made with “dummy” disconnected transistors and amplifiers to evaluate their effect on the pixel capacitance. {Ivan: “How will we measure capacitance? Maybe we need a test circuit on the chip for capacitance measurements”. Daniel provided a paper describing such a circuit[1]. Alex: Is this something to add on to the chip or as a separate IC?}

Table 3.1.1 lists the various pixel sizes that will be used in each HV-CMOS array. For cases where the pixel length exceed 400 m, the outer column of three pixels on the left and right of Figure 3.1.1 will be held to a length of 400 m in order that the total length of the structure not be excessively long.

**Figure 3.1.1: Layout of Typical Passive Pixel Array in HV-CMOS Technology  
Note two pads within pixel areas.**

The HR-CMOS technology will feature much smaller diode area fractions and will need extra voltage buffers to evaluate the (smaller) capacitance. The array would be larger, about 16x16 pixels to avoid stray effects. No variation of diode area fraction is foreseen. Each pixel will contain a source-follower with row and column lines attached for scanning the pixels as in an imaging array. A copy of the source follower will be included in the array of transistors (See section 3.6.) so that its contribution to the pixel capacitance can be measured.

The pad layout for this 16 x 16 array will form a rectangular ring around the array as 20-30 pads will be required.

**Figure 3.1.2: Pad Layout for Each “Passive Array” in HR-CMOS Technology**

{Renato to provide. }

### 3.1.1 Passive Pixel Array Specifications

The passive pixel arrays will have the following specifications. For each set of specifications, 1 array will be included.

**Table 3.1.1.A: Passive Pixel Array Spatial Specifications for HV-CMOS Technology**

|  |  |  |  |
| --- | --- | --- | --- |
| PPA # | Pixel Dimensions | Diode Area Fraction | Extra circuitry |
| PPA01 | 40 m x 100 m | 30% |  |
| PPA02 | 40 m x 100 m | 60% |  |
| PPA03 | 40 m x 200 m | 30% |  |
| PPA04 | 40 m x 200 m | 60% |  |
| PPA05 | 40 m x 400 m | 30% |  |
| PPA06 | 40 m x 400 m | 60% |  |
| PPA07 | 40 m x 800 m | 30% |  |
| PPA08 | 40 m x 800 m | 60% |  |
| PPA09 | 40 m x 200 m | 60% | Disconnected transistors |
| PPA10 | 40 m x 200 m | 60% | Disconnected amplifier |

The disconnected amplifier will be biased with its input tied to ground. The pixel array with a few disconnected transistors will have the transistors biased. {Confirm with Ivan.}

{Ivan: 60% is the maximum fill factor, however it probably does not make much sense. Realistic numbers are 20 to 40%. The structure with many small diodes is probably the best. Alex: Should we specify a diode size along with area fraction?}

**Table 3.1.1.B: Passive Pixel Array Spatial Specifications for HR-CMOS technology**

|  |  |  |
| --- | --- | --- |
| PPA # | Pixel Dimensions | Diode Area Fraction |
| PPA01 | 40 m x 100 m | Few % |
| PPA02 | 40 m x 200 m | Few % |

{Renato to confirm these pixel sizes.}

**Table 3.1.2: Assignment of pads for “Passive” Pixel Arrays in HR-CMOS Technology.**

{This table can be filled in later as long as there is a figure 3.1.2 with pad layout.}

## 3.2 Large Passive Array

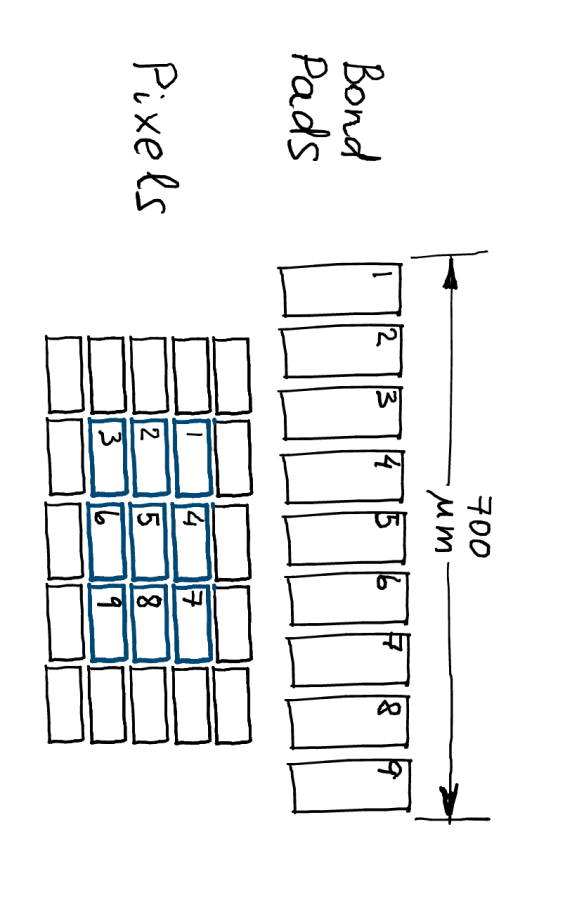
To facilitate charge collection measurements with a source one would need a structure with relatively large area. To that effect, a 2x2 mm^2 area should be implemented as a passive diode array with common output from all pixels. The pixel size to be used is 40 m x 200 m.

{What is the Diode Area Fraction for the HV-CMOS and HR-CMOS chips?}

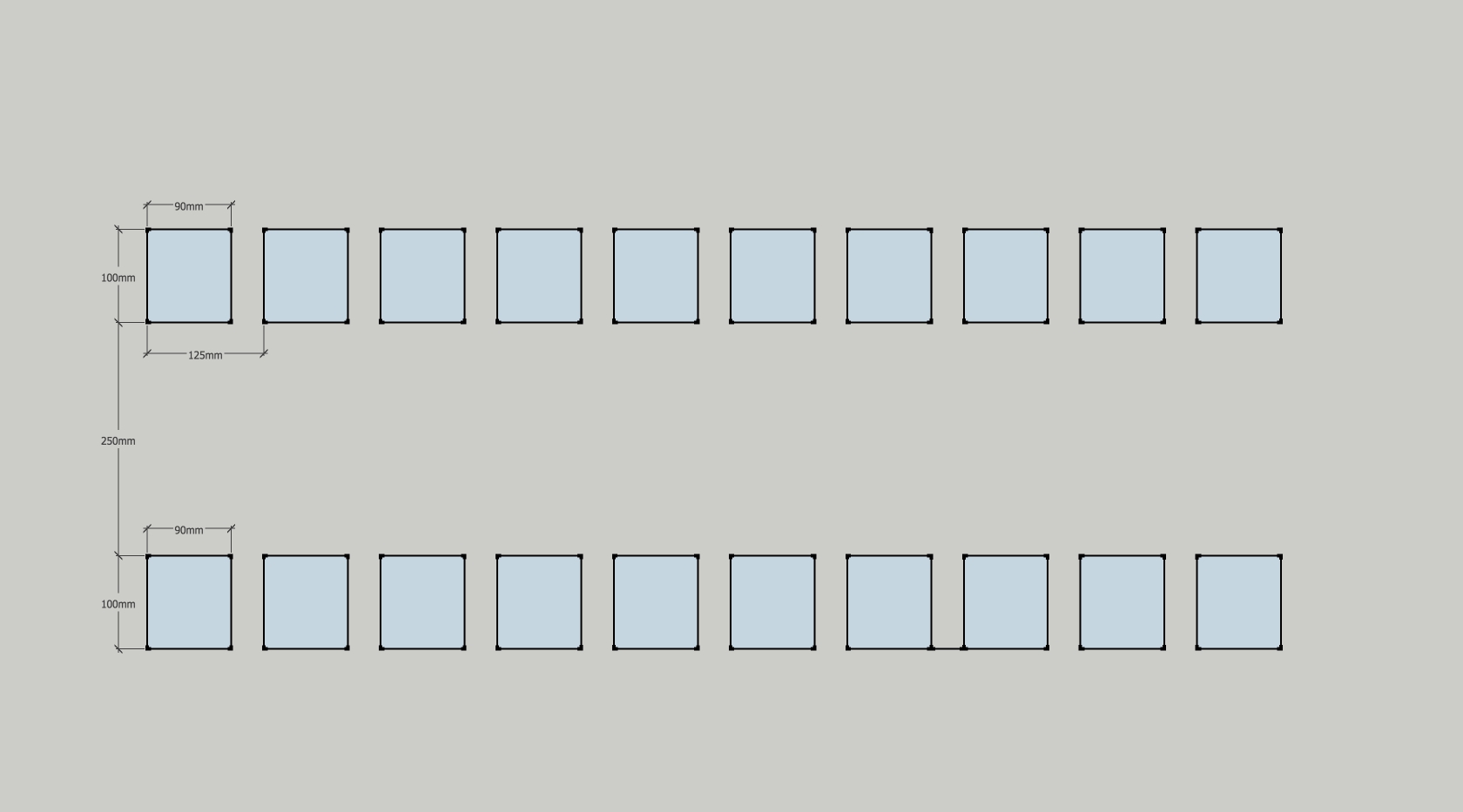
{Assumption is that only one output pad is required in addition to bias pads. To be confirmed with Ljubljana.}

## 3.3 Active Pixel Arrays

There will be groups of 5 x 5 pixels arranged in a rectangular array. {Ivan: for very long pixels geometry 5x5 is maybe not optimal. I would make e.g. 3x10. (so that the matrix is more square like) I would also make outer pixels short to avoid wasting of space. Maybe we don’t need to put so strict constraints - chip designers could decide by themselves about matrix size. Alex: Ivan is correct that for pixel lengths of 400 & 800, the 5x5 arrays become very long and narrow. See Figure 4.1. Is this OK or do we want to switch those arrays to 3x10?} Each pixel will include a fast amplifier circuit, which may not be representative of the amplifiers to be used in the actual CMOS strip sensors but is very fast to allow evaluation of the time structure of the collected charge. The power consumption of this amplifier is not a concern. The outer ring of 16 pixels are electrically tied together and connected to a single bond pad. The inner 9 pixels will be each connected to separate bond pads. An example of such a pixel array is shown in Figure 3.3.1 and the pad layout in Figure 3.3.2. The HV-CMOS and HR-CMOS chips will have examples of the same 5 x 5 arrays but the variations in pixel characteristics will be different as listed in Tables 3.3.1A and 3.3.1B. Again for cases where the pixel length exceed 400 m, the outer column of three pixels on the left and right of Figure 3.1.1 will be held to a length of 400 m in order that the total length of the structure not be excessively long



**Figure 3.3.1: Layout of Typical Active Pixel Array**



**250 m**

\\

**100 m**

**100 m**

**90 m**

**90 m**

**125 m**

**Test Structure**

**1**

**2**

**3**

**4**

**5**

**6**

**7**

**8**

**9**

**10**

**11**

**12**

**13**

**14**

**15**

**16**

**17**

**18**

**19**

**20**

**Figure 3.3.2: Pad Layout for Each Active Array at Center of Two Rows of 10 Pads**

{Verify that these pad sizes and spacings don’t violate design rules for both technologies.}

### 3.3.1 Active Pixel Array Specifications

The active pixel arrays will have the following spatial specifications. For each set of specifications, 1 array will be included.

**Table 3.3.1.A: Active Pixel Array Spatial Specifications for HV-CMOS Technology**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| APA # | Pixel Dimensions | Diode Area Fraction | ?? | ?? |
| APA1 | 40 m x 100 m | 30% |  |  |
| APA2 | 40 m x 100 m | 60% |  |  |
| APA3 | 40 m x 200 m | 30% |  |  |
| APA1 | 40 m x 200 m | 60% |  |  |
| APA2 | 40 m x 400 m | 30% |  |  |
| APA3 | 40 m x 400 m | 60% |  |  |
| APA2 | 40 m x 800 m | 30% |  |  |
| APA3 | 40 m x 800 m | 60% |  |  |

**Table 3.3.1.B: Active Pixel Array Spatial Specifications for HR-CMOS Technology**

|  |  |  |
| --- | --- | --- |
| PPA # | Pixel Dimensions | Diode Area Fraction |
| APA01 | 40 m x 40 m | Few % |
| APA02 | 40 m x 80 m | Few % |
| APA03 | 40 m x 120 m | Few % |
| APA04 | 40 m x 200 m | Few % |
| APA05 | 40 m x 400 m | Few % |
| APA06 | 40 m x 800 m | Few % |

**Table 3.3.2A: Assignment of pads for Active Array in HV-CMOS Technology.**

**Table 3.3.2B: Assignment of pads for Active Array in HR-CMOS Technology.**

**{These tables can be filled in later as long as there is a figure with pad layout.}**

It is preferable that the amplifier included in each pixel is fast enough to allow separation of drift and diffusion components of the charge collection. Due to the time constraints, the target speed is to be according to a “best effort” scenario. The amplifier circuit included in each pixel will have the following electrical specifications:

**Table 3.3.3: Fast Amplifier Specifications**

|  |  |
| --- | --- |
| Risetime | <= 30 ns (3 ) for HV-CMOS;  ~ 100 ns for HR-CMOS {Daniel: How will we separate drift from diffusion charge collection with this long risetime?} |
| Noise | <50 e- for HV-CMOS;{Confirm with Ivan} < 25 e- for HR-CMOS |
| Gain | On the order of 500 mV/fC {Confirm with Renato & Ivan} |
| ?? |  |

It is necessary that the inner 9 pixels have output routed to the probing pads for analog measurements. However, time-resolved digital readout can be additionally implemented if it does not interfere with the analog signals.

## 3.4 Isolated Fast Amplifier

An isolated example of the fast amplifier circuit used with the active pixel arrays will be included with an input and out pad. This is to separately test the characteristics of the amplifier in order to separate its characteristics and their evolution with radiation from that of the passive pixel sensors. The pad layout of Figure 3.3.2 will be used for this structure as well. Multiple copies of the amplifier will be included as can be serviced by the 20 pads. This is to allow testing of matching of amplifiers in close proximity to each other. It will also be necessary to compare the performance of amplifiers on several of the test chips available to test similar matching across a wafer.

### 3.4.1 Isolated Fast Amplifier Specifications

Substantially the same as what is used for Active pixel array in section 3.3.

**Table 3.4.1 Assignment of pads for Fast Amplifier in both Technologies.**

{This table can be filled in later as long as there is a figure with pad layout.}

## 3.5 Isolated Realistic Amplifier

Two types of realistic amplifiers should be included:

* An amplifier with “tuning knobs”, such as bias current, which can be used to find the technology limits with respect to noise, rise time, and power consumption when no special techniques are used to limit the rise time. (Ivan: i think that every amplifier on the chip, also the fast amps mentioned in previous sections, should have tuning knobs. We can reuse the bias block with dacs from my test chip.}
* An amplifier with additional timewalk correction scheme designed to improve the time resolution. {Ivan: notice that only the comparator has timewalk correction. Amplifier is just a standard amplifier. It has optionally a simple low pass filter (based on a source follower) attached.}

Two separate test structures will be provided, one for each of the two types described above. The pad layout will be the same as shown in Figure 3.3.2 and again multiple copies of the amplifier will be included in each structure as can be serviced by the 20 pads.

There is concern that there may not be enough time before the submission deadline to compete these two designs. It would help greatly if some previous design concept was available. If these two test structures cannot be completed in time for the submission deadline, then they should be left out rather than miss the submission.

{Is this an agreed course of action?

### 3.5.1 Isolated Realistic Amplifier Specifications

**Table 3.5.1: Realistic Amplifier Specifications**

|  |  |
| --- | --- |
|  |  |
|  |  |
|  |  |
|  |  |

{These specs are yet to be determined. Does someone have suggestions?}

**Table 3.5.2: Assignment of pads for Realistic Amplifier in both Technologies.**

**{This table can be filled in later as long as there is a figure with pad layout.}**

## 3.6 Array of individual transistors, resistors and capacitors

In order to evaluate the characteristics of individual components of each technology, which will be important for further improvements to the active circuitry to be employed in the final CMOS sensor, an array of transistors, resistors and capacitors will be included.

The pad layout is to copy one already developed by CERN for such purposes. This will allow the use of a probe card already designed and in existence at CERN to test all the devices in this array.

{Renato has the pad layout invented at CERN. Need to include it here.}

# 3.6.1 Specifications for Array of Individual Device Structures

A list of transistor types and sizes, resistors and capacitors along with the pads they are connected to are listed in table 3.6.1.

**Table 3.6.1: Individual Device Properties**

|  |  |
| --- | --- |
| Transistors |  |
| Resistors |  |
| Capacitors |  |
|  |  |

{Need to get this list from Renato and Ivan with other suggestions from design team.}

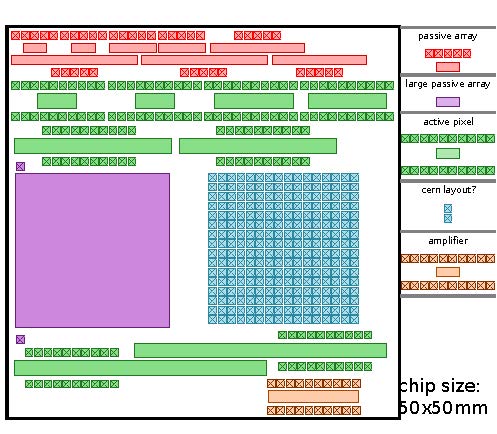
**Table 3.6.2: Assignment of pads for Array of Device Structures in both Technologies.**

{This table can be filled in later as long as there is a figure with pad layout.}

# 4 Top Level Chip Layout

The layout of the overall chip showing the locations of each type of test structure is shown in Figure 4.1. {Likely not feasible until more progress made on individual test structures.}

Some of the active and passive pixel arrays are to be located near the edge of the design area to allow edge-TCT measurements of the depletion region.



**Figure 4.1: Top View of the Full HV-CMOS Chip**

**{This is just a very rough trial to see how big a chip we might have. More   
optimization will be done after questions in the spec are answered.}**

# 5 References

1. M. Havranek, et al., “Measurement of pixel sensor capacitances with sub-femtofarad precision”, *NIM A714*, 83-89 (2013).