AMS H35 test chip for the ATLAS strip detector

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The AMS H35 test chip for the ATLAS strip detector (Europractice name “HVStripV1”) is a 1.7 mm x 2.3 mm large HVCMOS sensor. The block schematic of the chip is shown in Fig 1. The chip contains a pixel matrix of 22 x 2 active pixels (red in the figure). The pixel size is 40 µm x 400 µm. Every pixel contains a deep n-well sensor diode and a charge sensitive amplifier with a source follower SF. (SF acts as unity gain buffer.) The charge sensitive amplifier has a peaking time of about 140 ns. For test purposes, it is possible to inject charge signal into every pixel by using of an external injection pulse. The test injection can be enabled pixel-wise.

The outputs of the pixels (source follower outputs) are connected to the readout cells (RO-cell in the figure). Every pixel has its own readout cell. There are 44 these readout cells on the chip. They are arranged in one dimension – i.e. placed next to each other and connected to pixels as indicated in the figure.

Every readout cell contains three parts – the comparator block (Comp), the digital readout block (Dig. RO) and the configuration register (Conf).

Comparator block

The comparator block contains two comparators, one normal and one with the time walk (TW) compensation. These comparators are connected in parallel to the pixel output. It is possible to multiplex out the outputs of these comparators (CompOutN and CompOutTW). to two IO pads. The bits that control the multiplexer are stored in the configuration register. It is also possible to multiplex out the analog pixel output (AmpOut).to another IO pad.

The comparator thresholds and the delay time in the case of the TW-compensated comparator can be tuned by three 4-bit DACs placed in every readout cell.

Digital readout block

The digital readout block receives the outputs of the comparators. One configuration bit selects whether the normal- or the time walk compensated comparator is used for the readout.

The digital readout block is clocked by the external readout clock – the clock speed should be 40 MHz, like the bunch crossing period.

The purpose of one digital readout block is to send its own address (which corresponds to the pixel address) to one of the two address lines if a comparator rising edge occurred in the previous clock period. The address is valid for one clock period. The address word contains a 6-bit Gray coded address and a “Hit-bit” signalizing a valid hit.

Forty four digital readout blocks are serially connected.

The block uses the first address line if there are no hits in the blocks before. Otherwise (there is a hit before) the second address line is used. The existence of the hits before a block is detected by a hit-number-parity signal (ParIn/Out). The scheme works for zero, one or two simultaneous hits within one clock period. For three hits, one of the addresses will be scrambled, but we can know that it

happened by observing the parity signal. More detailed schematic of the digital readout block and the chip is in Fig 2. The pixel addresses (7 bits for both hits) and the parity bit (two copies) are readout serially via two LVDS links (one link for the first and one for the second hit). These LVDS output pads send the data with 8-times higher frequency than the clock of the digital block. The data transmission rate is 320 Mbit/s in the case of 40 MHz clock. The 320 MHz-clock for the seriallizer and the 40 MHz-clock for the readout cells are provided externally via two LVDS inputs.

Bias- and test circuits

The bias voltages necessary for the operation of the active pixels and the comparator blocks are generated by 14 on-chip 6-bit DACs. The DAC shift register is connected to the serial output of the configuration register.

The test detector contains additionally simple test structures. These test structures can be used without configuring the registers. Most of the test structures have separated dedicated pads. However, gnd, vdd, substrate-HV and some other pads are shared.

We have the following test structures:

One test pixel (Test pix. in Fig 1) of the same size as the active pixels (40 µm x 400 µm). This pixel does not contain any electronics inside the deep n-well. The diode is connected to a dedicated pad.

Nine test- n-well diodes (diode size 33 µm x 33 µm, matrix: 3x3) with the possibility to connect the middle diode and the outer diodes to three dedicated pads (Test Dio. in Fig 1).

Three MOSFETs (NMOS-linear, NMOS-enclosed and PMOS-linear) with the drains connected to dedicated pads for the measurement of radiation hardness (Test FETs in Fig 1). (The gates are connected to pads Th.)

The chip has 17 IO pads on the top and 17 pads on the bottom side. Additionally there are 14 test pads on the right side. The test pads are not necessary for the standard operation. The pitch of the pads is 100 µm.

Fig 3 shows the layout of one active pixel. The pixel consists of one main central diode with the electronics inside and 10 smaller diodes connected in parallel with the main diode. In this way I hope to reduce the diode capacitance by keeping the detection efficiency unaffected. The diode fill-factor is 34%.

Fig 4 shows the layout of the AMS H35 chip.

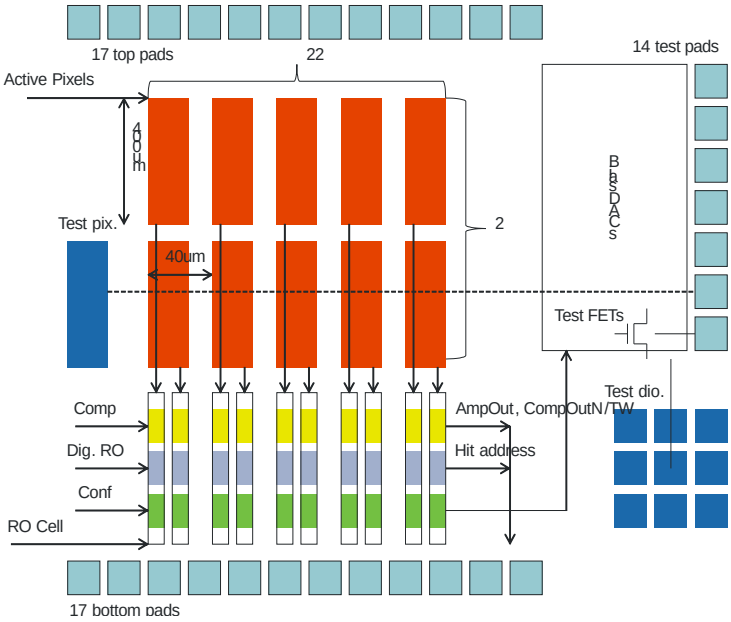

Figure 1: Block scheme of the AMS H35 test chip for the strip detector.

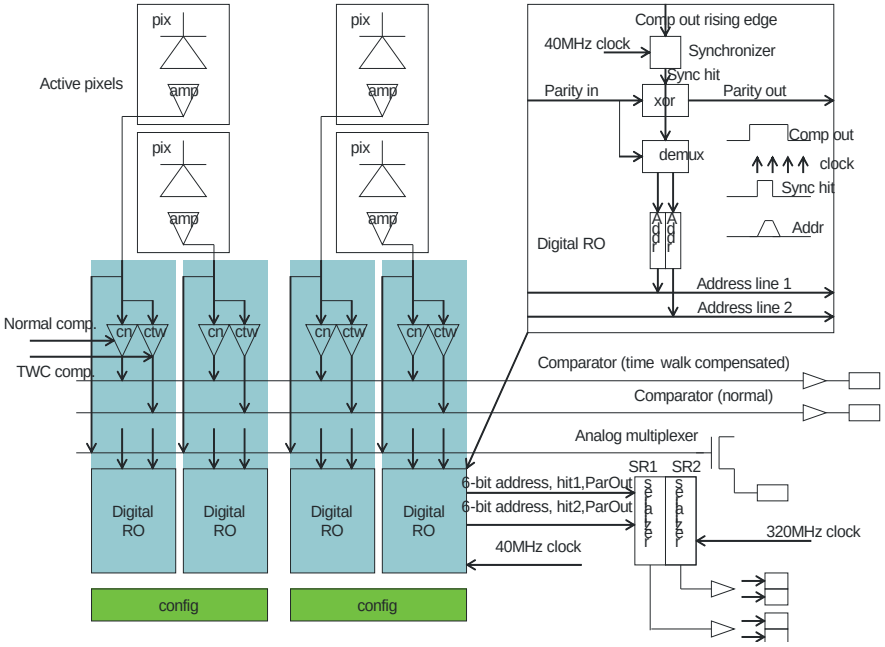

Figure 2: Detailed block scheme of the AMS H35 test chip.

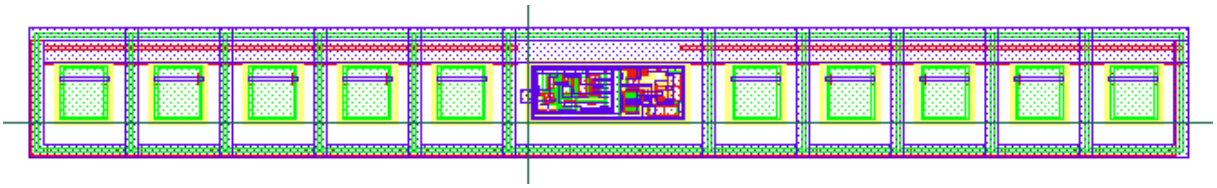

Figure 3: Layout of one active pixel.

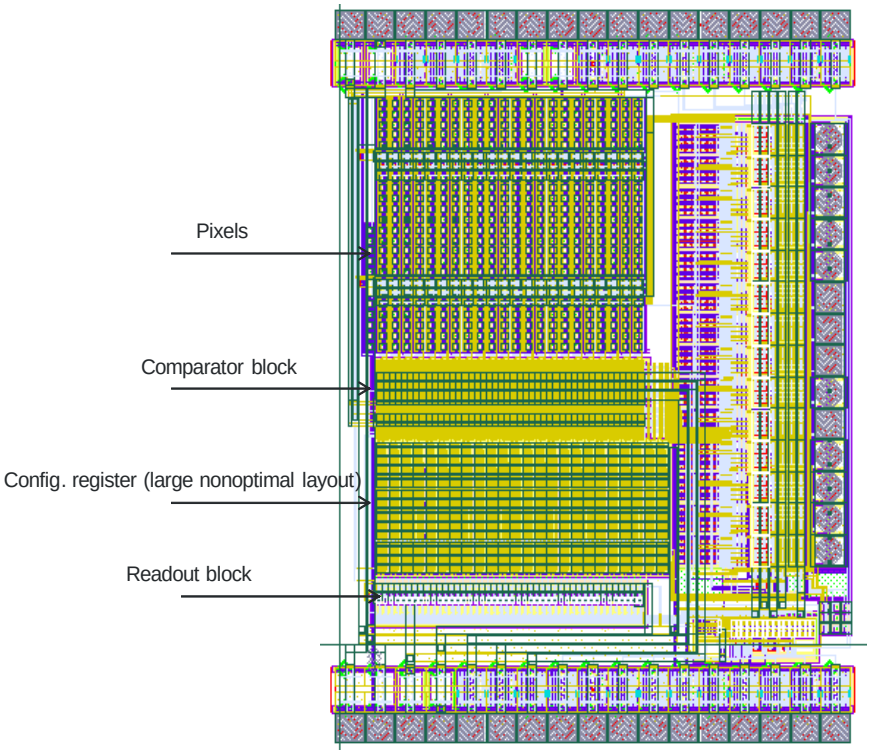

Figure 4: Layout of the AMS H35 test chip for the ATLAS strip detector.