ATLAS Strip CMOS Fortnightly Meeting - Minutes of 3rd July 2014 5pm CET

Attendance: D. Muenstermann, I. Mandic, J.J. John, T. Affolder, D. Lynn, M. Stanitzki, R. Nickerson, H. Grovas, A. Grillo, Z. Liang, Su Dong.

Meeting URL: <https://indico.desy.de/conferenceDisplay.py?confId=10520>

Apologies: C. Buttar, M. Warren

Next Meeting Date: **15/07/14 Tuesday 5pm – 6pm CET**

Continuing Actions from Previous Meetings

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| Action on | Action  | By |
| Richard, Steve | Talk to Steve about CERN agreement over shared submissions | 15/07/14 |
| Vitaliy, Alex | Complete specifications for the first submissions | 15/07/14 |
| Craig | Produce document showing tests, irradiations and schedule | 15/07/14 |
| Renato | Check Purchase Order Arrangements with Tower-Jazz | 15/07/2014 |
| Alex | Check Purchase Order Arrangements with AMS | 15/07/2014 |

Actions from this Meeting

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| Action on | Action  | By |
| Daniel | Communication between Groups | Ongoing |
| Richard, Marcel | Invite I. Peric to introduce MAPSIBO board | 15/07/2014 |
| Jaya John | Report on the Timescale of the testing board | 15/07/2014 |
| Ivan Peric | Report on Price/Timescale for ordering additional chips from AMS | 15/07/2014 |
| Ivan Peric | Send CADENCE files to UCSC | 15/07/2014 |

Agenda

* Minutes/ Actions
* Sensor Status
* Test Preparation Status
* DAQ status
* AOB

Minutes/Actions

Richard went through the actions from the last meeting.

The action concerning future arrangement for driving work areas has been resolved, Marcel will take over from Craig in August and Vitaliy will be taking over the design task from Alex soon. Concerning the discussion about the submission costs, Richard will confirm with Renato on the details. As discussed previously, DESY and the UK groups will be willing to help fund these submissions, however as there is significant money involved a formal agreement is most likely required. Richard will continue to discuss this

Daniel was charged to inform the Pixel CMOS community about developments in the Strip CMOS community and vice-versa.

The documents by Alex and Vitaly on the test structures and by Craig on the testing are almost complete, Action will be closed on the next meeting. A short discussion involved experiences shipping (irradiated) sensors around, something we need to do in the future and will need to provide some guidelines for this.

Sensor Status

Alex couldn't connect due to Vidyo issues, so Herve and Zhijan reported on his behalf. For the Design specification, there is Suggestion to put guard ring around each array, but this would require a spec for such a ring. They are still working on the Pad layout for the HR-CMOS (TowerJazz) passive array and questions like the size of the pixels and diodes. Concerning the rise time, the fast amplifier for HR-CMOS is spec’d at “~100ns”. A question will be how does one separate drift from diffusion charge collection with this long rise time. They appreciated a design suggestion for the amplifier, and appreciate input on the question of a calibration capacitor and the timewalk correction scheme. They still need a list of the transistors, Rs and Cs to include in the component test array.

For the design work, the AMS toolkit is installed at UCSC now. UCSC and SLAC will split the design effort, each doing layout for half of the test structures. SLAC has the design kit and has started designs of the passive arrays with Julie Segal as the designer

At UCSC, designs are starting today and Hervé Grabas will be the designer. Ivan Peric will send some CADENCE files to UCSC so they can get a head-start.

Testing Status

Craig send his apologies, but send some summary slides. A first conclusion of the group is, that the tests that we want to perform on the passive and active pixel arrays, which primarily focus on understanding charge collection before and after irradiation, can be done using oscilloscopes. This removes the need for a new DAQ system in the short term, although a DAQ based system will be needed for testing the "architecture" test samples. Hopefully this is easier for the different institutes as they can focus measuring pulse height and possibly pulse shape as a function of voltage and position.

As discussed at the testing meeting on Tuesday in the Testing Meeting, the plan is to develop a simple daughter board PCB that the chip can be mounted on and irradiated. This can then be mounted onto a motherboard, which will have the connections and any additional components necessary to make measurements. Two versions are being looked at, a "simple" mother board with connections and components necessary for powering the amplifiers.

Another version is being looked at by Matt and Jens that will interface with the DAQ. This is targeted at testing the architectural structures. Matt, Jens, Jaya John and myself are having a meeting tomorrow to discuss the PCBs. For the PCBs we need information on the pad layout and assignment for the new chips. We have the required information from Ivan. Jaya John will report on the outcome of the discussion and the timescales at the next meeting.

Ivan has received his HVStripV1 chip back from the foundry. Need to discuss getting the chip to groups to make the first measurements on probe stations. We also need to consider if we want to order more devices. No new groups have signed up for testing, so we currently have nice interested groups.

DAQ Status

Matt sent his apolgies, so Jaya John report on his behalf. The wew AMS H35 test chip arrived and Ivan is in contact with lots of new info. Jens has been researching and “interpreting” too. They started a twiki to store information: https://twiki.cern.ch/twiki/bin/view/Atlas/H35StripTestChip

Work on PCB spec has started (see also above). Needed is chip on a simple, low-activation daughterboard for the irradiation program. Then mount the daughterboard on a simple motherboard, do initial tests, remove, irradiate, remount and test again. The goal is to test the passive and active pixel devices. Simple connectors on the motherboard sound sufficient

For the full-functionality readout, a a motherboard with connectors to interface to DAQ systems is needed. Possible flavours of connectors to include: HSIO, USBPix and Mapsibo – they are gathering input now on this. One could mount the same daughterboard onto this motherboard, or mount the chip directly – gathering input now on this. One could also have footprints for both the daughterboard and the chip on this motherboard

The DAQ firmware modification (for HSIO) will start soon, after we get SCT and SLAC testbeam out the way (2 weeks). The HSIO port to Atlys will happen soon after (+1 week)

AOB