H35 Strip Test chip

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#	Date	Changes
0.1	02/07/2014	
0.2	02/07/2014	Operational description added by Ivan (mod by Jens)
0.3	04/07/2014	Minor corrections
0.4	09/07/2014	Additions for PCB Layout as well as operating instructions
0.5	25/07/2014	Minor information add-on about the simple test structure

Introduction

This document is to describe the use of the H35 Test chip (MOSIS submission “HVStripV1”), specifying I/O interfaces as well as control logic.

The chip delivers test structures to help identify whether HVCMOS is a viable technology for implementation of a strip-like sensor layout. It comes with a passive array of pixel type diodes that allow one to measure the sensor response, both in terms of timing and charge in a realistic environment. Additionally, individual test FETs and a big diode are implemented for measurements before and after irradiation. The chip also comes with a matrix of 22x2 strip-style pixels, implemented with active amplifiers, shapers and discriminators (both in a standard, and a time-walk compensated fashion). A block schema of the chip as implemented is shown in Figure 1 below. Active Cells are highlighted in Red, whilst passive components are shown in Blue.

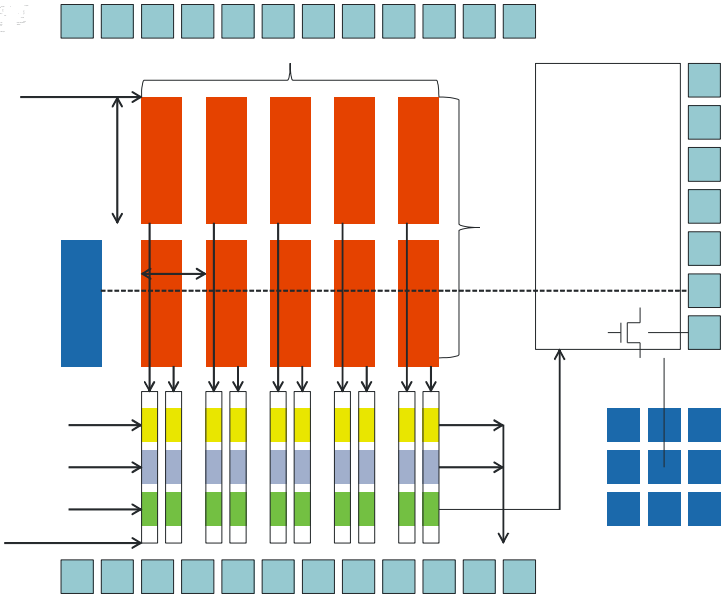


Figure 1: Schema of the HVStripV1 H35 CMOS test chip

In addition to analogue electronics, each pixel cell is supplied with a digital readout section and configuration memory. Hits recorded by the individual readout cells are pushed through a common readout block, serializing two recorded hits per base-clock cycle.

The following 2 sections will introduce the geometry and pin out of the chip, as well as functionality of the configuration and readout block.

Basic Description

Geometry

To be able to name the pads, a numbering scheme is given in Figure 2 below. The pad pitch is 100um always. The distance between Pads 1-17 and 32-48 is about 2130um. Pad names are given in Table 1.

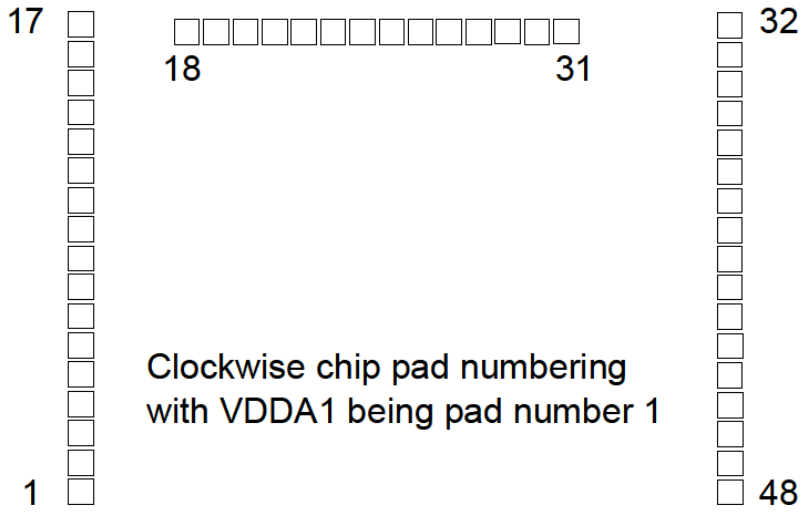


Figure 2: Pad numbering as used in table

Pinout Table:

Pad #	Name	Pad #	Name	Pad #	Name
1	VDDA	17	OutAB	33	OutHB
2	GNDA	18	SerOut	34	Out1P
3	VSSA	19	ThTuned	35	Out1N
4	DigInj	20	drainNMOSCirc	36	Out2P
5	SIn	21	drainNMOSLin	37	Out2N
6	AnaInj	22	drainPMOS	38	CkFastP
7	Sub	23	NWGuard	39	CkFastN
8	GuardRing	24	NWDiode	40	CkP
9	BL	25	NWGuardSimple	41	CkN
10	TH1	26	VCasc	42	GNDD
11	TH2	27	BigDiode	43	VDDD
12	VPBias	28	VNAmp	44	VDDRAM
13	LoadReg	29	VPLoadAmp	45	GND
14	CK2	30	VNTWDown	46	VDD
15	CK1	31	VNTW	47	GNDA
16	ShiftEnB	32	OutHBNor	48	VDDA

Table 1: Pinout Table for the HVStripV1 test chip

Maximum Ratings

Current consumption on all supply lines is less than 100mA.

The process is rated up to 3.6V continuous supply and should be able to withstand 5V stress voltage (no time known).

ESD protection is embedded through Diodes into VDDA/GNDA for Pads 1-17 and 18-31, other than for power pads and NVGuard, NWDiode, NWGuardSimple and BigDiode. The remaining pads (32-48) are connected through Diodes to VDDD/GNDD.

Pinout

Power

Ground
GND, GNDA and GNDD can be all shorted on PCB

Supply
VDD, VDDA and VDDD are all 3.3V and can be shorted on PCB

Additional Voltages
The chip needs 2.5V VSS and vddRAM, both can be shorted together on PCB
Substrate voltage is -60V, and the same voltage should be applied, or at least be applicable, to the backside pad of the chip
The GuardRing can either be -60V or floating with a capacitor

Slow Control

5 CMOS 3.3V inputs, 1 CMOS 3.3V output

SIn	Serial Input for control: Whilst bit is set, Ck1 and Ck2 need to be strobed one after the other, to correctly transfer the bit into the shift register
Ck1	First Clock for serial input, >= 20ns pulses
Ck2	Second clock for serial input, >= 20ns pulses
Load	After all configuration is shifted in, strobe Load to transfer from shift register to internal config register
ShiftEnB	Allows to shift configuration out by applying logic HI
SerOut	Serial output of shift register in case ShiftEnB is applied

Fast readout

Two LVDS inputs, two LVDS outputs

CkFast (P & N)	Hi frequency clock input (320 MHz foreseen, should work with 160 MHz as well)
CkSlow (P & N)	CkFast / 8 (i.e. 40 MHz or 20 MHz)
Out1 (P & N)	Serial output driven by CkFast, delivers Hit #1
Out2 (P & N)	Serial output driven by CkFast, delivers Hit #2

The LVDS I/Os require termination for input and output as given in Figure 3:

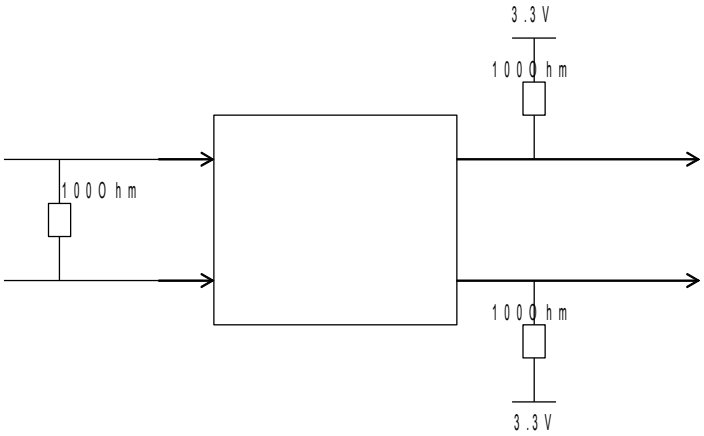


Figure 3: LVDS termination requirements

Test I/Os

AnaInjection

Allows to inject an analog pulse straight into the amplifier, pulse should be given from a pulse generator. Inside the chip, this signal routes towards every pixel and couples in through a capacitor (about 0.5fF)

DigInjection

CMOS 3.3V input – allows digital injection into pixel cell (after comparator)

OutHB

Current mode signal allowing to determine the state of the Hitbus (Timewalk compensated comparator output, ORed together) – Open drain input with 200uA, needs external pullup and comparator for proper 3.3V CMOS

OutHBNormal

Same as OutHB, but with the normal comparators being ORed

OutAB

(anallog buffer - pixel amplifier) can be connected to oscilloscope

Bias voltages

Th1 & Th2

Two thresholds (0-3.3V) with 1mV precision. Th1 current will be about a few mA. No currents will flow through Th2.

BL

Should be around 1.1V. This is not a very high precision signal with low expected current drawn and could thus be fed from a potentiometer.

VPBias, VNTW, VNTWDown, VPLoadAmp, VNAmp, VCasc & ThTuned

Internally generated bias voltages: They can be either left floating or bonded and connected on pcb to small 0603 decoupling capacitors to GND.
Recommendation is to at least prepare capacitor loaded pads for VNAmp, VPBias and ThTuned

Test devices

Notice: for the use of test structures power of the chip must be connected

BigDiode

N-well of the big test diode

NWGuardSimple, NWDiode & NWGuard

Three test diode structures in a 3x3 array:

- NWGuard: NWell of the leftmost column (c.f. Figure 1), should be bonded to VDDA, contains P-implants in the centre for test purposes
- NWGuardSimple: Simple diodes on top and bottom of the central column as well as the full right-most column
- NWDiode: The central diode, allowing the probing of a diode surrounded by others

The above mentioned I/Os are not equipped with ESD protection diodes!

drainPMOS, drainNMOSlin & drainNMOScirc

Three transistor drains for the tests of radiation hardness. (Gate connected to Th1)

Functional Description

Configuration

Configuration of the H35 test chip happens through 1 single 290 bit long shift register. The register is written using a serial input, as well as two clocks (CK1 and CK2, effectively used as strobes) as depicted in Figure 4. ShiftEnB should be 0 while shifting bits in. Pulses on CK1 and CK2 should at least be 20ns long.

The bits should be shifted in the reversed order - one should start from the last bit (c.f. Table 2 below), bit 289. After loading all data for the configuration register into the shift register, a single pulse on the LoadReg input will move the content of the shift register into latches attached to each bit of the shift register. These latches then provide the configuration bits as used in the chip.

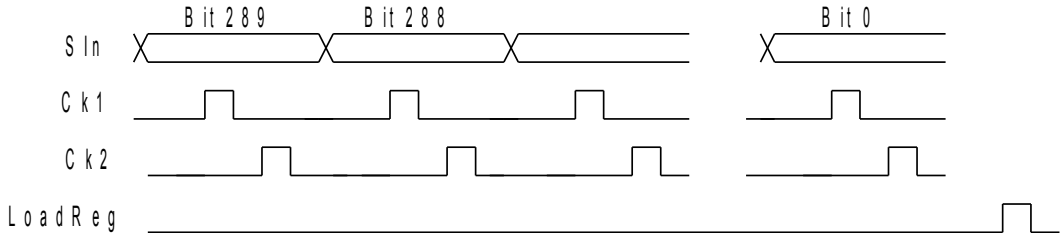


Figure 4: Slow Control Sequence

There is a possibility to read back the data stored in the latches to the shift register. This can be done by setting ShiftEnB to one and by applying Ck1 and Ck2. The bits that have been read back can be shifted out by applying 290 clock cycles (Ck1 followed by Ck2). The new data are visible on the SerOut pad when Ck2 = 1. The SerIn is taken when Ck1 = 1.

Register Content

The configuration register splits into two logical sections: The first 22 x 8 bits control 22 columns with two frontend cells each, the last 114 bits are the “global bits”.

Among the global bits, the first 16 are the control bits followed by 14 x 7 bits for 14 bias DACs. The DACs have 6-bit precision. Bits DAC#(5:0) control one DAC with bit 5 connected to MSB. Every DAC register segment (7 bits) has one spare bit.

All the bits are summarized in Table 2 below.

22 “Column pairs”				
Bit No	Bit	Name	Value	Description
0:1	Col0(0:1)	DigInjEn0(0:1)	b	Enables digital injection in RO-cell 0 or 1
2:3	Col0(2:3)	HBEn0(0:1)	b	Connects comparators to hit busses in RO-cell 0 or 1
	Col0(4:5)	Ld0(0:1)	b	Loads the TDAC values of the RAM in RO-cell 0 or 1
6:7	Col0(6:7)	AnaInj0(0:1)	b	Enables analog injection in RO-cell 0 or 1

	…	…	…	…
	Col21(0:1)	DigInjEn21(0:1)	b	c.f. CP0
	Col21(2:3)	HBEn21(0:1)	b	Connects comparators to hit busses (active high) and analog buffer to analog bus (active low) (provided ABEnB=0) in RO-cell 0 or 1
	Col21(4:5)	Ld21(0:1)	b	c.f. CP0
174:175	Col21(6:7)	AnaInj21(0:1)	b	c.f. CP0
16 global tune DAC bits (for transfer)				
176:179	TDAC2(0:3)	TDAC2(0:3)	b?	TDAC2 value to be stored in RAM (3 = MSB) (0 if not used)
180:183	TDAC1(0:3)	TDAC1(0:3)	b?	TDAC1 value to be stored in RAM (3 = MSB) (0 if not used)
184	ABEnB	ABEnB	b	Enables analog buffers if 0
185	CompOffBNormal	CompOffBNormal	b	Enables normal comparator if 1
196	CompOffB	CompOffB	b	Enables time walk comparator if 1
197	EnLowPass	EnLowPass	b	Reduces bandwidth of the pixel amplifier if 1
198:191	TDACNormal(0:3)	TDACNormal(0:3)	b?	“TDAC_normal” value to be stored in RAM (3 = MSB) (0 if not used)
14 bias DACs (6-bit DACs and one spare bit)				
Bit No	Bit	Name	Value	Description
192:197	DAC0(5:0)	VNCompNor	20	Normal comparator
198	Spare0	Enable B	0	Turns on the bias currents if 0
	DAC1(5:0)	VNTW	20	Time walk compensated comparator – main current
	Spare1	Tune DAC off	0	Turns off the tune DACs if 1
	DAC2(5:0)	ThRes	10?	Threshold tune resistance
	Spare2	Select input	0 or 1	0: normal comparator connected to readout 1: time walk compensated comparator connected to readout
	DAC3(5:0)	VNTWdown	20	Time walk compensated comparator – pulldown current
	Spare3	Not used	0	
	DAC4(5:0)	BLRes	10	Resistance of the base line holder
	Spare4	Not used	0	
	DAC5(5:0)	VNBiasRes	0	Bias resistance in the sensor diode
	Spare5	Not used	0	
	DAC6(5:0)	VNFB	5	Feedback resistance
	Spare6	Not used	0	
	DAC7(5:0)	VPLoadAmp	10	Load transistor current in the pixel amplifier
	Spare7	Not used	0	
	DAC8(5:0)	VNTune1	?	Tune DAC 1 range for time walk compensation (0 if not used)
	Spare8	Not used	0	
	DAC9(5:0)	VNSF	10	Source follower bias in the pixels
	Spare9		0	

	DAC10(5:0)	VNTune2	?	Tune DAC 2 range for time walk compensation (0 if not used)
	Spare10	Not used	0	
	DAC11(5:0)	VNTuneNor	?	Threshold tune DAC range (0 if not used)
	Spare11	Not used	0	
	DAC12(5:0)	VNAmp	60	Main bias current of the pixel amplifier
	Spare12	Not used	0	
	DAC13(5:0)	VPAB	10	Analog buffer bias and hit bus bias
289	Spare13	Not used	0	

Table 2: Configuration register content

Writing of Readout Cell Memories

Every readout cell has local memory attached to it, allowing it to hold configuration. Stored therein are 3 tune DAC values (4 bits each), TDACNormal, TDAC1 and TDAC2. Additionally there are 4 logic bits controlling parts of the readout cell:

- 2 enable bits allowing to switch On ('1') or Off ('0') both the normal comparator and the timewalk compensated comparator
- 1 Analog buffer enable bit (inverse logic, '0' means enabled)
- 1 Low Pass Filter Enable bit, reducing the bandwidth of the amplifier when set to '1'.

To access this local configuration memory, the corresponding values need to be written into the global configuration register (bits 176:191, c.f. Table 2) and then latched into the local memory by means of writing the same configuration into the global register multiple times whilst changing LdX(Y) bits – for example for column 0, row 0:

1) Write the full global configuration register, including the custom 16 bits that are to be stored and Ld0(0) = '1' (I.e. Bit No. 4 in Table 2 set)
2) Write the same configuration register but with Ld0(0) = '0'

(It is important to keep these 16 bits in the configuration register unchanged while Ld goes from one to zero.)

Configuration Examples

Configuration for simple measurements

We introduce a few settings for standardised scans here, allowing the user to get started with simple calibrations

Analog injection in pixel ColM(N) and the measurement of the comparator output response

For this measurement we need the following configuration:

- DigInjEnM(N) = 0 (not used)
- HBEnM(N) = 1, all other 0
- AnaInj M(N) = 1, all other 0 (select injection into the measured pixel)
- ABEnB = 1 (not used)
- CompOffBNormal = 1 (comparator used)

- CompOffB = 1 (comparator used)
- EnLowPass = b (low pass enable)

Analog injection in pixel ColM(N) and the measurement of the amplifier response.

For this measurement we need the following configuration:

- DigInjEnM(N) = 0 (not used)
- HBEnM(N) = 0, all other 1 (**bug**, active low – simultaneous measurement of analog- and digital response not possible.)
- AnaInj M(N) = 1, all other 0 (select injection into the measured pixel)
- ABEnB = 0 (used)
- CompOffBNormal = 0 (comparator not used)
- CompOffB = 0 (comparator not used)
- EnLowPass = b (low pass enable)

Digital injection in pixel ColM(N) and testing of digital output.

For this measurement we need the following configuration:

- DigInjEnM(N) = 1 (used)
- HBEnM(N) = 0 (not used)
- AnaInj M(N) = 0 (not used)
- ABEnB = 1 (not used)
- CompOffBNormal = 0 (not used)
- CompOffB = 0 (not used)
- EnLowPass = b (low pass enable)

If a pulse is applied on DigInj with the rising edge within the time bin *Bunch crossing 0*, we receive the address of the selected RO cell during *Bunch crossing 1 data* interval. It is also possible to inject in more than one cell.

Configuration for normal readout

Spare2 should be set to 0 or 1 depending whether we read out the normal- or time walk compensated comparator.

- DigInjEnM(N) = 0 (not used)
- HBEnM(N) = 0 (not used)
- AnaInj M(N) = 0 (not used)
- ABEnB = 1 (not used)
- CompOffBNormal = 0 (not used)
- CompOffB = 0 (not used)
- EnLowPass = b (low pass enable)

Readout Cells

The chip delivers 44 readout cells, grouped in 22 columns. Each column has two identical readout cells, 0 and 1, where 0 serves the 'upper' pixel and 1 serves the 'lower'. 8Figure 5 illustrates a two column section and the adjacent logic for hitbus and readout.

Each readout cell is comprised of the active pixel itself, a preamplifier and shaper, and two adjustable comparators. While one is a standard comparator with only threshold adjustment, the other is timewalk compensated and can be adjusted for peak timing. Either of these comparators then feeds into a digital readout block and can drive a global hitbus, allowing to externally tag whether the chip was hit.

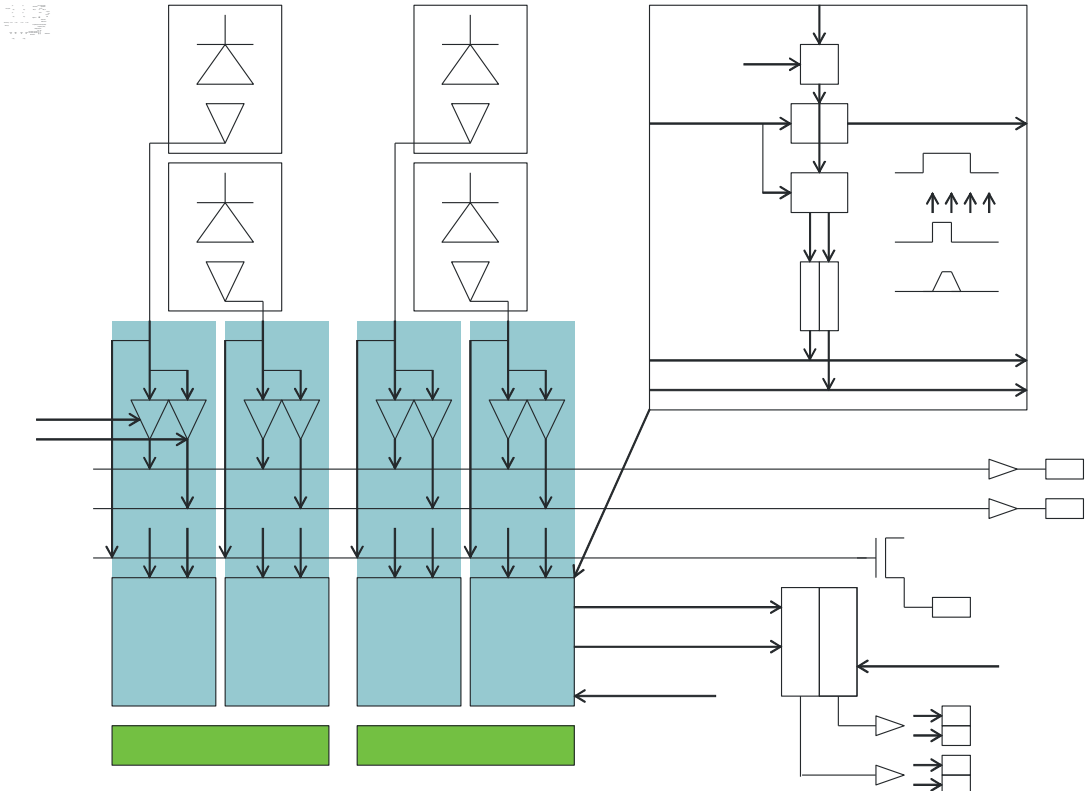


Figure 5: Simplified scheme of the Pixel Cells as well as readout and Hitbus

Pixel Cell Layout

The single Pixel Cell Layout is shown in Figure 6. 10 diodes of equal size are located around a single, slightly larger, diode that includes the active electronics. The total diode fill-factor is 34%.

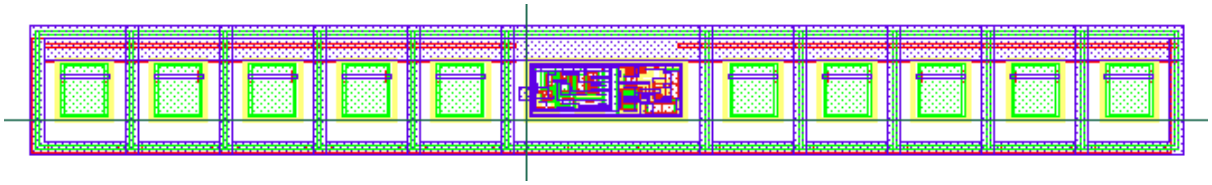


Figure 6: Single pixel cell layout.

Preamplifier

Need a pre-amplifier and shaper description, nothing exciting

Discriminators

Every RO-cell has three 4-bit tune DACs – TDAC1, TDAC2 and TDAC_normal.

TDAC_normal is used to fine tune the threshold – this threshold is connected to both comparators, with and without time walk compensation. A higher TDAC setting means a lower threshold. The local threshold can be calculated as Th_local = Th1 – TDAC_normal * VNTuneNor/ ThRes. Th1 is the external threshold voltage, TDAC_normal is the TDAC setting, VNTuneNor and ThRes are the bias DAC settings (see Table 2). TDAC1 and TDAC2 are used to fine tune the time walk compensated comparator. The functionality of these DACs will be explained later.

Digital Readout Block

The pixels become digital behind their two comparators. Both these inputs are delivered to a digital readout block, and a configuration bit selects which one read out. An external clock defines the timing of the digital readout block – 40 MHz is an expected operational clock frequency.

In Figure 5, on the top right, a block schematic of the readout block is shown.

The readout block is to send its gray-coded address (c.f. Table 3) to one of two address busses, when hit. A parity bit is handed from one block to the adjacent, being x-ored with its own hit state. It therefore shows whether any one of the previous pixels is hit and allows a pixel to send its address out on the secondary address bus. When a valid address is sent out, the cells also set a hit bit, tagging a valid hit. If more than two cells are hit, the bus is overloaded and therefore data can be corrupted (c.f. below).

9A fast readout block takes in the addresses generated by the pixels and sends them out serially using a high frequency clock (8 times higher than the readout block clock, typically 320 MHz). A timing sequence of hit generation and readout is shown in Figure 7 below.

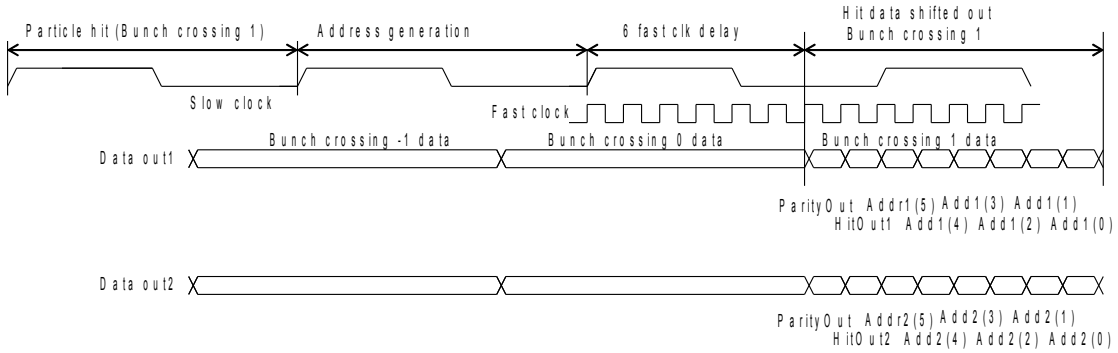


Figure 7: Readout timing diagram

9It is assumed that the slow clock is derived from the fast one – the active edge of the slow clock is slightly later than the active edge of the fast clock, which may need calibration when using the fast readout.

The data labelled by “Bunch crossing 1 data” which are shifted out serially from two LVDS outputs correspond to the time bin labelled with “Bunch crossing 1 (particle hit)”. This means – if there is a

particle hit in this time bin, the hit address will be shifted out during “Bunch crossing 1 data” interval, about 1.75 bunch crossings later.

9Reading out hits, we can distinguish the following cases:

1) No hit in the bunch crossing 1 bin:
   In this case ParityOut, HitOut1 and HitOut2 are zero. The addresses are invalid – probably all zeros.
2) One hit in the bunch crossing 1 bin:
   In this case ParityOut = 1, HitOut1 = 1 and HitOut2 = 0. The address of the hit is sent via the DataOut1 channel – Bits Addr1(5:0). The address is Grey coded according to Table 2.
3) Two hits in the bunch crossing 1 bin:
   In this case ParityOut = 0, HitOut1 = 1 and HitOut2 = 1. The addresses of the hits are sent on both channels - DataOut1 and DataOut2. The addresses are Gray coded according to Table 2.
4) Three hits in the bunch crossing 1 bin:
   In this case ParityOut = 1, HitOut1 = 1 and HitOut2 = 1. The address on the second channel corresponds to second hit. The address on channel one is in principle invalid – it is bitwise OR of addresses of hit 1 and 3. Gray coding will preserve a valid address if 1 and 3 belong to one cluster.
5) Four hits in the bunch crossing 1 bin:
   In this case ParityOut = 0, HitOut1 = 1 and HitOut2 = 1. This case cannot be distinguished from case 3.

Address table						
RO cell number	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	1
3	0	0	0	0	1	0
4	0	0	0	1	1	0
5	0	0	0	1	1	1
6	0	0	0	1	0	1
7	0	0	0	1	0	0
8	0	0	1	1	0	0
	0	0	1	1	0	1
…						
	0	0	1	0	0	1
15	0	0	1	0	0	0
16	0	1	1	0	0	0
	0	1	1	0	0	1
…						
	0	1	0	0	0	1
31	0	1	0	0	0	0
32	1	1	0	0	0	0
33	1	1	0	0	0	1
34	1	1	0	0	1	1
35	1	1	0	0	1	0
	1	1	0	1	1	0
…						
	1	1	0	1	0	0
40	1	1	1	1	0	0
41	1	1	1	1	0	1
42	1	1	1	1	1	1
43	1	1	1	1	1	0

Table 3: RO Cell address table (Gray encoded)

Test device description

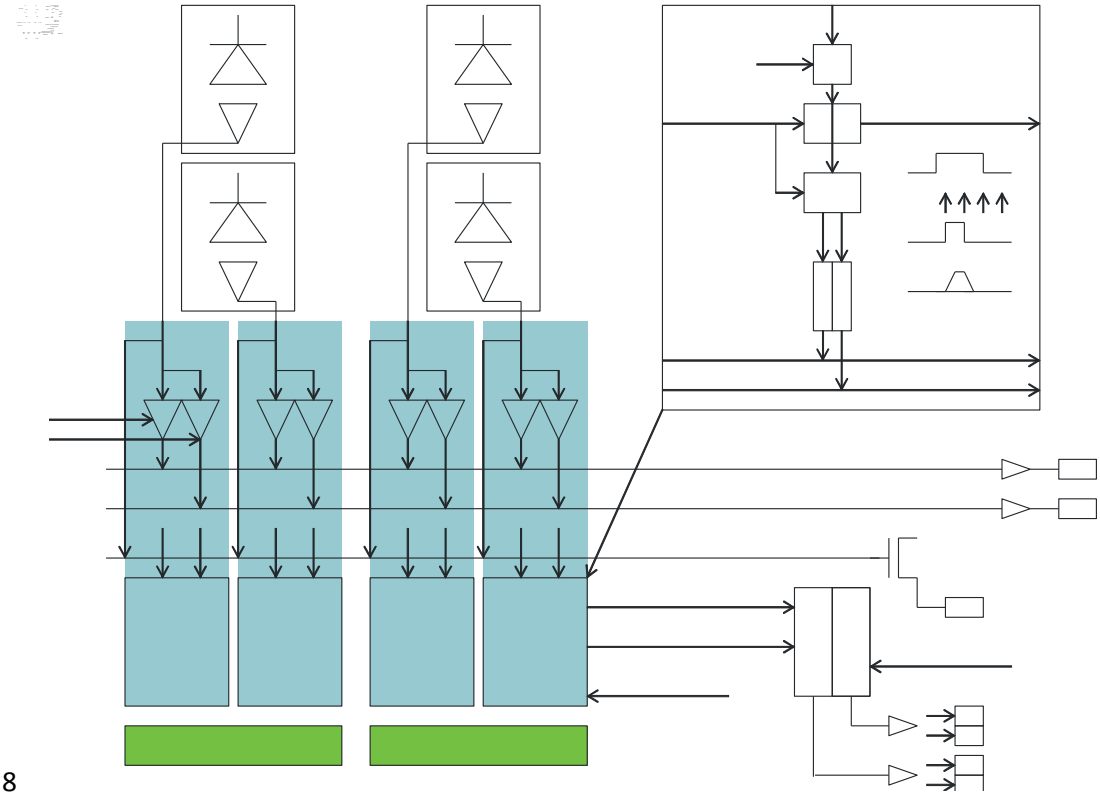
The chip holds two types of test devices: One big-diode, sized like the active pixel cells, and 9 test diodes in a 3x3 array. To use the test devices and not introduce unknowns, all power should be connected and VDDA/VDDA, as well as substrate should be powered up. Yet, the chip doesn't need to be in a configured state, nor receive any clocks.

BigDiode

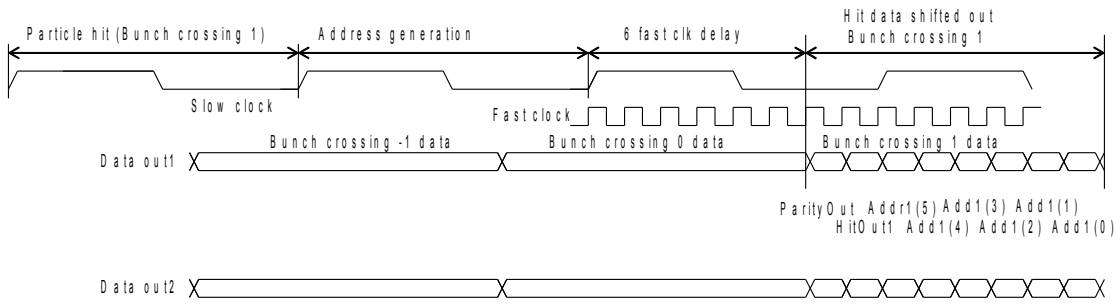
One test pixel (Test pix in Figure 1) of the same size as the active pixels (40 µm x 400 µm). This pixel does not contain any electronics inside the deep n-well. The diode is connected to a dedicated pad.

Test Diode Array

Nine test- n-well diodes (diode size 33 µm x 33 µm, matrix: 3x3) with the possibility to connect the middle diode and the outer diodes to three dedicated pads (Test Diode in Figure 1).



8 8Table



29 999T

est MOSFETs

Three MOSFETs (NMOS-linear, NMOS-enclosed and PMOS-linear) with the drains connected to dedicated pads for the measurement of radiation hardness (Test FETs in Figure 1). (The gates are connected to pads Th1)

Stuff to be added below