

# ATLAS CMOS Strip Testing

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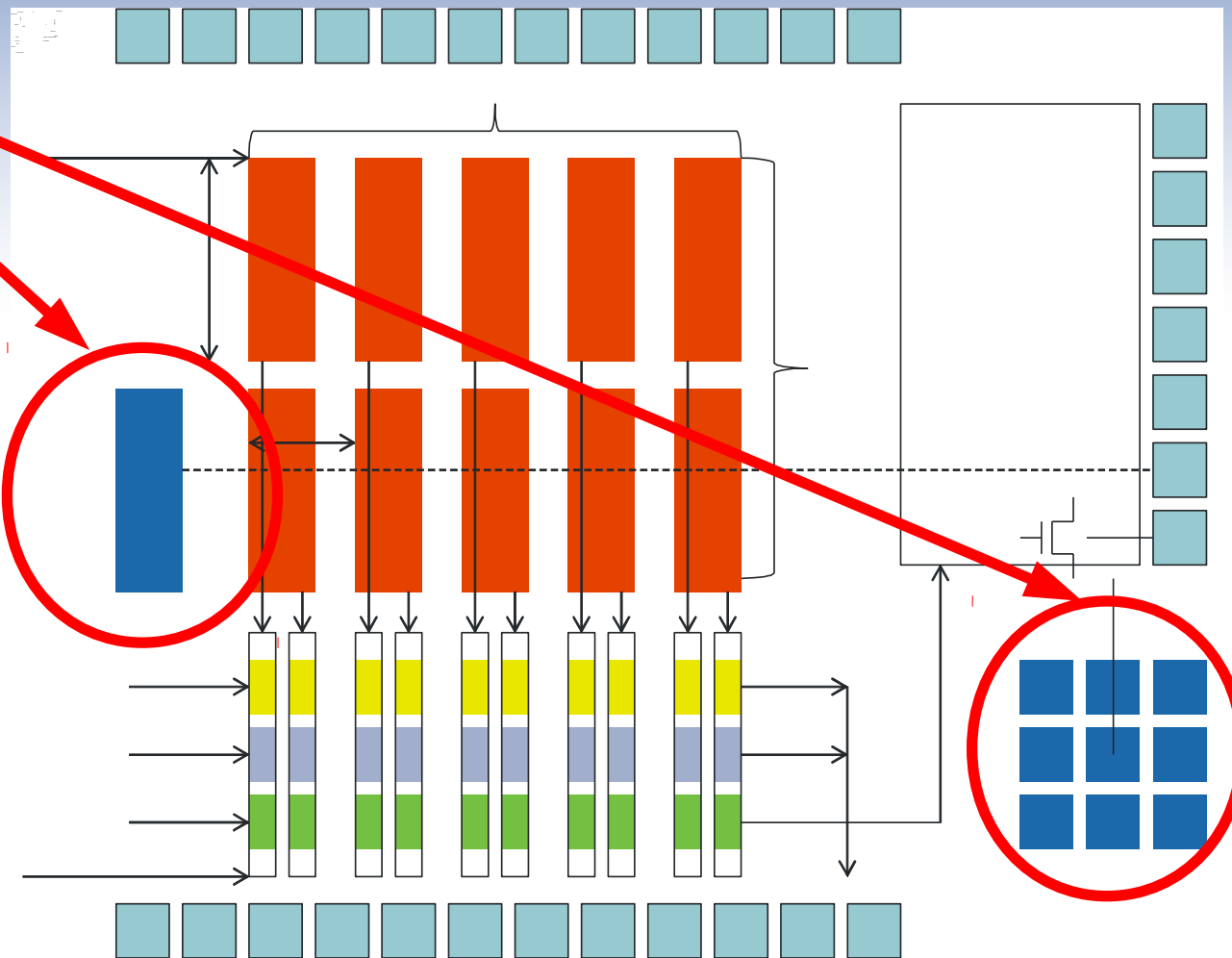


# HV Strip Test sensor

- Ivan Peric has submitted HV strip test structure for us
- These now came back
- Jaya John has designed a daughter board and a motherboard for these
  - Four daughter boards went to Geneva to get them bonded
  - Motherboard is in the works
- Jens has compiled a document describing the details of this chip
  - <https://twiki.cern.ch/twiki/bin/viewauth/Atlas/H35StripTestChip>

# Chip Overview

Passives



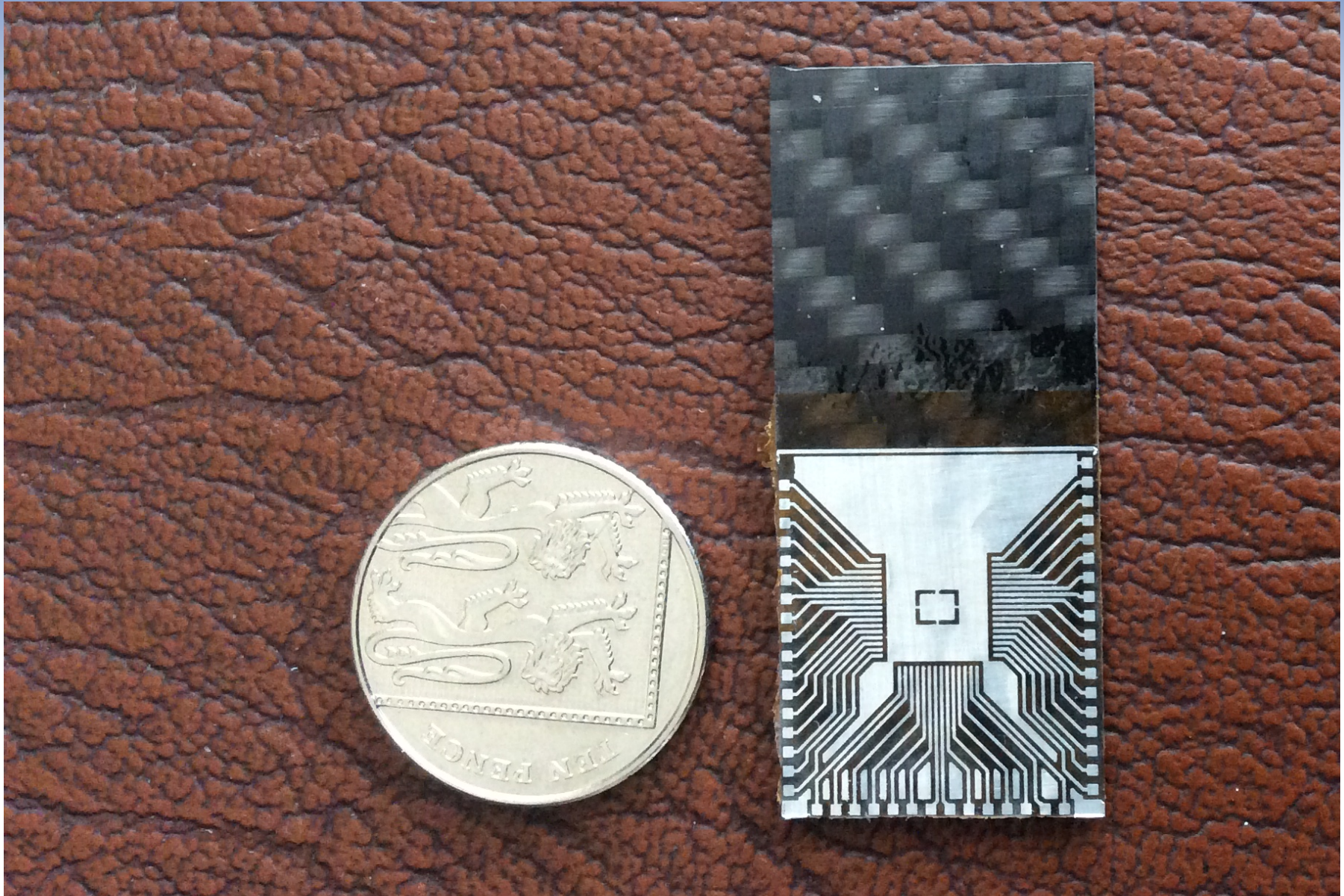
# Testing the passive structures

- Diodes and Transistors
  - Very basic setup required
- **Note:** Jens says:
  - requires good preamps like Amptec 250/250CF
  - **CAUTION:** Structures have no ESD protection at all
- Would characterize these devices
  - Build up experience
  - Measure noise
- (Limited) Irradiation campaign
  - Measure radiation damage to structure





# The daughter board



# Testing the active array

- Needs “real” DAQ
  - Firmware being ported to ATLYS board
  - A bit further down the line
  - Once all hardware there, < 1 week for firmware
- Will allow more detailed tests
  - Sources
  - Laser
  - Beam (?)
- And of course Irradiation

# Plans

- Have 35 chips
- Step 1
  - Passive structures (get them to work)
  - Initial studies done on probe stations or PCB's with low capacitance cables.
  - Both using fast amplifiers
- Step 2
  - Irradiating a subset (depending on supply)
- Step 3
  - Active array studies using bonding daughter board to mother board
- As many of these are very similar to CHESS
  - Headstart for testing CHESS



# Cont'd

- For more detailed studies
  - Particular irradiation studies
  - More chips needed
- Will find out how many and how much ...
- Discussion ?

# Distributing chips

Group	Amount	Plans
Oxford	10	DAQ, Irradiation, Testing
RAL	5	Testing
Santa Cruz	7	Testing
Glasgow	5	Testing
Ljubljana	5	TCT, Testing
DESY	3	Testing
Total	35	

**Comments, Corrections ?**