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Atlas Pixel Meeting
9th September 2014

Strip HR-CMOS

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STFC-RAL, UK
02/09/14

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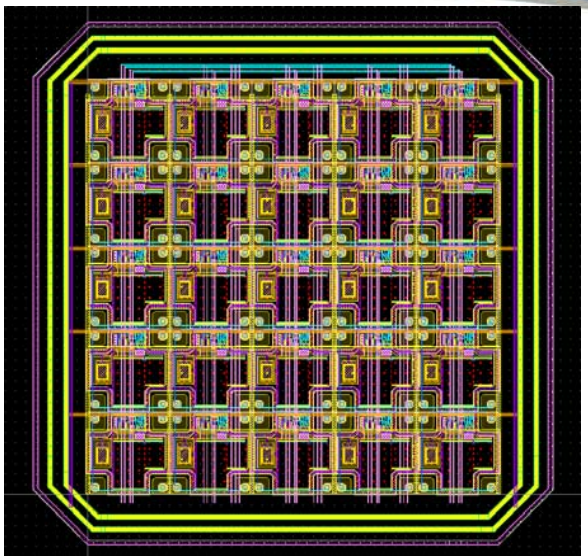
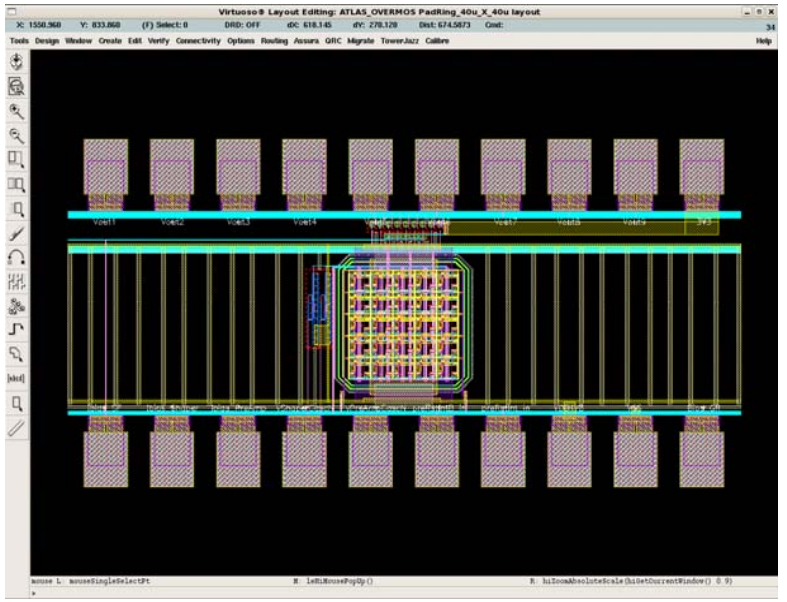
Status. 1

Active Pixel 5x5 arrays.

Hole collecting array completed for 40umx40um pitch



Integration in 20-pad test structure completed. Post-layout checks in progress.



In parallel pixels with different Y-pitches, i.e. 80, 120, 200, 400 and 800, have been designed.

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Status. 2

Design review for full chip planned for mid September.

Non-standard wafers (see previous meeting's slides) already bought as they are on long lead times

Paperwork between DESY and STFC in progress. Awaiting confirmation from DESY.

From last week's action.

- Fill in HR-CMOS part of the specification document. Still ongoing. Finalising arrays and pad layouts.

- To look into adding test transistors and passives to TJ chip design. The best strategy, also because of existing test kit, would be to re-manufacture the same array on the new substrates. CERN has agreed to provide the GDS.