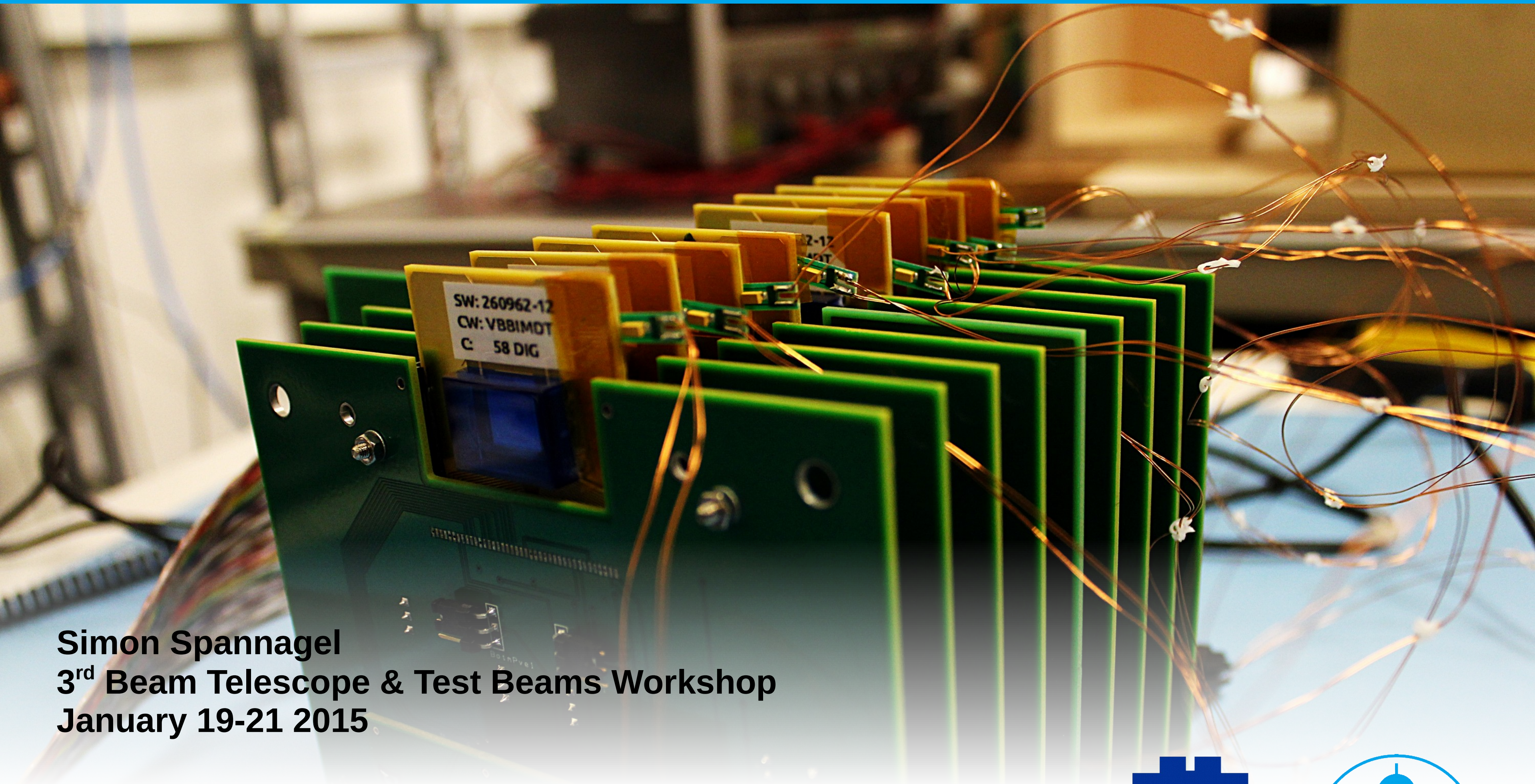
High Rate Test Beam w/ CMS Pixel Telescope



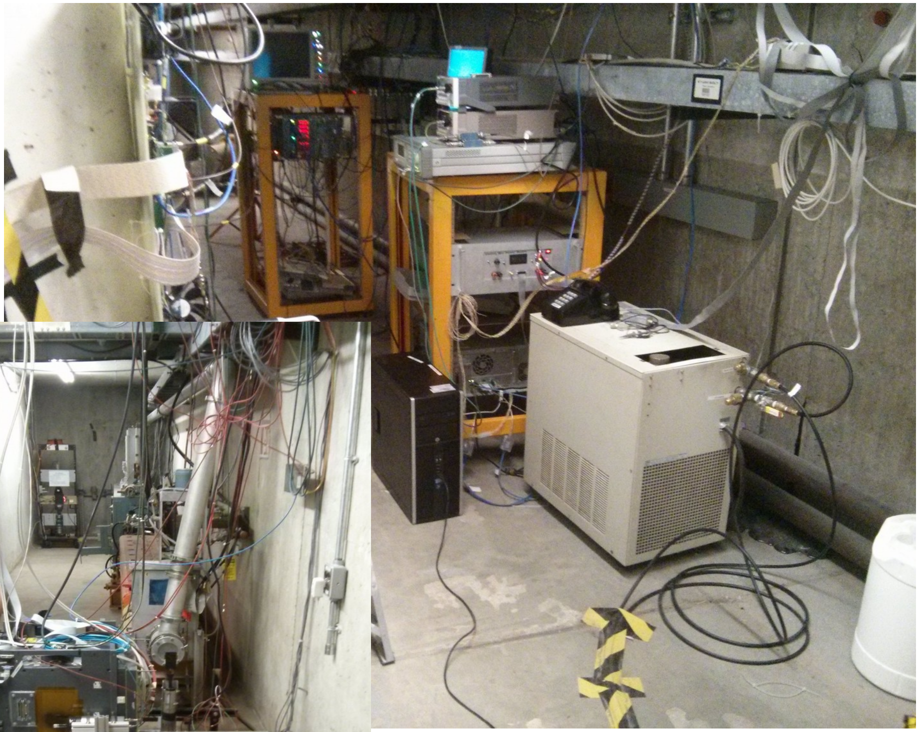
Simon Spannagel
3rd Beam Telescope & Test Beams Workshop
January 19-21 2015

HELMHOLTZ ASSOCIATION

DESY

Outline

- CMS Phase I Upgrade
- High Rate Beam Test
- The FTBF Beam
  - MTest Beam Environment
  - Beam Structure
- The Beam Telescope
  - The Readout Electronics
- QIE: Beam Intensity
  - Trigger Configurations
- DQM, Analysis Software
- Preliminary Results



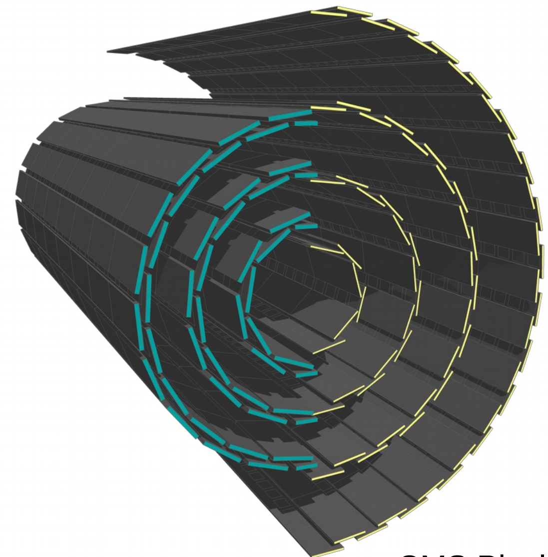
Phase I Upgrade of the CMS (Barrel) Pixel Detector

> Maintaining & extending tracking efficiency at higher luminosities

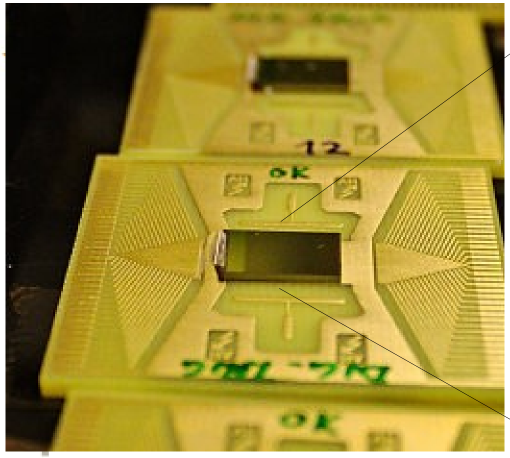
> 3 end disks, 4 barrel layers

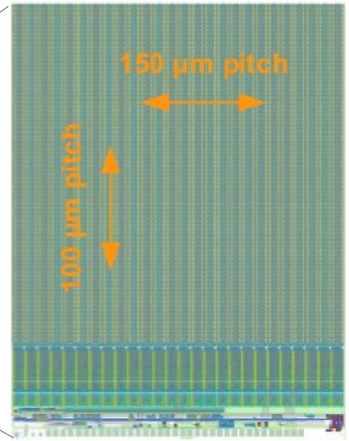
> New readout chip (ROC) to cope with occupancy & data rates

- Additional buffer cells
- Reduced readout dead time
- Fully-digital 160MHz data transmission
- Reduced threshold



CMS Pixel Phase I TDR





> New ROC is incremental upgrade of present chip

> Is able to operate w/ flux of up to 250MHz/cm^2

High Rate Beam Test

> Confirm the simulated ROC performance at fluxes similar to HL-LHC

- Up till now only tested in lab with calibration pulses
- See tracking performance and correlation of devices in the beam

> Two beam telescopes with 8 ROC planes each

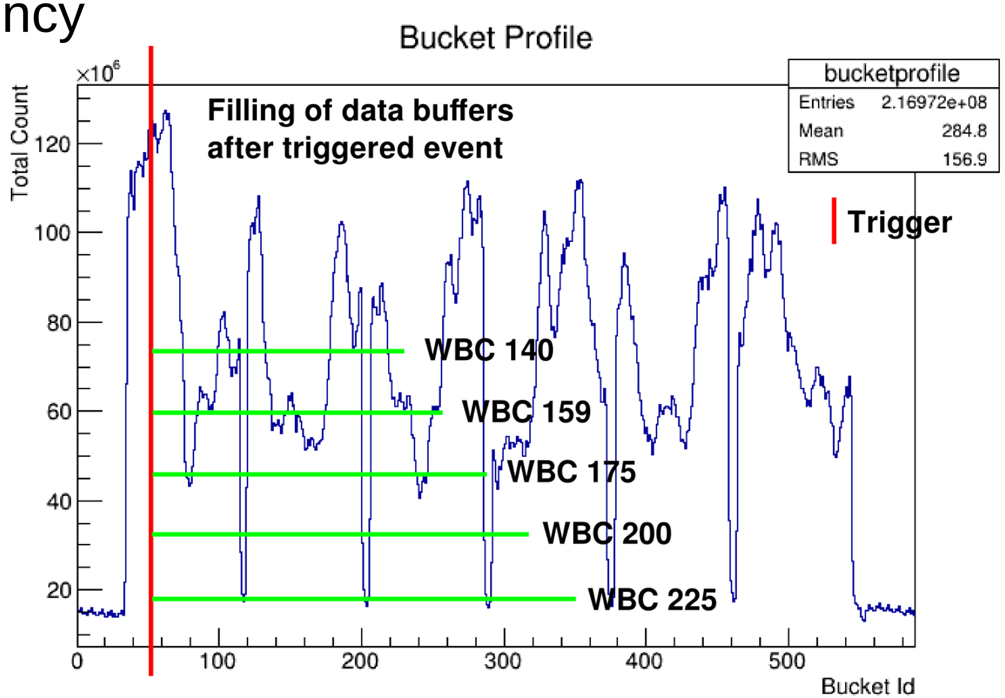
- Pixel planes orthogonal to the beam: focus on timestamp buffer issues, small clusters
- Inclined planes with respect to beam: focus on data buffers, larger clusters

> 4th high rate beam test

- CERN H4Irrad, summer 2012: beam line only designed for irradiation, system tests
- PSI pi@320MeV, summer 2013: commissioning of new DAQ system, integration
- FNAL MTest, October 2013: issues with accelerator (MI) delivering requested beam
- FNAL MTest, March 2014: commissioning of trigger system, successful data taking

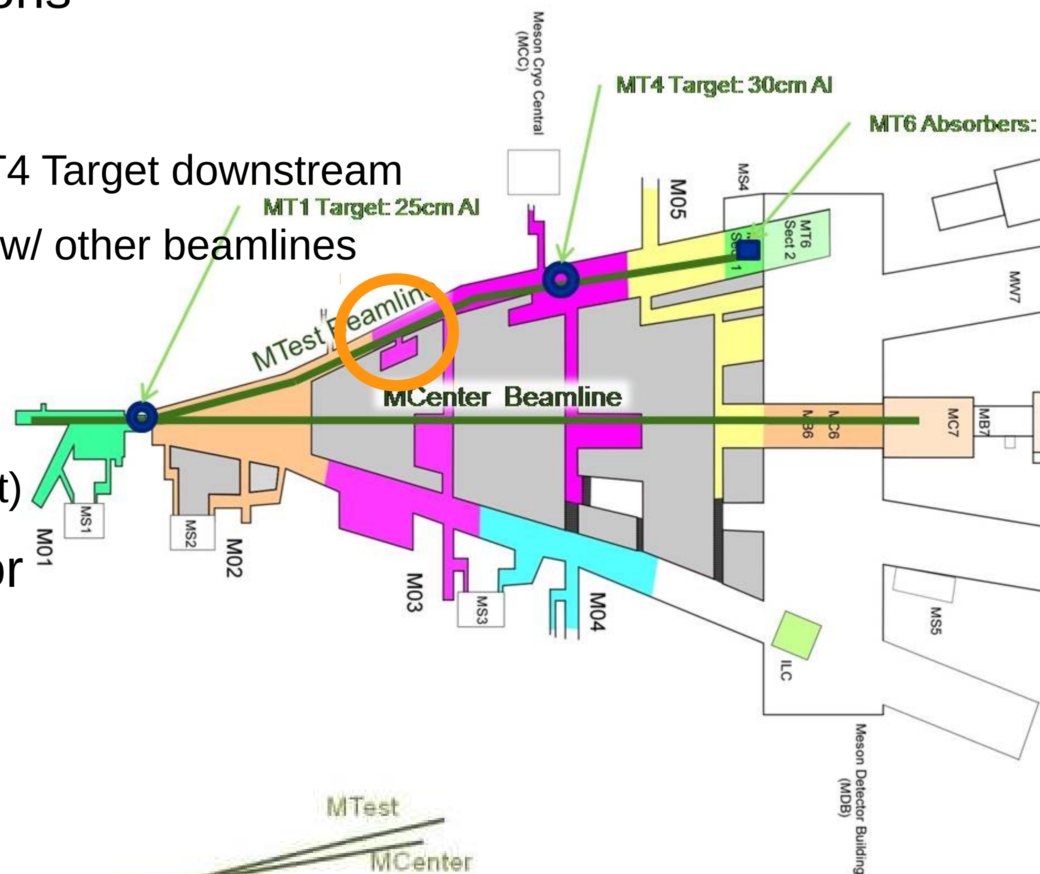
High Rate Beam Test: Challenges

- Difficult beam environment (primary beam not used for tracking so far)
- Complex test setup (boards, telescope, QIE...) running on different clocks (CMS @ 40 MHz, MI @ 53 MHz)
- Measurements of correlated parameters,
- Efficiency depends on history & future of triggered event, depending on configured latency



MTest Beam Environment

- > Possible MT3 Beam Configurations
- > 120 GeV proton beam
  - primary beam from Main Injector, MT4 Target downstream
  - High intensity, total MI beam shared w/ other beamlines
- > 60 GeV π- beam
  - Secondary π beam from MT1 target
  - Very low intensity (~1 proton / bucket)
- > Spill extraction from Main Injector
  - one spill per 60sec
  - Spill duration ~4sec



also see:
Status of the FNAL Testbeam Facility
Tue, 16:50h

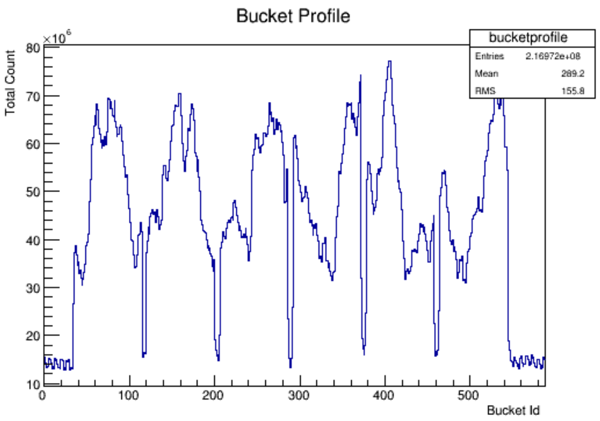
Beam Structure

> Spill (4sec) is structured
  - direct extraction of 369k turns from Main Injector
  - Turns: bunch structure with 588 buckets

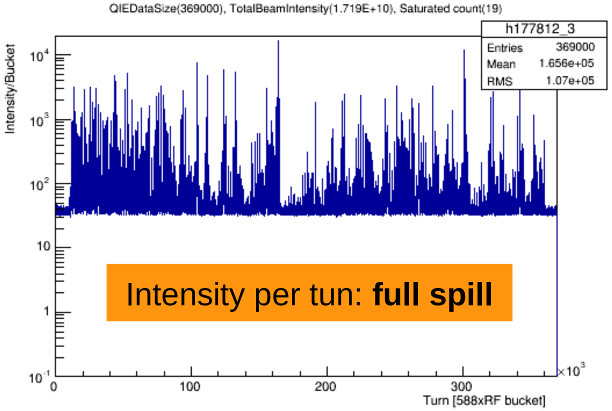
> MI frequency
  - 53MHz → 1 bucket ~ 18.8ns
  - Ramping during acceleration (60sec)
  - not suited for synchronized operation

> Out of 588 buckets per turn 504 filled
  - 6 Booster batches x84 buckets

σ ~ 6mm (HORZ/VERT)

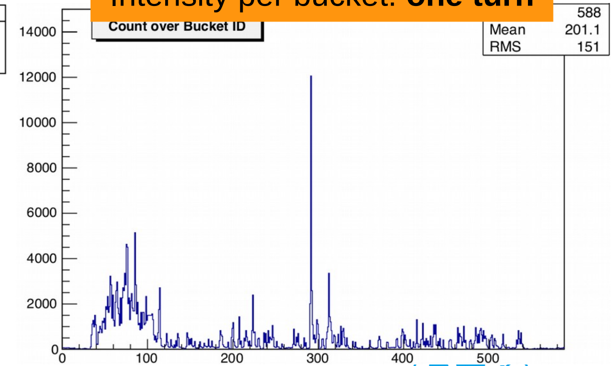


Intensity per bucket: **Σ all turns**



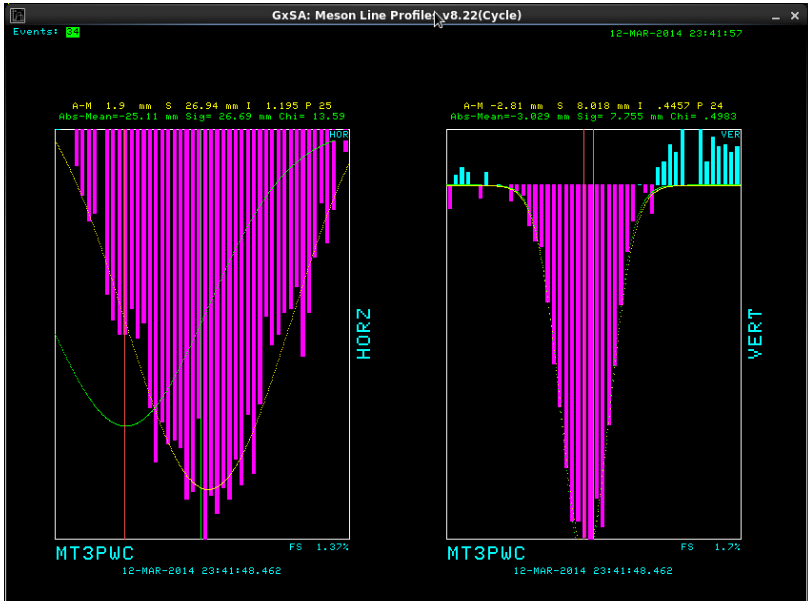
Intensity per tun: **full spill**

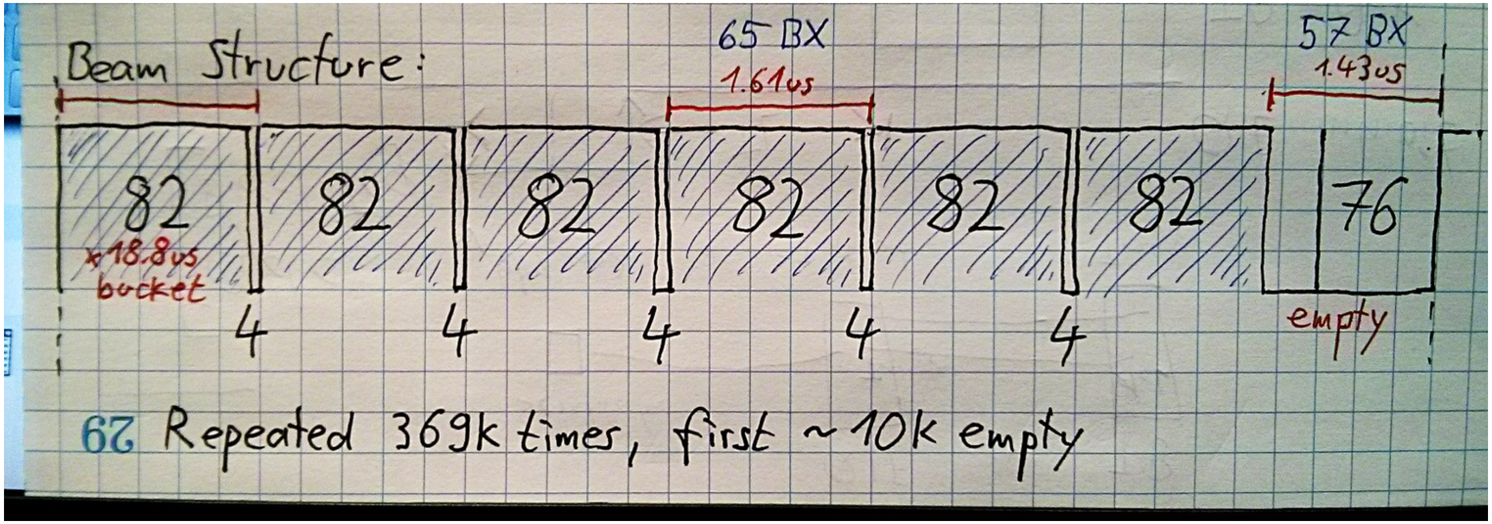
Intensity per bucket: **one turn**



Beam Structure ctd'

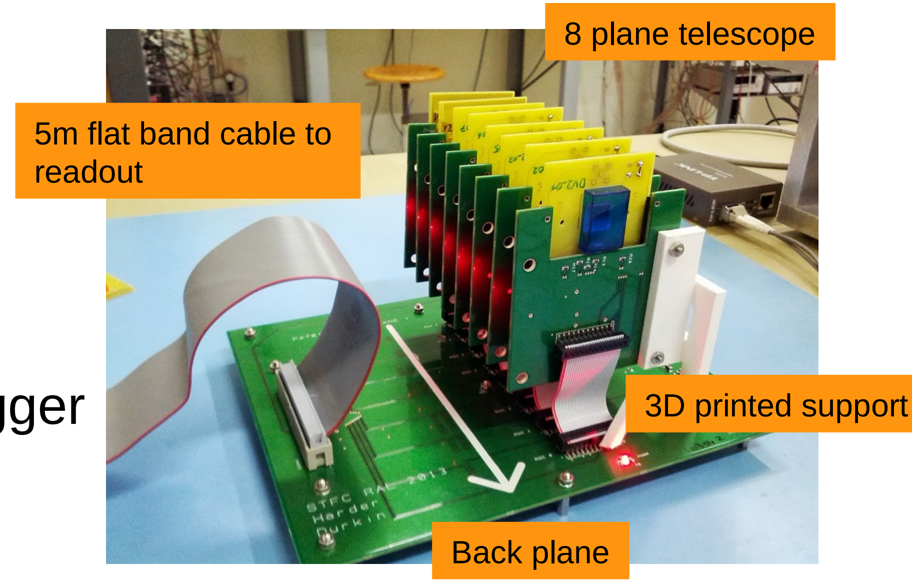
- 60 GeV π- beam profile broader
- Averaged around 1proton / bucket
- Can be used for calibration of the QIE data to single protons

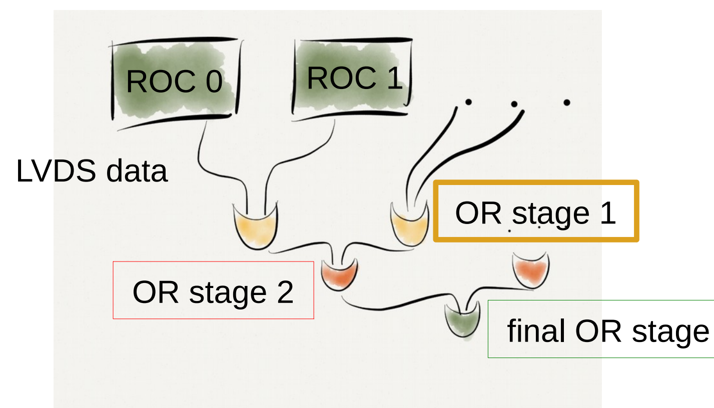




The Beam Telescope

- 8 planes of CMS pixel chip modules
  - 7 planes used for tracking
  - 1 plane used as DUT (variable)
- Back plane board responsible for trigger and clock distribution
- Equipped with several stages of concentrator chips (OR-gates) to create one data stream from all ROCs
- Several signal drivers ensure a clean signal transmission over a 5m flat band cable

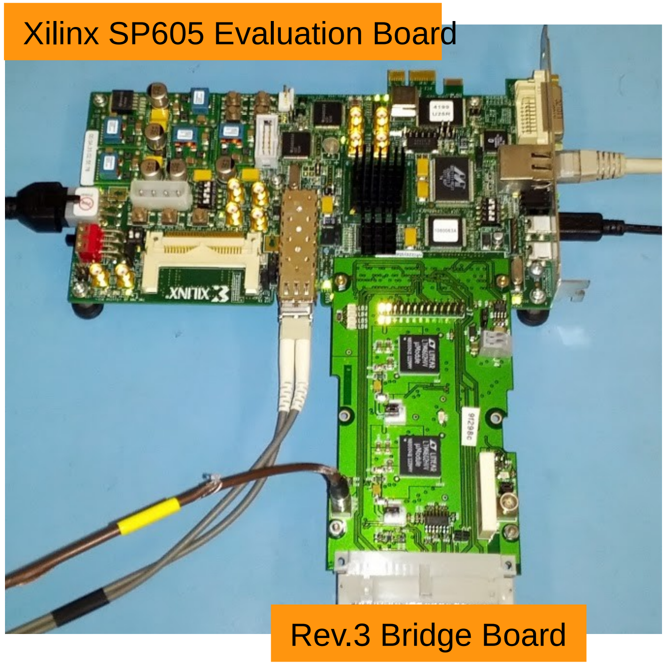




The Readout Electronics

> Commercial available Xilinx SP605 evaluation board
  - Xilinx Spartan-6 FPGA, RAM,
  - 320MHz or 160MHz sampling frequency

> IPBus/uHAL firmware data transmission
  - First prototype for future CMS DAQ electronics



> Additional Bridge Board
  - Interface card for SP605 to telescope
  - Controls power for ROCs (analog and digital supply voltage)
  - Trigger input to DAQ system
  - Sensor Bias HV relay

QIE: Beam Intensity Measurement

> CMS Charge Integrating Encoder chip
  - Readout chip of the CMS HCAL
  - Able to integrate and register charge signals bunch-per-bunch

> Fermilab board, running on 53MHz Main Injector clock

> Gets signals from
  - The accelerator, can separate turns and buckets
  - A scintillator (10x10mm) in the proton beam

> Beam intensity from scintillator is recorded separately for every single bucket (18.8ns)

> Allows calculation of history and future of triggered event in the ROC buffers

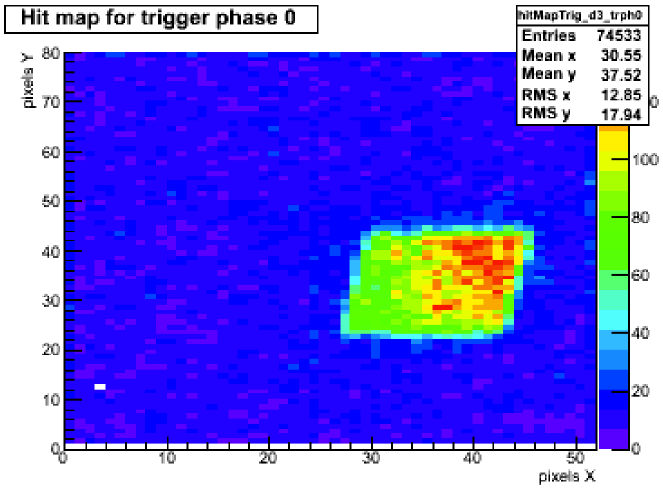
> Allows various trigger schemes (see next page)

Trigger Configurations

> Three trigger sources available and used

> Scintillator trigger

- 2x2x2mm small scintillator in front of telescope
- Very good alignment



> QIE threshold trigger

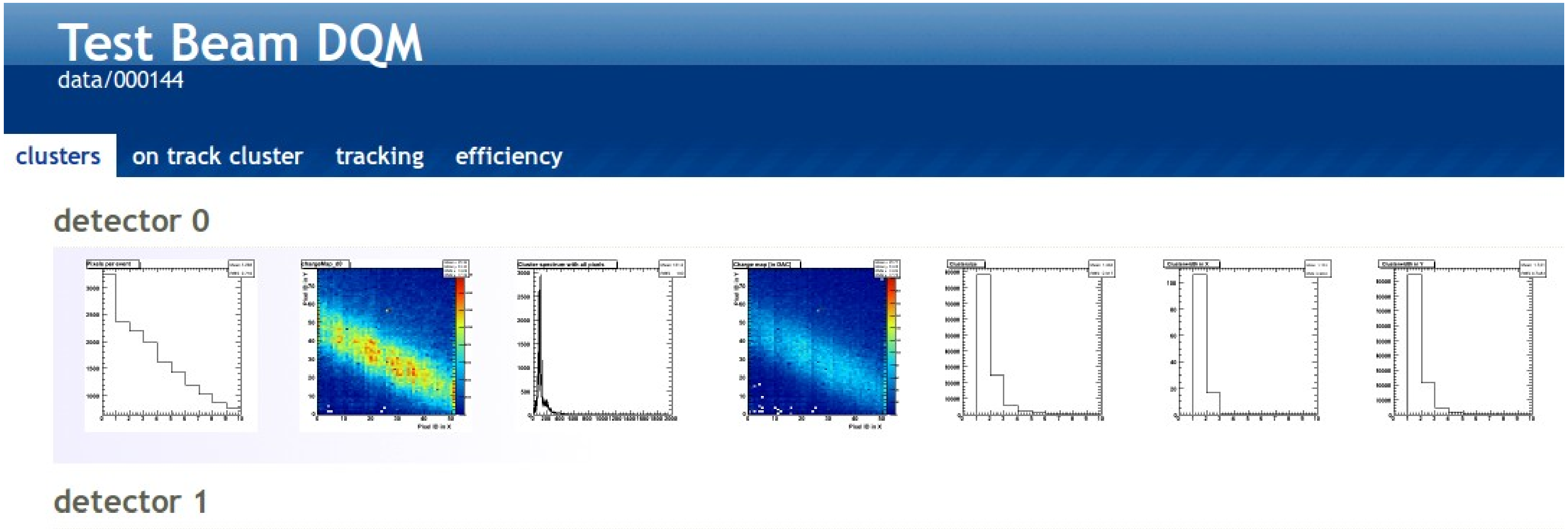
- trigger issued when bucket intensity is above threshold (information from 10x10mm beam scintillator)

> QIE cyclic trigger

- trigger signal synchronous with the beam, one trigger per MI turn
- fixed frequency ~90kHz
- Position within the turn (so: bucket number) selectable

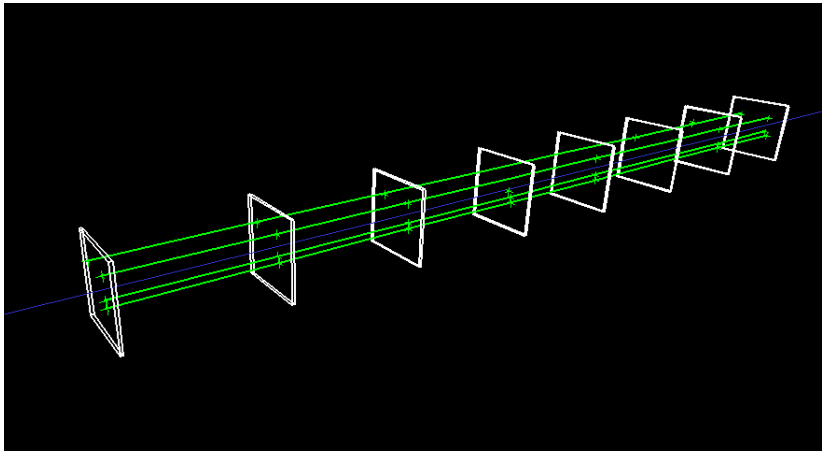
DQM & Analysis Software

- EUTelescope used for data analysis and data quality monitoring
  - Fully-configurable modular framework for beam telescopes
  - Provides processors for clustering, alignment, track fitting, etc.
- DQM runs through a simplified analysis chain and exports root histograms to a website
  - Quasi-online since data has to be downloaded from test boards & transfered to CERN

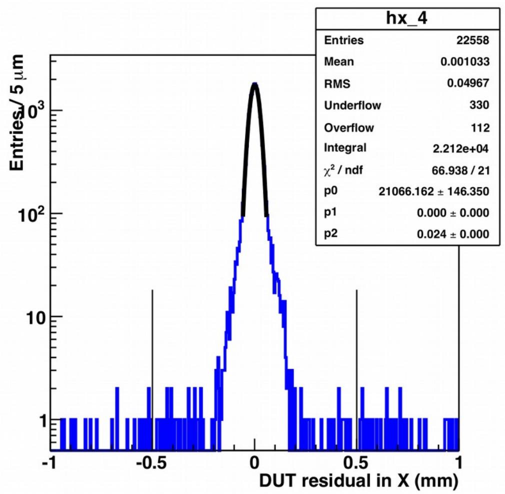


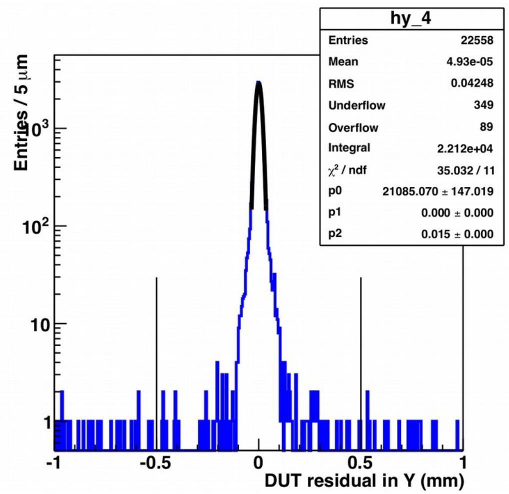
Preliminary: Performance

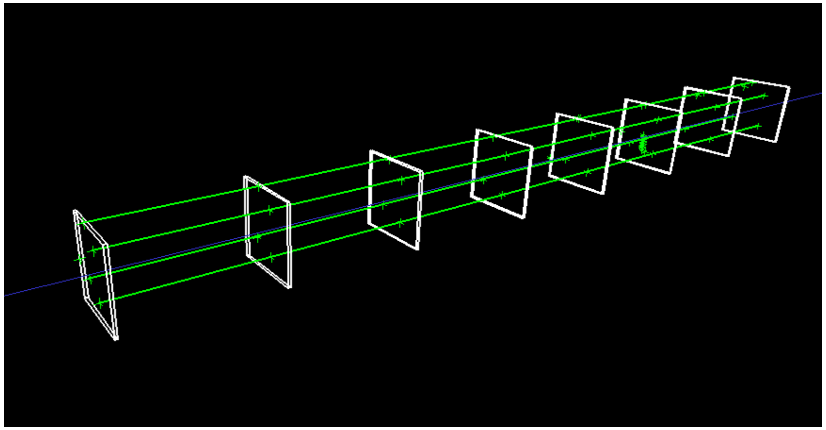
- Straight line fit (120GeV p), DUT can be selected (usually plane 4)
- Alignment w/ Millepede II processor
- Overall tracking performance is good



- DUT residual for inclined telescope:
  - 24µm across columns (x axis)
  - 15µm across rows (y axis)





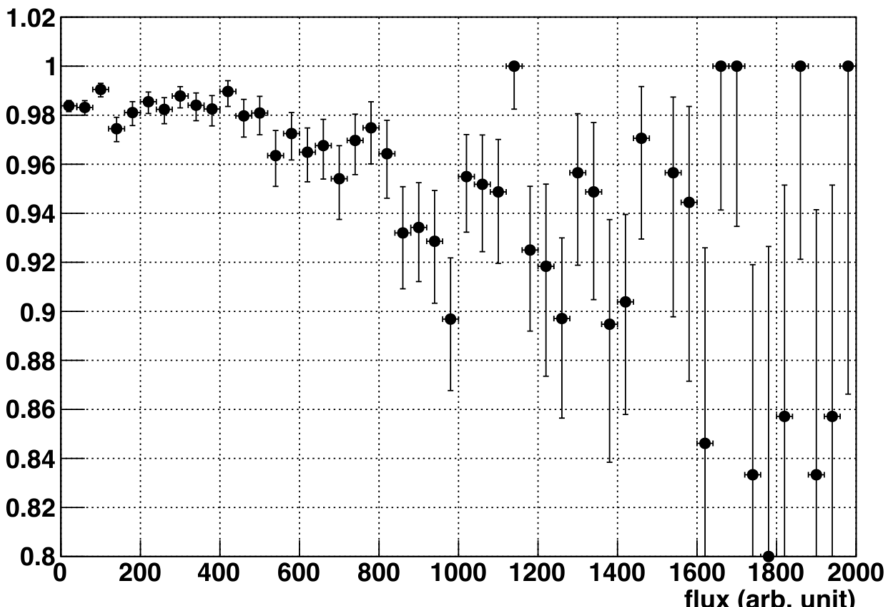


DESY

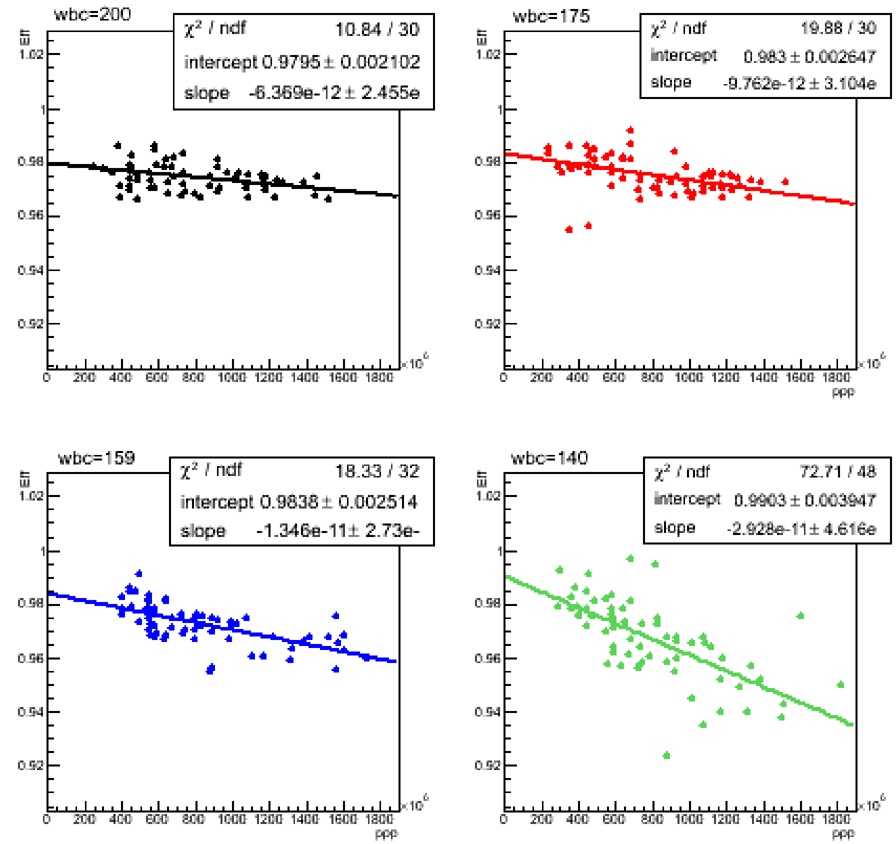
Preliminary: Performance ctd'

- Efficiency values for different latencies
- Values shown for the tilted telescope
- Challenges:
  - Track multiplicity
  - Correlation tracks & QIE charges

QIE triggered @ bucket #270 (middle of spill)
tilted telescope

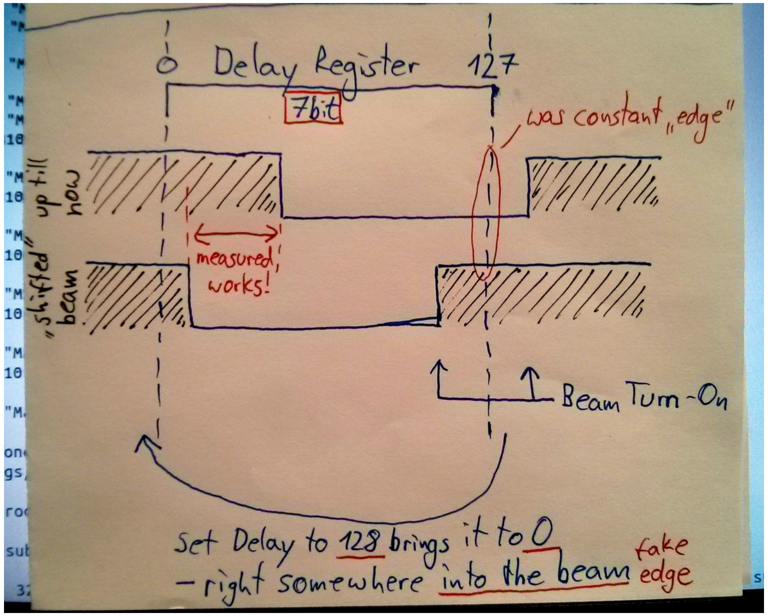


Efficiency as function of flux, one spill



flux averaged over spill by using total proton count

Thanks.



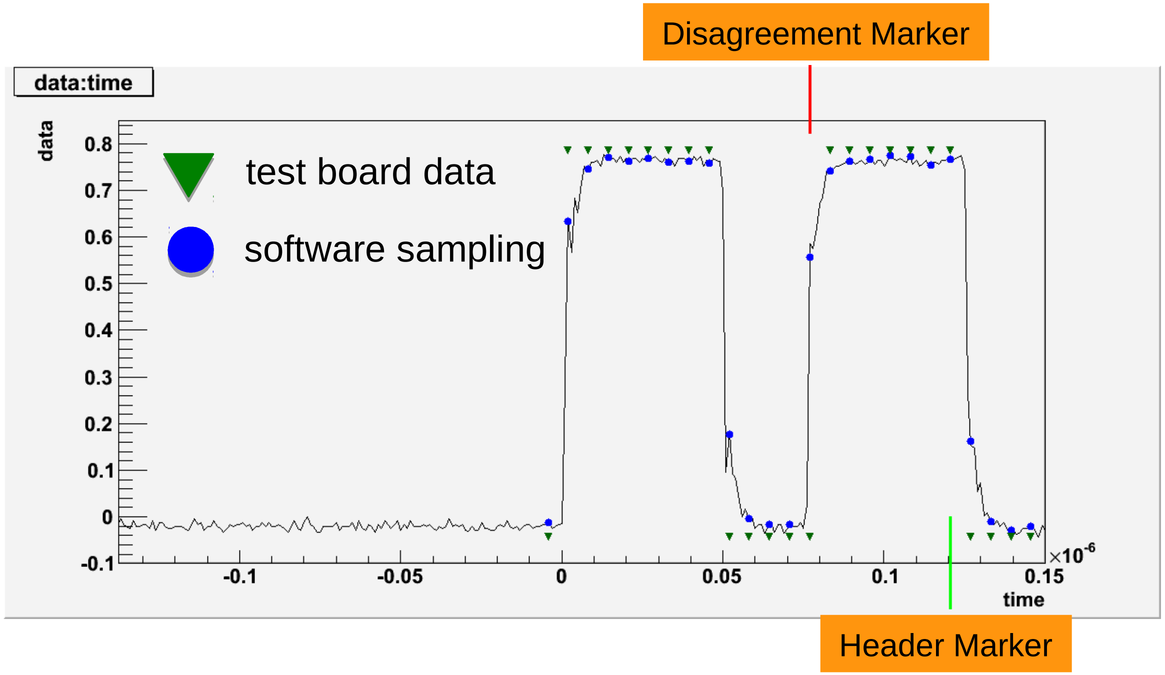
0
Delay Register
127
7bit
was constant „edge"
„shifted" beam
up till now
measured, works!
Beam Turn-On
Set Delay to 128 brings it to 0
– right somewhere into the beam
fake edge

People involved

- Spokesperson
  - Anna Elliot-Peisert (CERN)
- FNAL & FTBF
  - Lenny Spiegel, Aria Soha
- Visiting team
  - Imtiaz Ahmed, Ulysses Grundler, Andreas Kornmayer, Kristian Harder, Tomas Hreus, Rong-Shyang Lu, Stefano Mersi, Simon Spannagel
- Remote support from Taiwan
  - Yeng-Ming Tzeng (Jacky)
- Operational Readiness Clearance document
  - Kevin Burkett
- SeaQuest (QIE) support
  - David Christian, Kazutaka Nakahara
- FCC support
  - Alan Prosser, Ryan Rivera, Lorenzo Uplegger

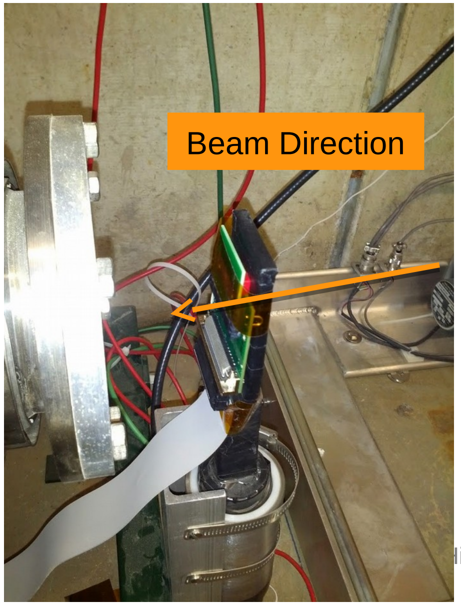
Readout Signal Sampling: Comparison to Scope Traces

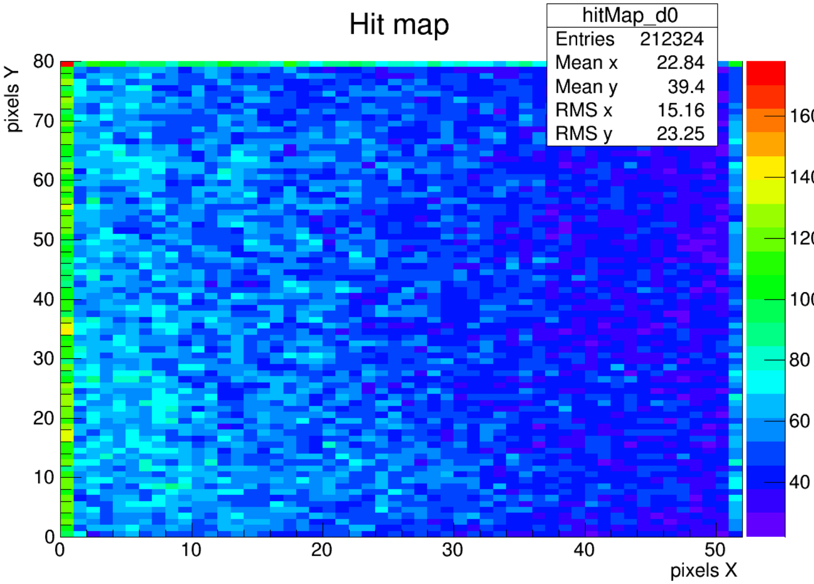
- Active differential probe connected to the data path as close as possible to the FPGA
- Sending periodic triggers, decoding the data simultaneously
- Stopping triggers as soon as an invalid header or invalid pixel address was detected, event data frozen on the scope.
- With an additional trace of the clock signal we created a software sampling



Data Taking using the DTB as DAQ System

- As cross-check a PSI DTB w/ single ROC has been put into the p beam
- Quick test in the last nights
  - no alignment with beam possible, no external triggers (not implemented in firmware)
  - HV limited to 90V by power supply used
- Random triggers w/ DTB pattern generator, no sync w/ telescope or QIE
- See beam spot, seems to work fine

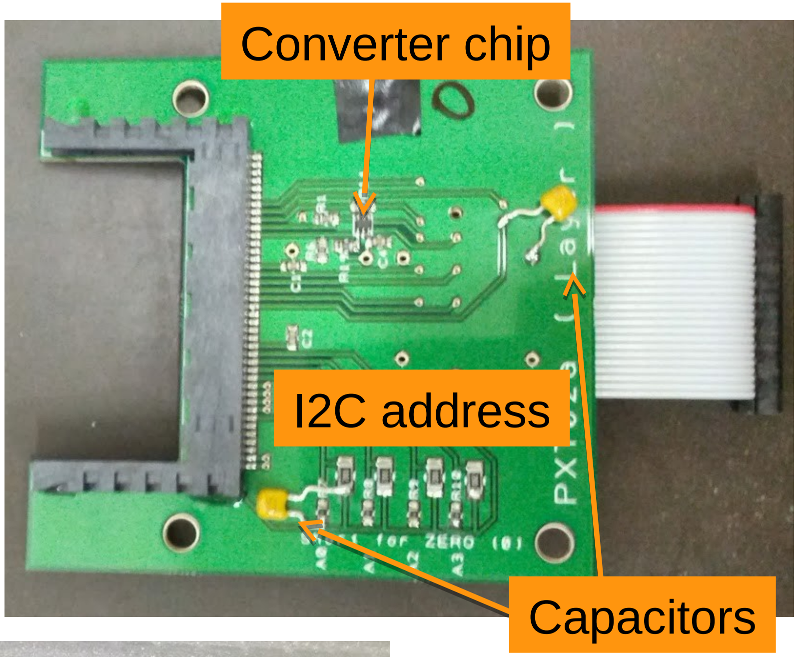




The Telescope Backplane Board

- Responsible for trigger and clock distribution
- One signal arrives from the test board and is fanned out on the back plane to all ROCs. To ensure that the signals arrive synchronous at all ROCs the signal paths where designed to be exactly the same length.
- Concentrates the data from all ROCs into one data stream
- The data of the ROCs is transmitted in LVDS. Three stages of concentrator chips (OR-gates) combine the data form all 8 ROCs into a single data stream.
- At both ends of the data transmission cable a signal driver ensures a correct transmission and termination of the signal.

The Telescope Plane PCBs & Chip Carriers



> Telescope Planes

- Commonly used 40pin SMD connector
- Configurable I2C address
- Capacitors to balance out fluctuations in analog and digital supply voltage
- LCDS-to-LVDS converter chip
- slightly asymmetrically terminated to cope with high impedance state of the ROC data output
- 26pin connector to back plane board

> Single ROC Chip Carriers

- DESY layout, slightly modified
- Added HV filter

Data Line Scope Trace (at FPGA input)