
# Trigger and Synchronization for Beam Tests

## High Rate
## Synchronous as well as Asynchronous



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# Introduction 1/2

- Two sorts of beam telescope
  - Homogeneous – all one technology and read-out.
    - Not considered here
  - In-homogeneous – Telescope of one technology, hosting a “device under test” (DUT)
    - EUDET/AIDA/etc. Beam telescope offered as a service.

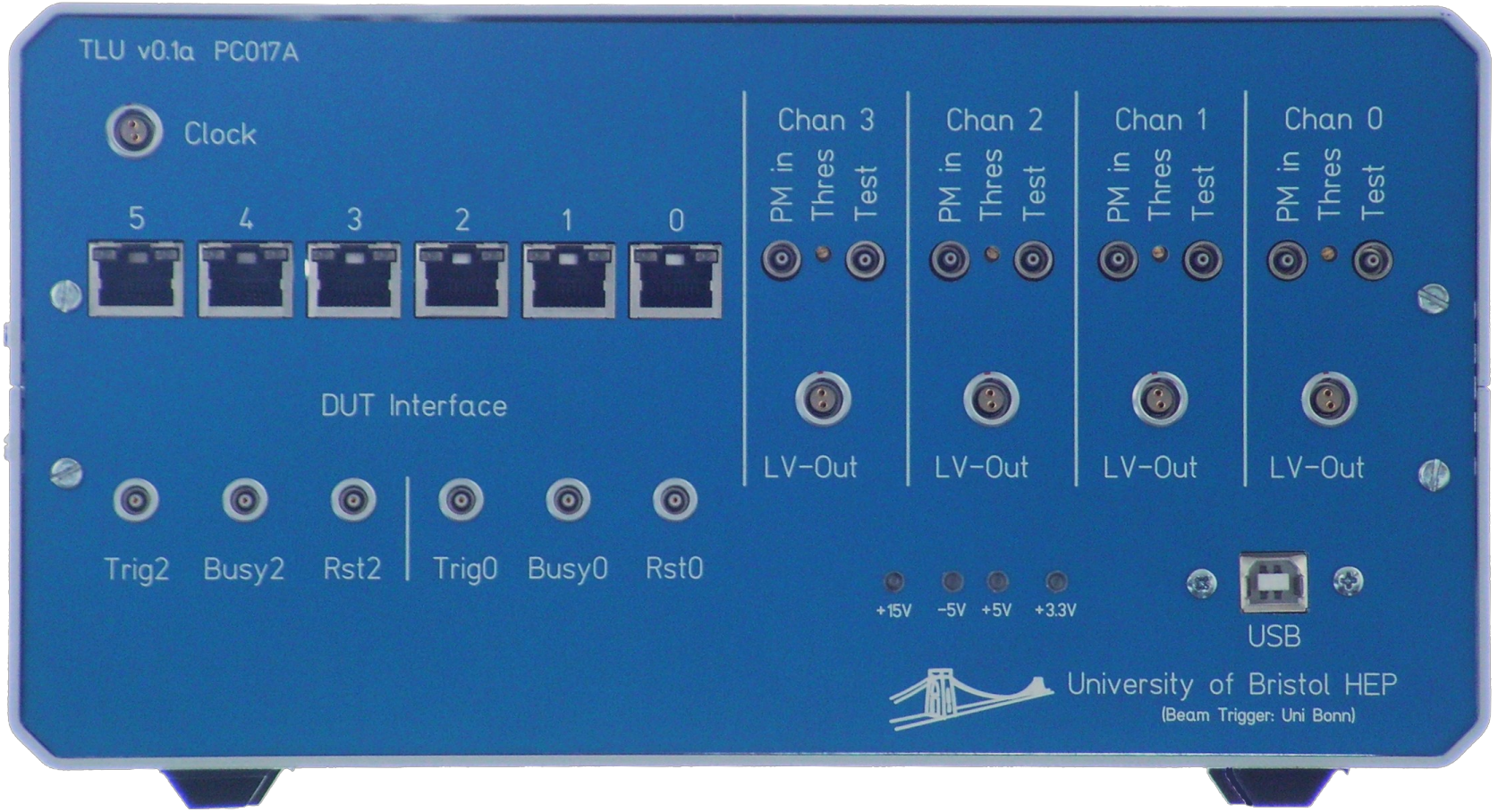
# Introduction 2/2

- For in-homogeneous telescopes ( operating with a DUT) need to correlate data from telescope and DUT.
- Different detector have different integration/sensitive times. E.g.
  - Continuously active ( e.g. MAPS , TimePix )
  - Triggered ( data only stored on receipt of trigger, e.g. LHC detectors )
- Different ways of sychronization
  - Triggers.
  - Shared clock.

# TLU Versions - EUDET

- EUDET
  - Uses COTs FPGA board with custom daughter-boards ( FPGA almost obsolete)
  - Asynchronous TLU and DUT clocks. Triggering modes:
    - Trigger/Busy handshake
    - Trigger only
  - Documentation at http://www.eudet.org/e26/e28/e42441/e57298/EUDET-MEMO-2009-04.pdf

# TLU Versions - EUDET

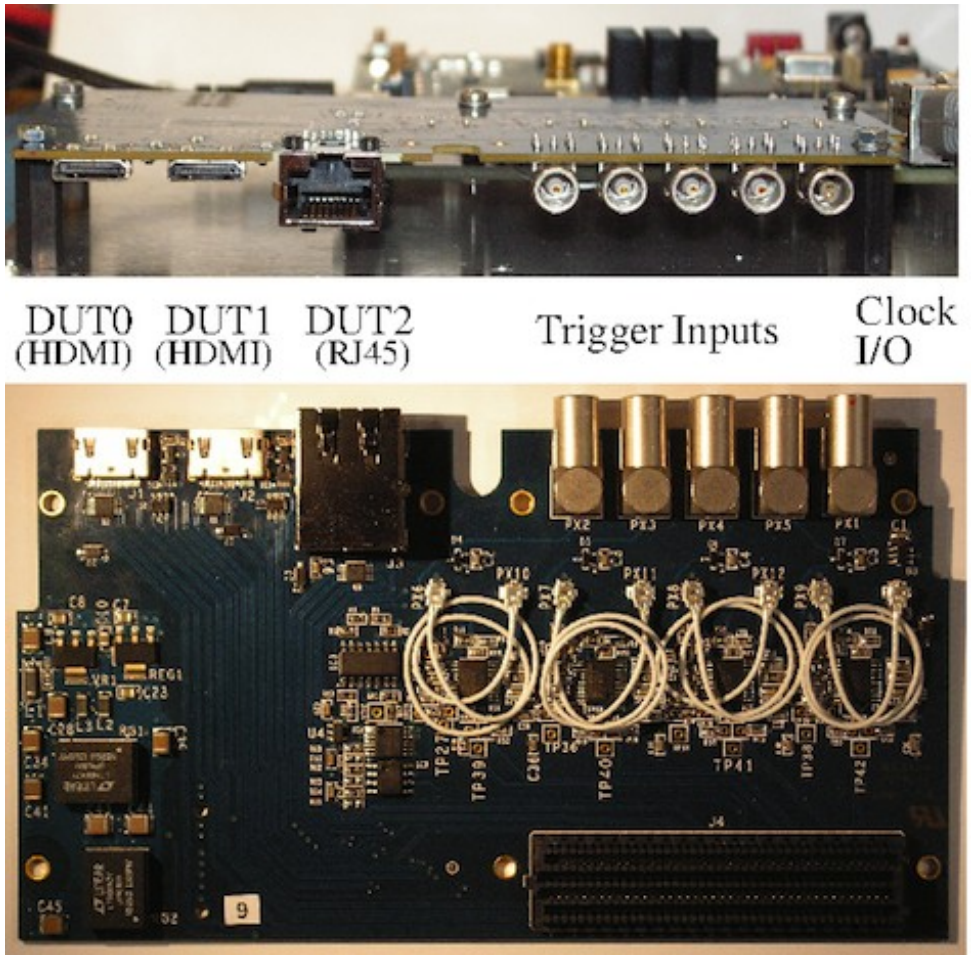


# TLU Versions - AIDA

- Allows synchronous (shared clocks) interface.
  - Allows higher trigger rate than trigger/busy handshake.
- Interface by Gigabit Ethernet.
  - Readout PC can be remote.
  - IPBus protocol (https://svnweb.cern.ch/trac/cactus/wiki)
- High rate discriminators ( > 10 MHz count rate)
  - Threshold and constant-fraction
  - Thresholds remotely controllable.
- Timestamps on each scintillator input
  - Timestamp granularity  800ps (c.f. 3.2ns on EUDET TLU)

# AIDA TLU - Hardware

- Implemented as double-width “FPGA Mezzanine Card” ( VITA 57 )
- Uses low-cost FPGA development board as carrier ( currently SP601, SP605 )
- Three interfaces for DUT ( 2x HDMI , 1x RJ45 )
- Four trigger inputs ( threshold + CFD )
- One clock I/O





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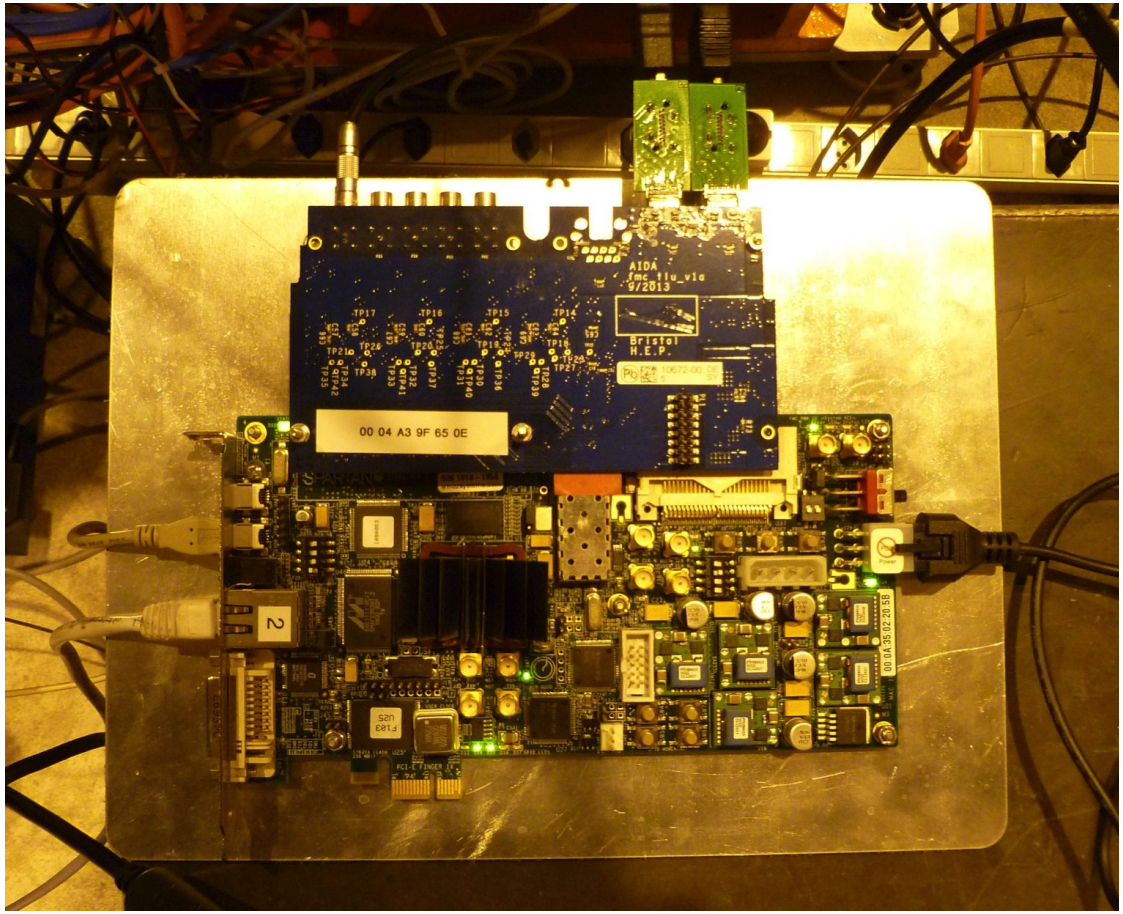
# Hardware

- Currently only as boards bolted to plate
- Design for box in progress



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# Hardware

- LVDS --> TTL converters exist.
- This example from NIKHEF

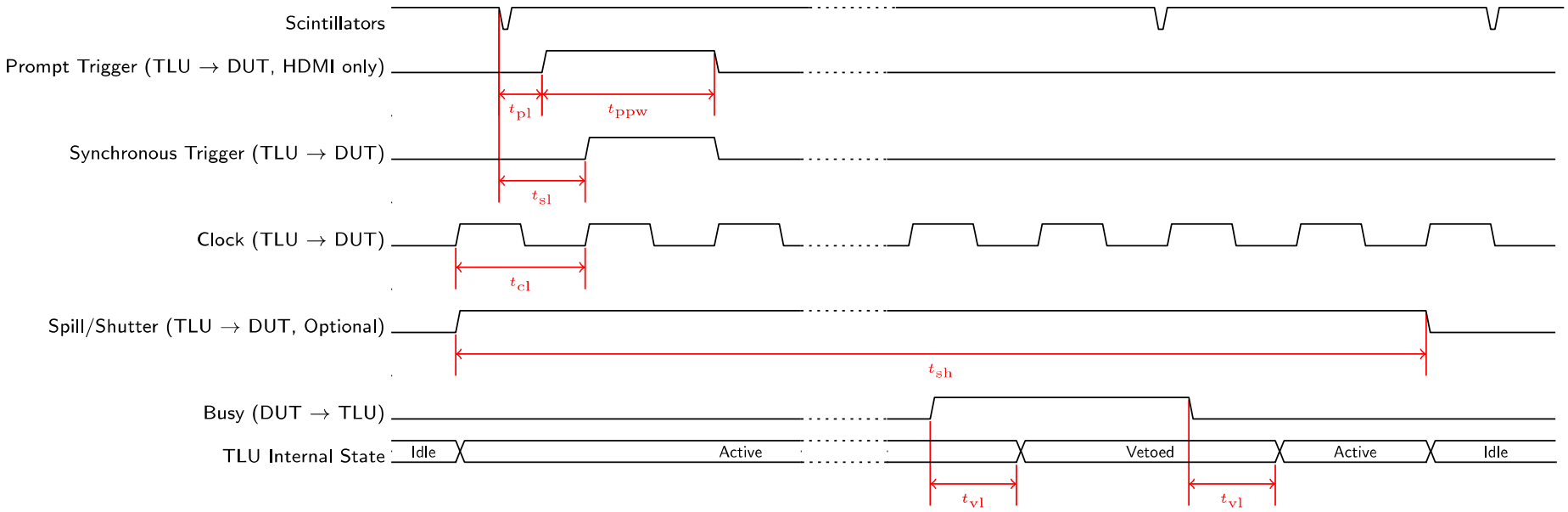
# AIDA TLU Documentation

- http://www.ohwr.org/projects/fmc-mtlu/wiki
  - Describes hardware , firmware , firmware-simulation
  - PCB layout in Cadence Allegro ( CERN libraries )
  - Firmware uses Xilinx ISE , needs Gigabit Ethernet Core if using 1000Base-T interface.
- Data format from TLU described at http://svn.ohwr.org/fmc-mtlu/trunk/documents/firmware/latex/AIDA_TLU_note.pdf

# Synchronous Interface

- Clock from TLU to DUT
  - Configurable frequency
- Trigger pulse only only clock cycle long
  - Trigger rate up to 40MHz ( though photo-multipliers will limit this )
- Busy from DUT to TLU
- Check synchronization from time-stamp of each trigger ( measured in clock cycles)

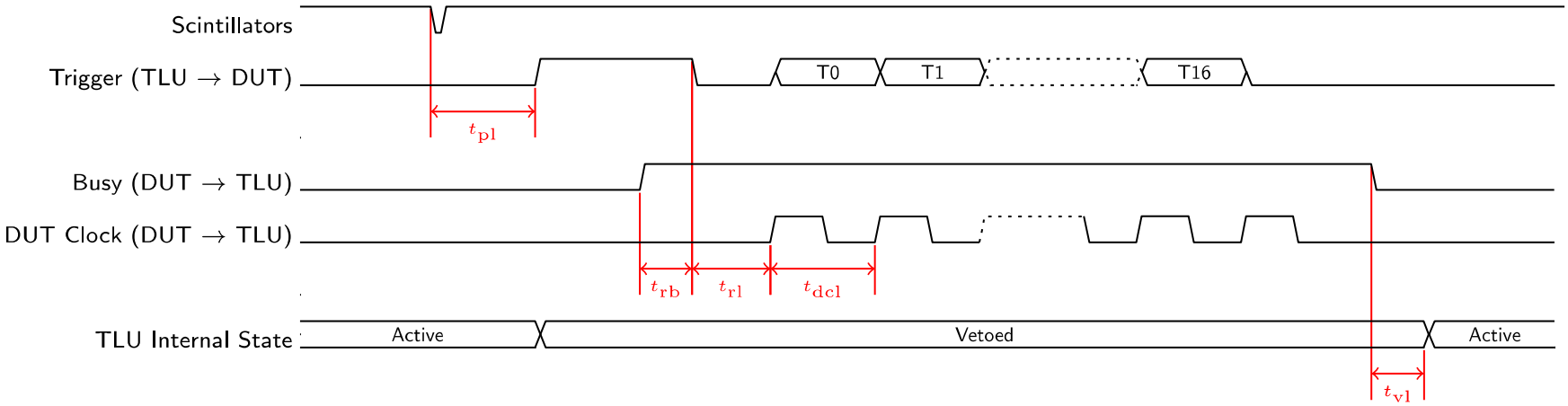
# Synchronous Interface



# Asynchronous Interface

- EUDET style asynchronous interface
  - TLU sends trigger
  - DUT responds with busy
  - Optional read-out of trigger number by DUT
    - Maximum DUT_Clock frequency
      - EUDET ~ 1MHz ( depends on firmware )
      - AIDA ~ 20MHz
- Implemented in both EUDET and AIDA TLUs

# Asynchronous Interface



# Spill/Shutter signal

- Optional , programmable spill/shutter signal
- In short term will be a fixed on/off period
- Could extend to be on for a fixed number of triggers, or a fixed time, or whichever comes first.
- Useful for a number of Linear Collider detectors / readout system.

# Large Number of Devices

- AIDA mini-TLU has only three DUT interfaces
- Fan-out one interface with external hardware
  - Take “or” of BUSY signals
- Options:
  - 1:6 using Uni Mainz board, VME format
  - 1:30 using Uni Bristol board.
    Mother+daughterboards, custom format
- Allows AIDA mini-TLU to interface to e.g. TimePix telescope ( 8 sensors )
- Fan-out can also operate stand-alone.

# AIDA TLU - Some Practical Issues

- The IP address is 192.168.200.(16*D) where "D" is the value set by the DIP switches.
  - Change by re-building firmware.
  - IPBus allows setting IP address by RARP, but not (yet) implemented in mini-TLU firmware.
- If using 1000Base-T (“Copper”) Ethernet, the link **must** negotiate to 1GBit/s (with current firmware).

# AIDA TLU Hardware Status

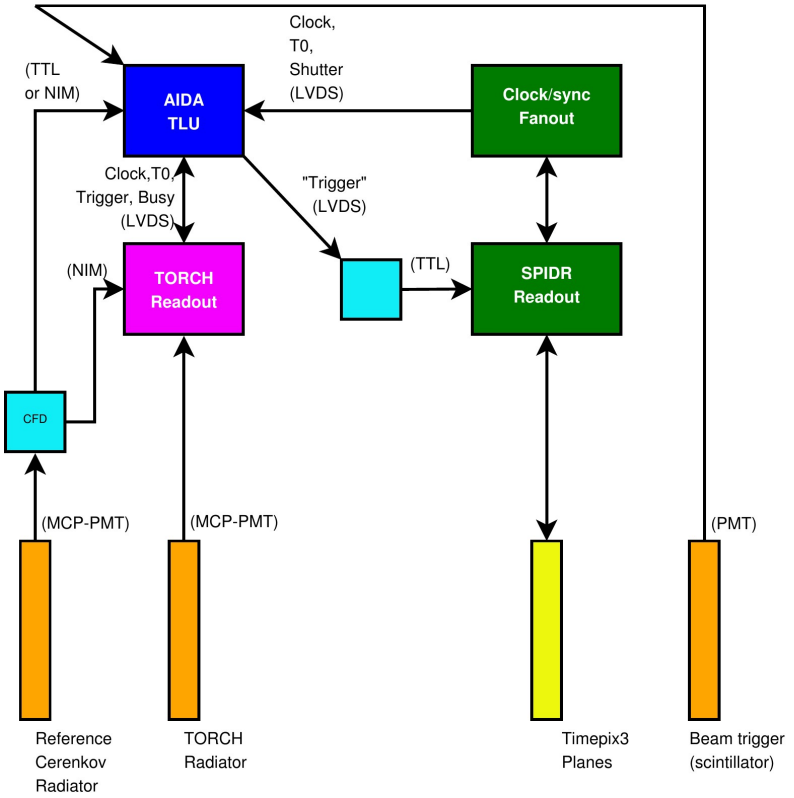
- Serious “bug” delayed production.
- Three prototypes with corrected design have been produced.
- Seven more boards produced
  - Not all available instantly – need testing.
  - Contact DESY for availability.
  - Cost likely to be about €1500 (TBC)
- Custom enclosure under design.

# AIDA TLU Firmware/Software Status

- Prototype EUDAQ Producer for AIDA TLU written by Francesco Crescioli, LPNHE/IN2P3
- Prototype firmware written by Alvaro Dosil, USC and D.Cussans, Bristol.
- Only synchronous mode at the moment, asynchronous mode later this year.

# TLU in action

- Operation with non-AIDA telescope:
- Interfacing TORCH ( LHCb upgrade proposal ) DAQ with LHCb TimePix3 telescope.
- Accepts clock and synchronization signals from LHCb telescope
  - Provides “AIDA synchronous interface” to DUT



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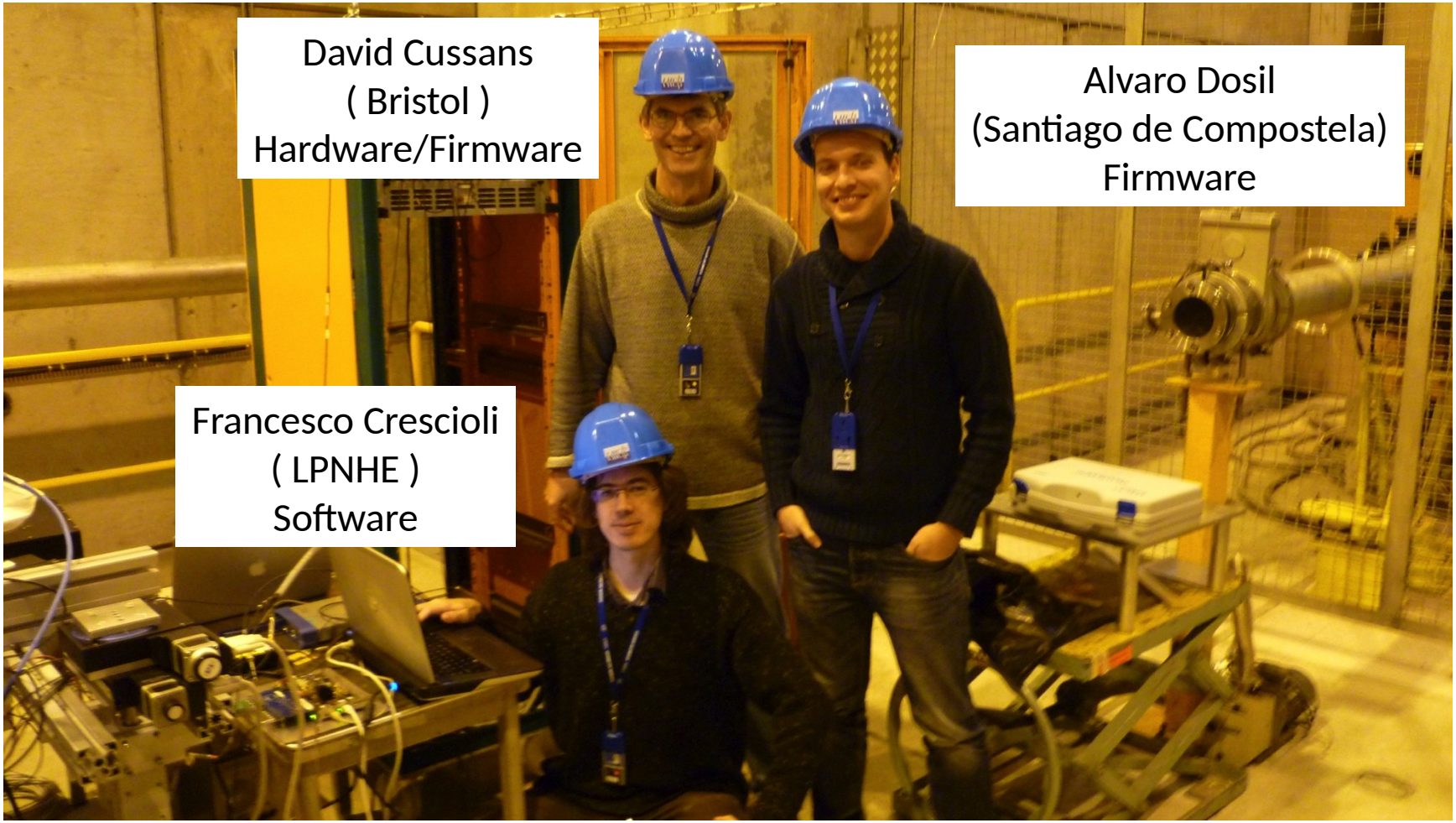
# Development Team



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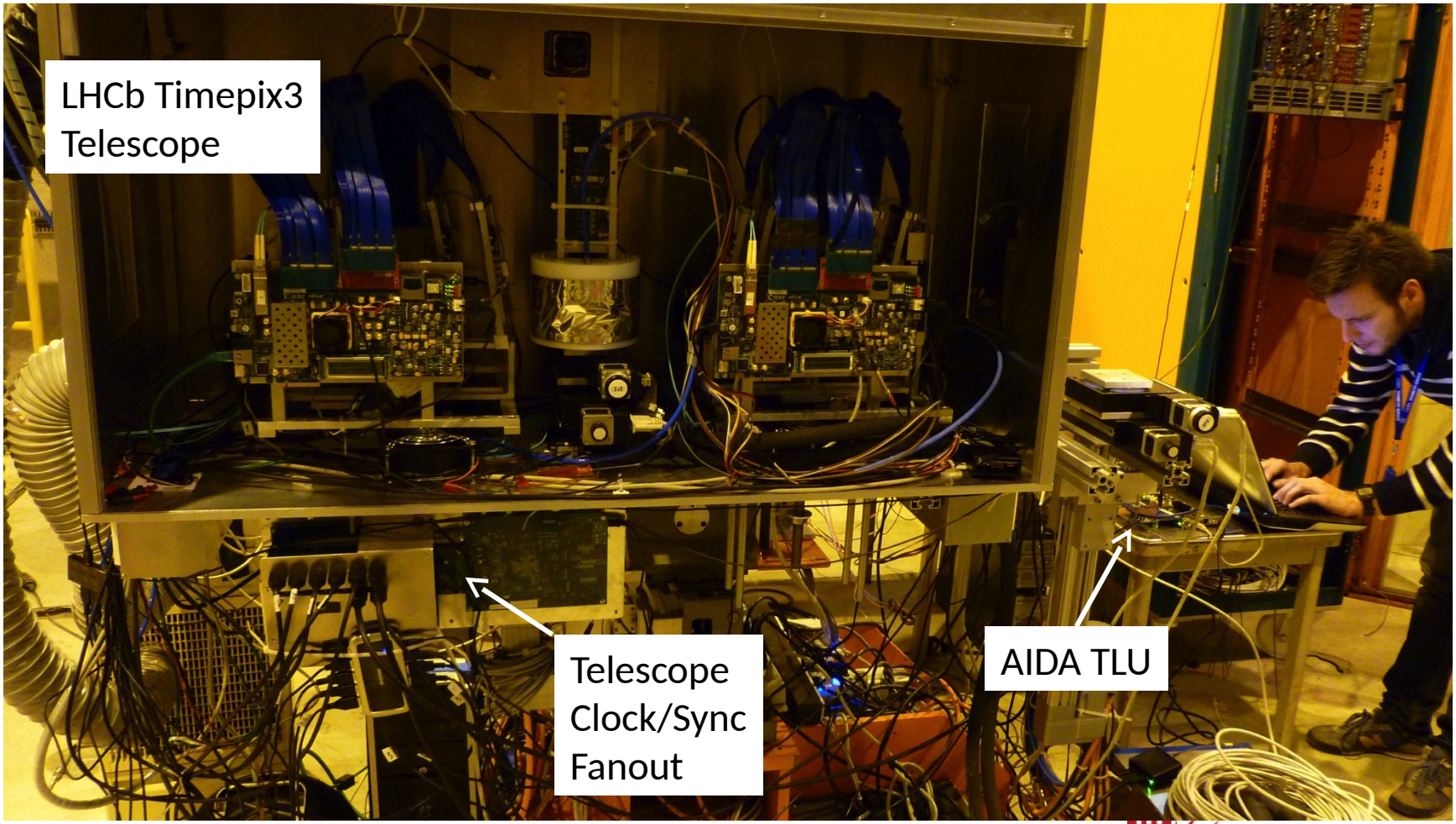
# AIDA TLU with non-AIDA Beam-Telescope



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# Clock/Syncronization Fanout

- Up to 30 DUT
- Compatible with miniTLU (in synchronous mode)



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# Plans

- AIDA-2020 funded.
  - Common DAQ work package will integrate closely with beam test infrastructure work package maintaining EUDAQ
- Current firmware/software team available until end March 2105
  - Aim to have “finished” AIDA TLU code by then.
- New version of AIDA TLU version this year.
  - Funding model to be decided.
- EUDET TLU in maintenance mode