Specifications for HV-CMOS test chip submission in 2014.

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Introduction

The submission is meant to prototype the HV-CMOS technology for the purpose of upgraded ATLAS SCT tracker for HL-LHC luminosities. The submission is meant to provide the monolithic devices that can allow definitive answers to the key technological questions:

* Studies of radiation hardness in the relevant range of fluences. The expectations, including safety factors of 2, are between 1.2 x 1015 1-MeV neutron-equivalent (neq)/cm2 for the innermost barrel layer and 5 x 1014 1-MeV neq/cm2 for the outermost barrel layers [1] and maximum in the inner most endcap region of 1.6 x1015 1-MeV neutron-equivalent and 576 kGy.
* Signal-to-noise ratio (S/N)
* Operational thresholds
* Noise hit rate
* Spatial efficiency map
* Timing resolution, sigma(T)
* Power consumption (P)
* Interplay between S/N, sigma(T), and P.

Evaluation features

The monolithic devices necessarily couple the “sensor” functionality of the devices which originates the charge signal with the “amplifier” functionality of the signal analog processing. There is also some amount of digital readout circuitry anticipated on the final incarnation of working prototype. To be able to test these aspects of the final device in depth, it would be a good idea to provide several sub-circuits which implement these aspects separately.

We would need two submissions: the first to determine the radiation tolerance and optimal single pixel geometry and the second to look at characteristics of the array and periphery. This would allow for the earlier submission of the first as the second will most likely require more design FTE. As it would have practically no periphery (just bond pad locations from access to pixels, the biasing infrastructure and services for the PA, I believe), it could be small (~2x2mm2).

First submission:

It would be good to have two sections; one with direct access to the collection diode which require electronics that can measure signals in the 1-3 ke- with a response time to distinguish drift from diffusion signals and a second section with a pre-amplifier which would able to make signals large enough to measure well with standard analogue strip chips (signal of 8-12 e-). This implies gains of 6-12x.

* First section: For the diodes it would be good to test more than one geometry. Each should be in at least blocks of 3 x 3 pixels where the middle one is accessed. The cells on the outer pixels can be connected together to minimize the amount of probing/interconnect required. As there will be no threshold and the noise is dependent on external electronics, the only thing that can be studied is the development of signal and the depletion region/capacitance. I would suggest making 3 sections of 37 by 100 pixel with three different diode configurations (full coverage, minimal, somewhere in between). It would be beneficial to avoid metallization on at least a part of the central pix. This would enable charge injection with lasers.
* A second section with amplifiers to get signal into range of analogue ASICs (8-12 ke-) This requires the PA to have the total gain of 6x12x. Several amplifiers in series can be used to make up the total gain required. The PA would also have to have a rise time consistent with LHC electronics (<12 ns). For efficient testing, it could have a different geometry (~80 um pitch of wire bonds). Such device enables studies of depletion region, radiation hardness, and the charge collection mechanism. Individual pixels would have be accessed. To look at cluster size, etc, I would consider 5x5 pixel sections of 37 x 100 um pixels with the central 9 accessible by bond wires. If the connections are done on the long sides 80 um pitch bonds with a size of 60x200 um would take about 700 um per section (8x80 um + 60 um for the outer pad sizes). For this section you would also want 3 copies of it matching the three diode configurations.
* A circuit that only contains the front-end amplifiers without the sensor connection should also made available with connections available to the input and output to determine changes to pre-amplifier with irradiation and gain Here probing pads (50x50 um) should be made available. The digital programmability of the amplifier features could be used.

Second submission:

In the second submission, we would like to try to make some tests of architecture and periphery. Hopefully, some measure of the achievable thresholds can be made.

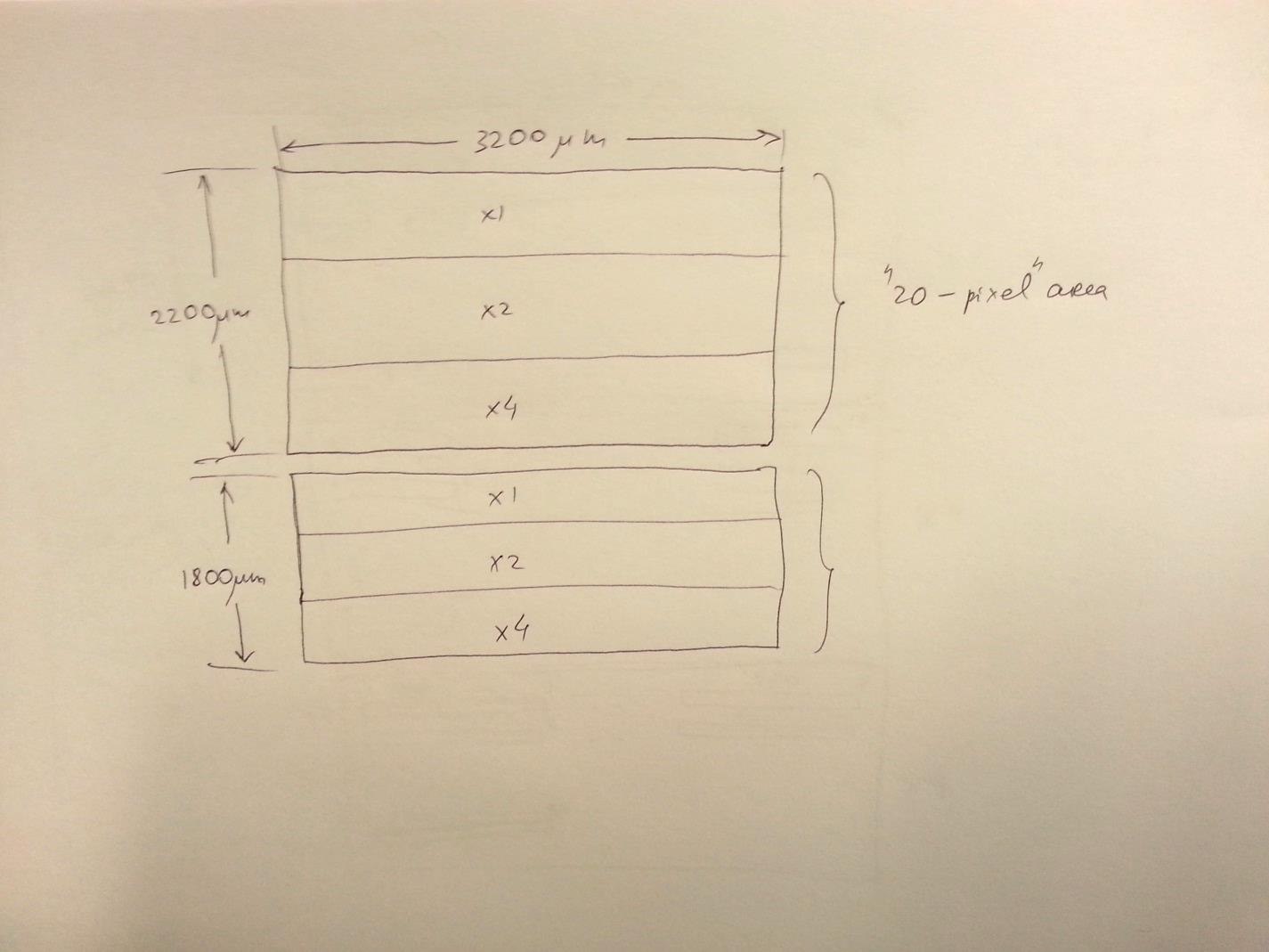
In general ~1.8 mm will be available for periphery and ~3.2 mm for the array. We think we would like 3 sections of the array to allow trialing of effects of pixel size on threshold (Figure 1). If 37 x 100 um is roughly the smallest area needed for the functionality in the pixel we would like, we would like to suggest 2x and 4x length pixels to try to get at the balance of power vs. capacitance vs. threshold.

With 3 sections in the 5 mm length, you can segment into 36 longitudinal parts. We would like:

* 20 pixels with amplifier output lines going to the periphery while matching the channel density . This would imply bringing every 37 x 100 um pixel to the periphery individually with 32 in a row for the smallest pixel sections, so the pixel matrix would be 20 x 32, all 640 pixels going to periphery. For the 2x sections, it would be 37x200 um pixels, pixel matrix of 20x16, with 320 pixels. For 4x, it would be 37x400 um pixels, pixel matrix of 20x8 with 160 pixels. The geometry is shown in Figures 1 and 2. The section will show we can bring back the density of channels to the periphery properly and see if there is an obvious benefit making smaller/larger sub-pixels. It would be desirable to also implement traces near some of the pixels which can be used to inject external signals. They can be used to assess the system susceptibility to digital and analog signaling and cross talk.
* 16 segments reproducing 2 “channels” with the expected length in the final object (37 um by 24 mm). The channels would consider of pixels made up of 8 OR’d subpixels (37x 800) with the minimal size subpixel. This means 4 pixels per row. To reproduce the full length, the metal connecting to the periphery will snake up and down to the next segment (the last snaking up and down all 8 segment. The 2 “channels” would end side-by-side at the periphery. For 2x sections, it would be 4 OR’d subpixel; for 4x sections is would be 2 OR’d subpixels. The geometry is shown in Figures 1 and 3. This section show that the OR’s do not cause issues.

The periphery should be close to the final concept and therefore output digital location. To be readout by FPGA (??). Might need time stamp or bunch crossing depending if it isn’t obvious how to read out synched with beam. Capability to change the power of the preampliers, turning thresholds, etc. needed. Controls should use 3V circuits on the external connection points of common DAQ can be used for different foundries.

* In the 20 segment sections, it might make sense to have a fraction with traditional design techniques, and others with new idea of time walk compensation [3].

  
Figure 1. General outline of the active pixel area in the 2nd submissions’ test chip.

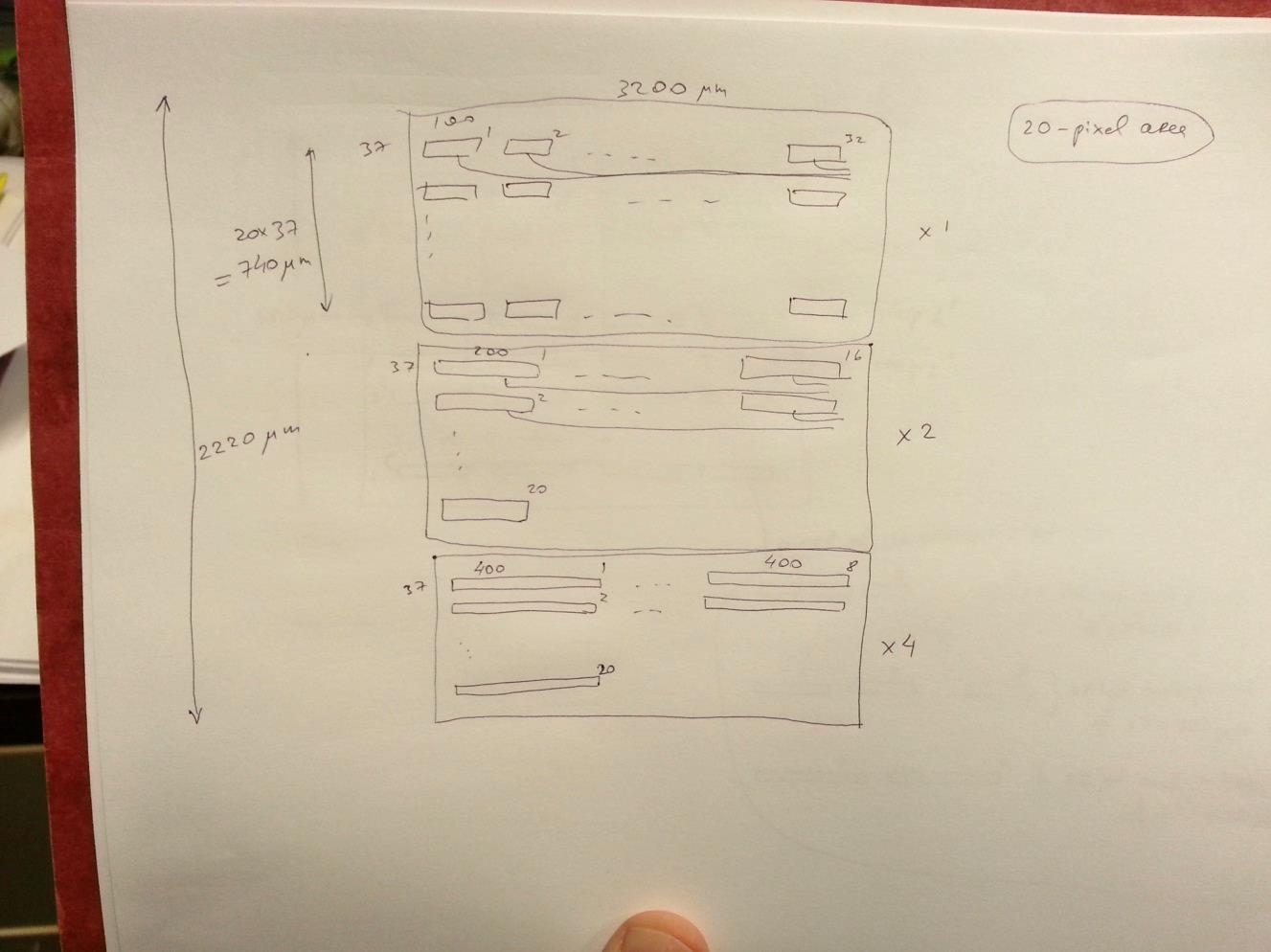


Figure 2. 20-pixel wide active areas in the 2nd submissions’ test chip.

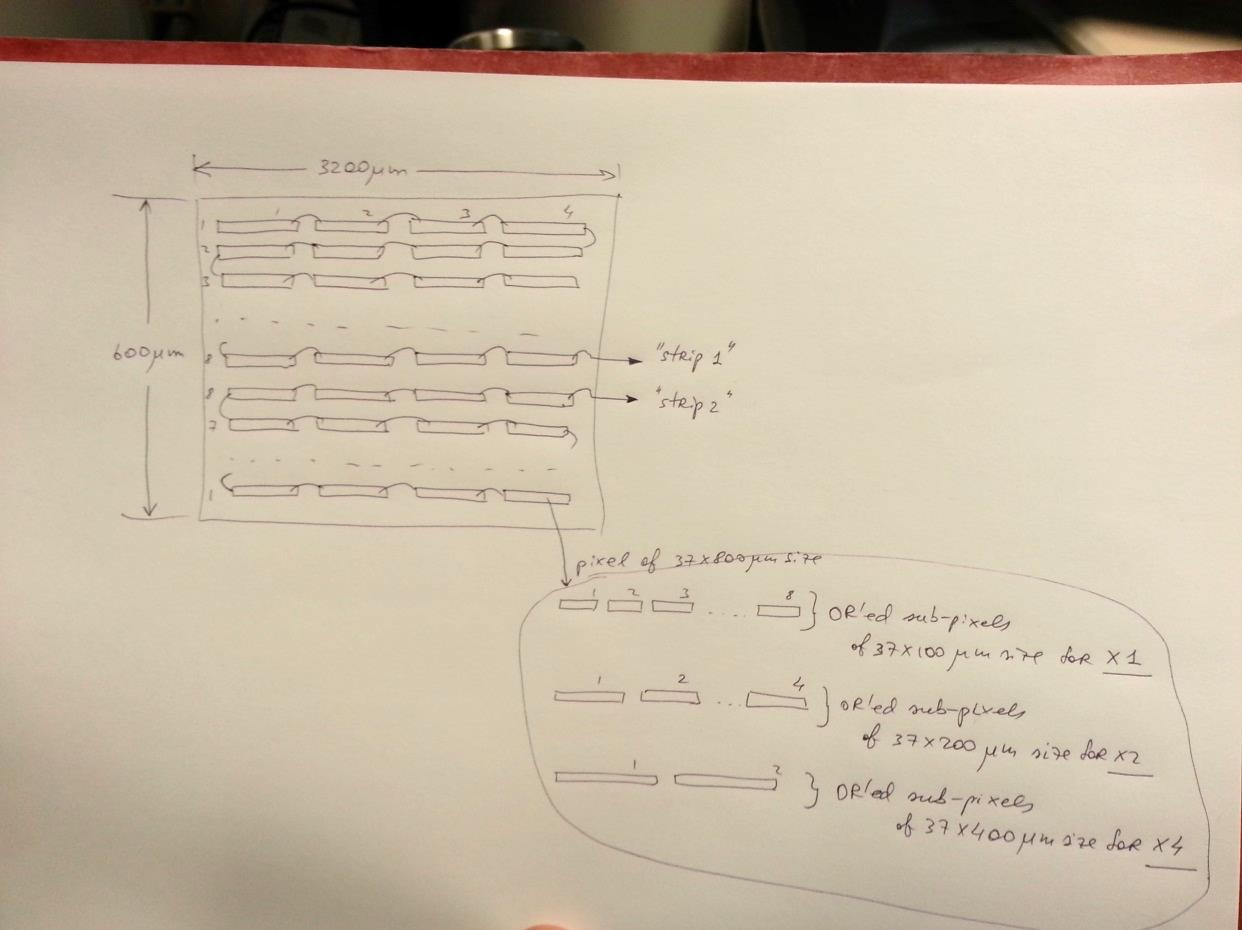


Figure 3. 16-pixel wide active areas (making 2 “snaked” strips each) in the 2nd submissions’ test chip.

Thoughts On Production:

In the production mode with traditional sensors we usually make simple structures on the wafer periphery for quality control. This is only possible due to usage of 1:1 mask in the sensor design. Monolithic design makes such technique unusable due to 10:1 masks and reticle constraints. However, allowing a small space at the reticle periphery for the test structures might still work for large enough reticle sizes (Figure 4). It may allow for diagnostics of final device performance variation.

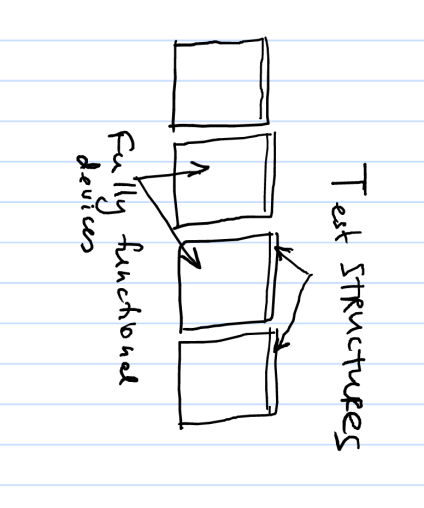


Figure 4. Test structure possibility with final device production.

Other features

Pixel size

The default pixel size is 37.5 um by 800 um, composed from 8 37.5x100 um^2 sub-pixels. This provides roughly x2 better spatial resolution than the baseline strip program.

Power

Studies with ABCN-130 indicate a ballpark power consumption of 1 mW/channel. This gives the area power of 53 mW/cm^2. To keep the CMOS device power density the same, the 37.5x100 um^2 sub-pixels would have to have the power per channel of 200 uW. This is not a spec, but rather a comparative number to be aware of in the chip design.

Time resolution

A variation of shaping time (at least 3 nodes), with the smallest aiming at single-bucket time resolution (time jitter <= 25 ns). Largest should be x4 to x8 longer.

Configuration Registers

Although programmability through external digital buses is possible, built-in operational defaults, including strip and chip numbering would be highly desirable.

Masking of bad pixels and strips

Being able to mask off bad pixels and strips in the fully functional test structures would be highly desirable for evaluation of data rates and operational thresholds.

Wafer parameters

Ideally, we would like to vary the wafer thickness and resistivity in the first submission. We are unlikely to be granted this option in the MPW submissions. Nonetheless we would need to find out these options from the foundry before the submission.

References

[1] Supply of Silicon Microstrip Sensors of ATLAS12 specification.

[2] Renato’s table of foundries.

[3] Ivan Peric, Monolithic Detectors for Strip Region.