Strip CMOS “Architectural” Submission

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Strips Specifics

The 3-year CMOS workplan had “architectural” submission in the first year. This was driven by several factors:

- Too little space on the MPW run to put everything we want to test in a single run
- Different things we want to test in “basic” and “architectural” submissions
- It is anticipated that the architectural aspects of information readout along the strip will require more complex/intensive design work.

This meeting is meant to figure out what exactly we’d like to put in the submission and when to have it:

- Next AMS Europractice deadline is Nov 3rd. The schedule for 2015 is not completely clear (Alex asked for clarification). But in 2014 the deadlines were Feb 10, April 28, Aug 11.
- Realistically, for getting the answers by the end of the 1st year we need to submit soon.
- Waiting for feedback from the 1st (“basic”) submission is probably not wise: it addresses different issues, and we may not get the full picture from testers even if we delay the 2nd submission until early 2015.
- Making the November deadline might be tough. IMHO this is the biggest constraint.

Goals and Submissions

The goal of the 1st year study (R. Nickerson's talk) is to study the following performance parameters :

- Radiation hardness (Barrel: 1.2×10^{15} neq/cm^2 for innermost layer. Endcap: 1.6×10^{15} neq/cm^2 and 58 MRad.)
- Signal-to-noise ratio (S/N)
- Timing resolution, sigma(T)
- Power consumption (P)
- Interplay between S/N, sigma(T), and P.
- Spatial efficiency map
- Pixel size
- Readout architecture of signal transfer along the strip
- Operational thresholds
- Noise hit rate

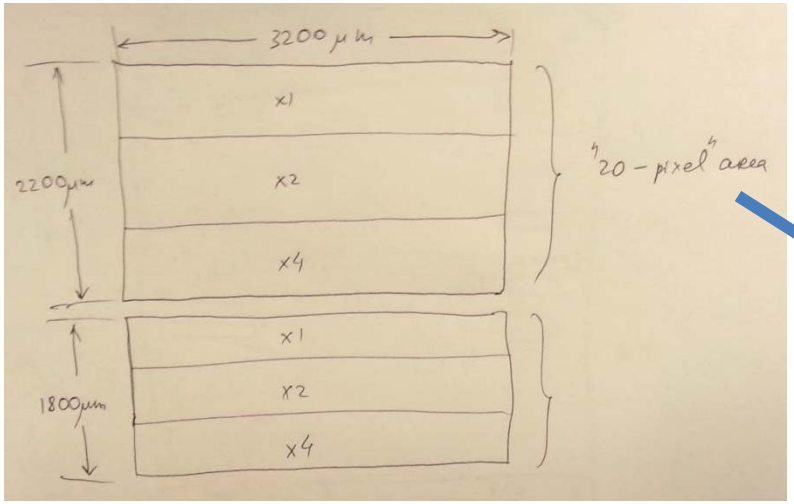
We'll need different submissions with MPW runs to assess basic properties and architectural issues. Some key aspects might be difficult to figure out with small size prototypes, although we could check noise and cross-talk susceptibility.

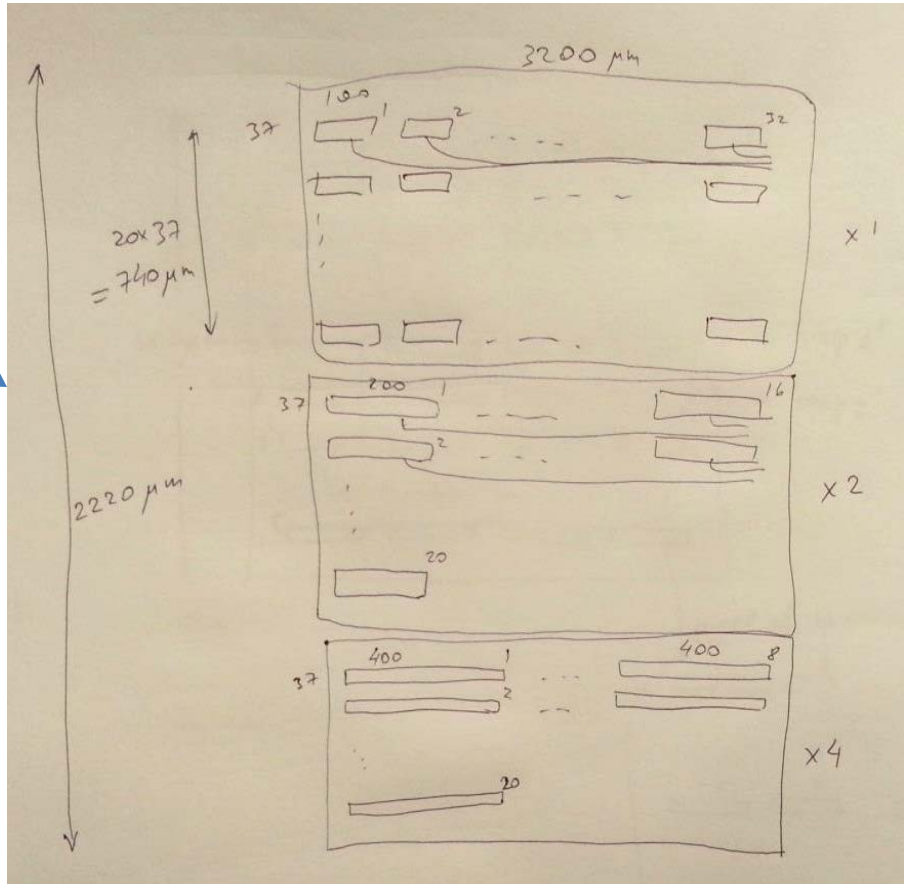
Note: "Organic growth" development would probably not have the architectural submission now. But we have a very aggressive schedule to meet.

"Architectural" Submission

Partitioning the available area (assume 5x5 mm^2) into 3 sub-sections to investigate the effect of different pixel size. Initially considered 3 sizes: x1, x2, x4.

Part 1: parallel traces to the periphery. Tests the channel density, pixel size. Can use different timewalk design for different pixels. Can implement traces near pixels to inject external signals (noise susceptibility).

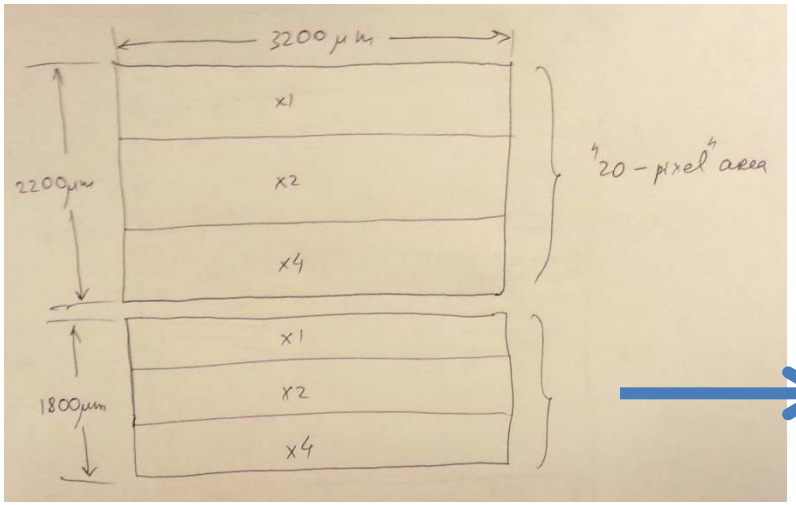


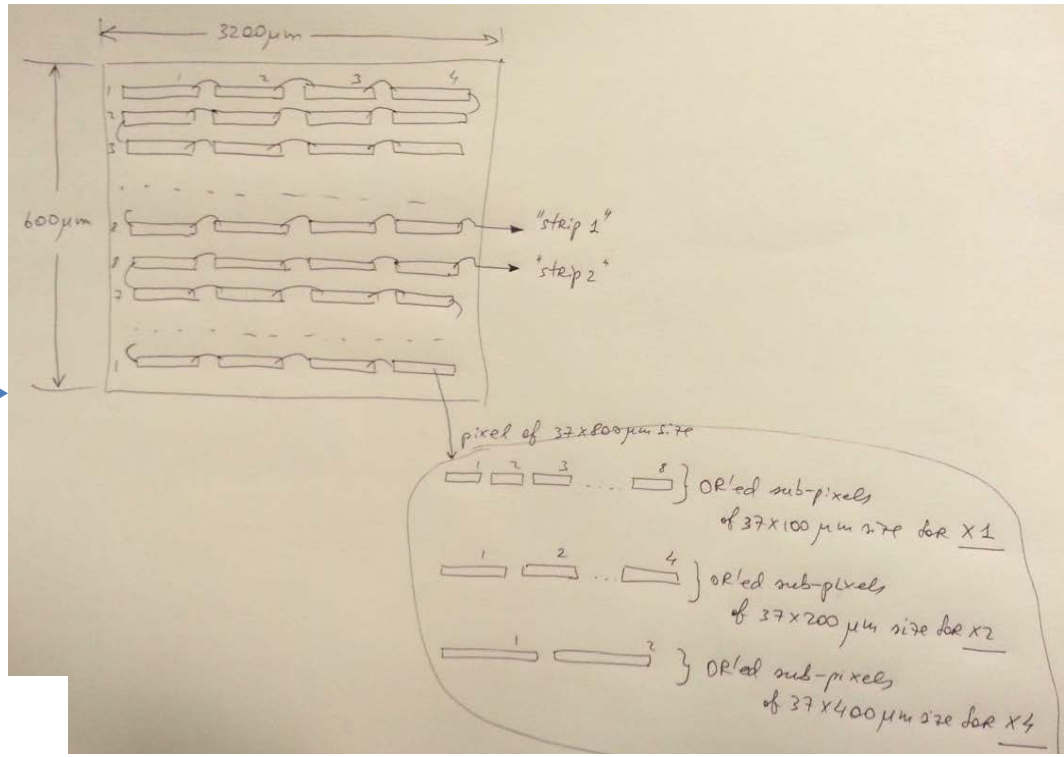


To limit to 1 pixel size?

“Architectural” Submission (2)

Part 2: 2 complete channels with correct total length implemented in a “snaked” geometry. The idea is to test that OR’ing pixels does not cause problems.





Note:
This arrangement also tests the possible issue of threshold Matching within a pixel segment.

Peripheral Circuitry

Chip periphery should be close to final :

- Timing and location information.
- Tuning of shaping/thresholds, changing power.
- Channel information multiplexing
- Readout to an FPGA or equivalent.
- Charge injection for calibration (?)