A New GBT Implementation for ngFEC

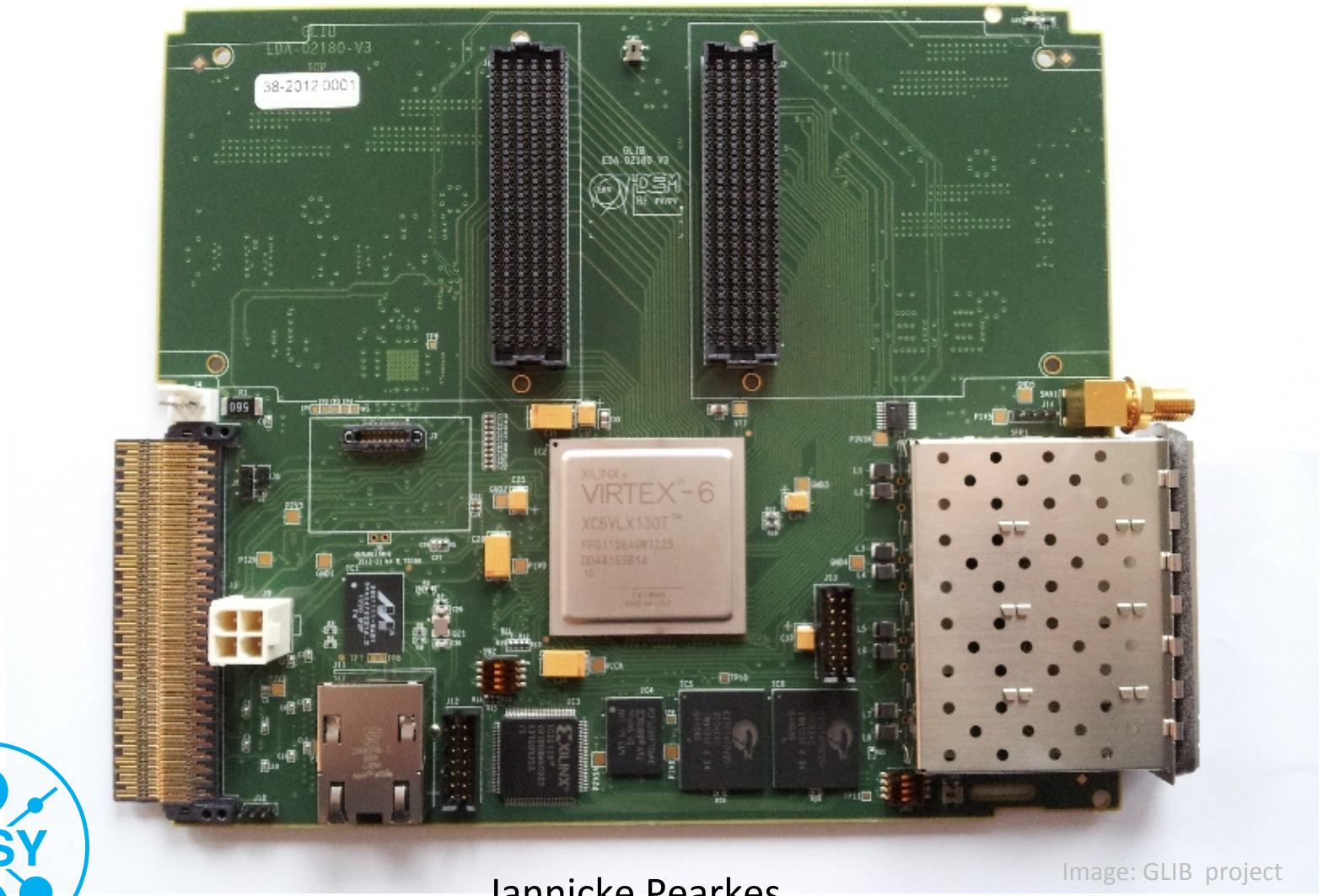


Image: GLIB project

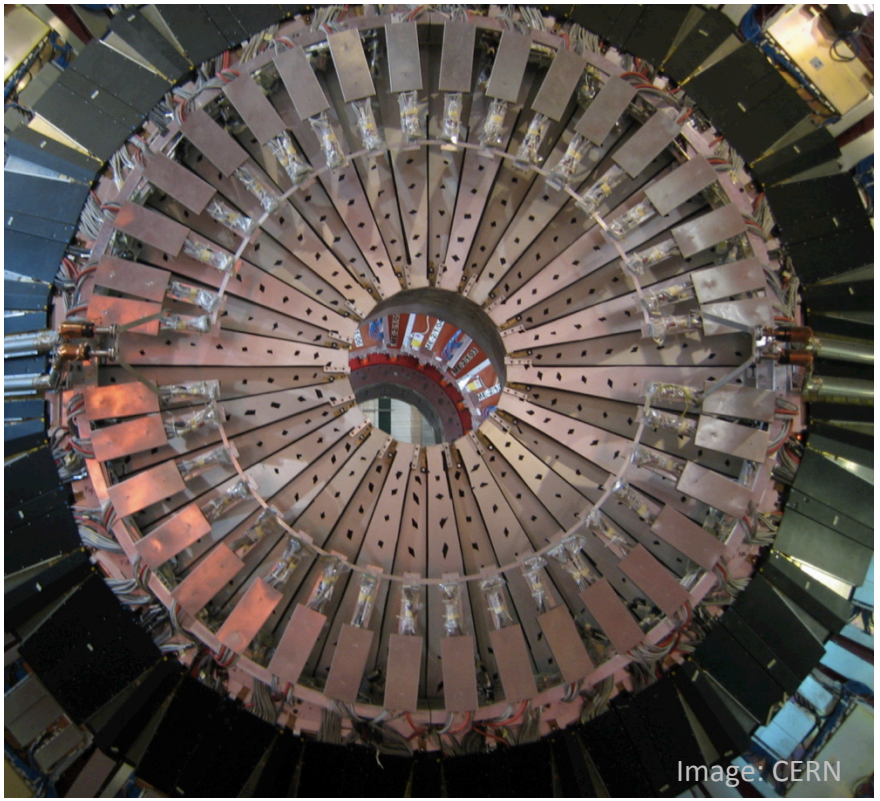
Jannicke Pearkes
Supervised by: Özgür Şahin & Ulf Behrens

What is Front-End Control?

Allows us to remotely control detector electronics:

- distributes clock
- fast controls
- power enable
- reset
- read temperatures
- check for malfunctions

Particularly important in hard to access or heavily radiated environments



Hadron Calorimeter Electronics Overview

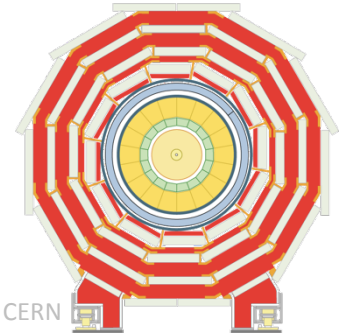


Image: CERN

HCAL Detector Electronics

Front-End Electronics

Control System

Readout

shielding

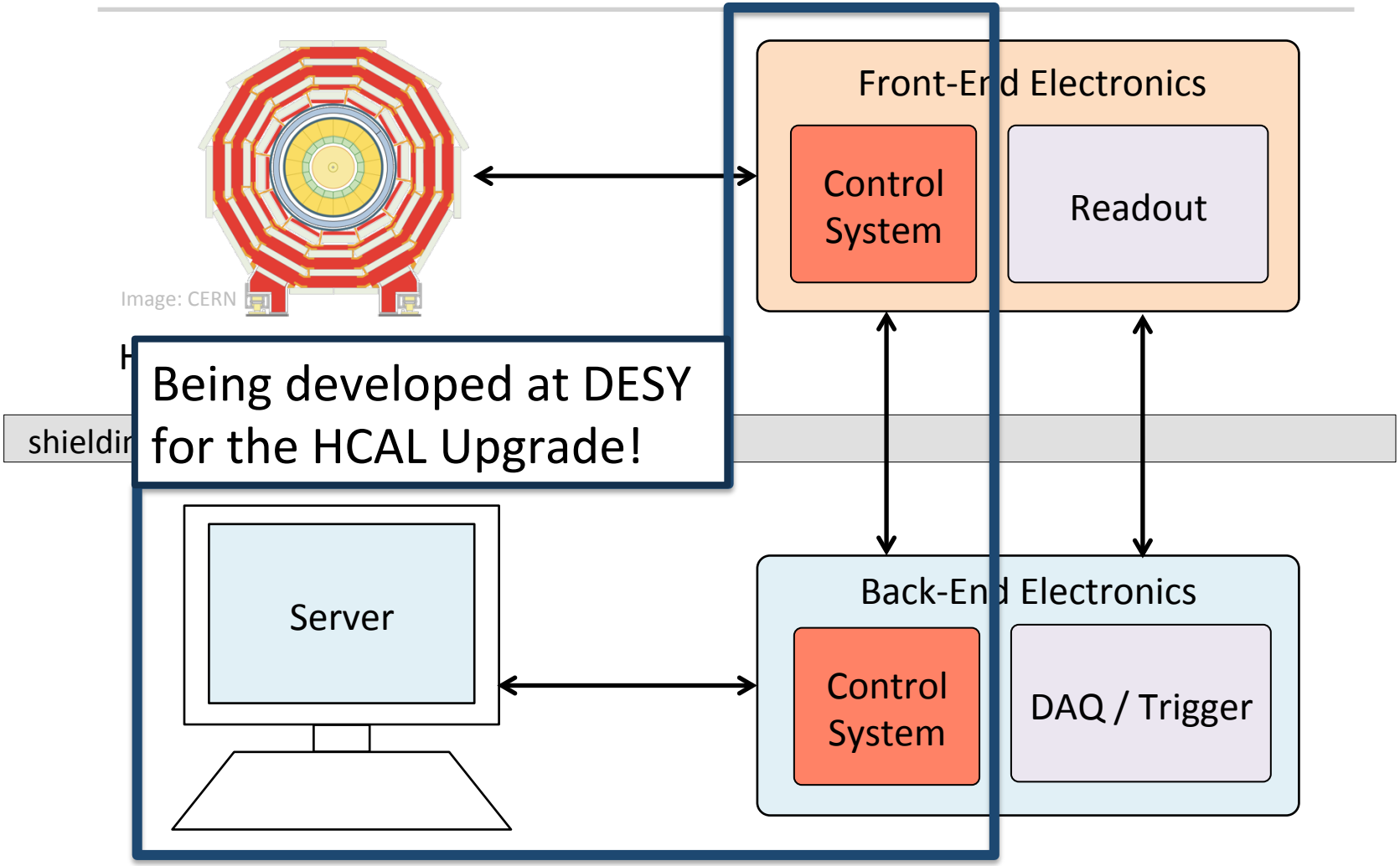
Server

Back-End Electronics

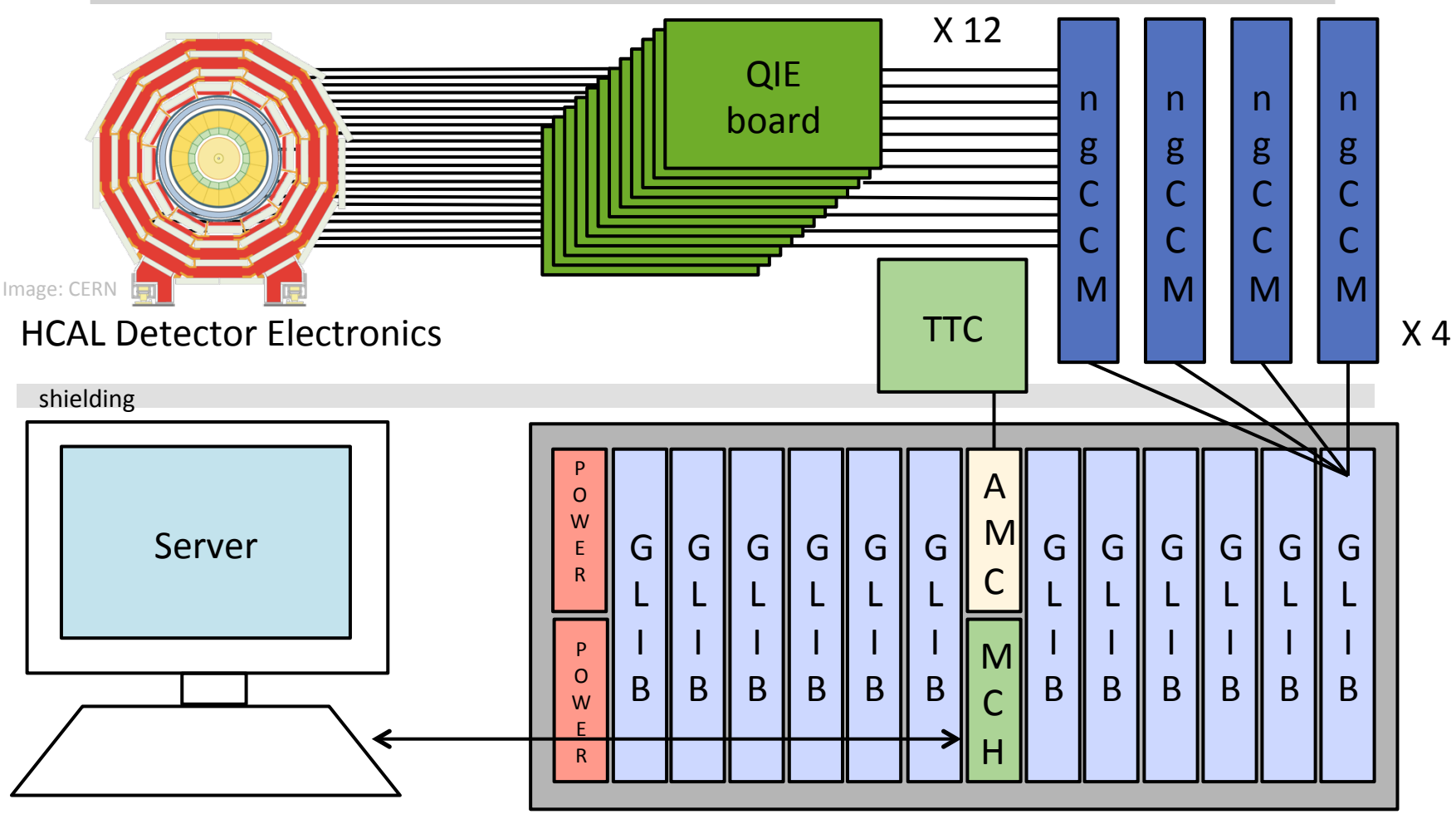
Control System

DAQ / Trigger

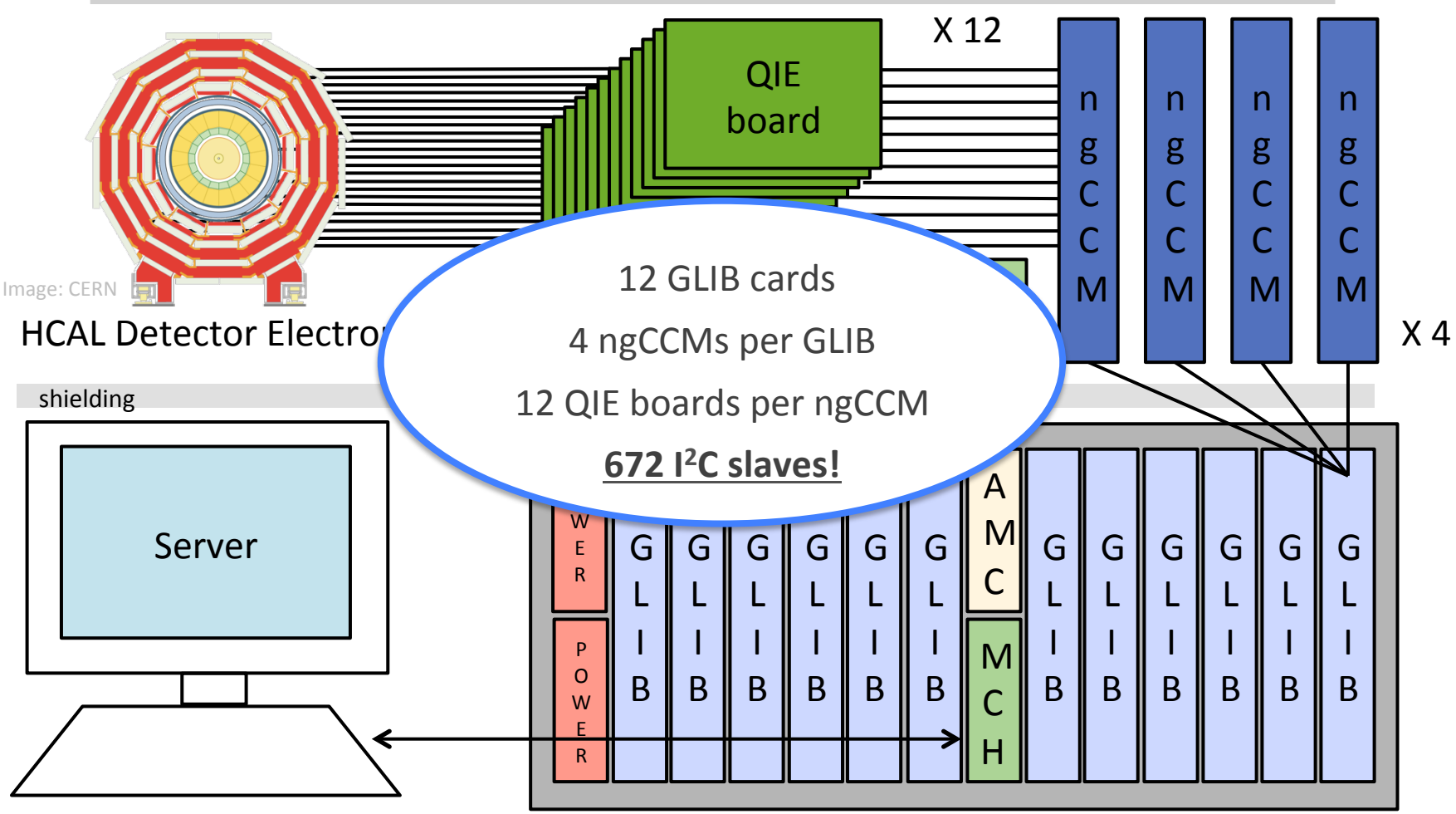
Hadron Calorimeter Electronics Overview



HCAL Control Path

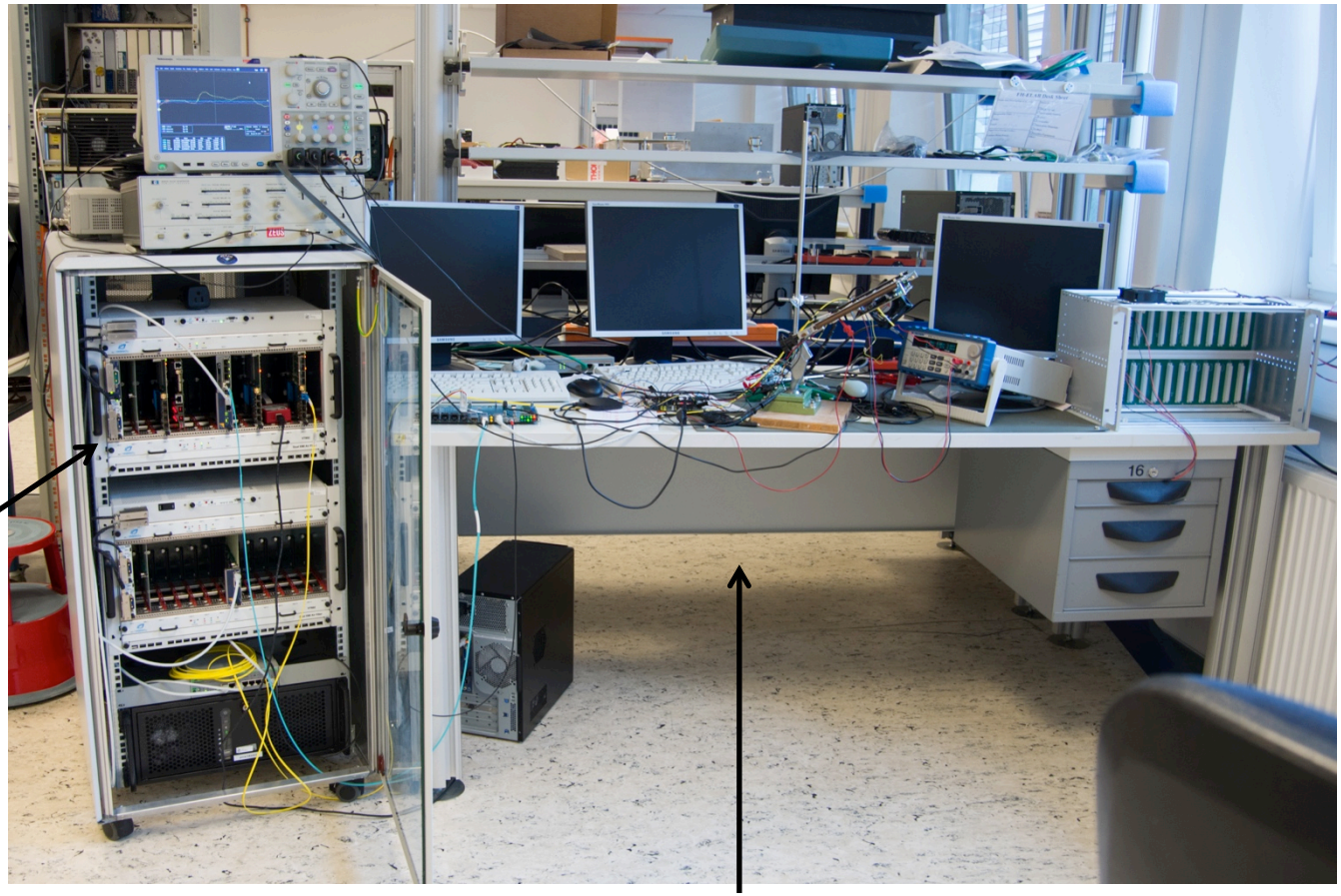


HCAL Control Path



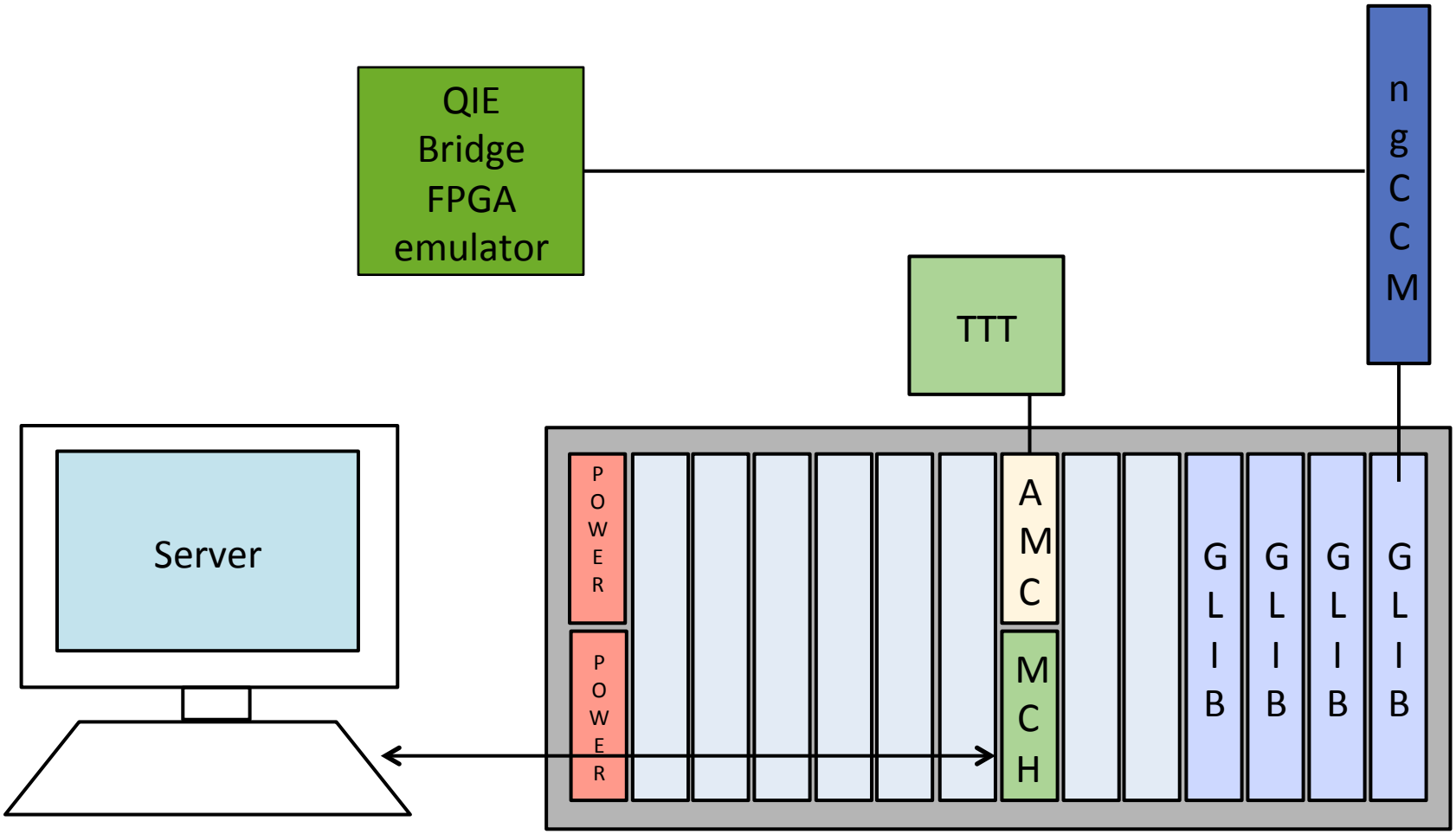
DESY Test Set-Up

back-end electronics in microTCA crate

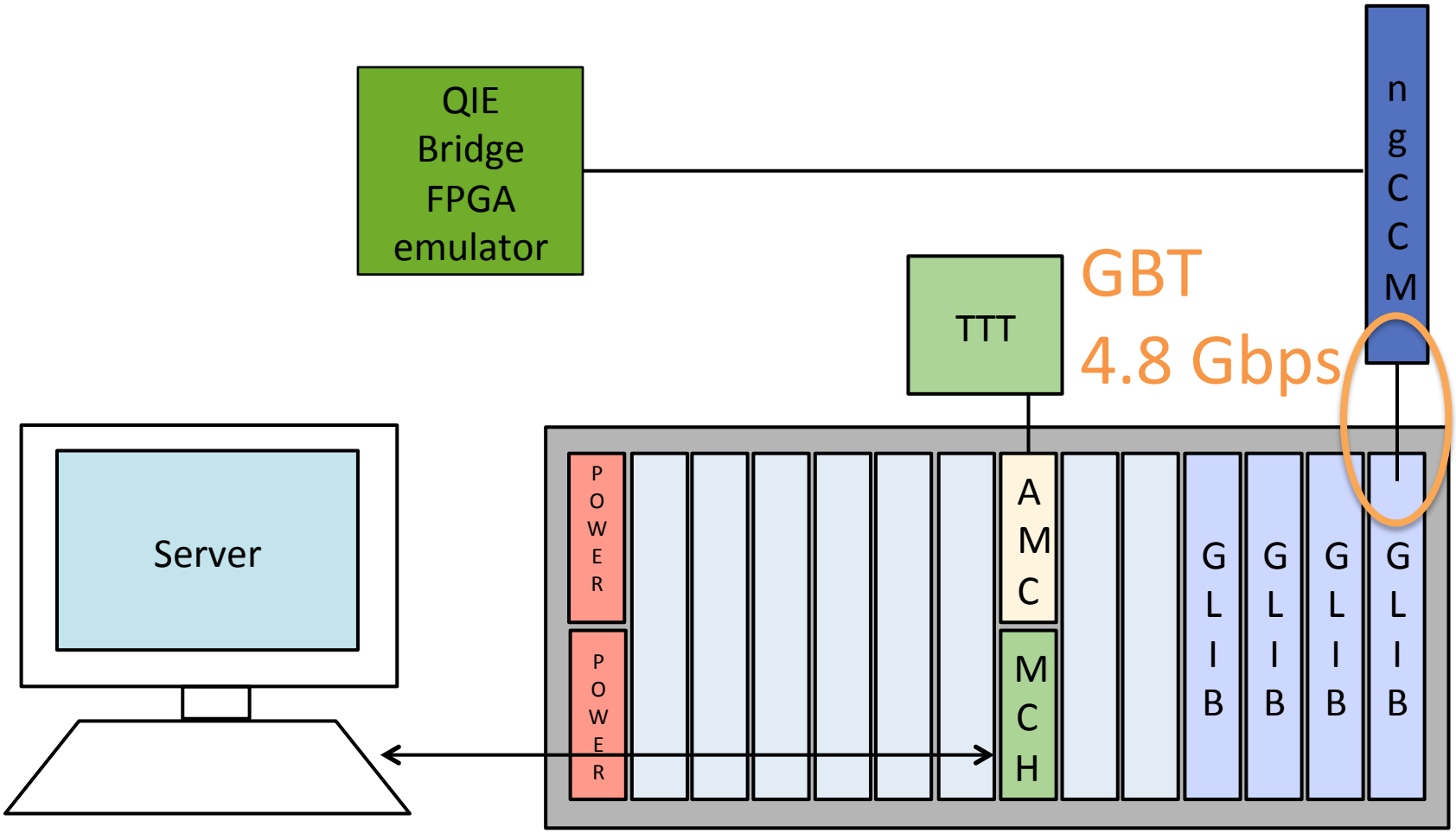


front-end electronics

DESY Test Set-Up

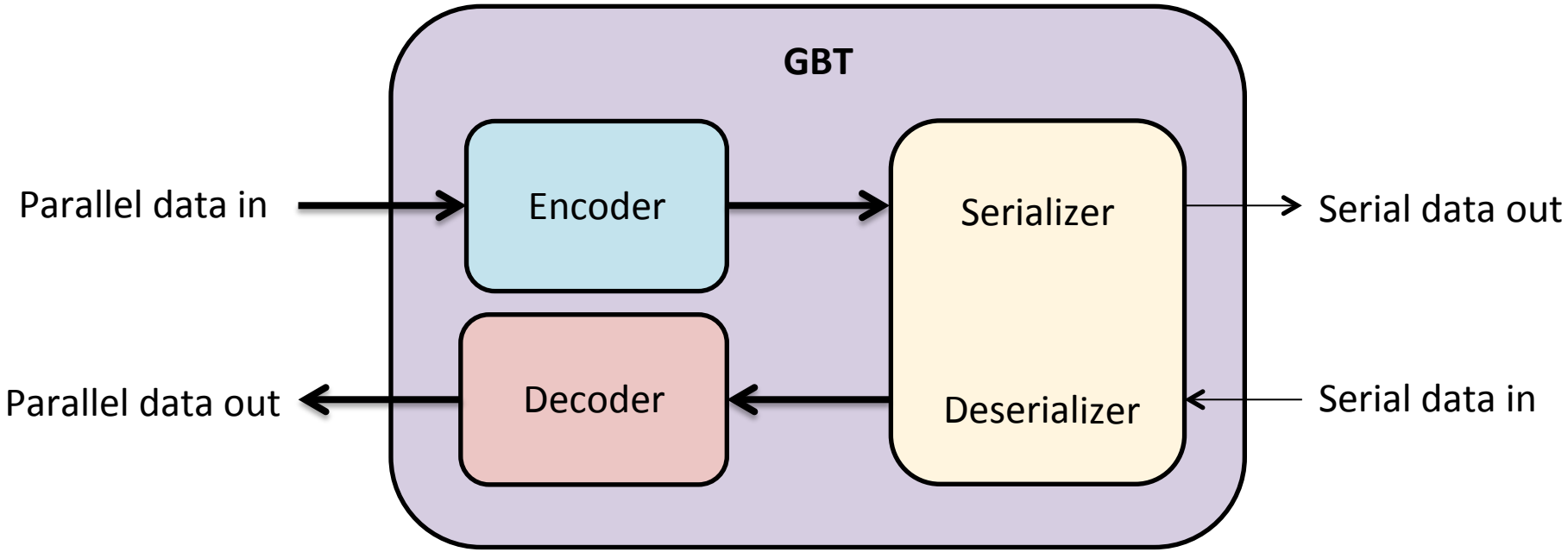


DESY Test Set-Up



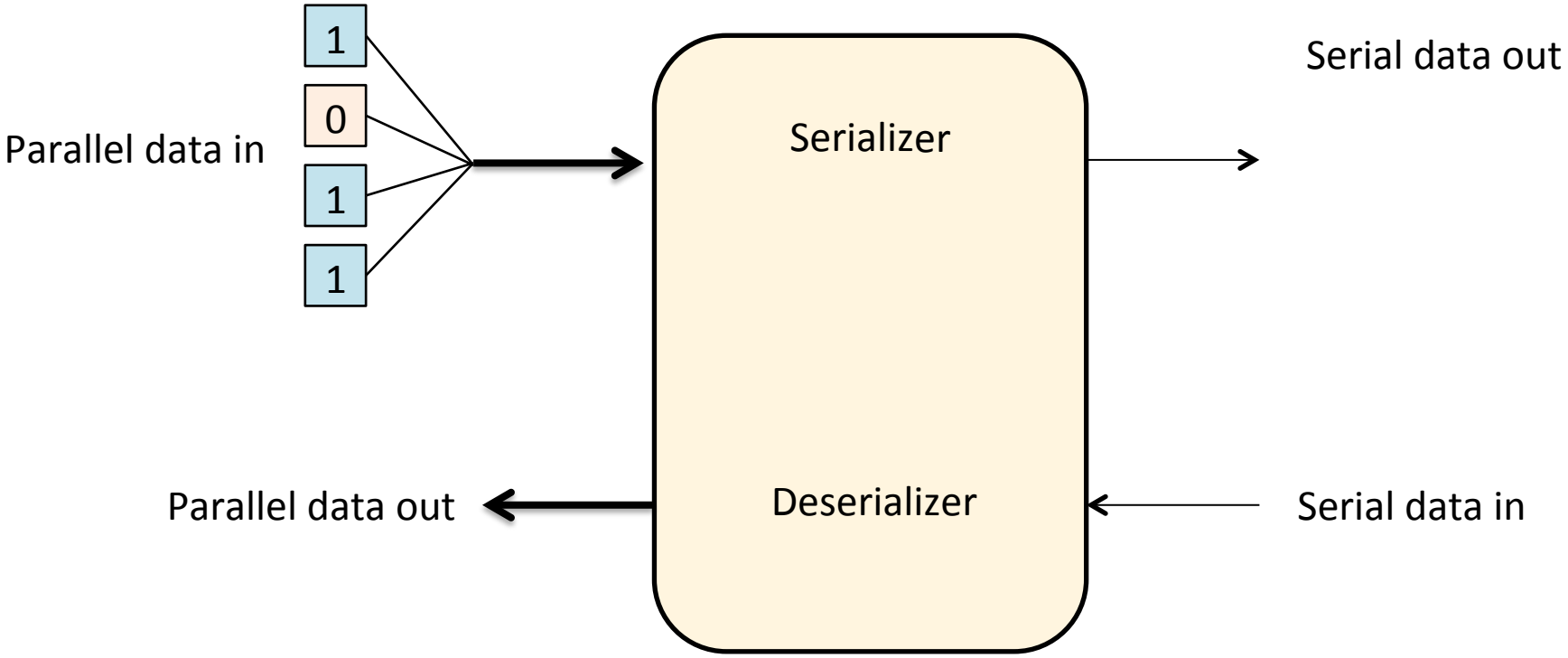
What is GBT?

Serial communications protocol developed for High Energy Physics Experiments



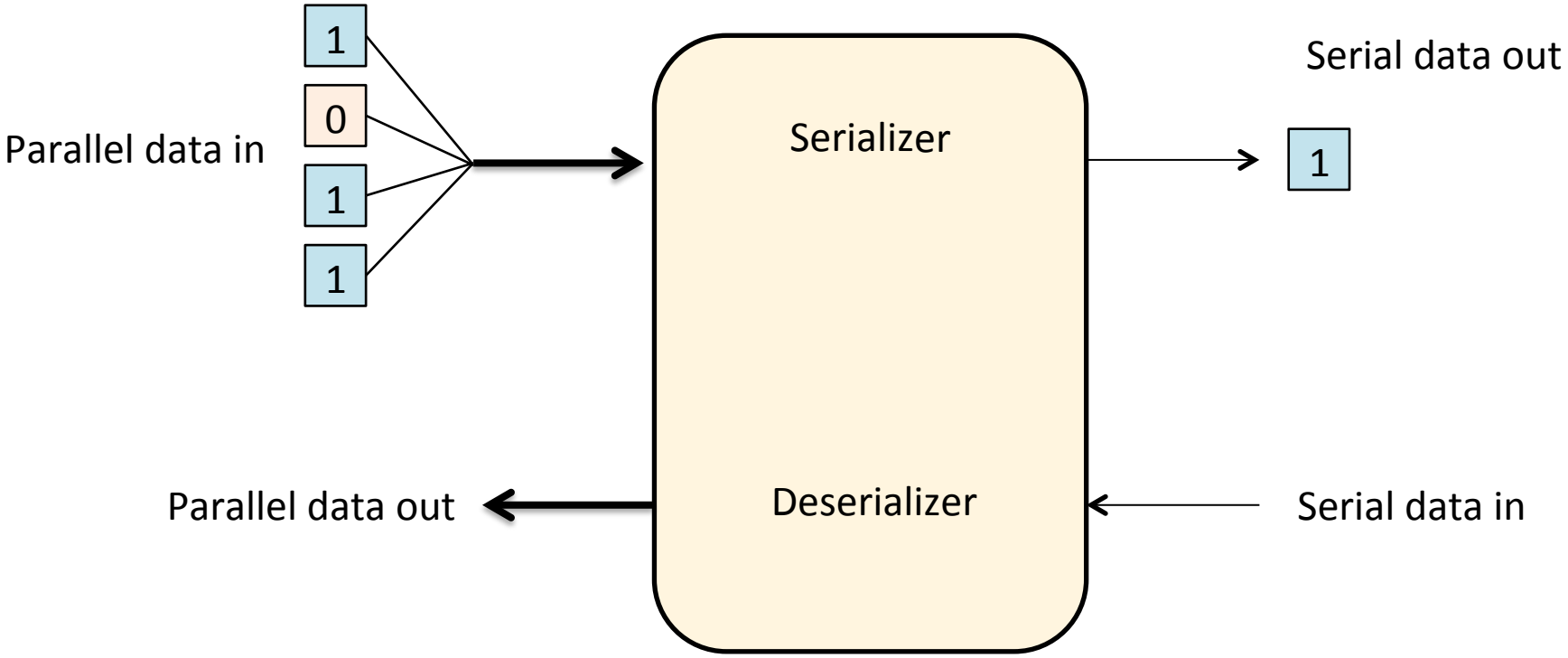
What is GBT?

Serial communications protocol developed for High Energy Physics Experiments



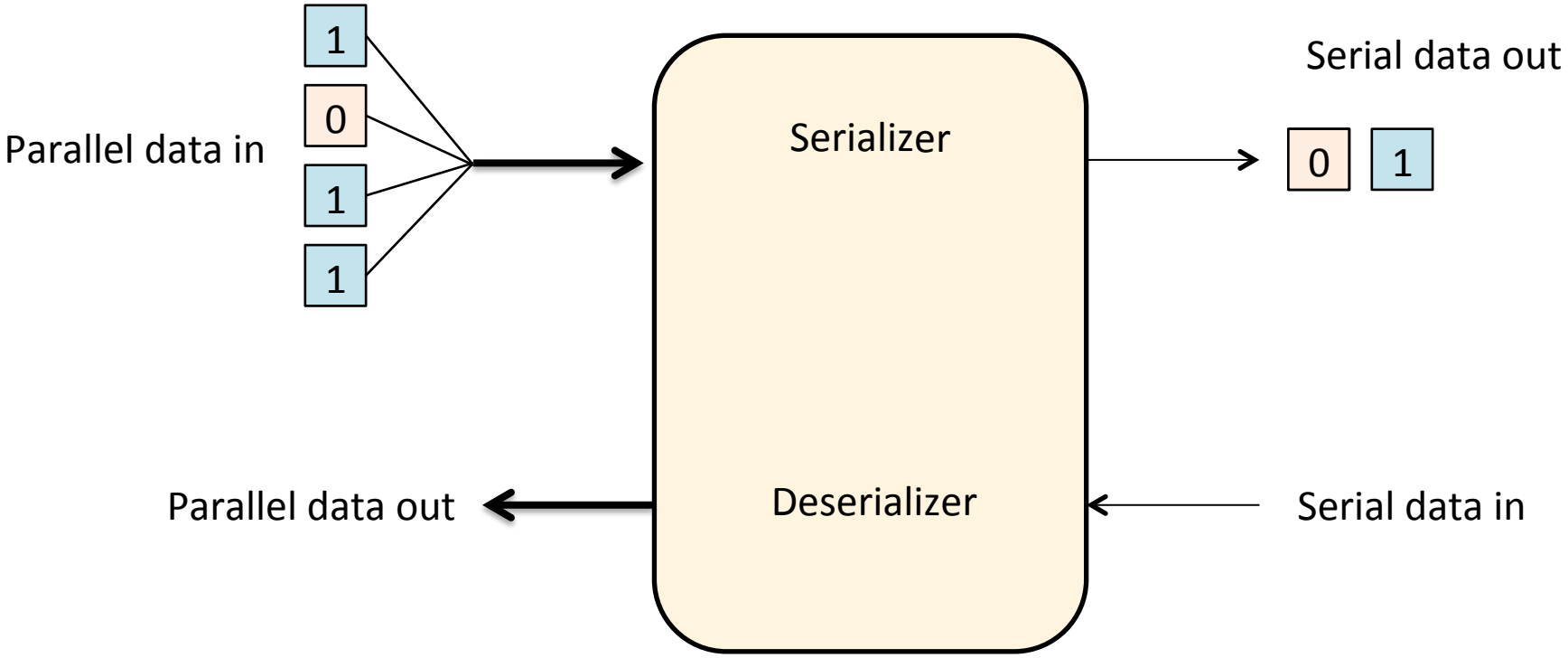
What is GBT?

Serial communications protocol developed for High Energy Physics Experiments



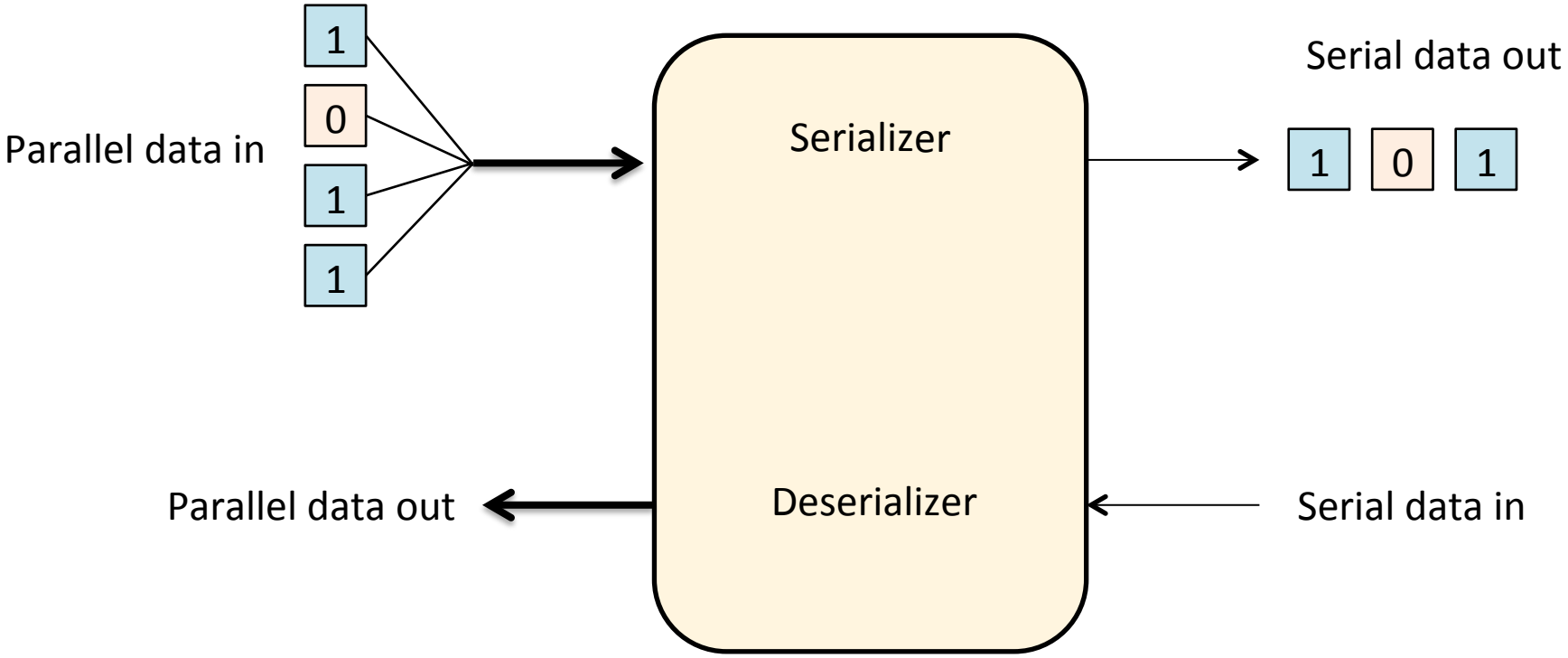
What is GBT?

Serial communications protocol developed for High Energy Physics Experiments



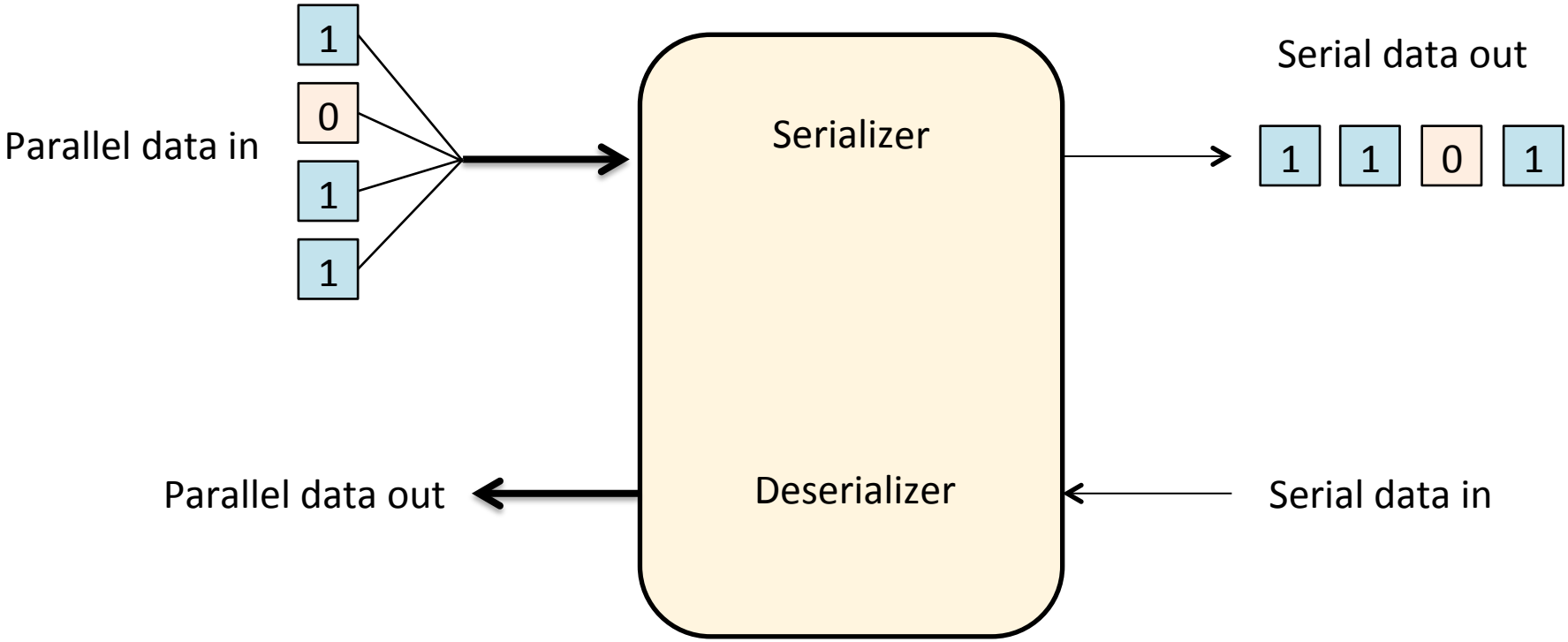
What is GBT?

Serial communications protocol developed for High Energy Physics Experiments



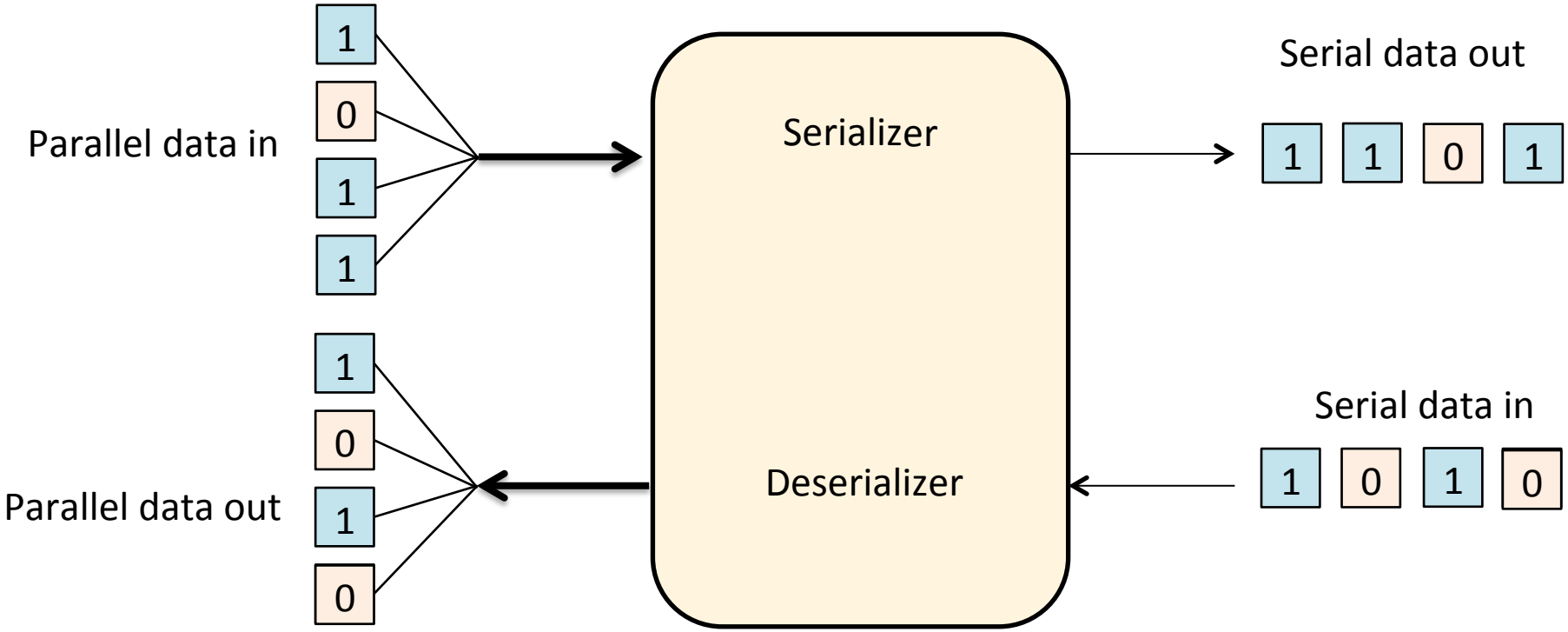
What is GBT?

Serial communications protocol developed for High Energy Physics Experiments



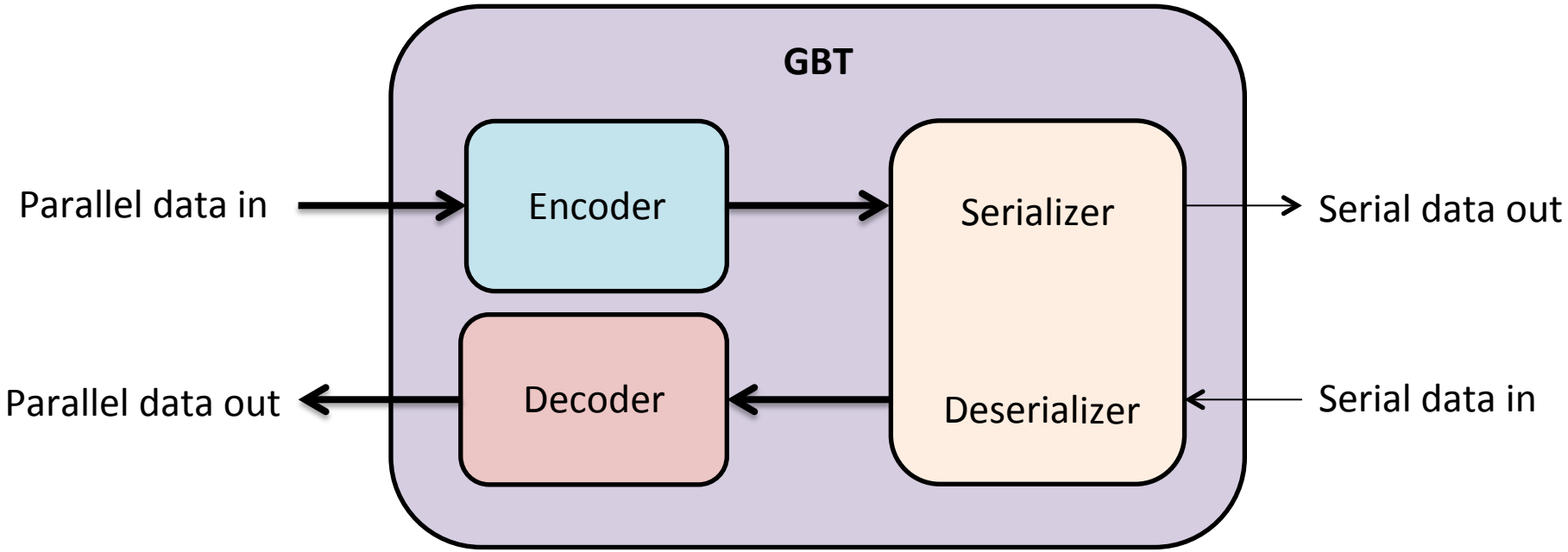
What is GBT?

Serial communications protocol developed for High Energy Physics Experiments



What is GBT?

Serial communications protocol developed for High Energy Physics Experiments



How is GBT implemented?

Field Programmable Logic Gate Array

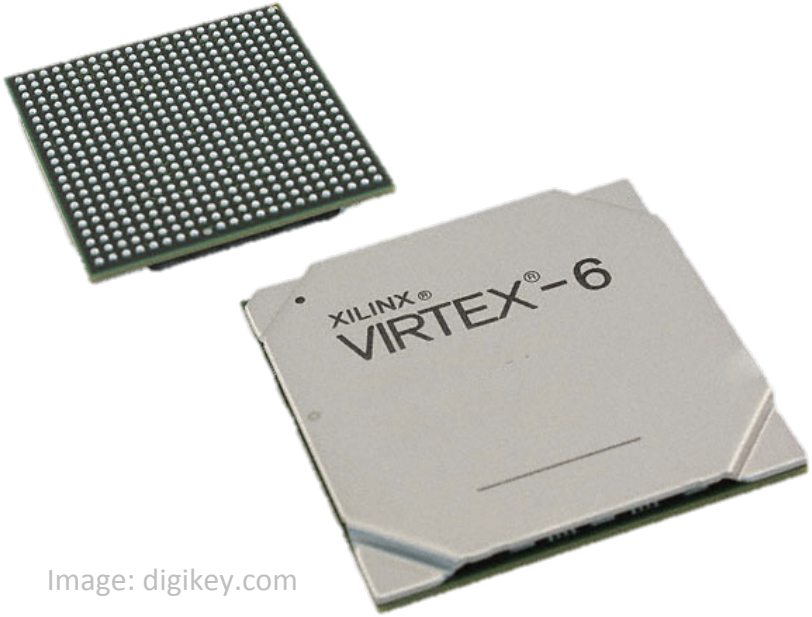
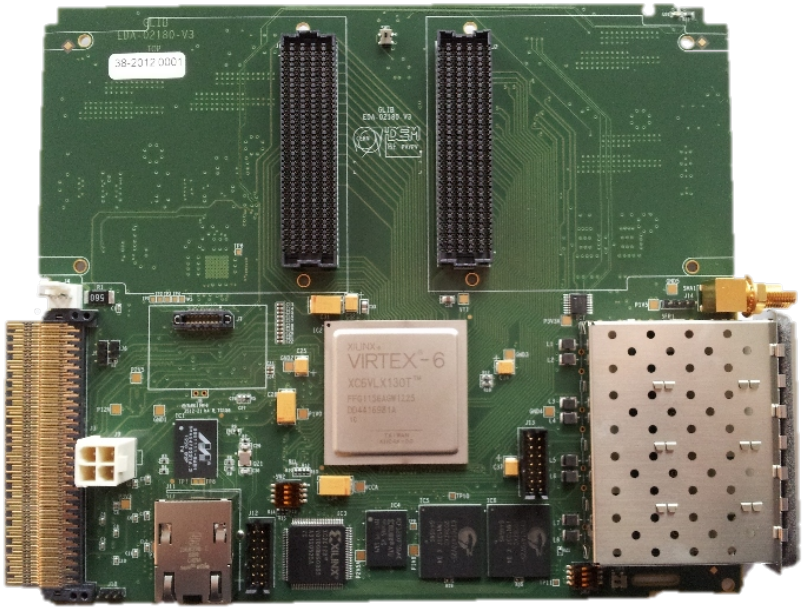


Image: digikey.com



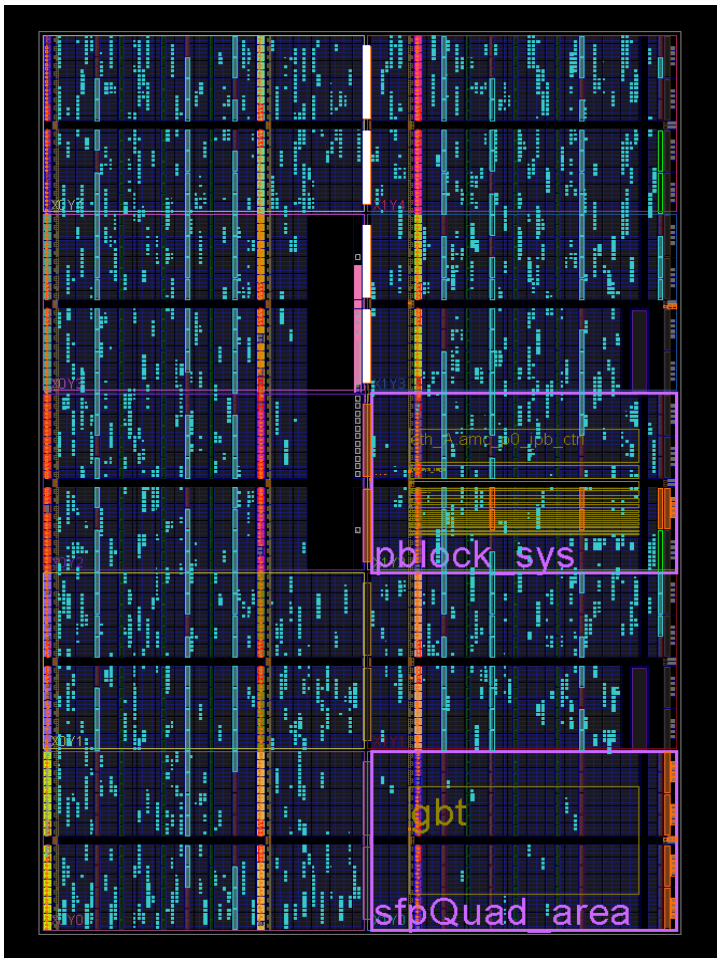
Example VHDL Code

```
Entity AND_GATE is
        port ( A, B : in std_logic;
                Z : out std_logic);
End AND_GATE;

architecture MY_DEFN of AND_GATE is
begin
        Z <= A and B;
end MY_DEFN;
```

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1

Things are a bit more complicated!

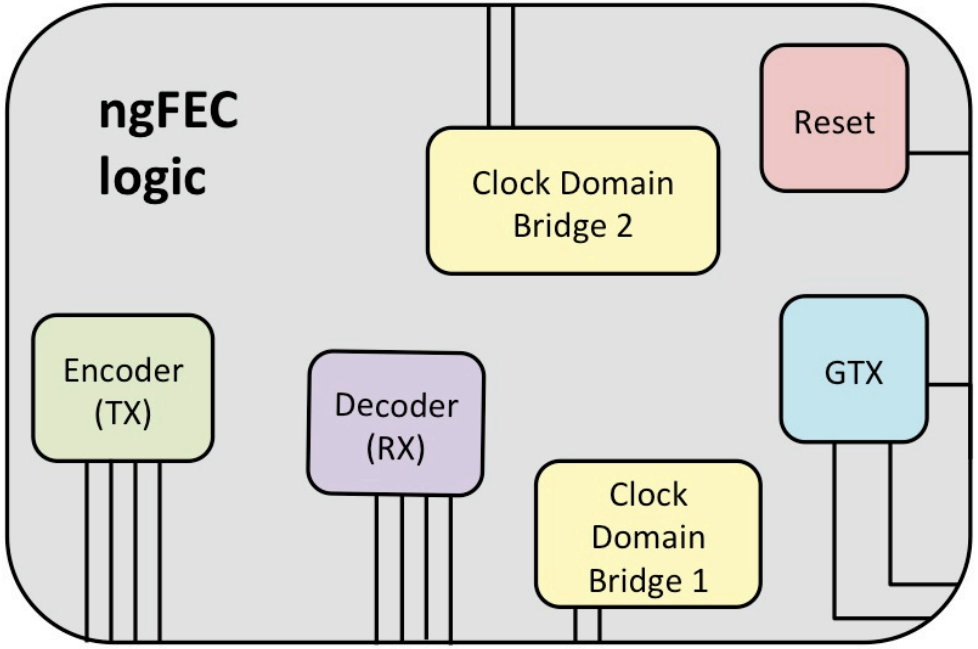


Over 20,000 logic blocks on our FPGA!
(Virtex 6 - XC6VLX130T)

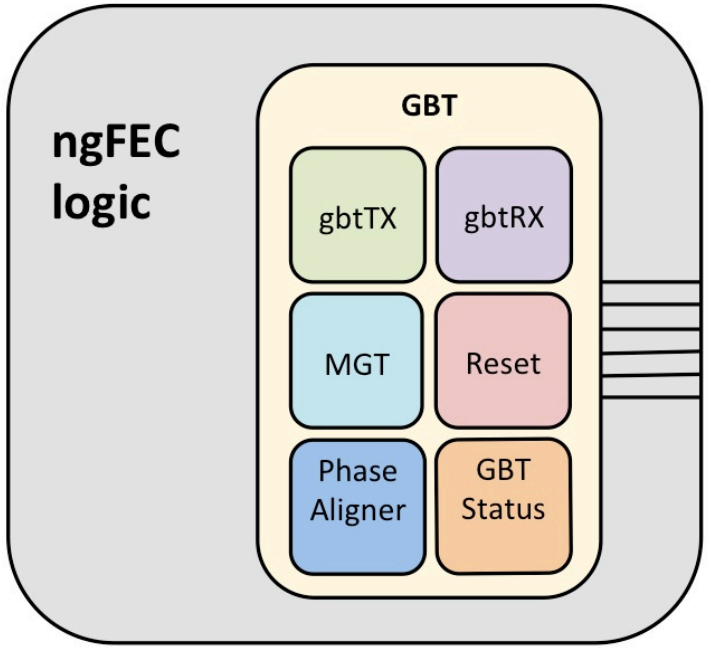
Paths and timing delays between components are constrained

Results

Original Implementation (2012)



New Implementation (2014)



New design is modular, easier to update and uses fewer resources

Results

2 GBT Link Connection

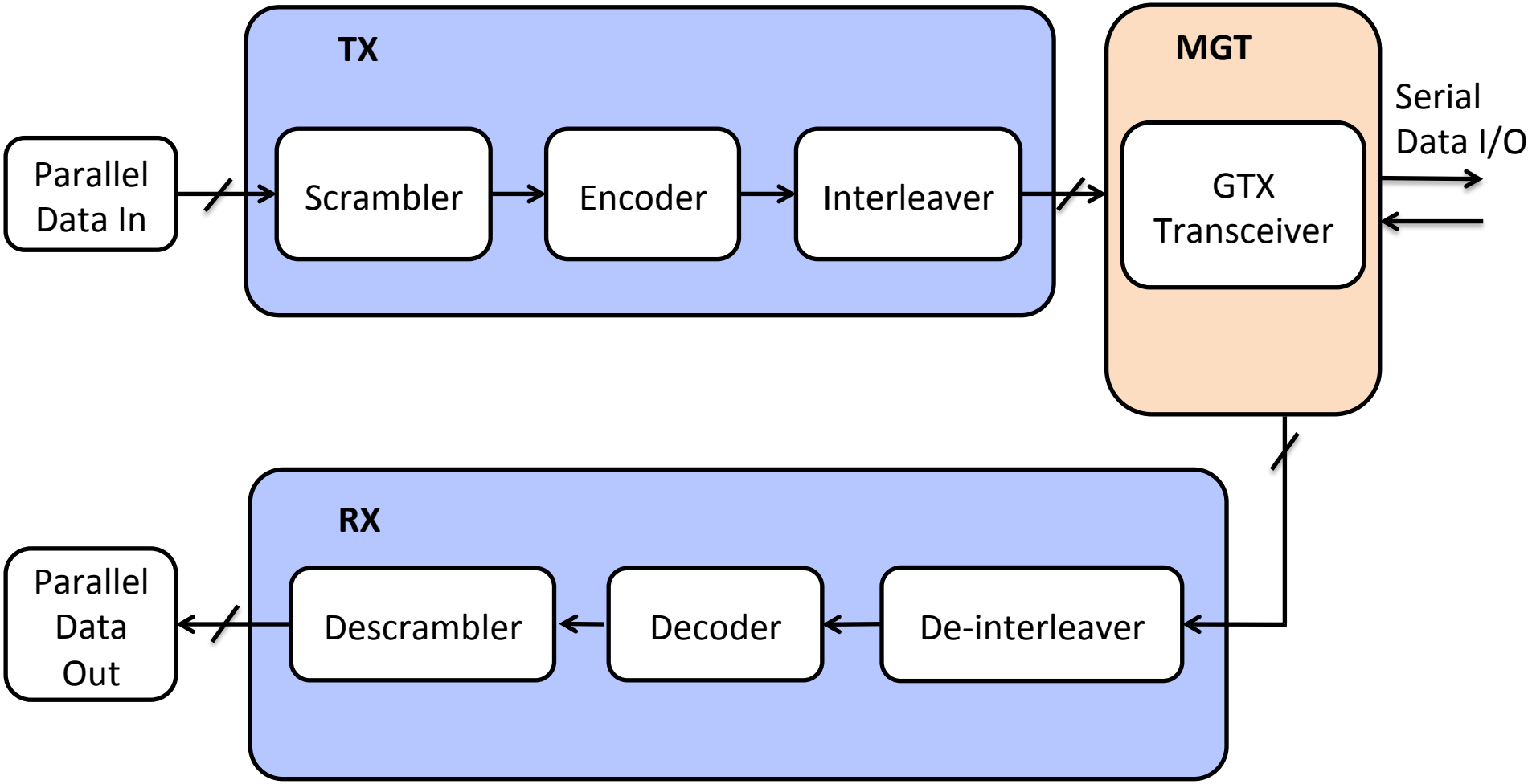
Resource Type	Resources Used Original Design	Resources Used New Design	Resources Available
Slice Registers	24,409 (15%)	24,583 (15%)	160,000
BRAM	108 (40%)	112 (42%)	264
MMCM ADVs	7 (70)%	6 (60%)	10
BUFG	26 (81%)	24 (75%)	32

New GBT implementation uses fewer limiting resources

Thank you!

Back Up Slides

What is GBT?


TX
Parallel Data In
Scrambler
Encoder
Interleaver
MGT
GTX Transceiver
Serial Data I/O
RX
Parallel Data Out
Descrambler
Decoder
De-interleaver

Scrambling

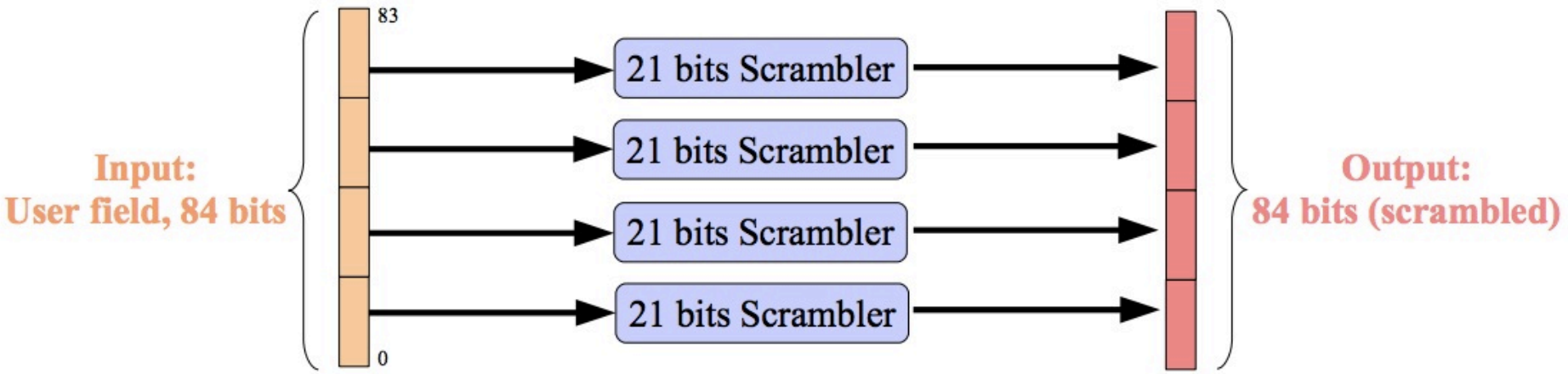


Image source: Implementing the GBT data transmission protocol in FPGAs, Frederic Marin

DC Balancing: Reduces bit errors due to long sequences of ‘1’s

Reed-Solomon Encoding

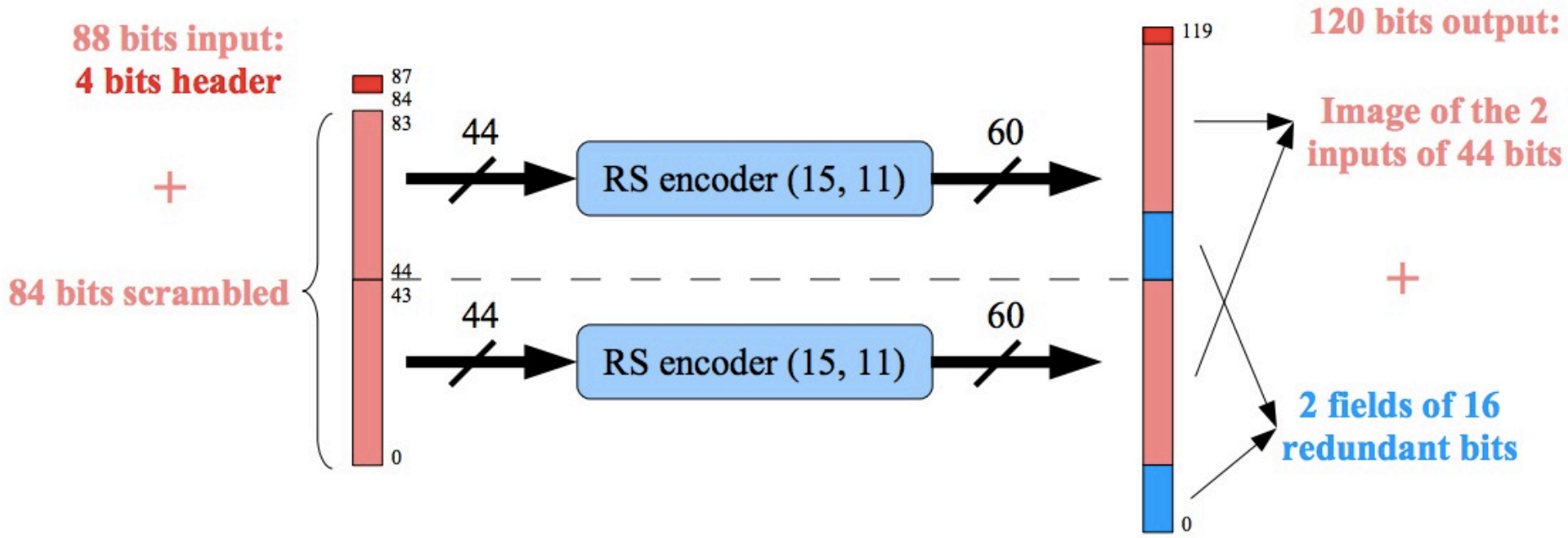


Image source: Implementing the GBT data transmission protocol in FPGAs, Frederic Marin

Protects against transmission errors

Interleaving

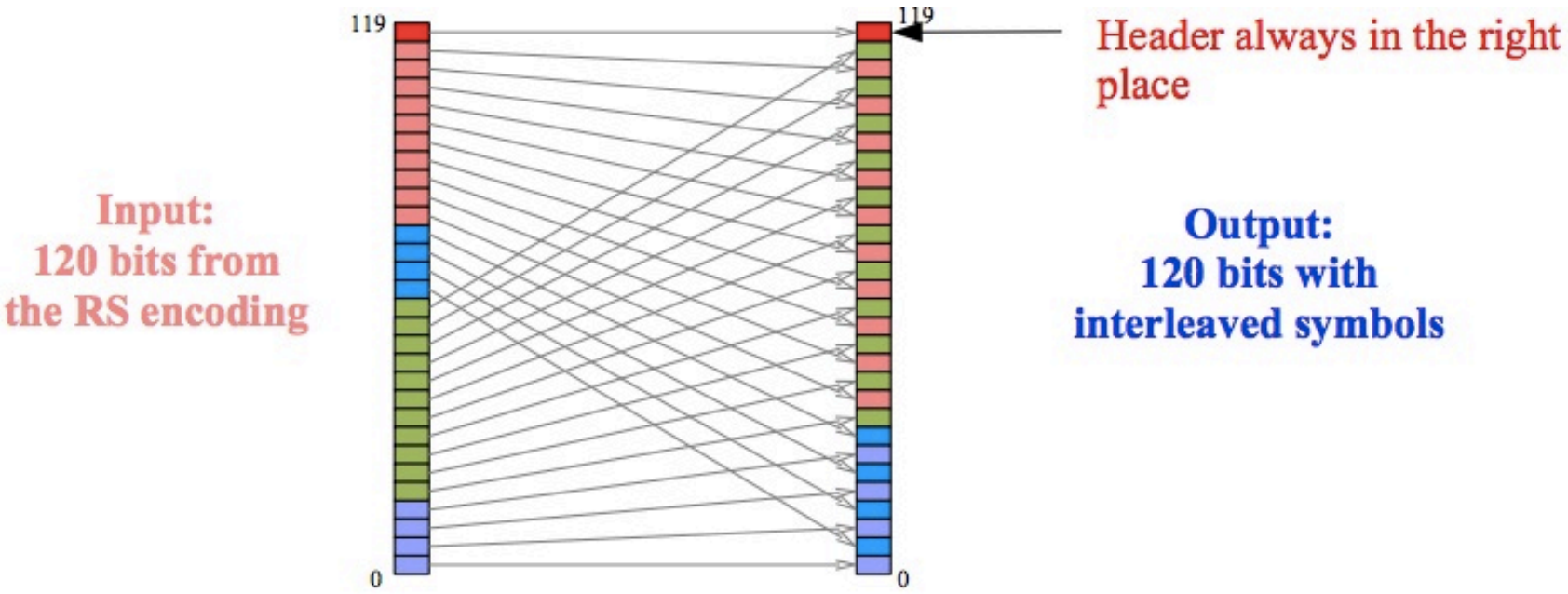


Image source: Implementing the GBT data transmission protocol in FPGAs, Frederic Marin

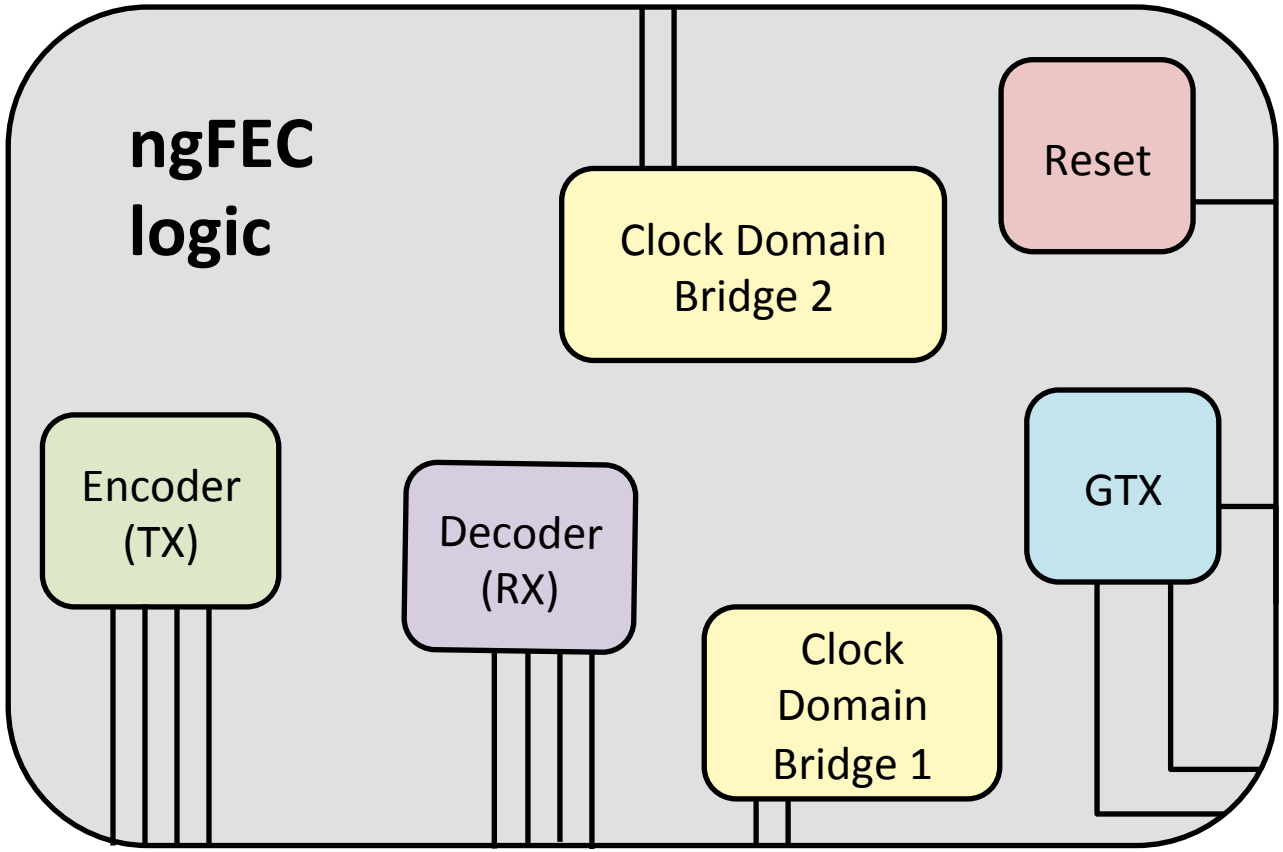
Improves error correction after long bursts of errors

Original GBT Implementation

Older GBT implementation (2012)

Not modular

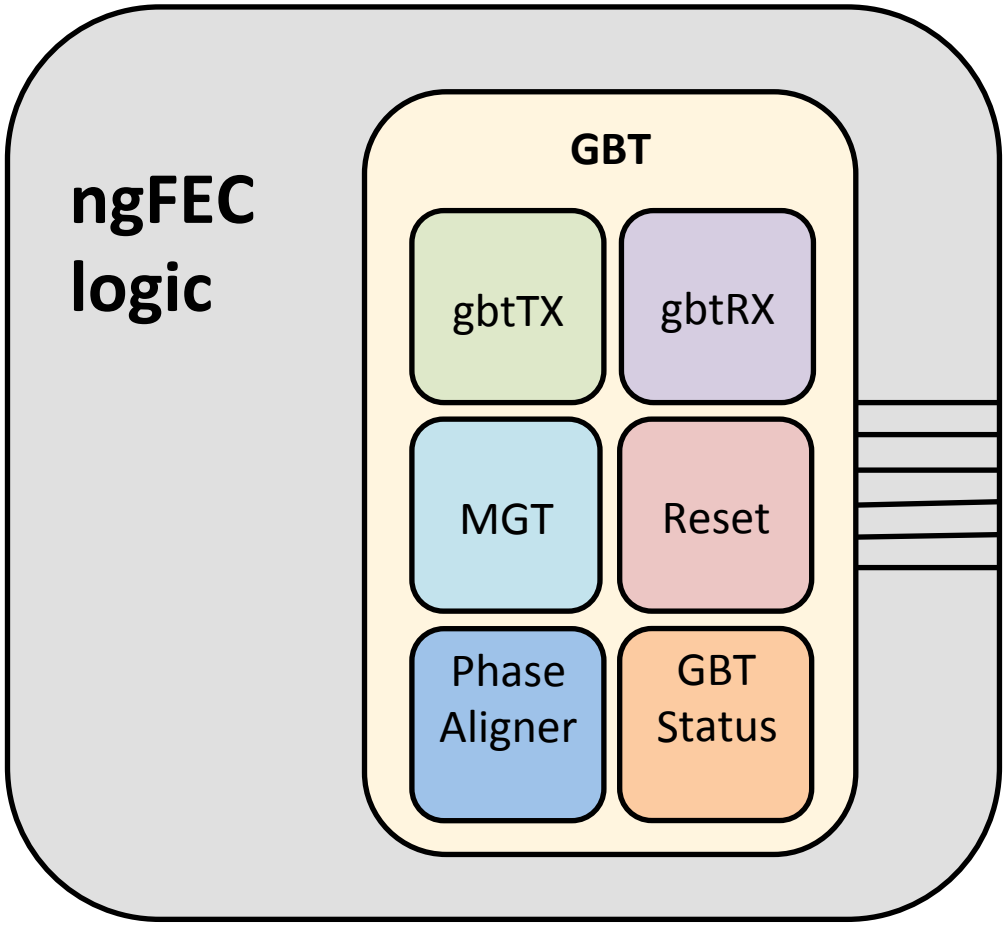
Tricky to update



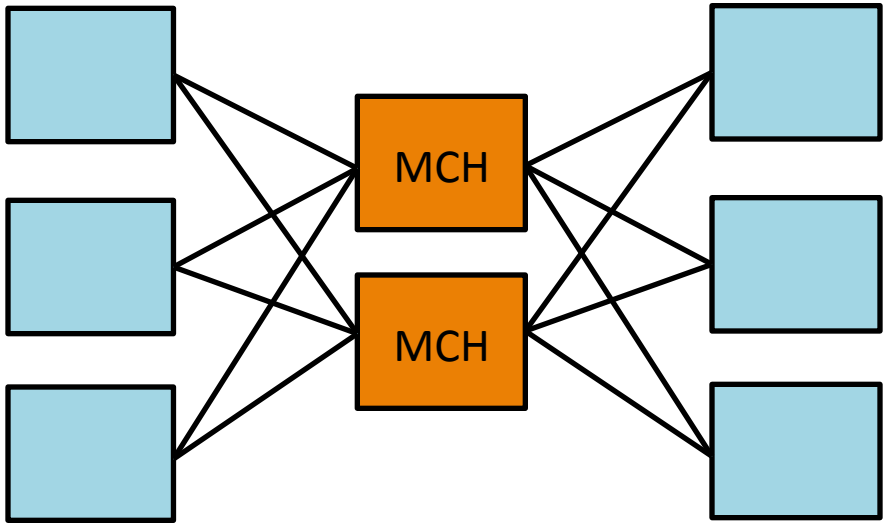
Updated GBT Implementation

More recent design (2014)

Modular, easier to update



MicroTCA Standard



MicroTCA is replacing out-dated VME Standard at CMS

<u>MicroTCA Advantages:</u>

- Compact
- Power Efficient
- Dual star topology
- Hot swappable
- Industry users

Phase Locked Loop

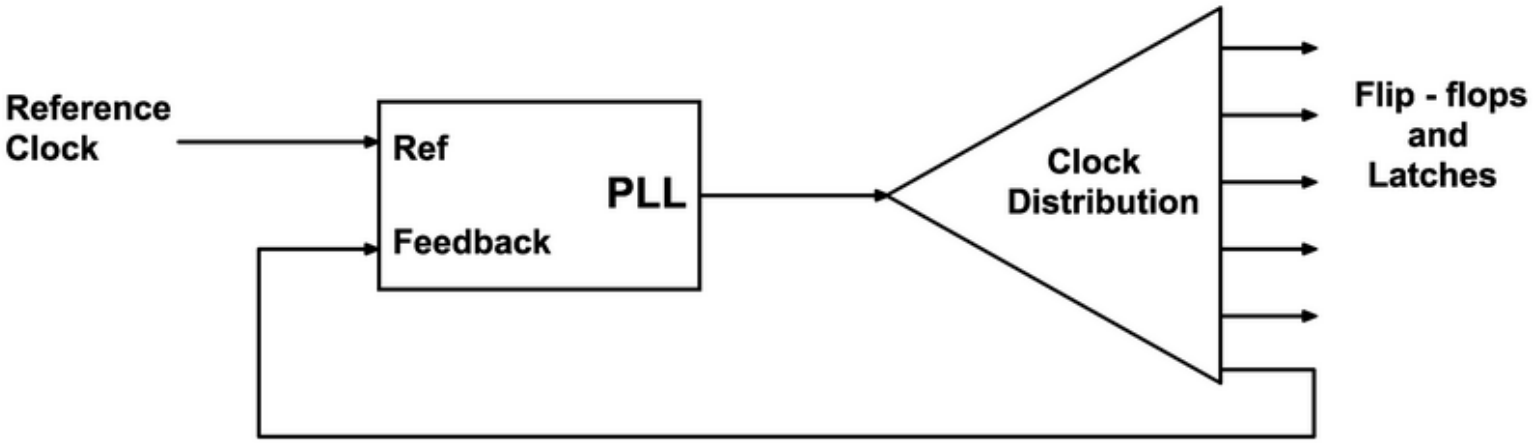


Image source: wikimedia commons

GLIB

Image: GLIB Project

DESY Test Set-Up