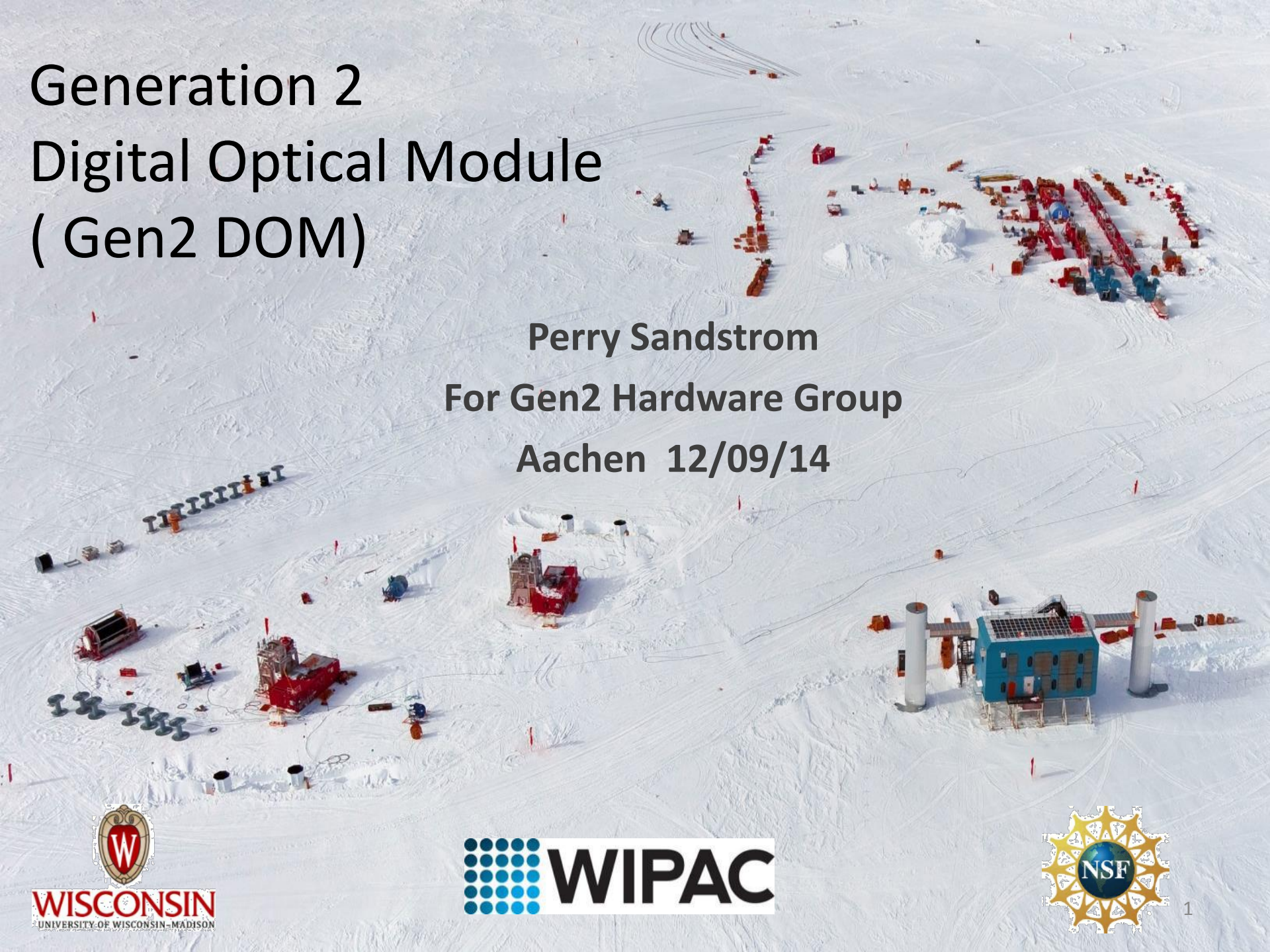
Generation 2 Digital Optical Module (Gen2 DOM)



Perry Sandstrom

For Gen2 Hardware Group

Aachen 12/09/14

WISCONSIN
UNIVERSITY OF WISCONSIN–MADISON

WIPAC

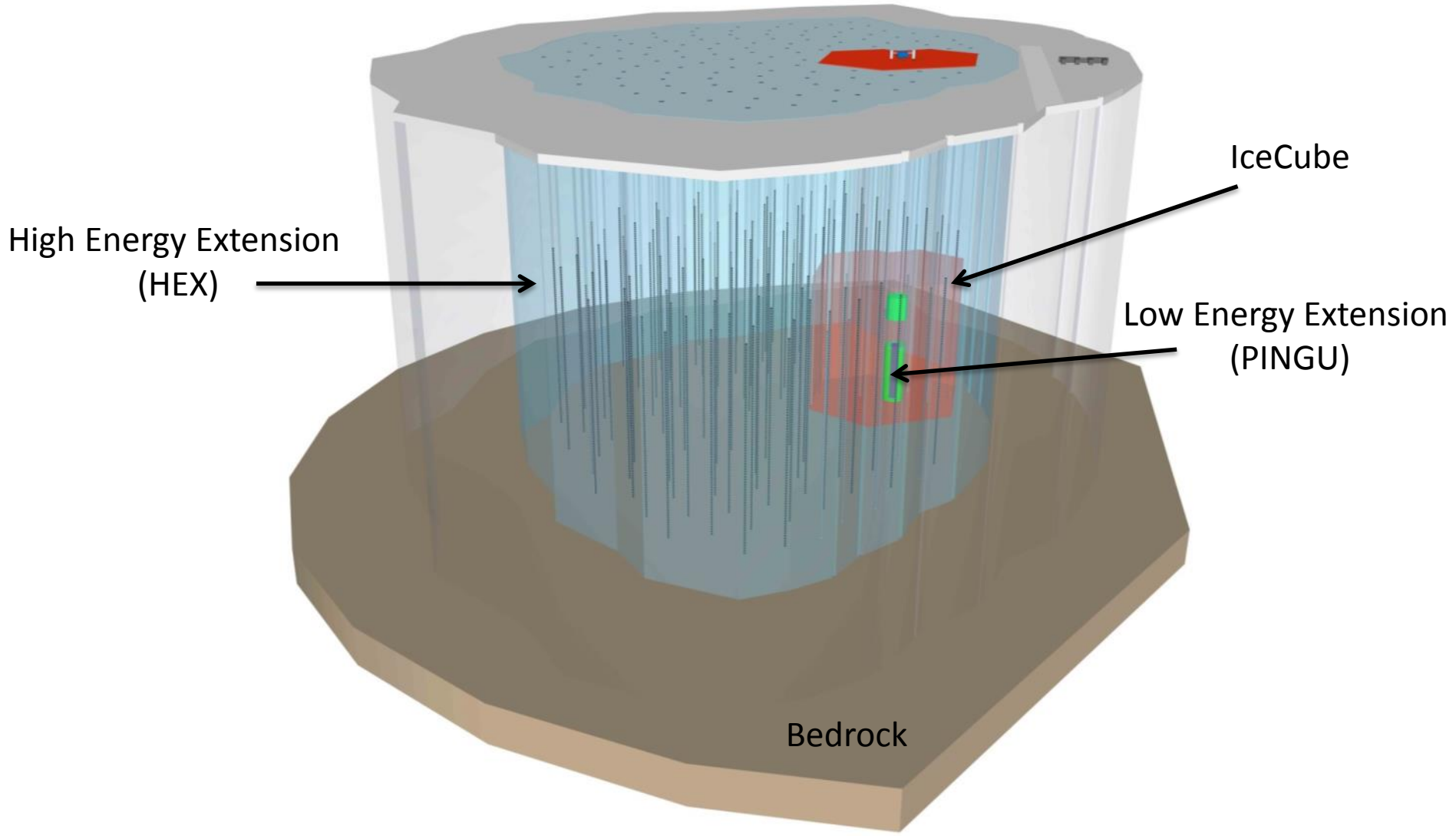
NSF

Gentoo Penguin

A fast-swimming bird (and LINUX Variant)

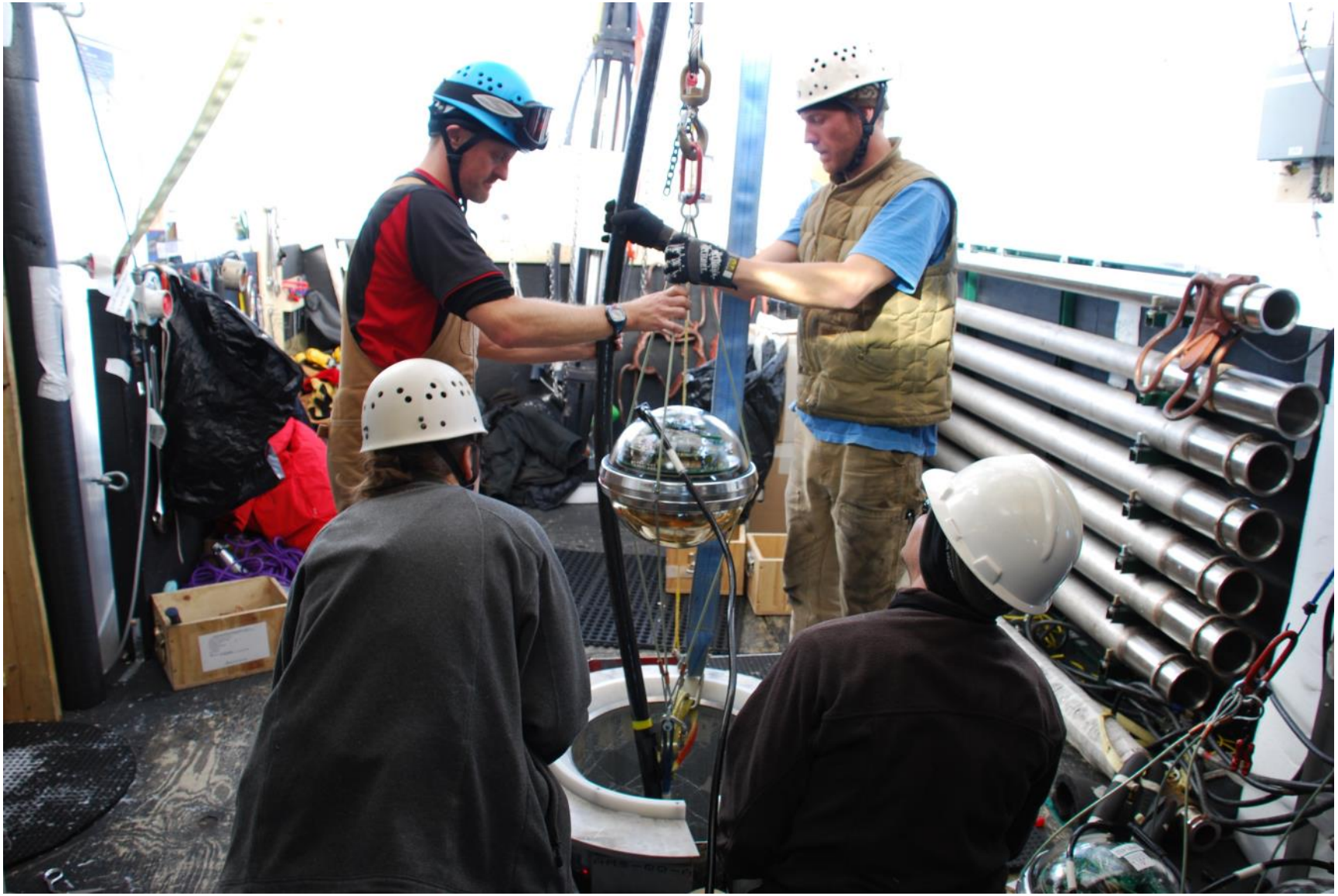
World Wildlife Fund

Possible Extensions to IceCube



"PINGU" = **P**recision **I**ceCube **N**ext **G**eneration **U**pgrade

DOM Deployment



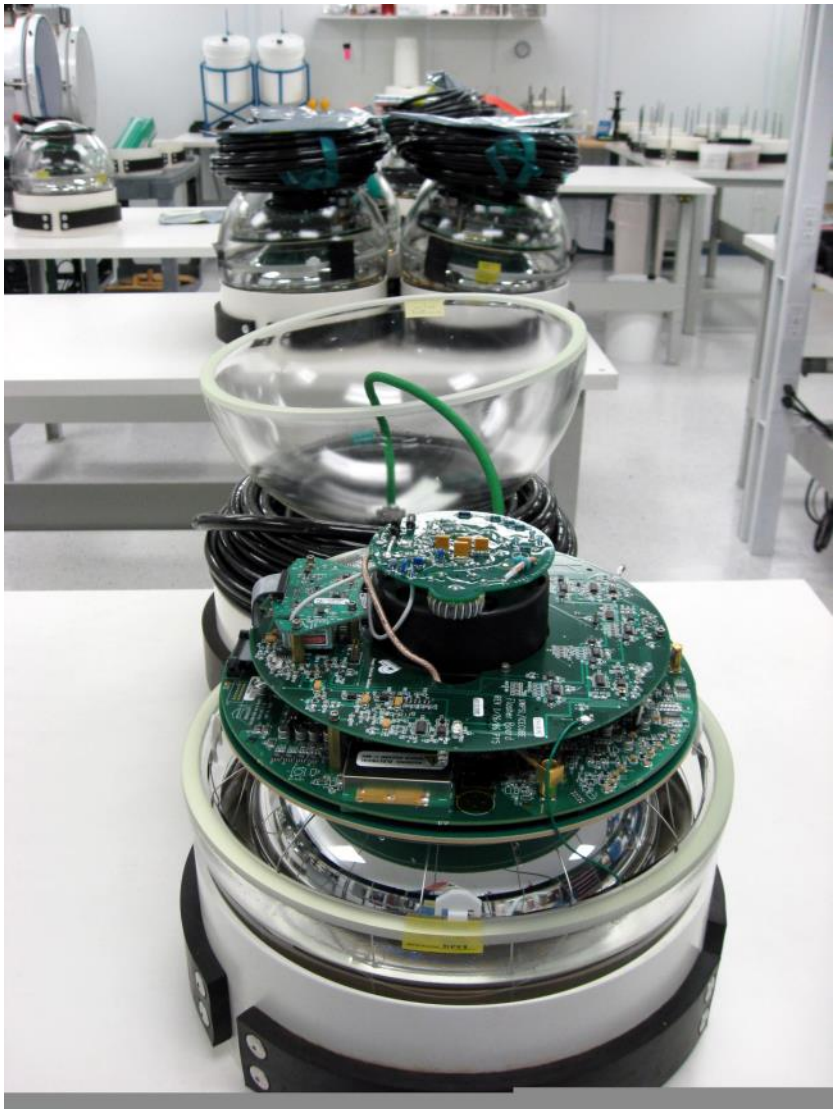
DOM going down the hole

Total of 5160 (Gen1) DOMs now frozen into the icecap

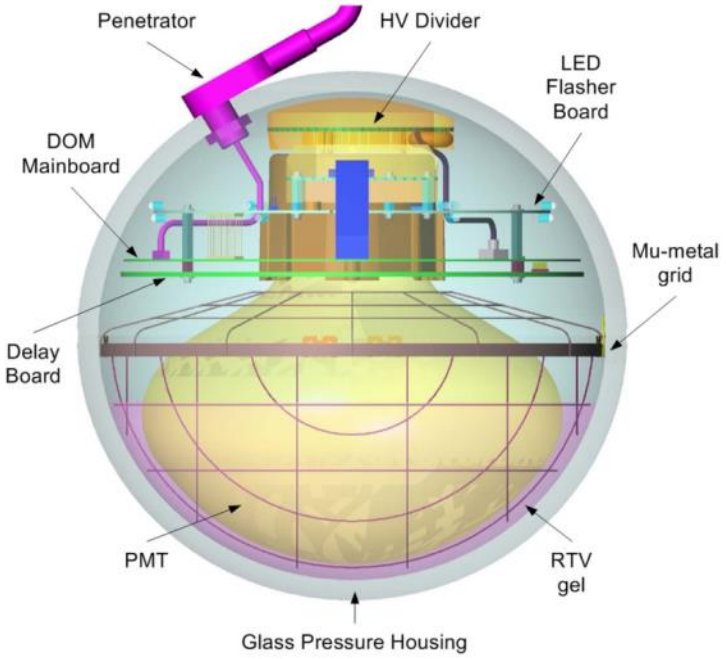
> 99% Survived Deployment

IceCube DOM Fabrication (3-sites)

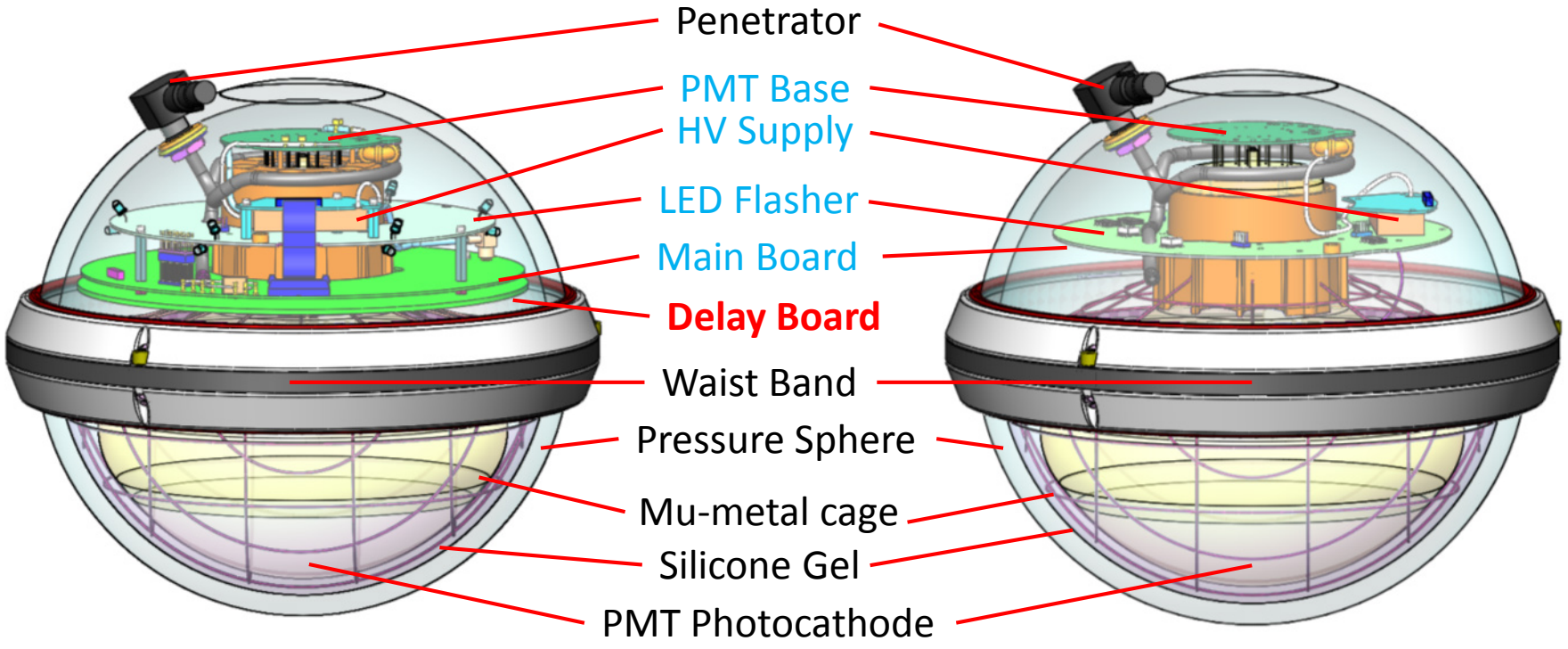
Quality of Gen1 design was a major key to IceCube's success



- Records PMT Waveform of every "hit"
- Timing synchronization between all DOMs <2ns
- Data/Timing/power over 3.3 km copper pair
- Power consumption ~3W
- Withstand > 8000 PSI freeze-in pressure
- Survive shock-vibration; ships, planes, sleds
- Built-in gel cushioning for PMT & electronics
- ESD proof



Gen2 DOM Design



IceCube DOM

Gen2 DOM

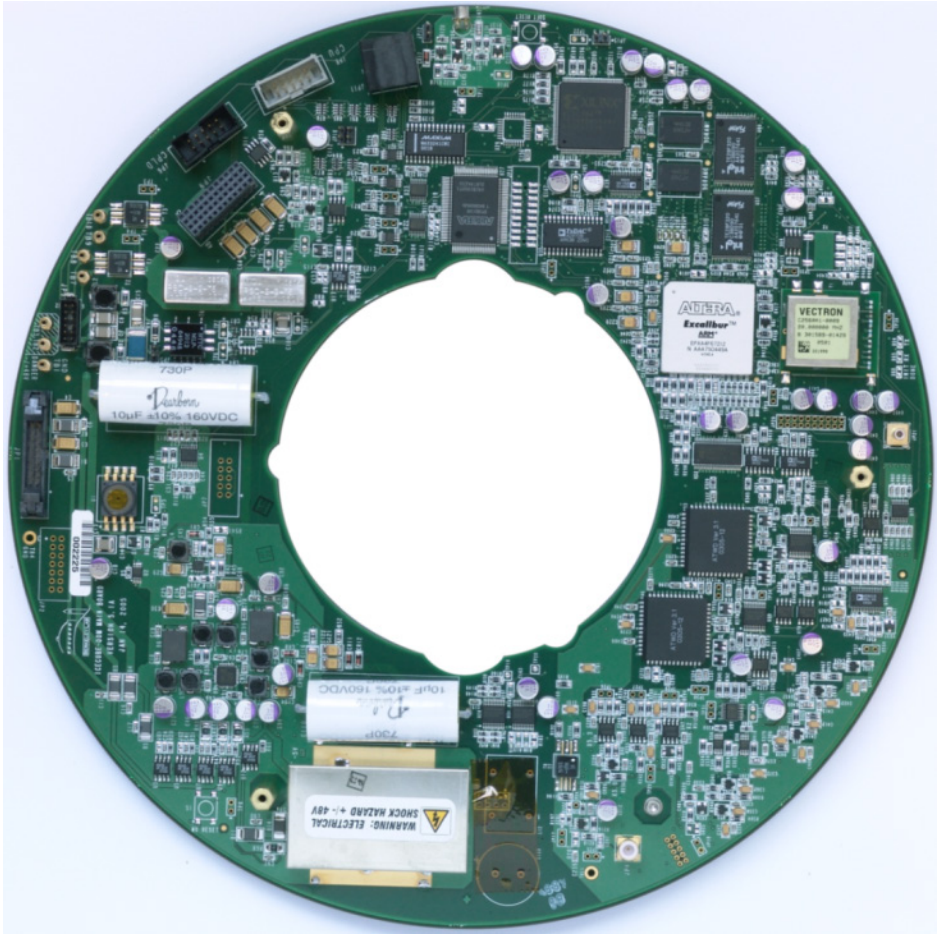
KEY:

Component identical

Component eliminated

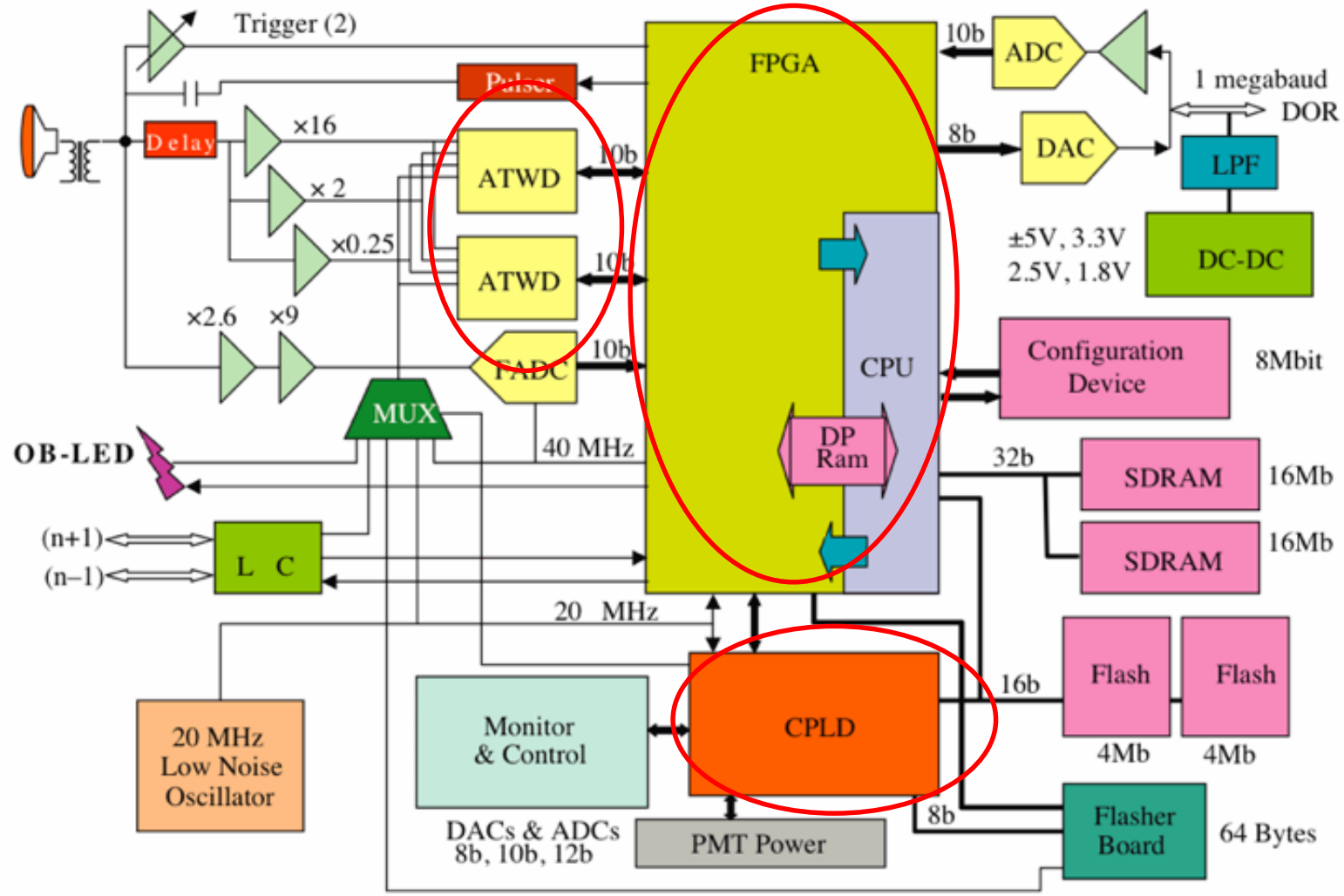
Component re-designed

IceCube DOM Main board (LBNL)



- High Reliability Components
- Thorough design verification
- ~5 (early) revisions then FROZEN
- DFM- Design for Manufacture
- Good vendor for PCB assembly
- IPC610 Class2 on Class3 line
- PCB: IPC Class3 w/no rework
- HASS screening (Temp & Vibration)
- Built in Self-Test

IceCube DOM Block Diagram



Obsolete or unavailable in quantity

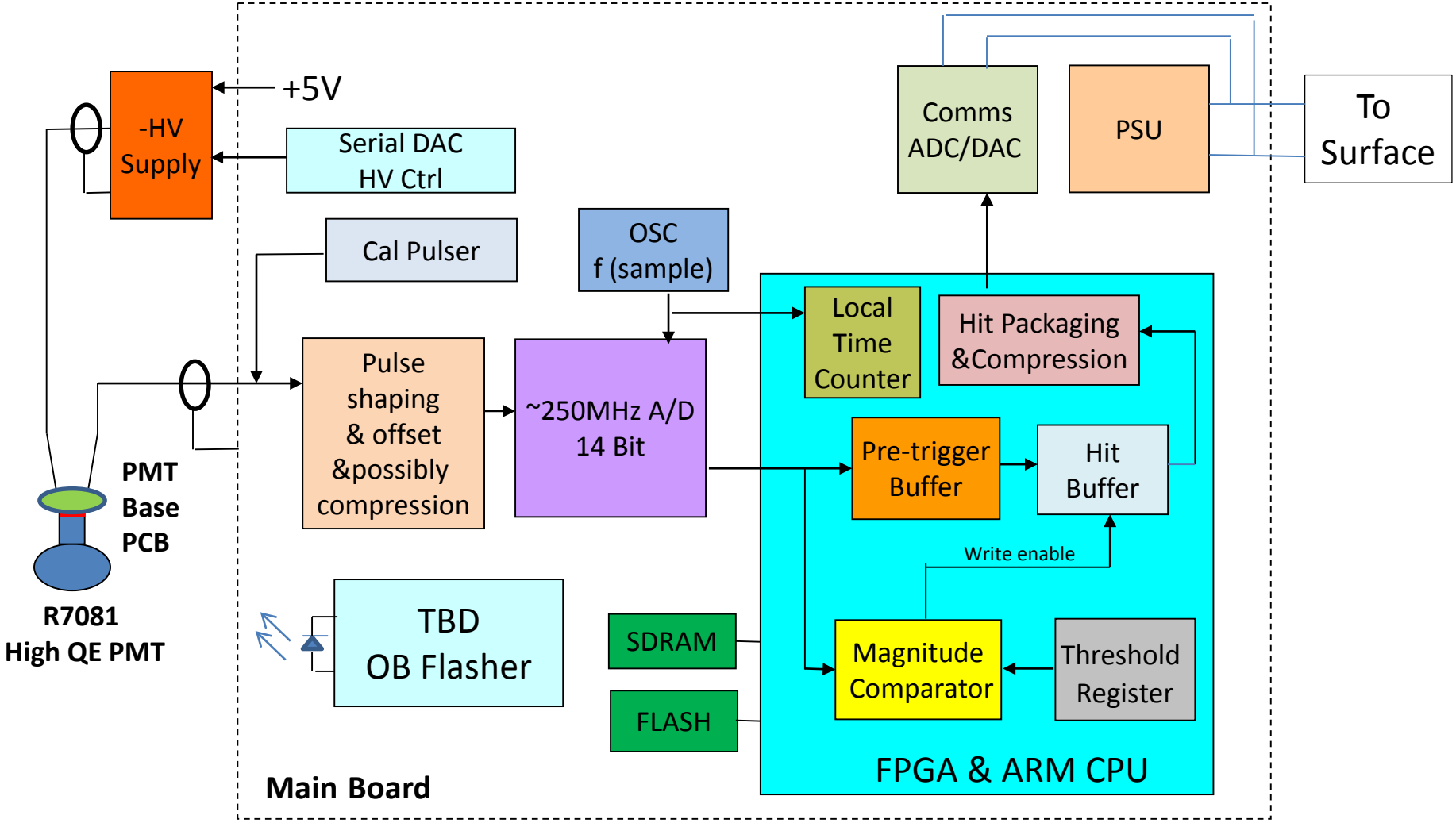
Gen2 DOM Design Upgrades

Change:	IceCube	Gen2 DOM	Rationale
PMT digitizer	triggered record	continuous	new technology allows high speed, low power Analog-Digital Converters
Waveform format	fixed length	variable length	digital discriminator detects waveform duration (Time Over Threshold)
Local coincidence	hardwired	none	better hit compression; simpler cabling & electronics
DOMs per wire-pair	1 “U” + 1 “T” types	4 identical	easier DOM manufacture; smaller cables

Significant Part Reduction Opportunity

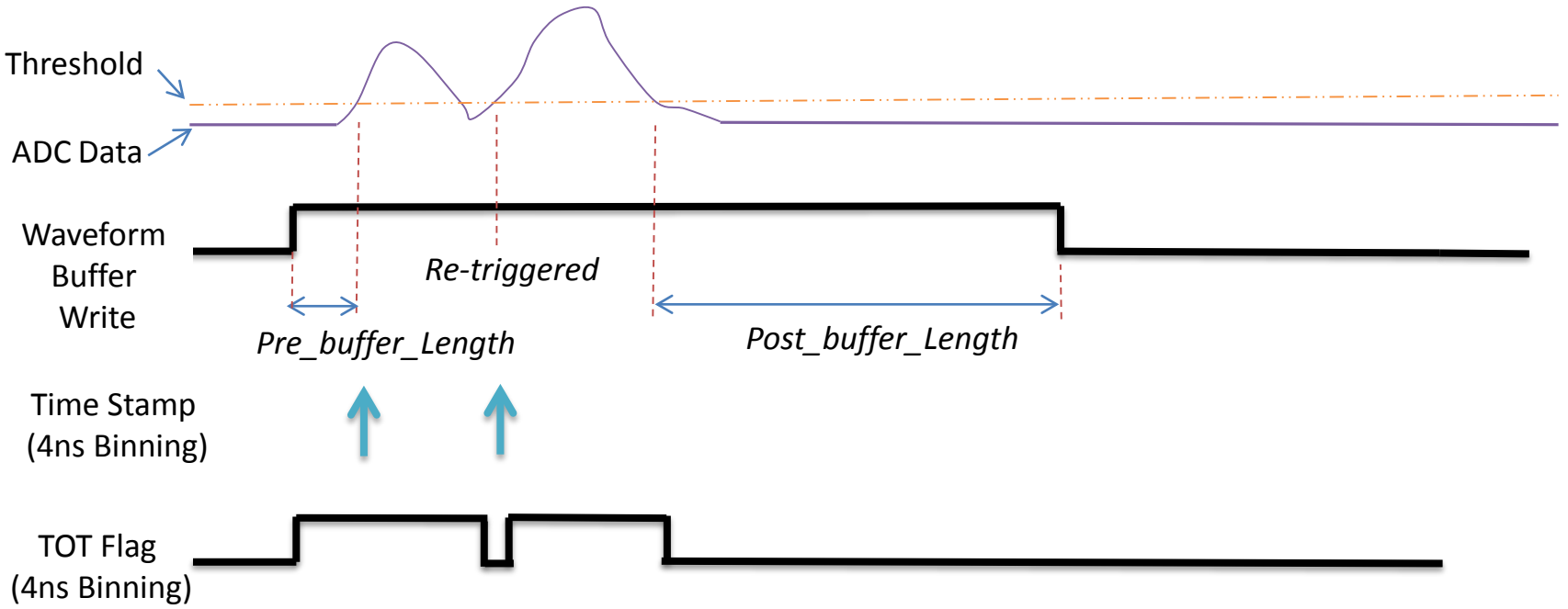
- Gen2 DOM Design Eliminates:
  - Delay Board
  - Two ATWDs replaced by one fast ADC
  - Most Gain Stages
  - Analog Discriminators
  - Local Coincidence (LC) Components
    - Cable wiring simplification

Gen2 DOM Block Diagram

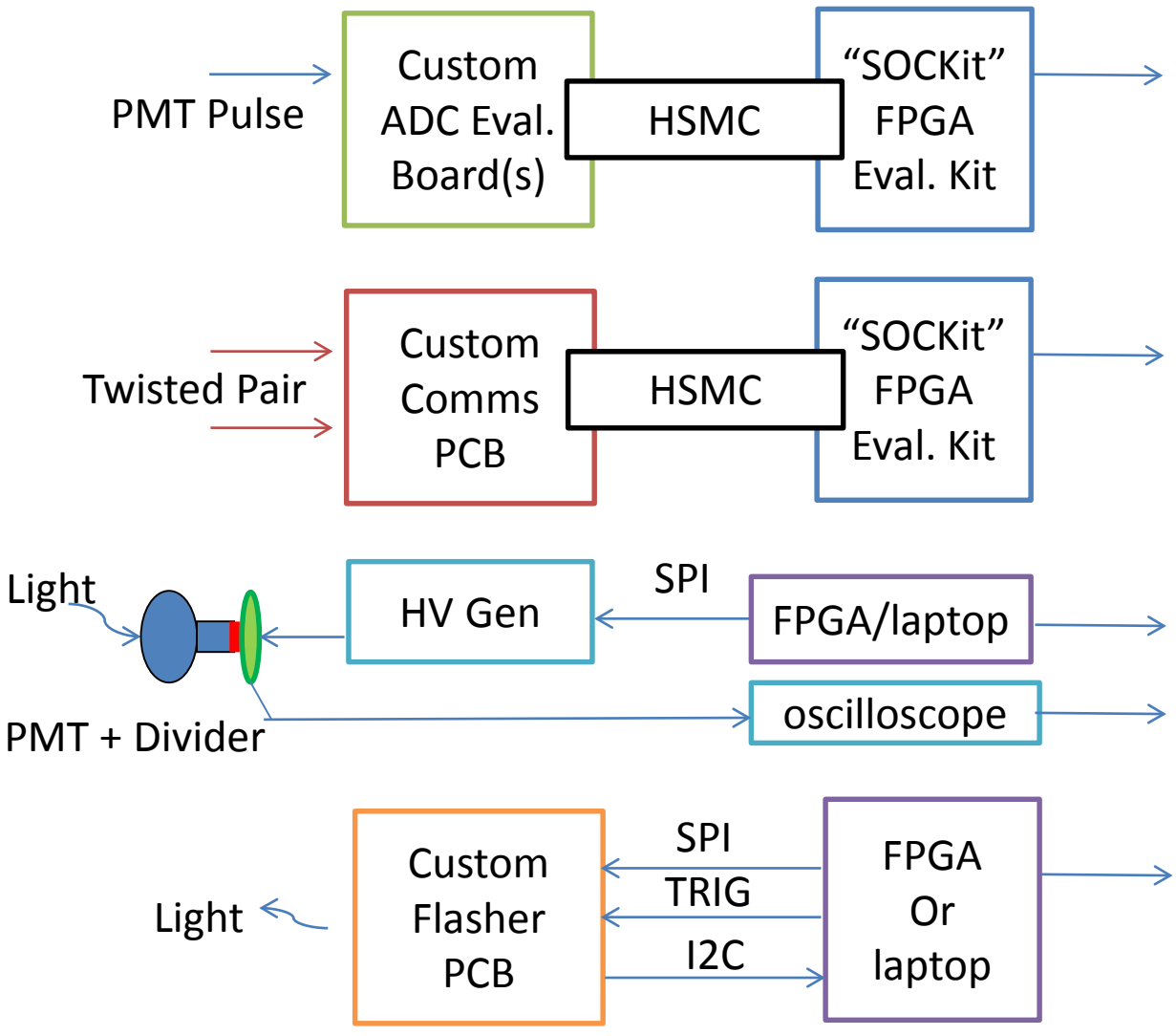


Gen2 Triggering and Buffering

- Pre-trigger buffer (e.g. (16) samples before trigger (replaces delay board)
- Post trigger buffer (e.g (16) samples after falling below threshold
- Waveform buffer (e.g. 16K samples, multi-hit, replaces LBM)



DOM Main Prototyping Sections

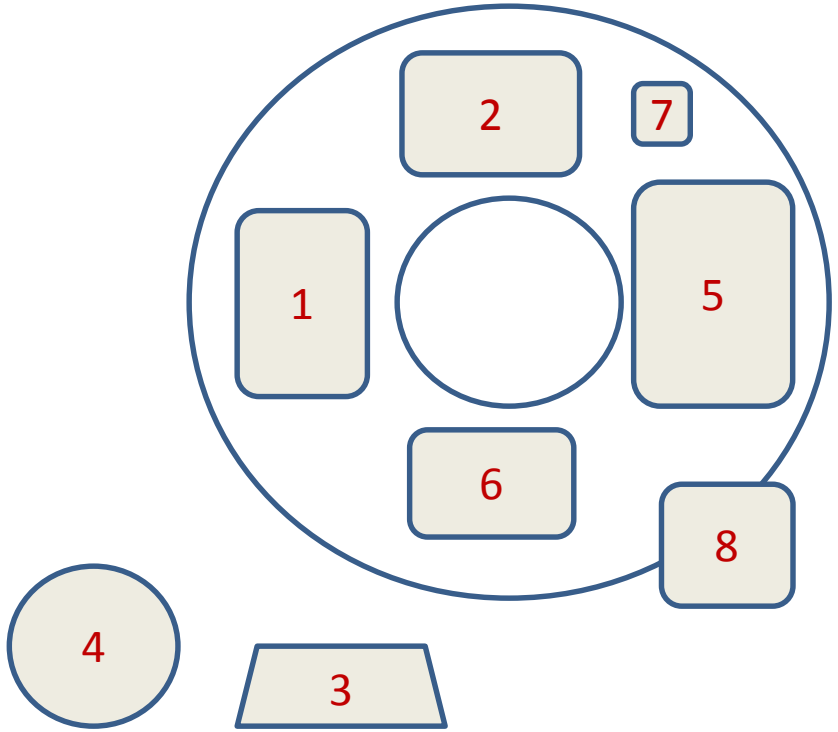


HSMC = High Speed Mezzanine Connector

DOM Electronic Subsystems

Total power consumption target: 1W-2W

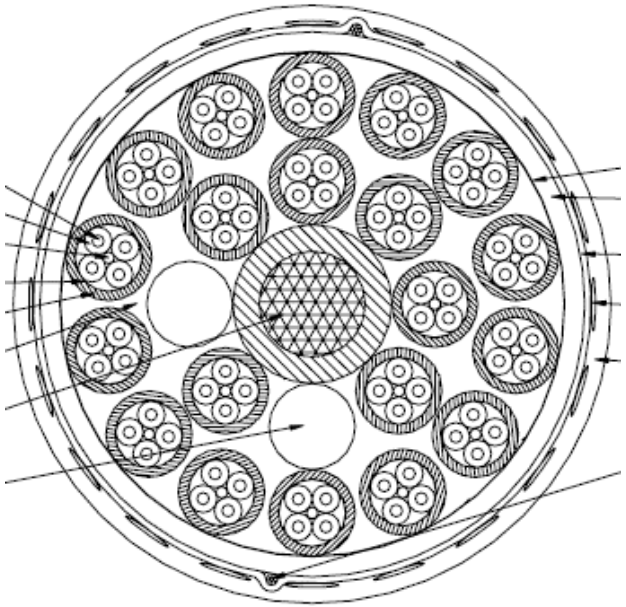
1) Communications/Rapcal
2) Digitizer (with offset & shaping)
3) HV Supply (HVS)
4) PMT Divider (HVD)
5) Logic & Processor
6) Low Voltage Supply
7) Oscillator
8) Flasher
9) Sensor Interfaces



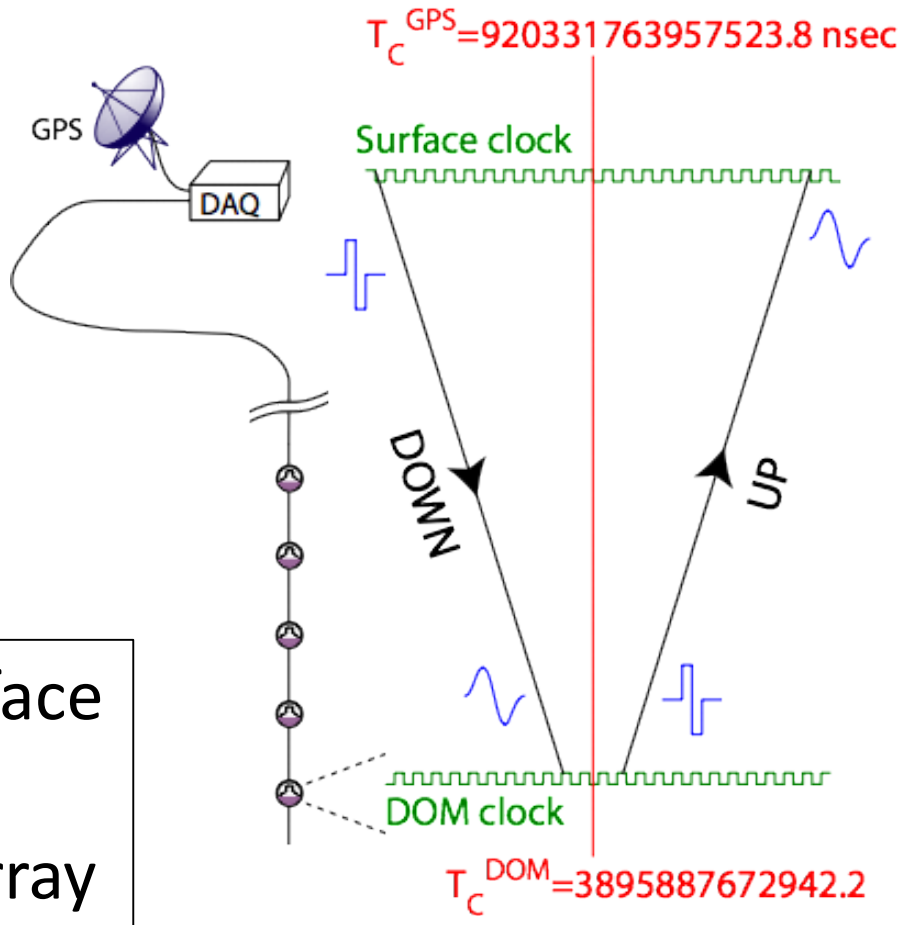
Remote Power, Communications and Timing

Everything happens over *3km long* AWG#19 copper pairs

46mm Diameter Downhole Cable



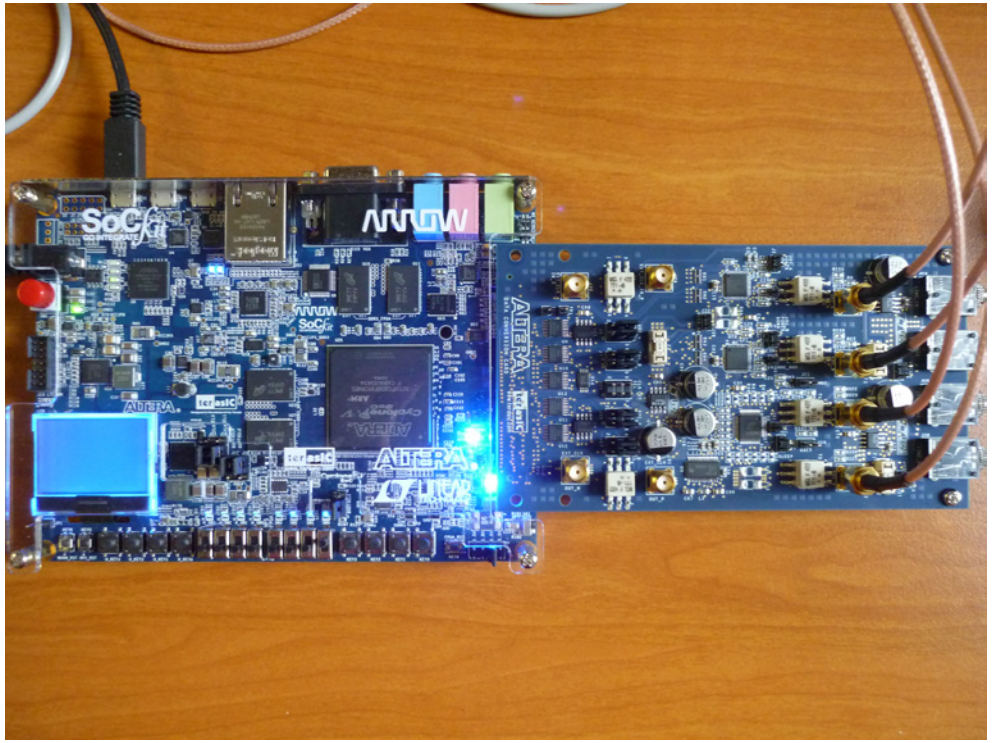
RAPCAL
Reciprocal Active Pulse CALibration



Power: 100V supplied at surface
Comms: 1Mb/s, half duplex
Timing: <2ns across whole array

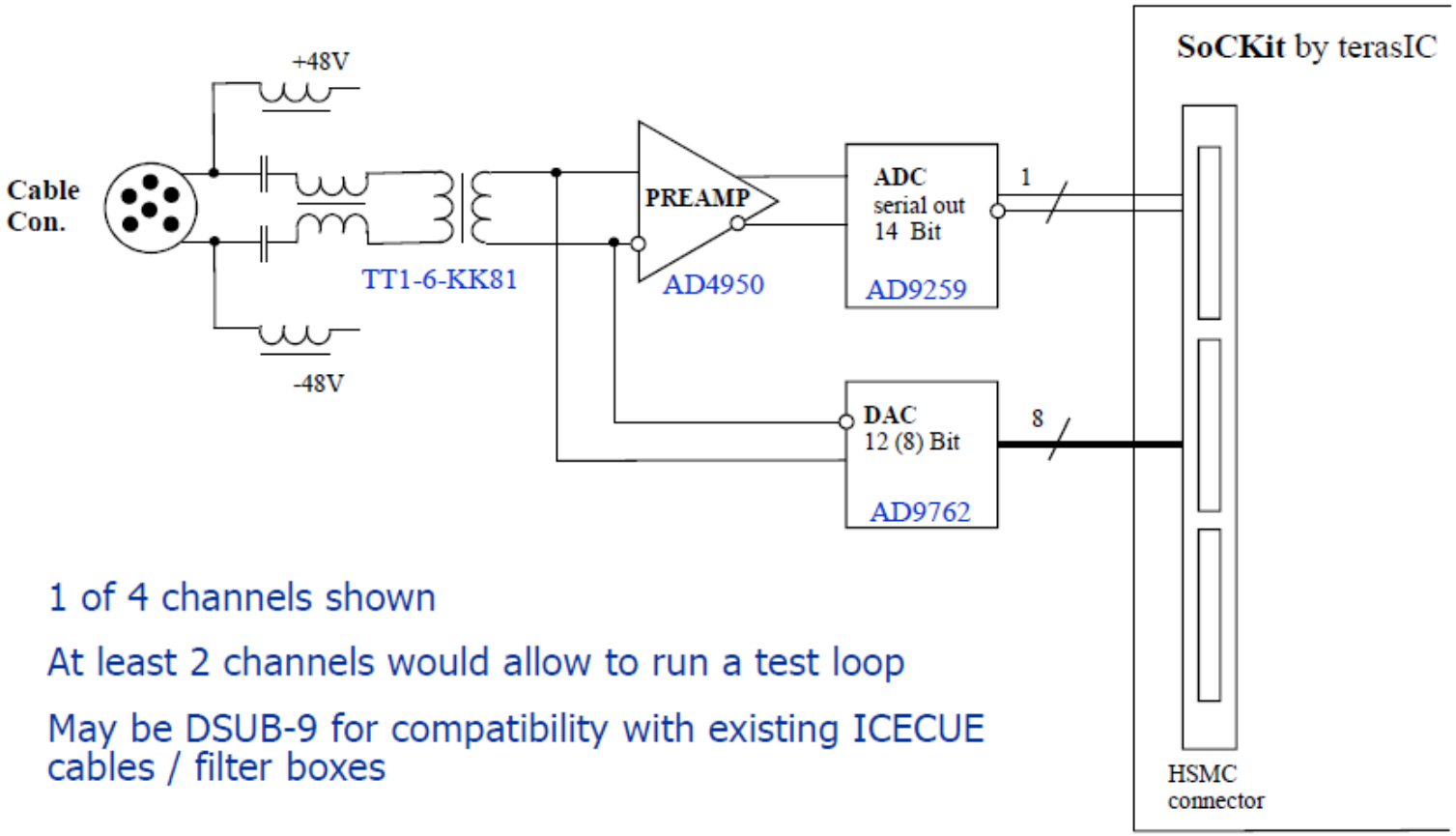
QAM16 Communications Development

- 1st prototype of Gen2 DOM Communications
- Uses Altera SOCKit Cyclone V FPGA Eval. kit
- Uses Commercial Terasic AD/DA Card



Comms Hardware Development

Communications Daughter Card (CDC)

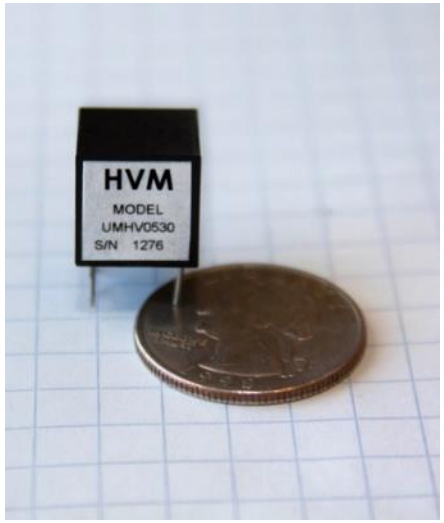


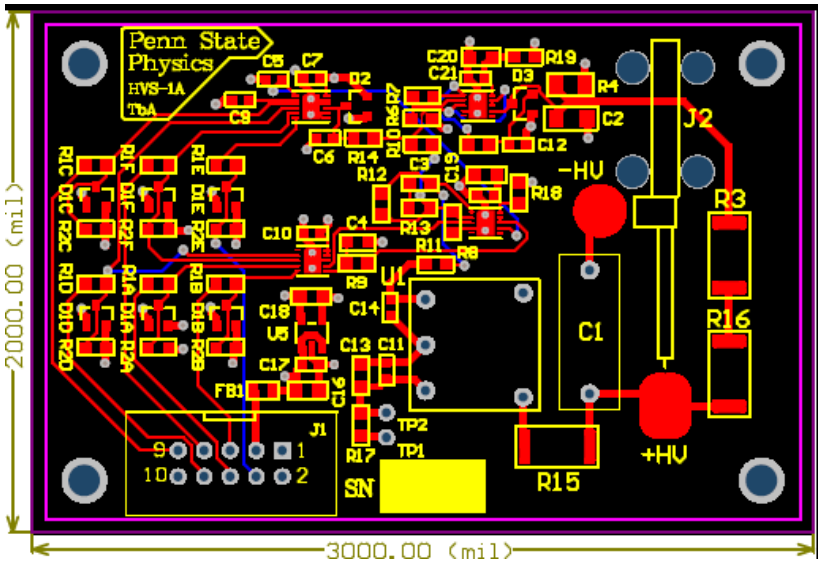
- 1 of 4 channels shown
- At least 2 channels would allow to run a test loop
- May be DSUB-9 for compatibility with existing ICECUE cables / filter boxes

K.-H. Sulanke, *DESY*

GEN2 High-Voltage Supply (HVS)

- Rev1 HVS design now finished at Penn State
- Designed using Altium schematic capture and layout tools
- Platform to investigate EMI, noise coupling
- Power consumption of 100mW vs. 300mW in Gen1 DOM
- Uses military night-vision module; >100k manufactured
- Resonant converter technology; rated -55C

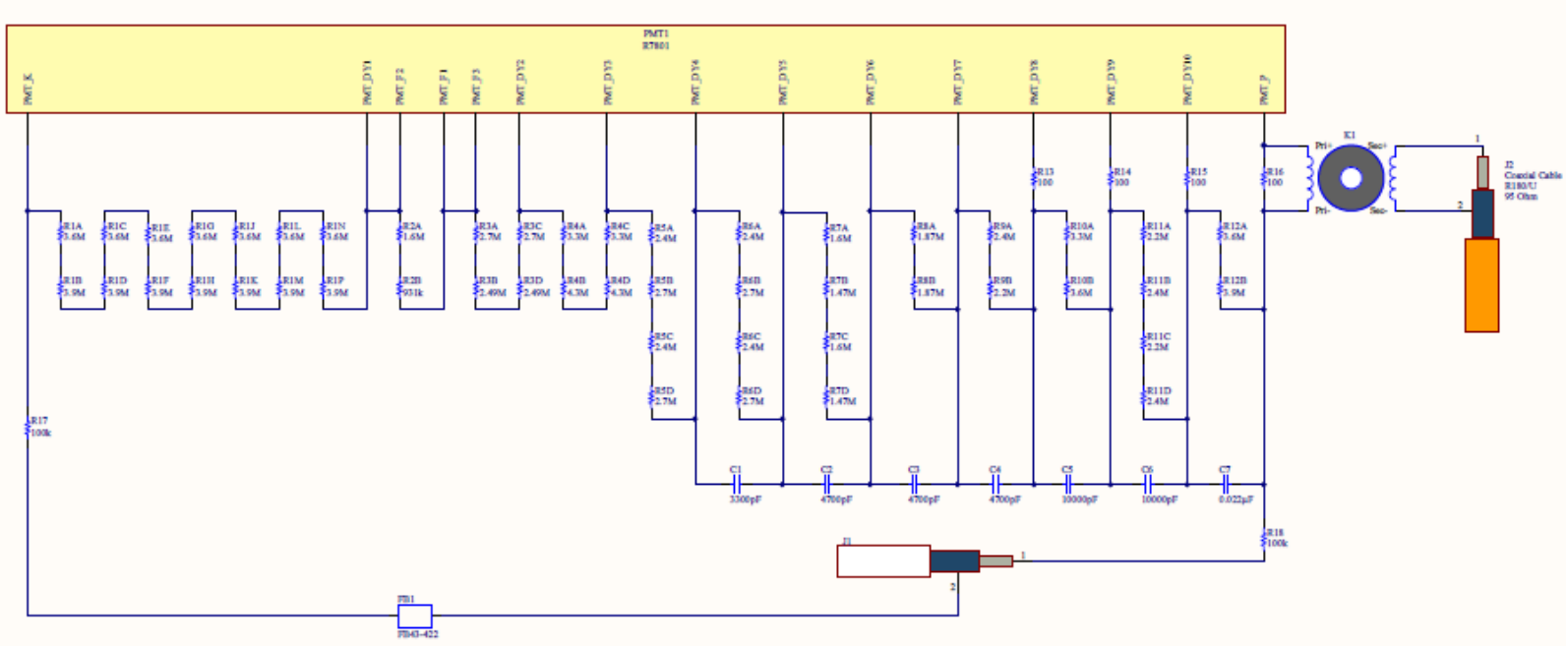




Tyler Anderson - *Penn State*

GEN2 High Voltage Divider (HVD)

- "PMT-base" updated with surface-mount components
- Same component values and performance
- Better de-rating with improved manufacturability
- Options for improved PMT attachment being explored
- Evaluating new toroid design (Gen1 "H" cores now unavailable)



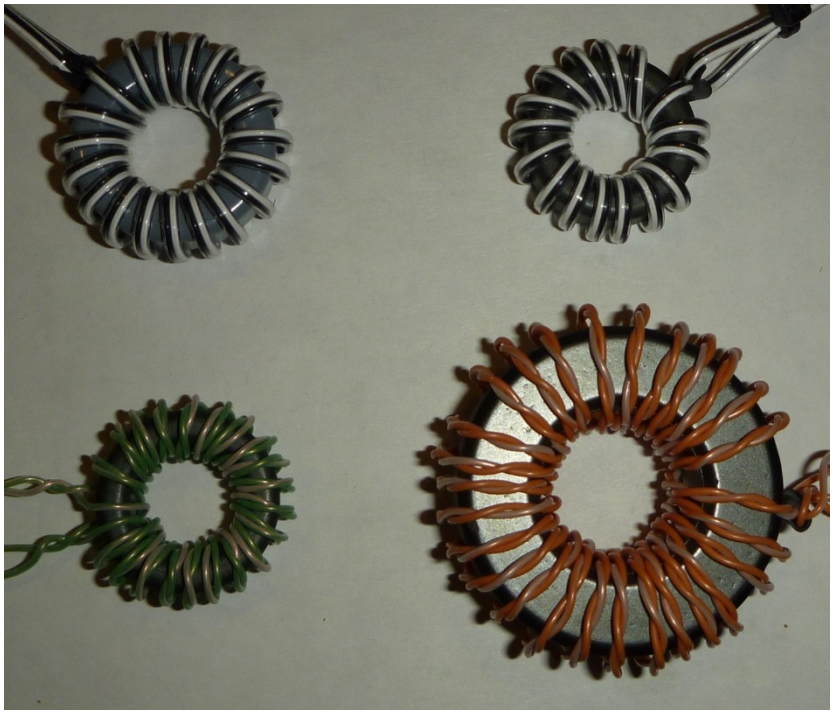
Tyler Anderson - *Penn State*

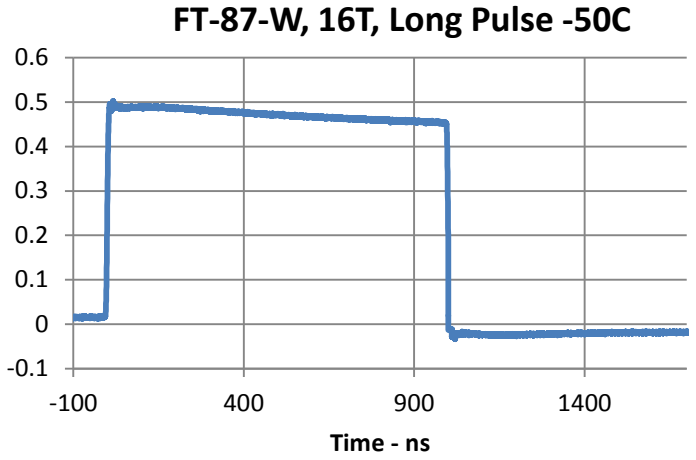
New Toroid Design

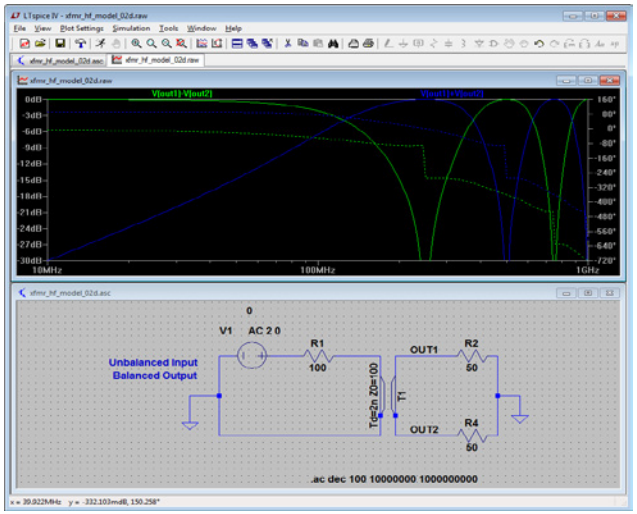
Bench Testing and Simulation

IceCube transformer
18 turns, 15g, 10 x 28 mm

FT-87-W with twin-lead
16 turns, 10g, 9 x 25 mm



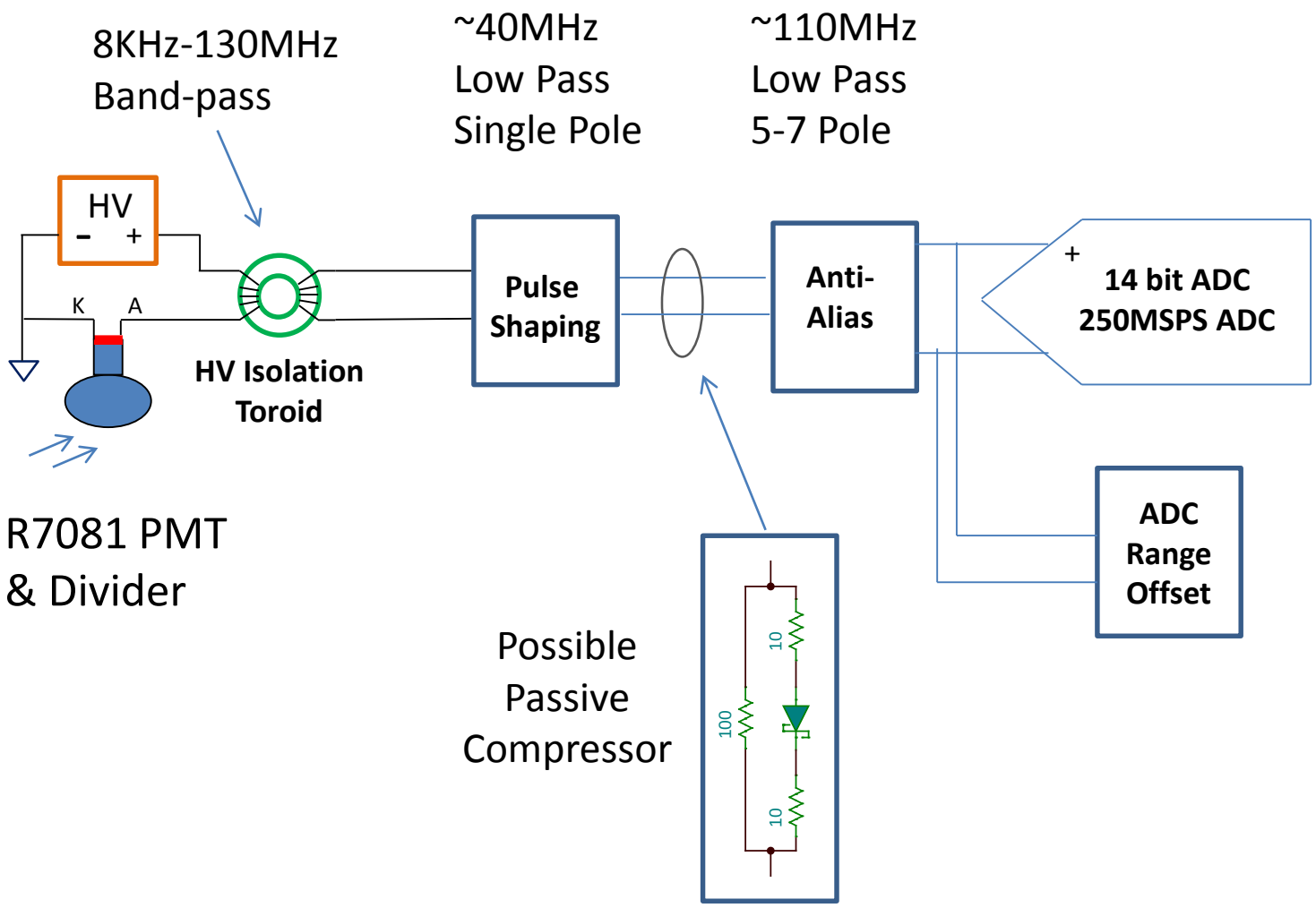




FT-87-W, CAT5e twisted pair
20 turns, 10g, 9 x 25 mm

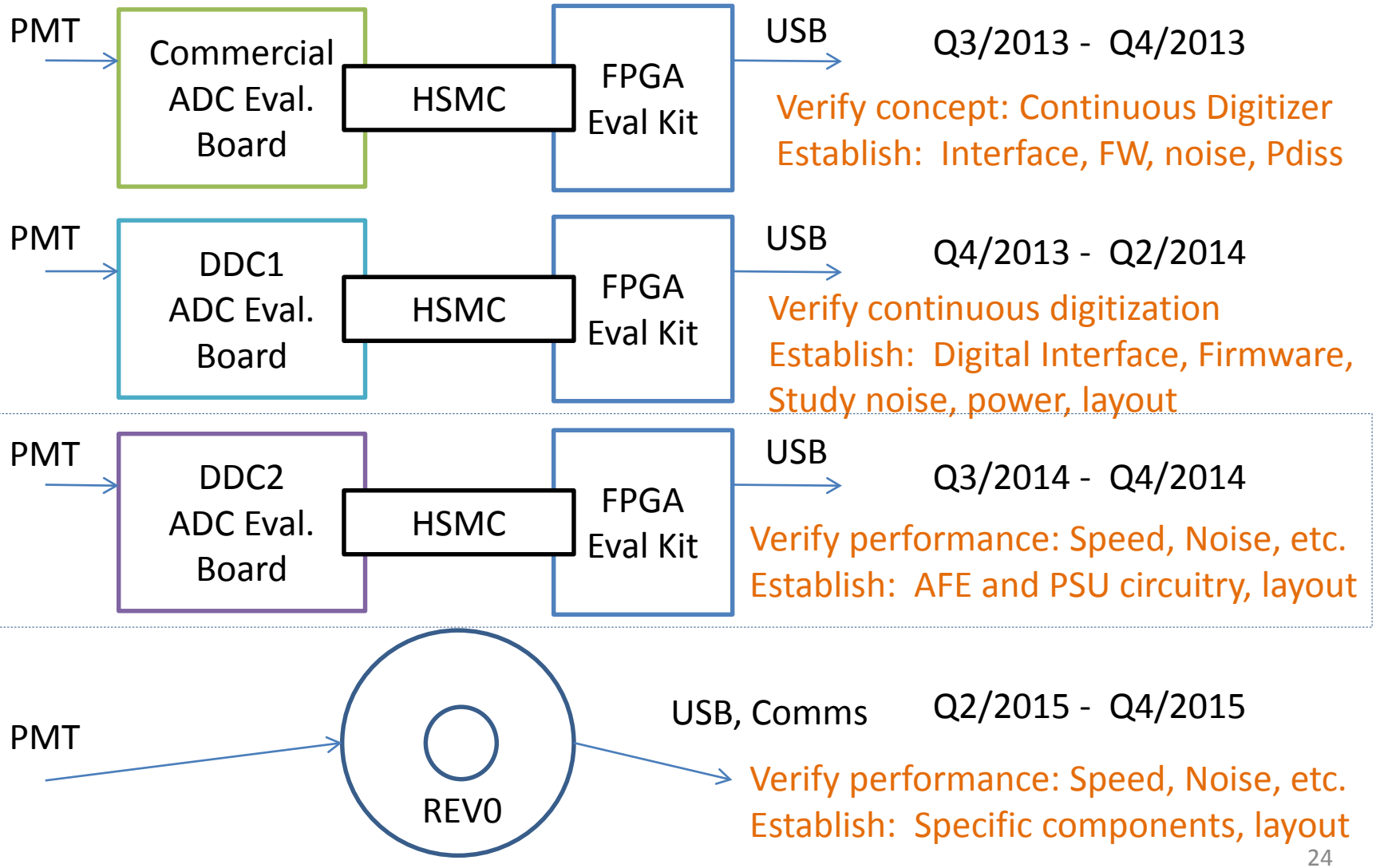
FT-150-W, CAT5e twisted pair
27 turns, 59g, 16 x 40 mm

PMT Signal Path

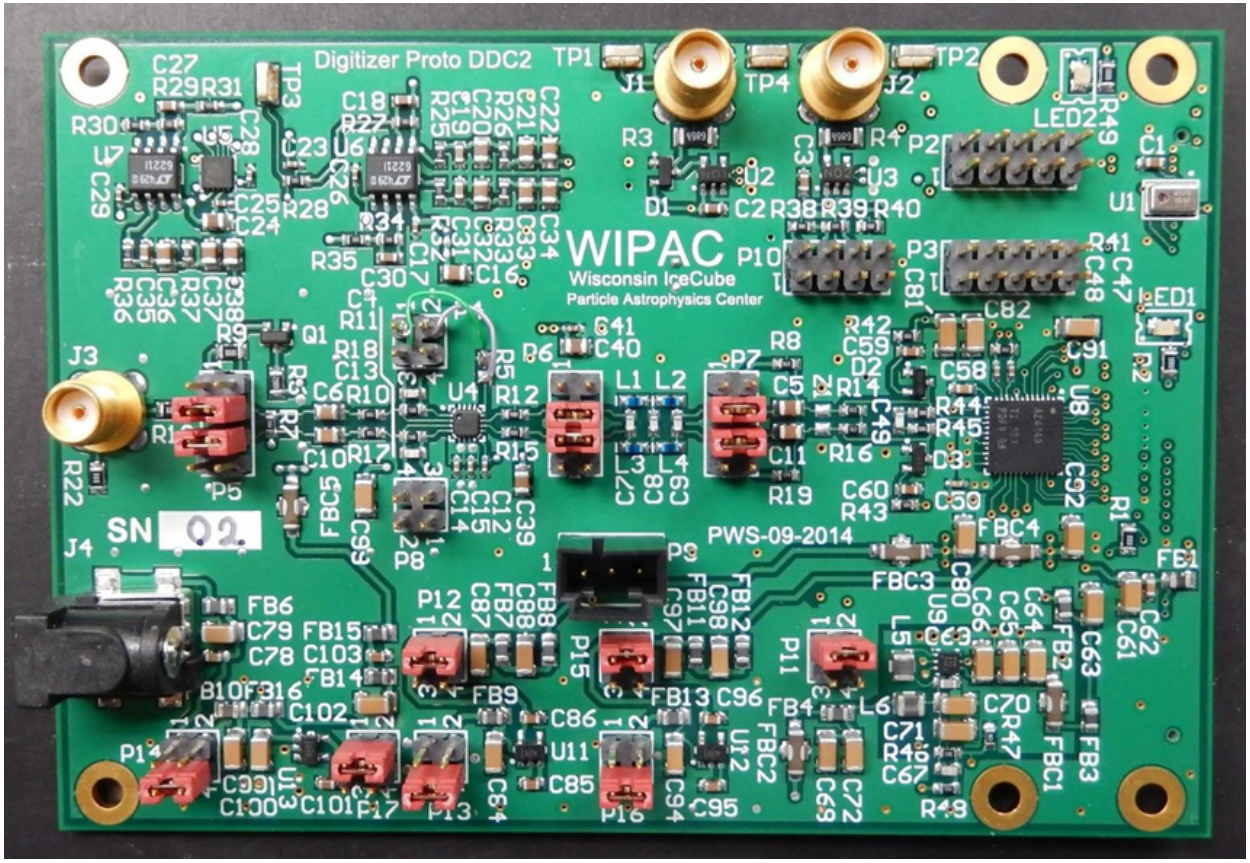


Gen2 Digitizer Prototyping Sequence

(DDC=Digitizer Daughter Card)

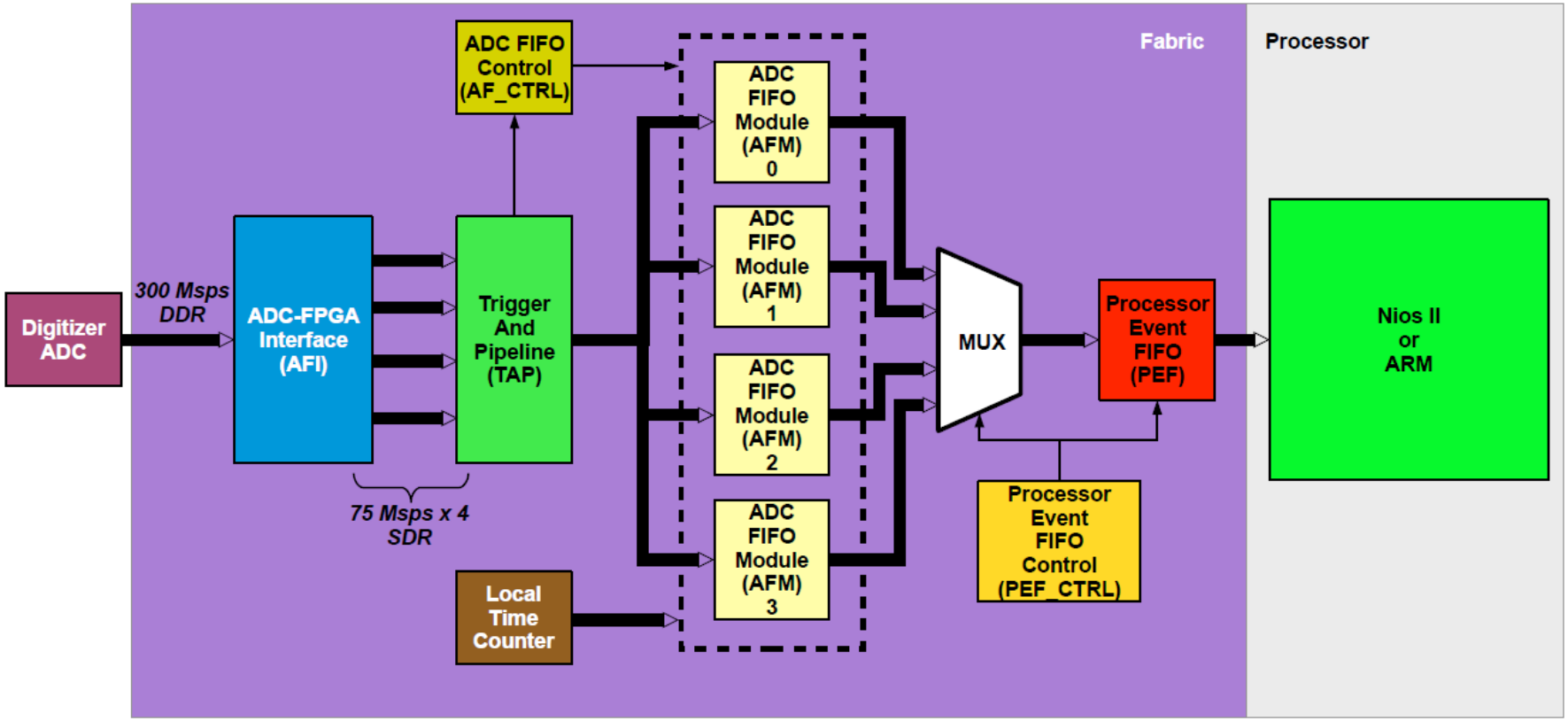


Digitizer Daughter Card (DDC2)



- UW Fabricated QTY (10); 250 MSPS, <300mW, powered by FPGA kit
- Single-ended and differential inputs
- Jumper-selectable signal path, compression, and power supply configurations
- Header for power/control of High Voltage Supply (HVS)
- Designed using Altium schematic capture and layout tools

Digitizer Readout Firmware

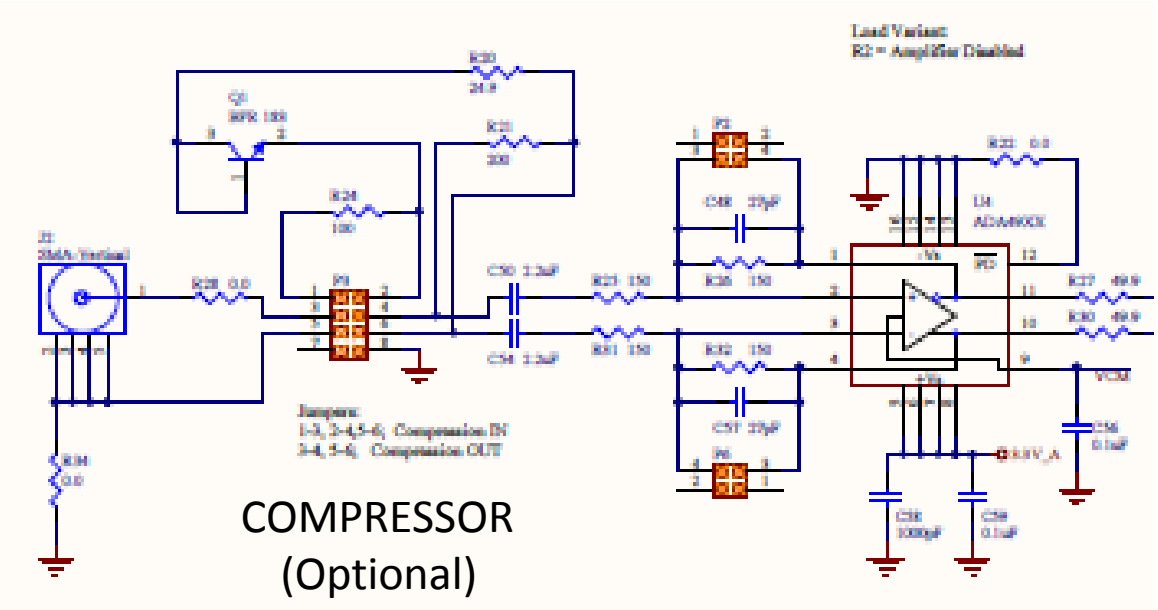


Study: ADC noise, feature extraction, power dissipation, processing requirements

T. Anderson, J. Groh (Penn State)

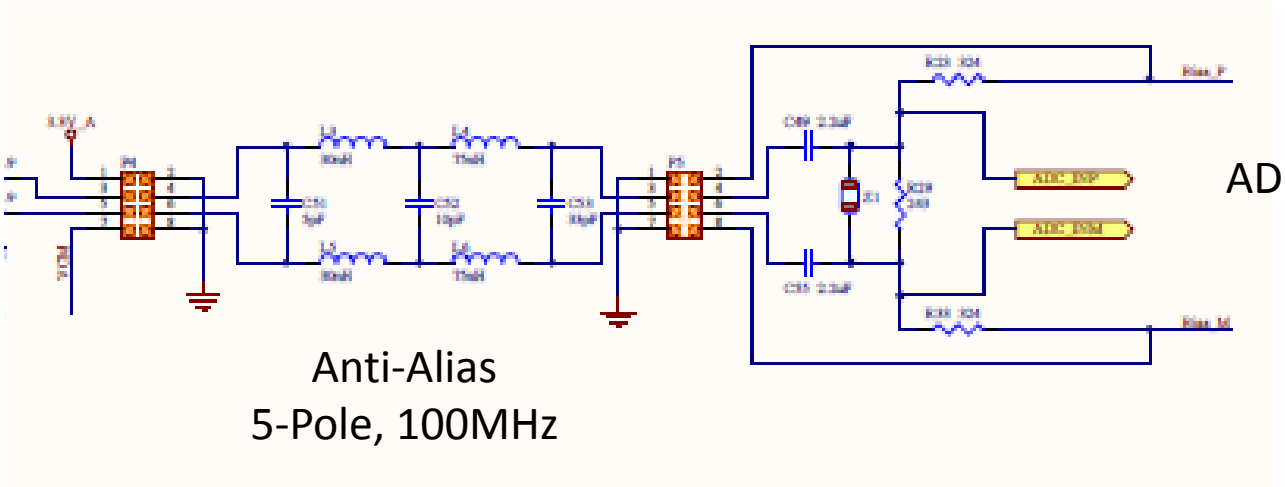
DDC-2 Front End

INPUT



COMPRESSOR
(Optional)

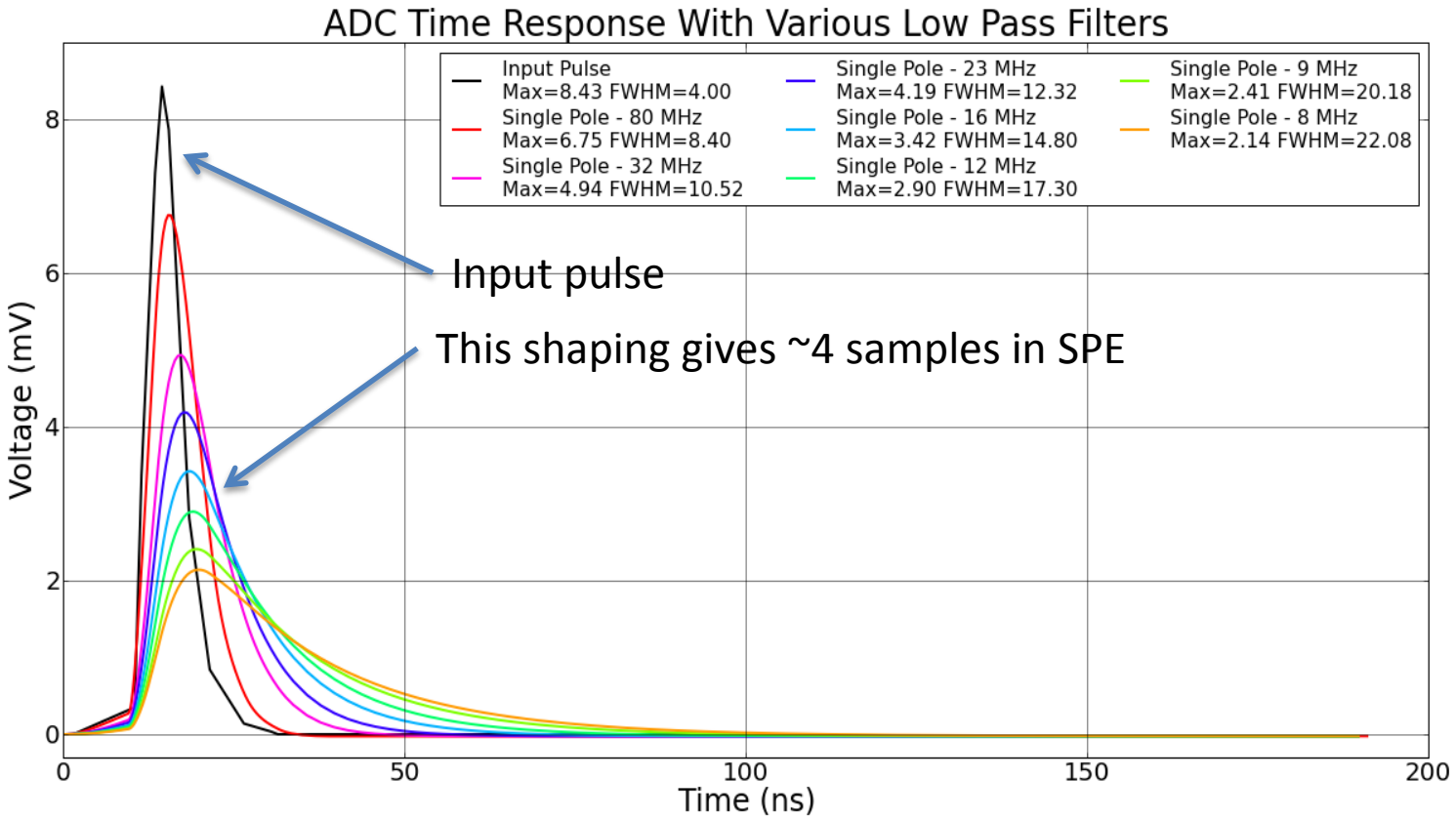
Single-Differential
and Pulse Shaping



Anti-Alias
5-Pole, 100MHz

ADC Input and
DC Bias

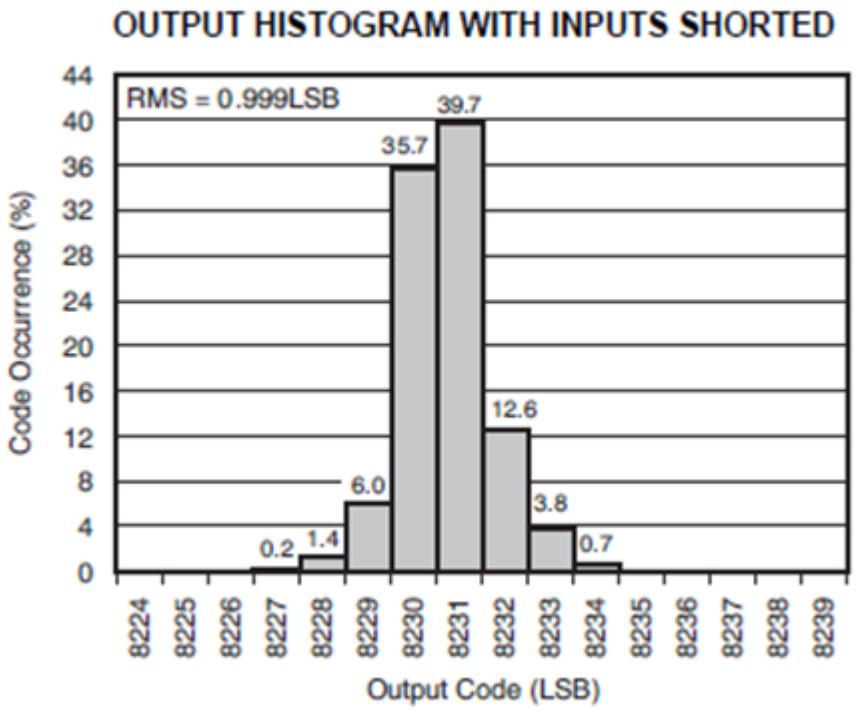
Front End Pulse Shaping (Simulations) Goal= 4samples/SPE; ~ 15ns FWHM



Kyle Jero, *UW Madison*

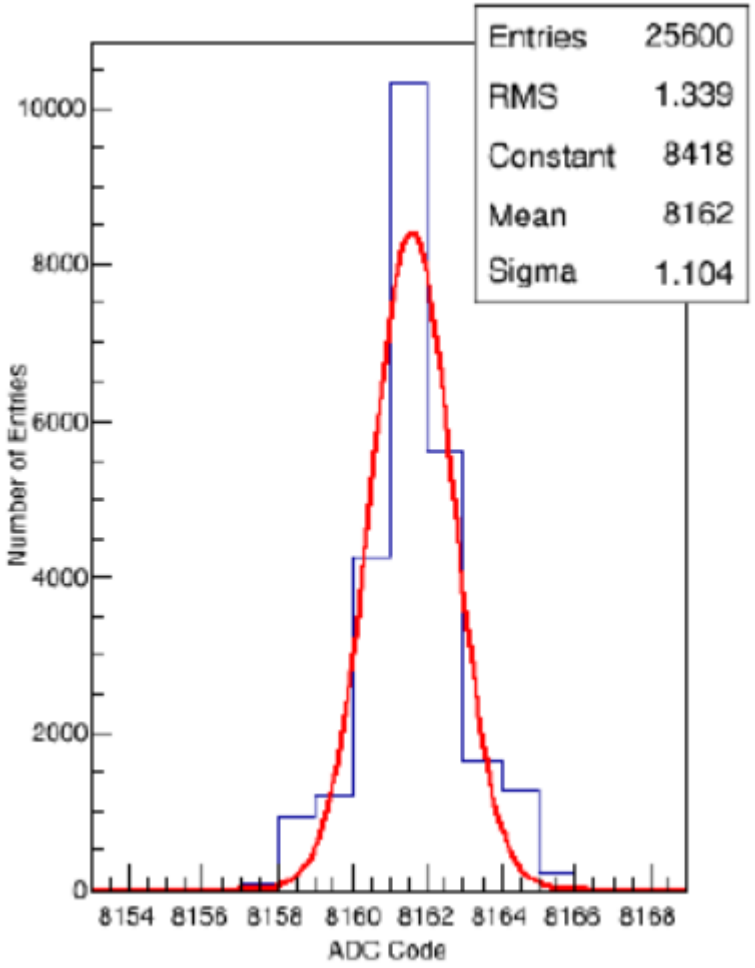
Initial Tests: DDC2 Noise Baseline

(Noise from: Power supplies, Input Amplifier, DC Offset Circuitry, EMI)



ADC Inherent Noise

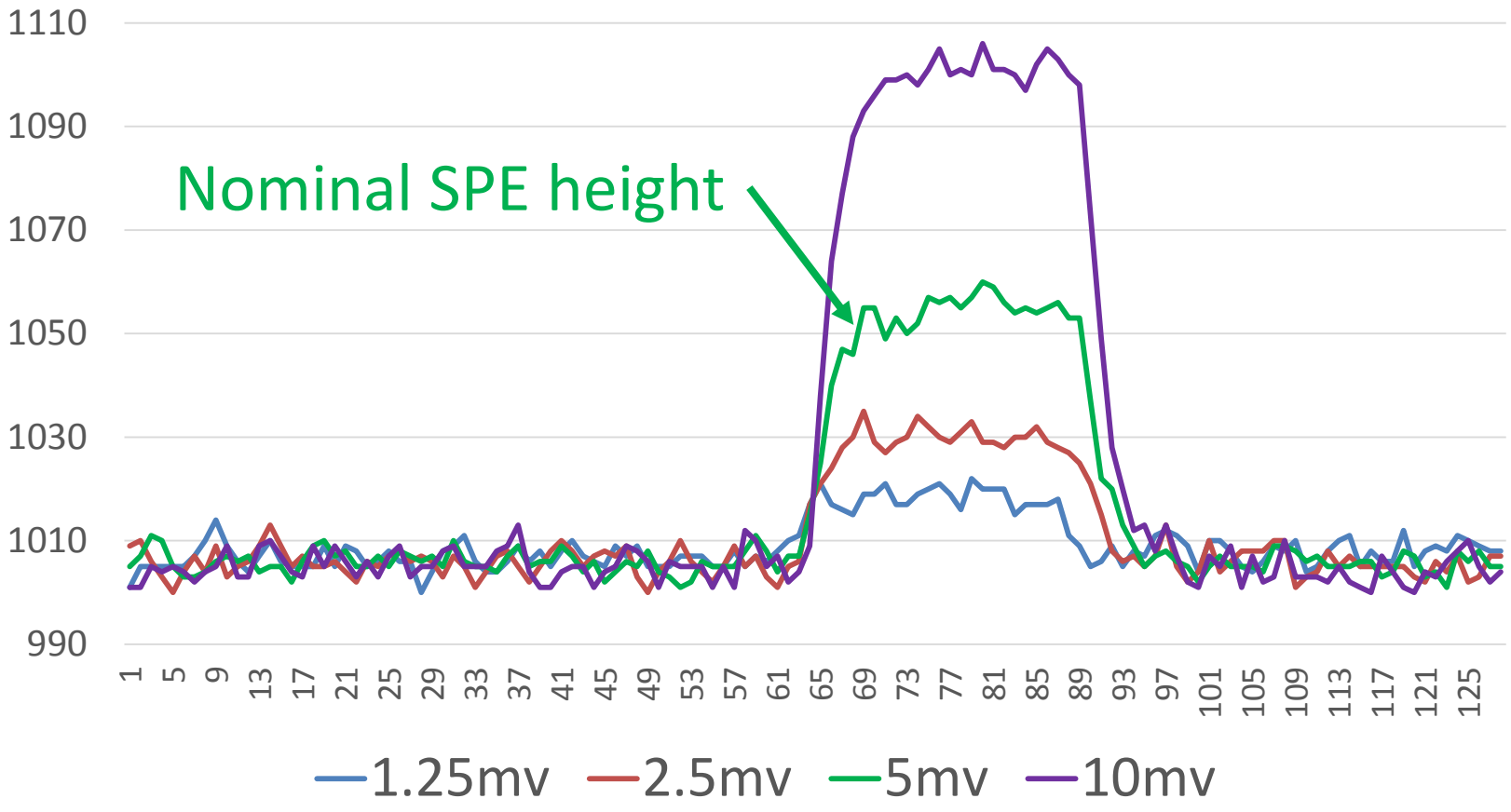
(ADS 4149 data sheet)



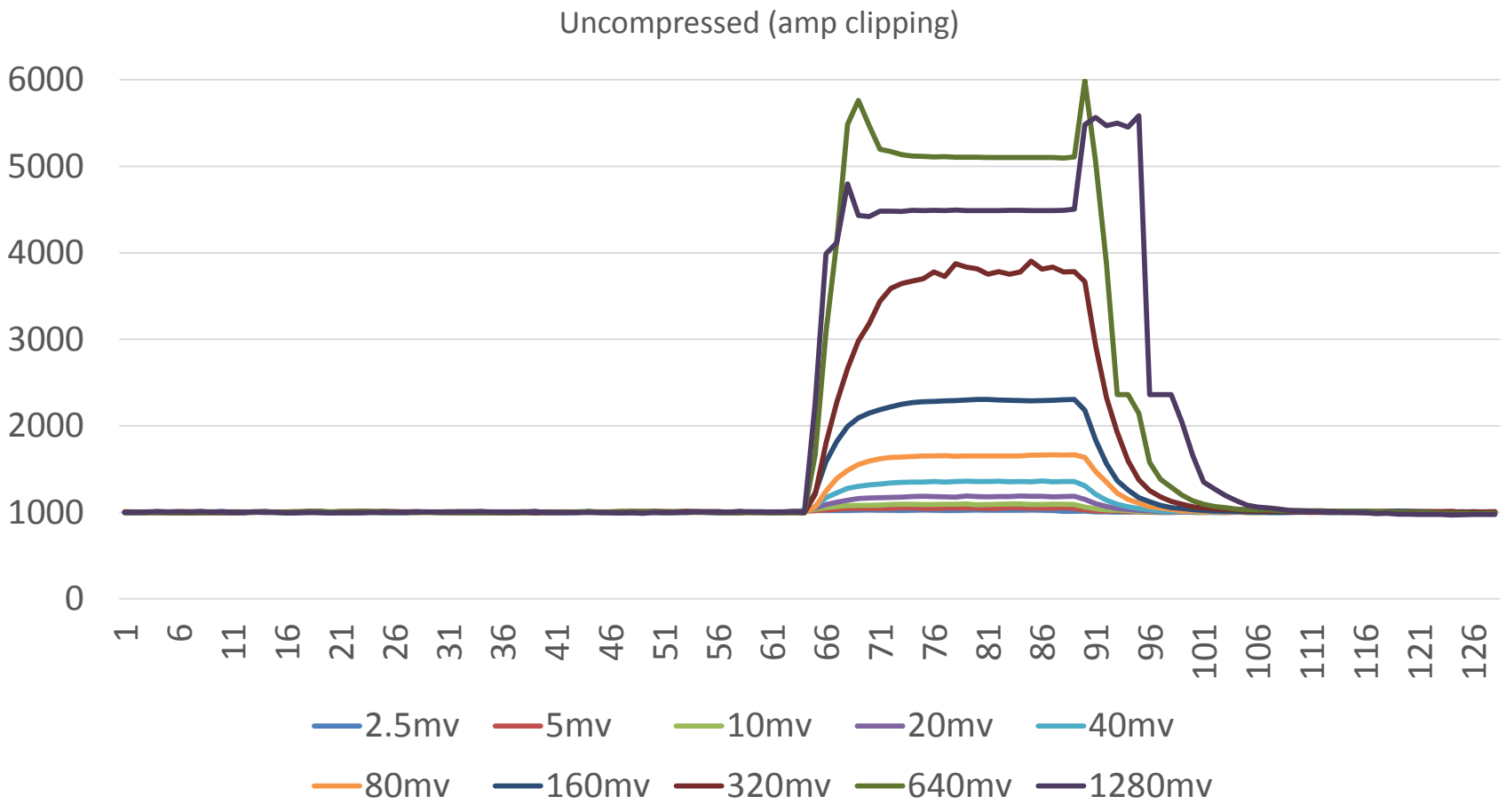
DDC2 Noise (measured)

DDC2 Low amplitude pulses vs noise;

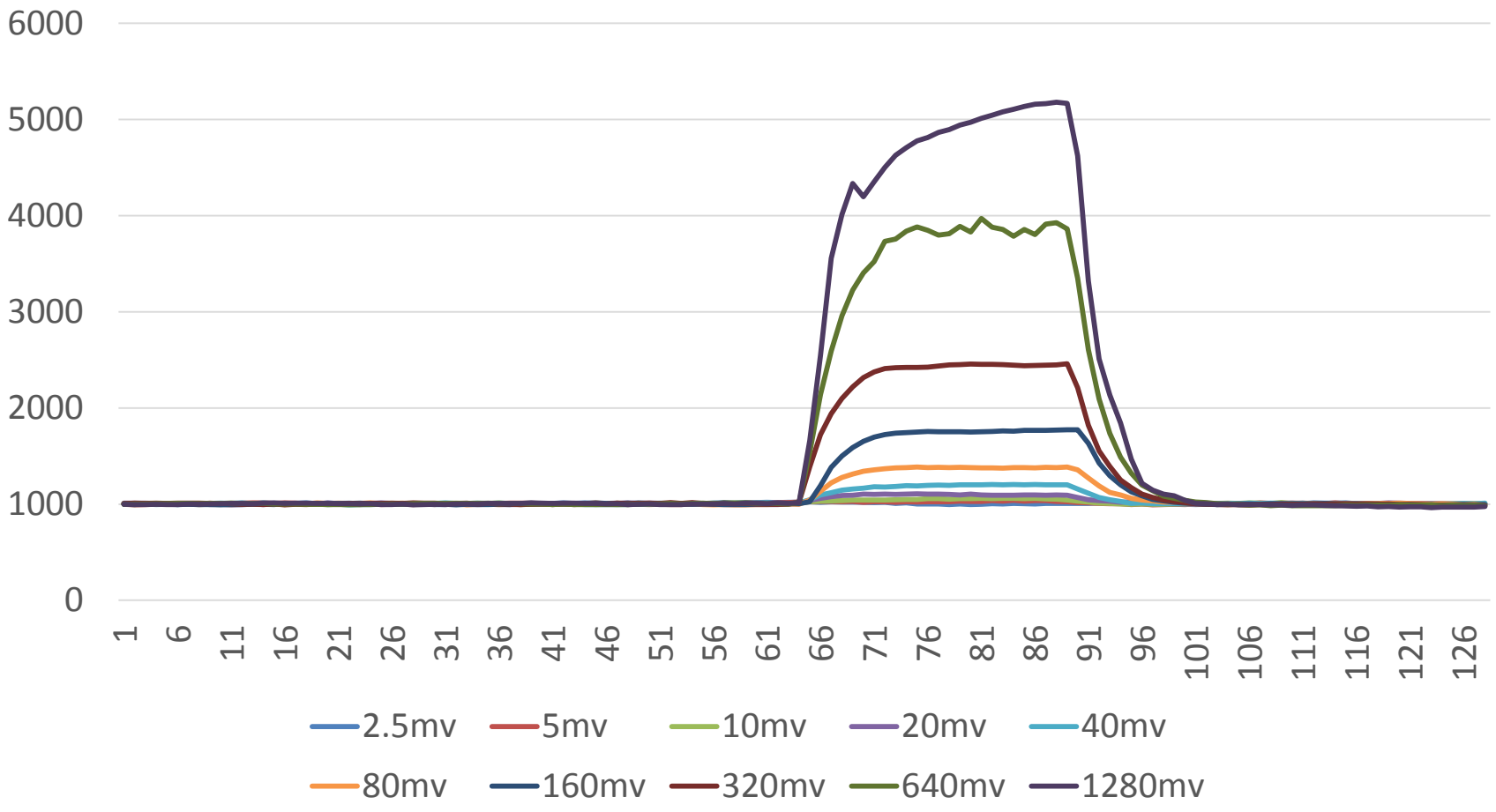
100ns wide, 18MHz Rolloff



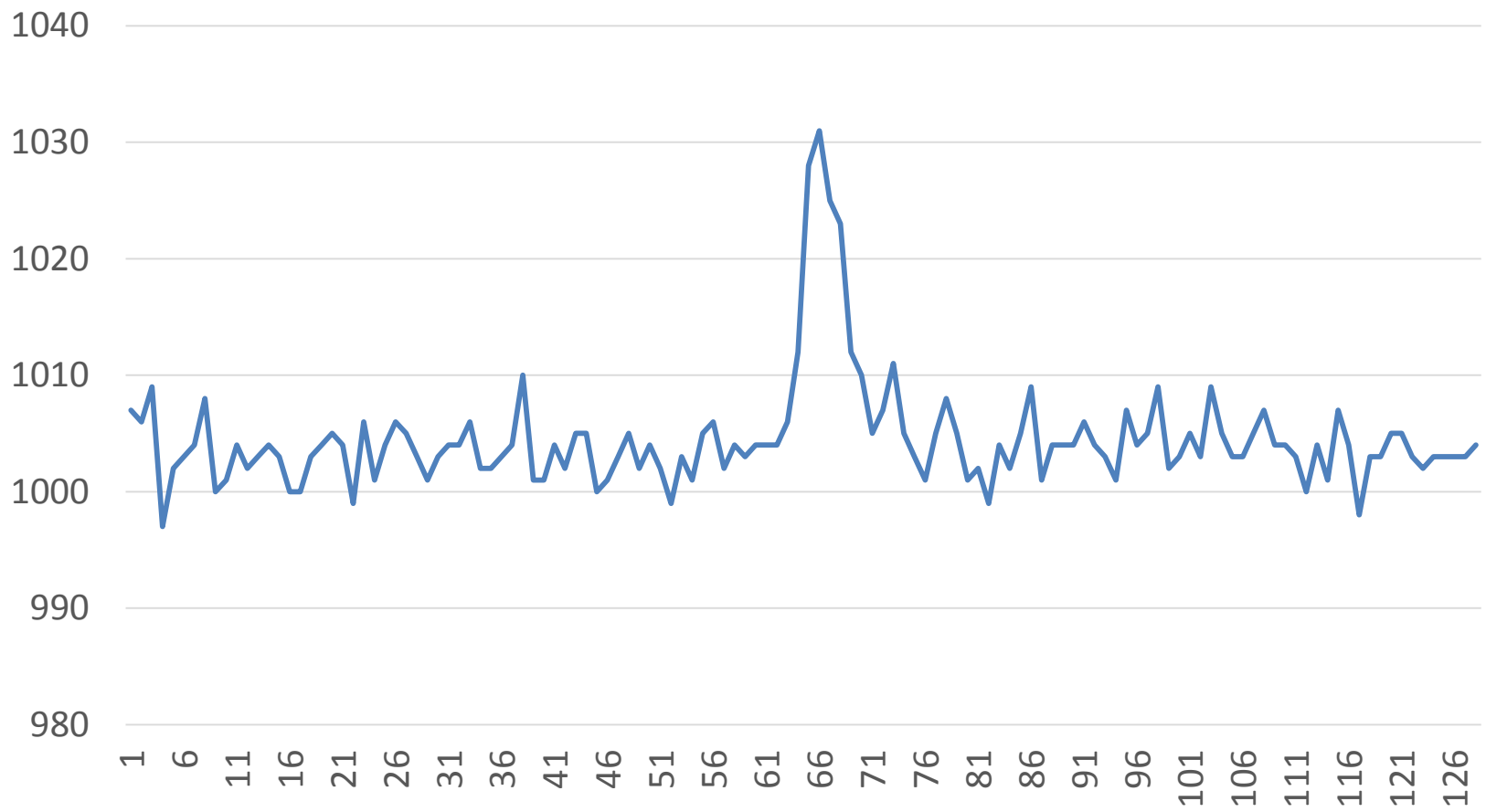
Large pulses w/o compression



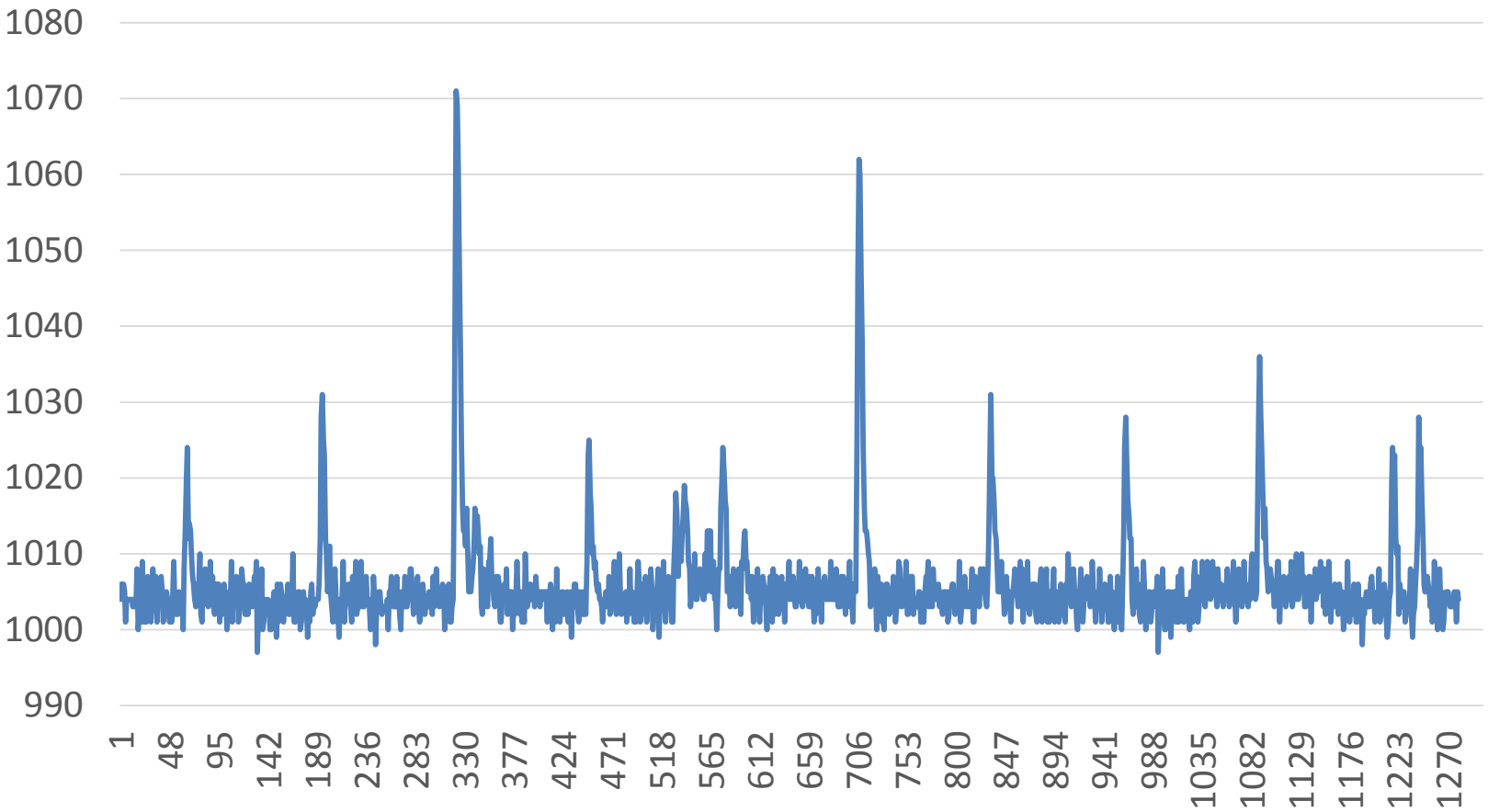
Large pulses with compression



PMT SPE Pulse with DDC2



PMT Pulses with DDC2



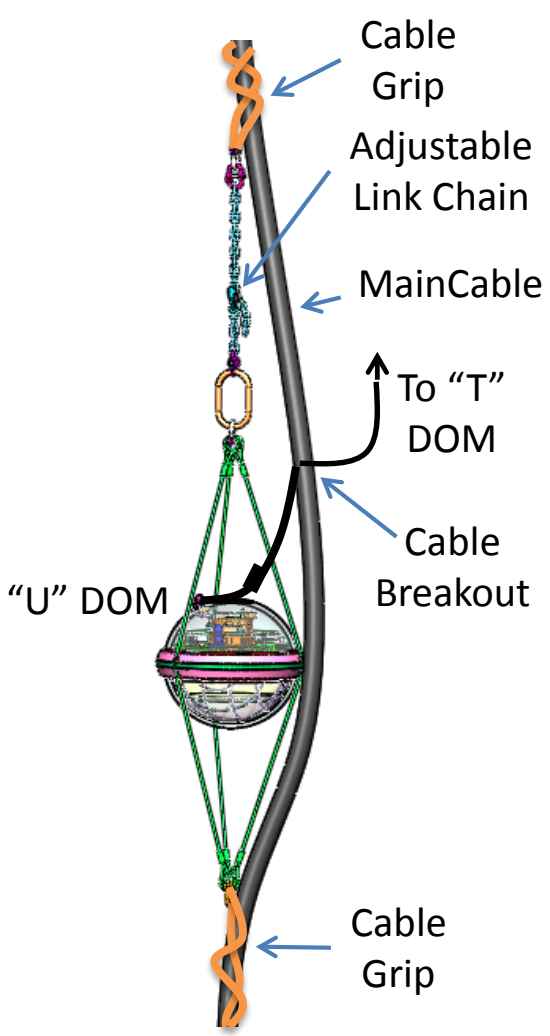
Thank You!

Subsystem Requirements Draft

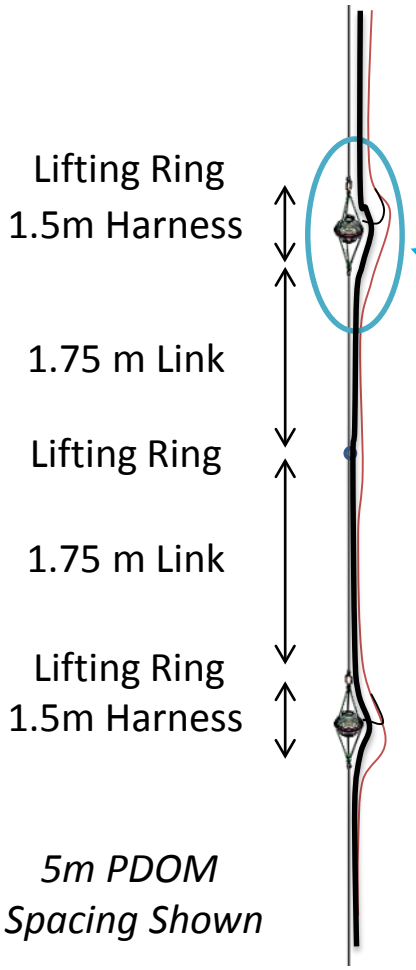
- Gen2 DOM requirements Draft:

https://drive.google.com/open?id=0Bxm9S-Ib8bhxbFFPUHZ6ekJSM0E&authuser=0

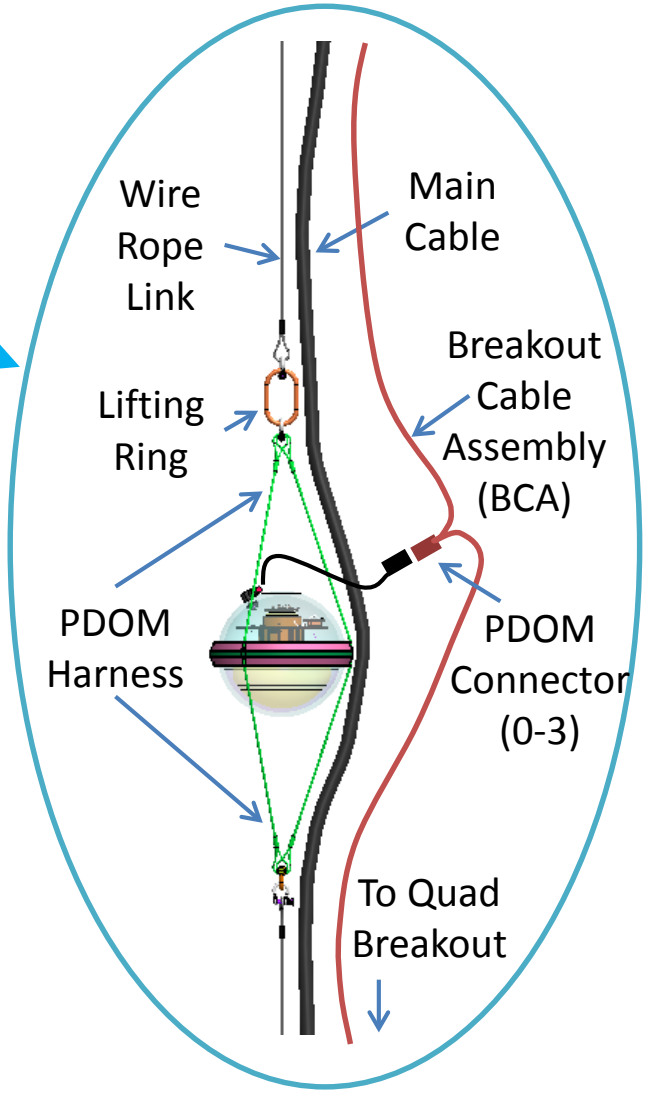
Proposed PINGU String Architecture



IceCube Detail



PINGU String



PINGU Detail

Continuous Digitization in Gen2 DOM

- Main functional departure from Gen1 DOM
  - Gen1 discriminator only detects waveform onset
  - Gen2 Digitizer always sampling when DOM is active
  - Establish digitizer baseline continuously
- Uses digital discriminator for “storage” trigger
  - Eliminate analog comparators and signal chain
  - Can easily implement multiple threshold levels
- Variable-length waveform record
  - Built-in data reduction (vs. fixed-length record)
- Facilitates further data compression
  - TOT flag enables near-real-time SPE detection
  - Get relative pulse length without analyzing waveform

SUPPLEMENTAL SLIDES

Drilling and Deployment Leap-Frog

Main FPGA and OS Candidates

Requirements: Low Power, Stable, Non-Brickable

- FPGAs
  - Cyclone 5 FPGA w/ HPS ARM9 hard processor
  - **Cyclone 5 FPGA w/ NIOS2 soft processor**
  - Igloo2
  - Igloo2+ARM (“Smartfusion”)
  - MAX10 (New Altera FPGA w/ Built-in config flash)
- Operating Systems
  - None (“baremetal”)
  - RTOS (e.g. freeRTOS)
  - Linux

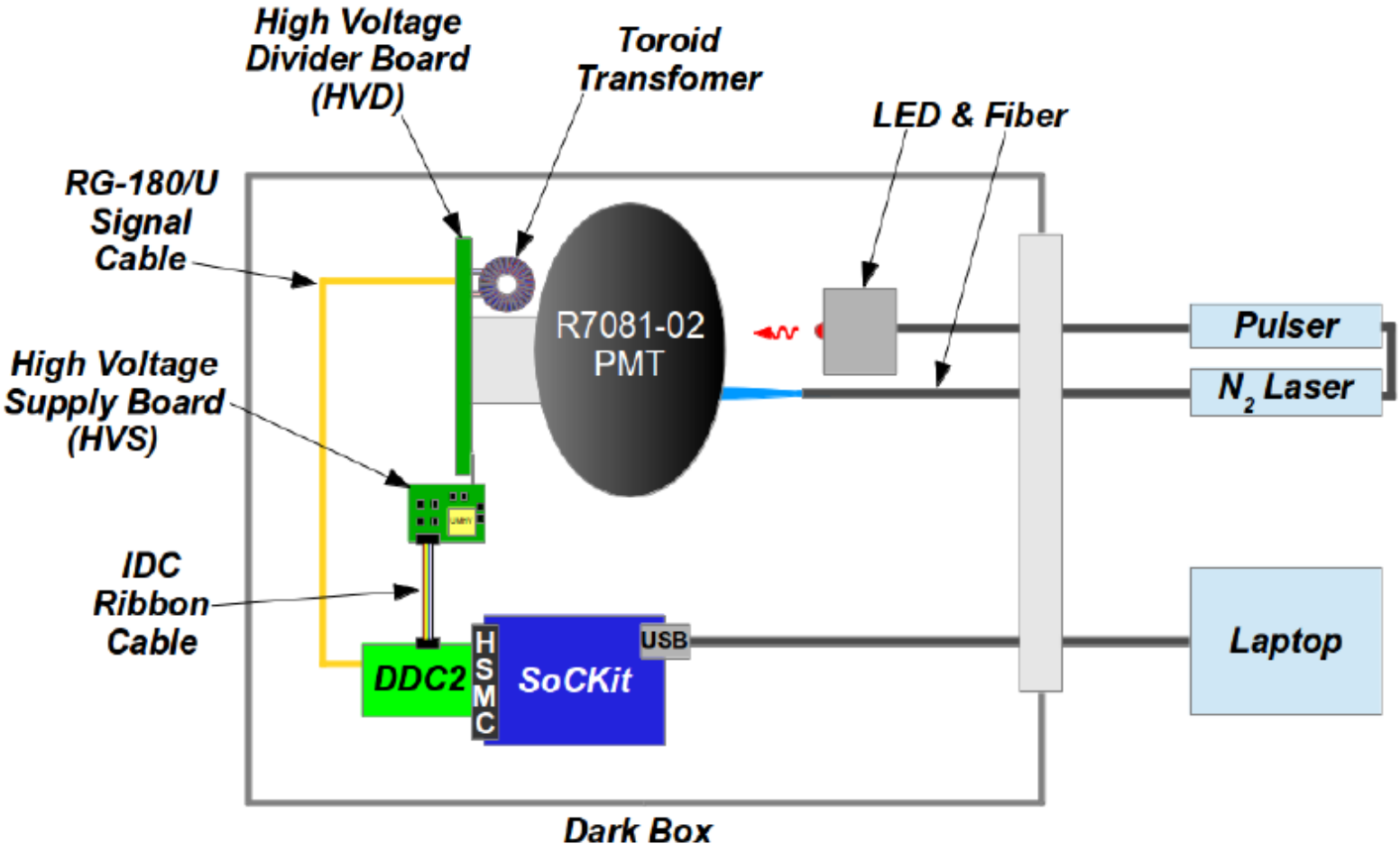
Potential Gen2 DOM Interfaces
(Platform for Power, Timing and Communications)

- Interface provided on Mainboard
  - Camera (development ongoing)
  - Magnetometer? (orientation, geophysics)
  - Inclinometer? (need better accelerometer)
  - Other? (*e.g.* TOA Signals)
- Adapt mainboard circuitry for:
  - Multi-PMT “M-DOM” Interface
  - Dual-PMT “WOM” Interface

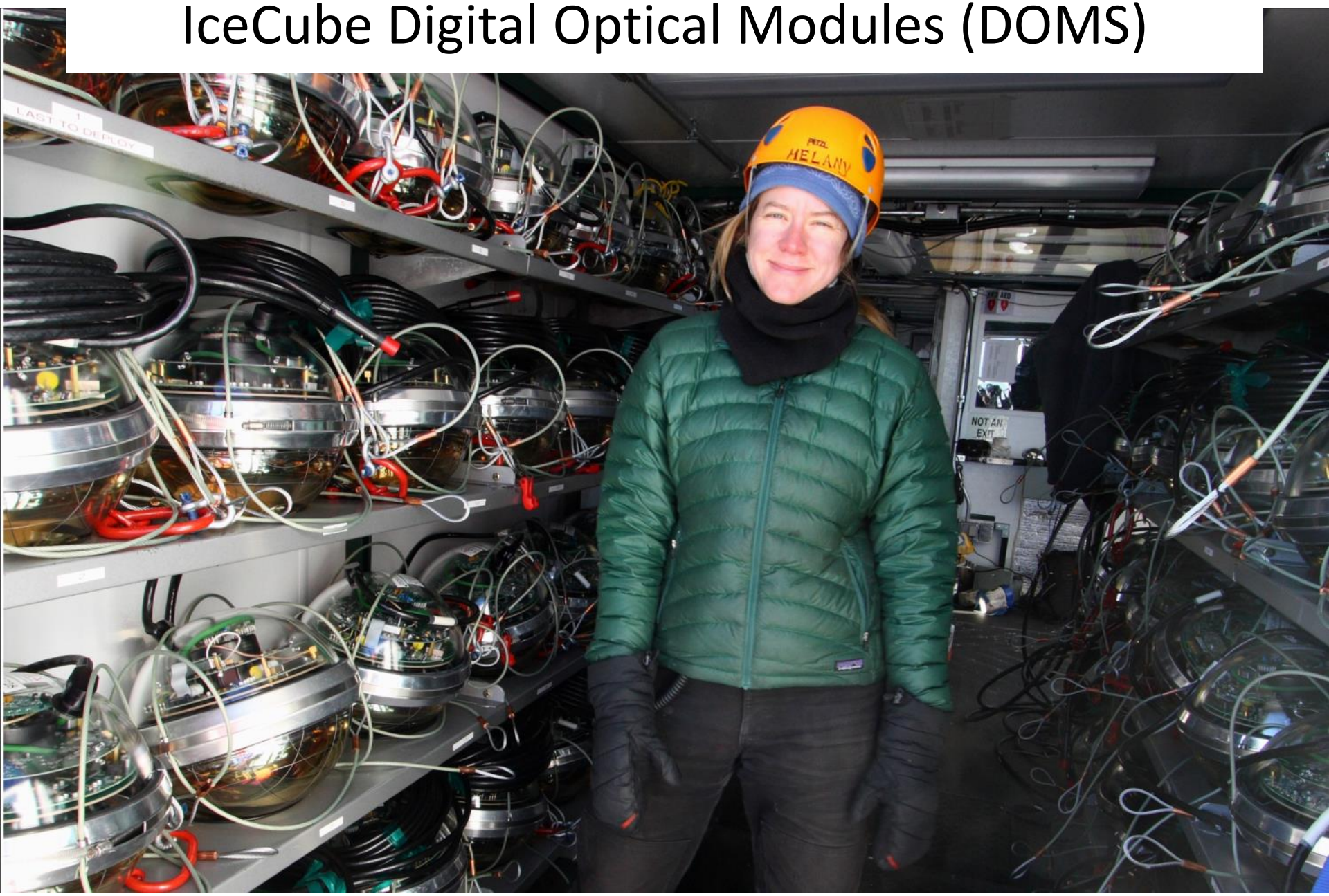
General System Requirements

Requirement	IceCube	PINGU	HEX
Timing	<3ns	Same as IC	Same as IC
LSB	~0.13mv	~0.08mv	~0.08mv
Range (bits)	16	14 compressed?	14 compressed?
Calibration Circuitry	IC flasher	Better Flasher	~Brighter Flasher
Production Calibration	Minimal	Maybe Every Unit	Maybe Sampled
Hole Ice quality	Bubbles	Clearer than IC	Clearer than IC
Sensors-String/quad	60/4	60/8	80/8
PMT	Standard	Hi QE	Hi QE? (double$)
Wired Coincidence	Yes	No	No
Hole Spacing	125m	~30m	~300m
Vertical Spacing	17m	5m	17m
Hub	ICL	ICL	Top of hole
Drill Design	SES-based	Transitional	Modular

Prototyping Goal: Gen2 DAQ System



IceCube Digital Optical Modules (DOMS)



Surface Cables into ICL

IceCube Gen1 Seasonal Construction

Strings Deployed:

Season	Strings	Total
2004-05	1	1
2005-06	8	9
2006-07	13	22
2007-08	18	40
2008-09	19	59
2009-10	20	79
2010-11	7	86