

Data Analysis Results of TowerJazz Test Structures

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Presentation Outline

- 1 Introduction
- 2 Measurements
- 3 Data Analysis
- 4 Results

TowerJazz Test Structures

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- Investigated devices were CMOS structures located on TID_TJ180_v2 test chip

TowerJazz Test Structures

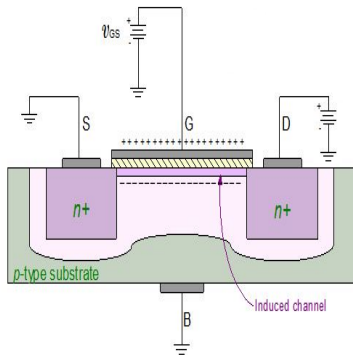
- Investigated devices were CMOS structures located on TID_TJ180_v2 test chip
- Primary results of threshold voltages are of un-irradiated nMOS transistors

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Measurement Conditions (1)

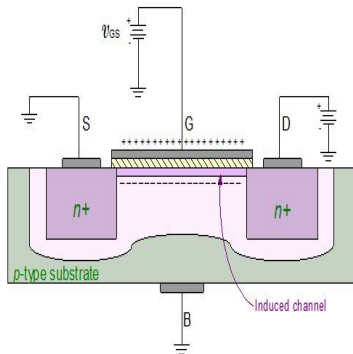
- Gate voltage sweep from 0V to 1.8V was performed on 26 nMOS transistors with various W/L
- Source and substrate terminals were connected to common ground
- Drain voltage was kept at maximum value of 1.8V to keep operation of transistor in saturation mode



n-channel MOSFET cross-section

Measurement Conditions (2)

- Compliance currents of $10^{-5}A$ order were set to drain and source
- Current limit of $10nA$ was also set to gate
- These measures were taken to protect the test sample



n-channel MOSFET cross-section

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Fitting Method (1)

- Main goal is to extract threshold voltages from the dataset
- Shockley 1st order transistor model in saturation region was applied

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_{th} \\ \frac{\mu_n C_{ox} W}{2L} (V_{gs} - V_{th})^2 & V_{gs} > V_{th} \end{cases}$$

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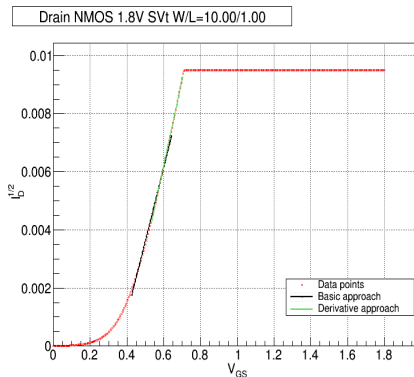
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Fitting Method (2)

- For simplicity $\sqrt{I_{ds}}$ and V_{gs} data was used for analysis
- This allowed linear fitting
- The main concern was to select fitting region
- 2 approaches were implemented

Fitting Method (3)

- 1st option was to exclude all the data point correspond to less than 20% or greater than 80% of the maximum drain current value
- 2nd option - all the points are excluded that correspond to less than 80% of the maximum $\frac{dI_{ds}^{1/2}}{dV_{gs}}$
- Results are prepared for both approaches



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Results (1)

Name	W/L	V_{th} Derivative	V_{th} Basic	$ \Delta V $	$ \Delta V $ in %
AD01	0.44/0.18	0.396	0.402	0.006	1.49
AD02	0.70/0.18	0.437	0.429	0.008	1.86
AD03	1.00/0.18	0.444	0.426	0.018	4.23
AD04	2.00/0.18	0.426	0.393	0.033	8.40
AD05	10.00/0.18	0.404	0.347	0.057	16.43
AD06	10.00/0.36	0.417	0.371	0.046	12.40
AD07	10.00/0.54	0.404	0.368	0.036	9.78
AD08	10.00/1.00	0.387	0.357	0.03	8.40
AD09	10.00/2.00	0.378	0.361	0.017	4.71
AD10	10.00/10.00	0.354	0.355	0.001	0.28
AD11	0.70/0.18	0.542	0.528	0.014	2.65
AD12	1.00/0.18	0.546	0.531	0.015	2.82
AD13	2.00/0.18	0.520	0.489	0.031	6.34
AD15	10.00/1.00	0.467	0.439	0.028	6.38
AD16	1.80/0.18	0.454	0.428	0.026	6.07
AD17	5.00/0.50	0.420	0.392	0.028	7.14
AD18	100.00/10.00	0.324	0.297	0.027	9.09
AD19	0.22/0.18	0.360	0.363	0.003	0.83
AD20	0.50/0.18	0.417	0.419	0.002	0.48
AD21	10.00/0.18	0.414	0.357	0.057	15.97
AD22	10.00/1.00	0.388	0.356	0.032	8.99
AD23	10.00/10.00	0.354	0.355	0.001	0.28
AD24	2.98/0.19	0.464	0.435	0.029	6.67
AD25*	4.10/0.55	0.402	0.394	0.008	2.03
AD26*	5.85/1.11	0.385	0.373	0.012	3.22
AD27*	9.35/2.24	0.367	0.359	0.008	2.23

*Enclosed-Layout-Transistors

Results (2)

- Maximum difference in results
 $|\Delta V|_{max} = 0.057V$
- Minimum $|\Delta V|_{min} = 0.001V$

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Thank you for your attention!

References

1. nMOS structure illustration, Tales Pimenta, Robson Moreno and Leonardo Zoccal, \Rightarrow [Link to picture](#)