# Testing of CMOS test structures

This document describes the testing of the CMOS test structures described in [1]. The aim of the testing sensor structures manufactured in the HV-CMOS and HR-CMOS processes:

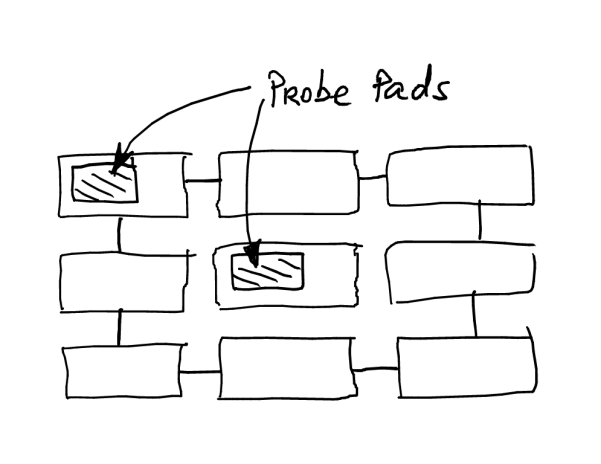
* Compare the behaviour of sensor and amplifier test structures manufactured in the HV-CMOS and HR-CMOS processes
* Understand the charge collection and depletion region properties in HV-CMOS and HR-CMOS sensors
* Evaluate the effect of radiation on the sensors manufactured in HV-CMOS and HR-CMOS processes

Specific

* Determine C-V characteristics of simple deep N-well diode structures as a function of pixel size and diode fraction to provide input to noise calculations and to characterise changes in bulk after irradiation
* Measure response of simple deep N-well diode structures to mips before and after irradiation as a function of bias voltage and position within the sensor
* Measure response of deep-N-well sensor with fast amplifier before and after irradiation and determine signal due to diffusion and drift current
* Measure response of deep-N-well sensor with fast amplifier before and after irradiation to determine signal as a function of depth and position across the surface of the sensor
* Measure the spread in response of sensors both within a wafer and across a number of wafers before and after irradiation,
* Characterize properties of a stand-along amplifier (gain, noise, etc) and their change with radiation dose
* Characterize simple electronic elements (transistors, resistors, capacitances) and their change with radiation dose.

## Passive pixel arrays

The passive pixel arrays consist of 9 simple deep N-well diode arranged as below. The outer 8 pixels are ganged together can be accessed through a single probe pad. The central pixel can also be accessed via a probe pad.

***Table of geometries from [1]***

Measurements to be made:

C-V measurements to **XV** for HV-CMOS **and YV** for HR-CMOS

* Different geometries
* Different fill factors
* Before and after neutron/proton irradiation, using different frequencies

These measurements will be made on a probe station.

Outer pads are connected together used as guard ring. The capacitance of the central pad is measured as a function of voltage.

The capacitances are in the range 50-100fF for HV-CMOS.

C-V measurements on irradiated die should be made at 10kHz, 100kHz and 1MHz.

***Need to also measure for different annealing conditions***

***For HR-CMOS an alternative structure has been implemented***

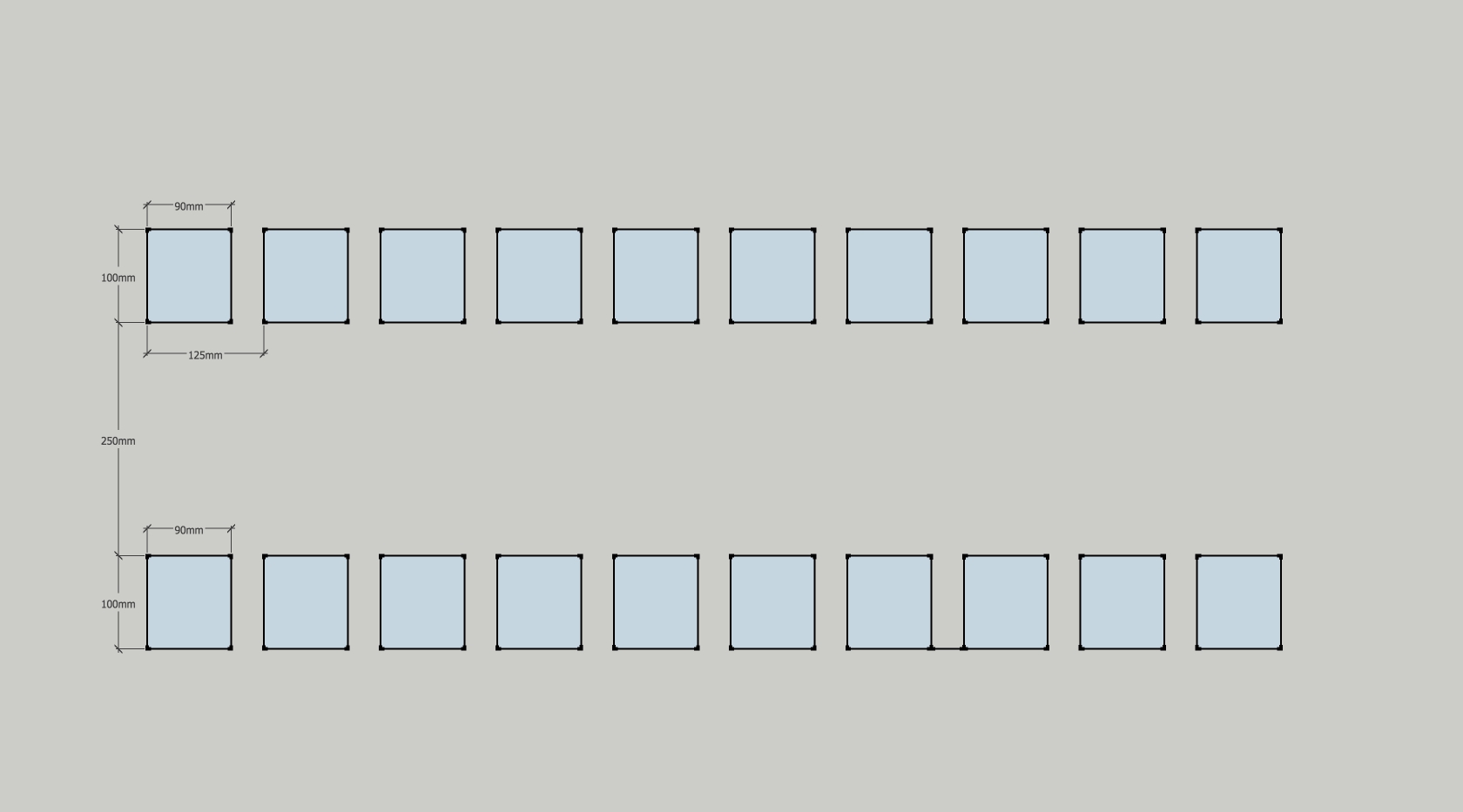
***To be added***

## Large Passive Array

***For source tests, details to be added from [1]***

***Need to also measure for different annealing conditions***

## 5x5 active pixel array



**250 m**

\\

**100 m**

**100 m**

**90 m**

**90 m**

**125 m**

**Test Structure**

**1**

**2**

**3**

**4**

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**11**

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**19**

**20**

Readout of central 9 pixels from row of bond pads, outer pixels are ganged together and accessed via a 10th bond pad.

The output of the pixels is through a fast risetime amplifier. The specifications are given in Table 3.3.3.

***Table 3.3.3: Fast Amplifier Specifications [1] (to be finalized)***

|  |  |
| --- | --- |
| ***Risetime*** | ***<= 30 ns (3 ) for HV-CMOS;  ~ 100 ns for HR-CMOS {Daniel: How will we separate drift from diffusion charge collection with this long risetime?}*** |
| ***Noise*** | ***<50 e- for HV-CMOS;{Confirm with Ivan} < 25 e- for HR-CMOS*** |
| ***Gain*** | ***On the order of 500 mV/fC {Confirm with Renato & Ivan}*** |

***Is there a test injection input to the amplifier to test it? {For stand-alone amplifier, there is an input pad available.}***

Measurements of pulse height and risetime/pulseshape to be made with a fast scope (**scope specs to be added: 1GHz BW & >2Gb/s sampling for 10ns rise time?)** for different geometries before and after irradiation using X-ray/laser/sources as available

1. as a function of bias voltage
2. as a function of position across the surface of the diode

Characterise signal to noise and time structure of pulses as a function of amplifier bias voltages **(are there parameters to be tweaked, is there a default set?).**

***What is the effect on the amplifier? Compare to standalone amplifiers***

***Is it possible to get spice simulations of output from amplifier for different inputs eg different fractions of drift and diffusion?***

## Irradiations

Maximum fluence: 2x1015 1MeV/cm2 neq and dose: 500kGy.

### Annealing

Devices will undergo standard annealing prior testing: 80 minutes at 60oC or 1 week at room temperature. Note this is based on annealing high resistivity substrates and so some measurements should be made to look at the properties of the devices for different annealing times.

***Suggested annealing to be added***

## Edge TCT

***Ask Igor to add something***

## Test preamplifiers

***Section to be added***