Digital Camera Trigger for the Cherenkov Teleskope Array

March 2015

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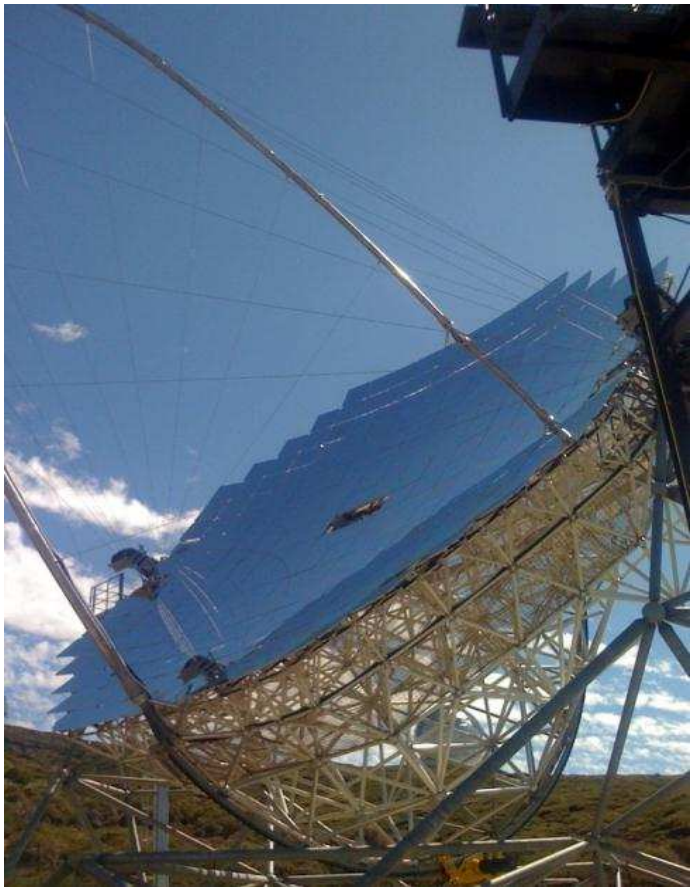
DESY

CTA, Cherenkov Telescope Array

- about 100 telescopes, on the northern & the southern hemisphere
- 3 sizes: LSTs, MSTs and SSTs, similar already exist :

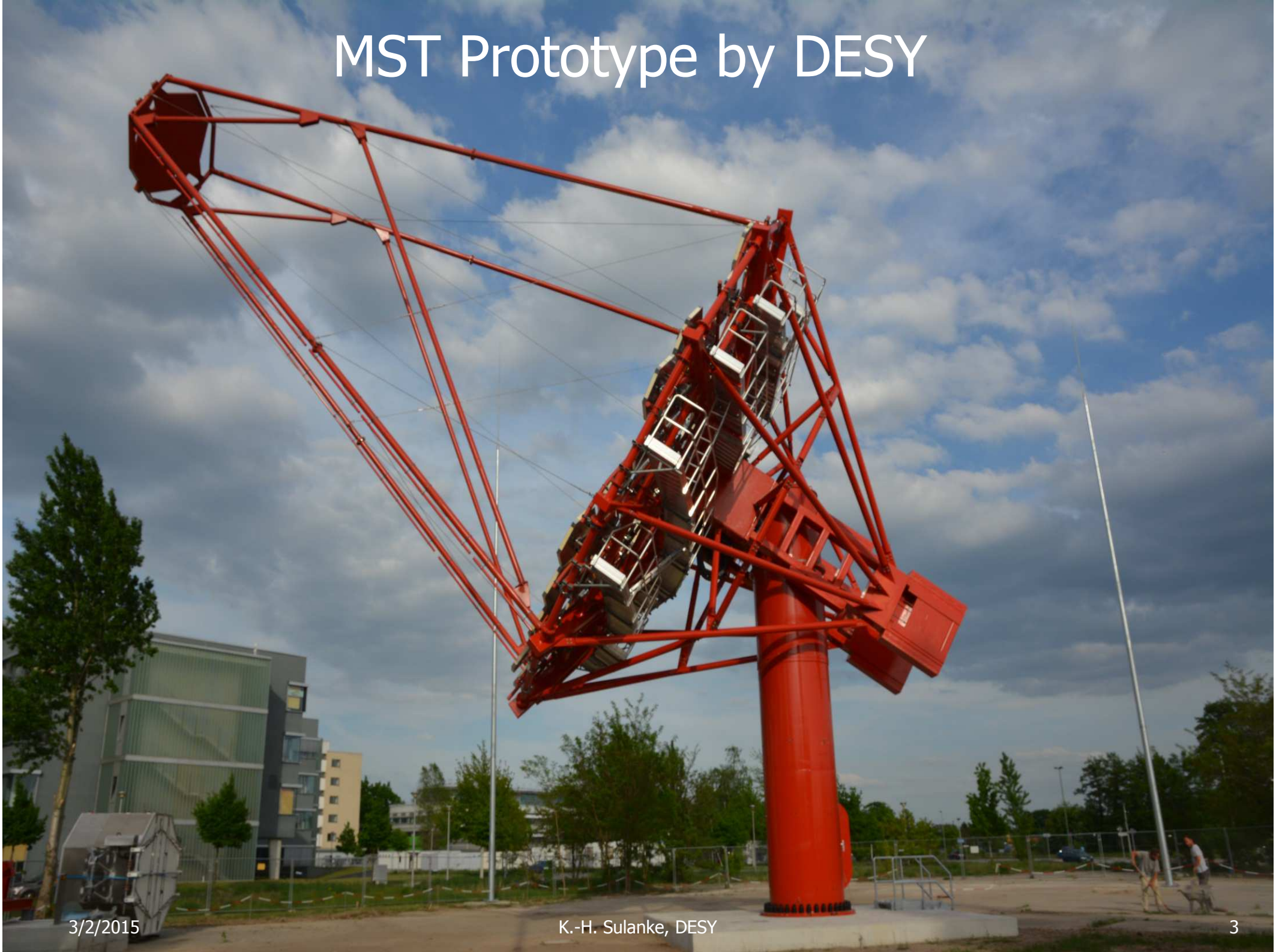
H.E.S.S. in Namibia



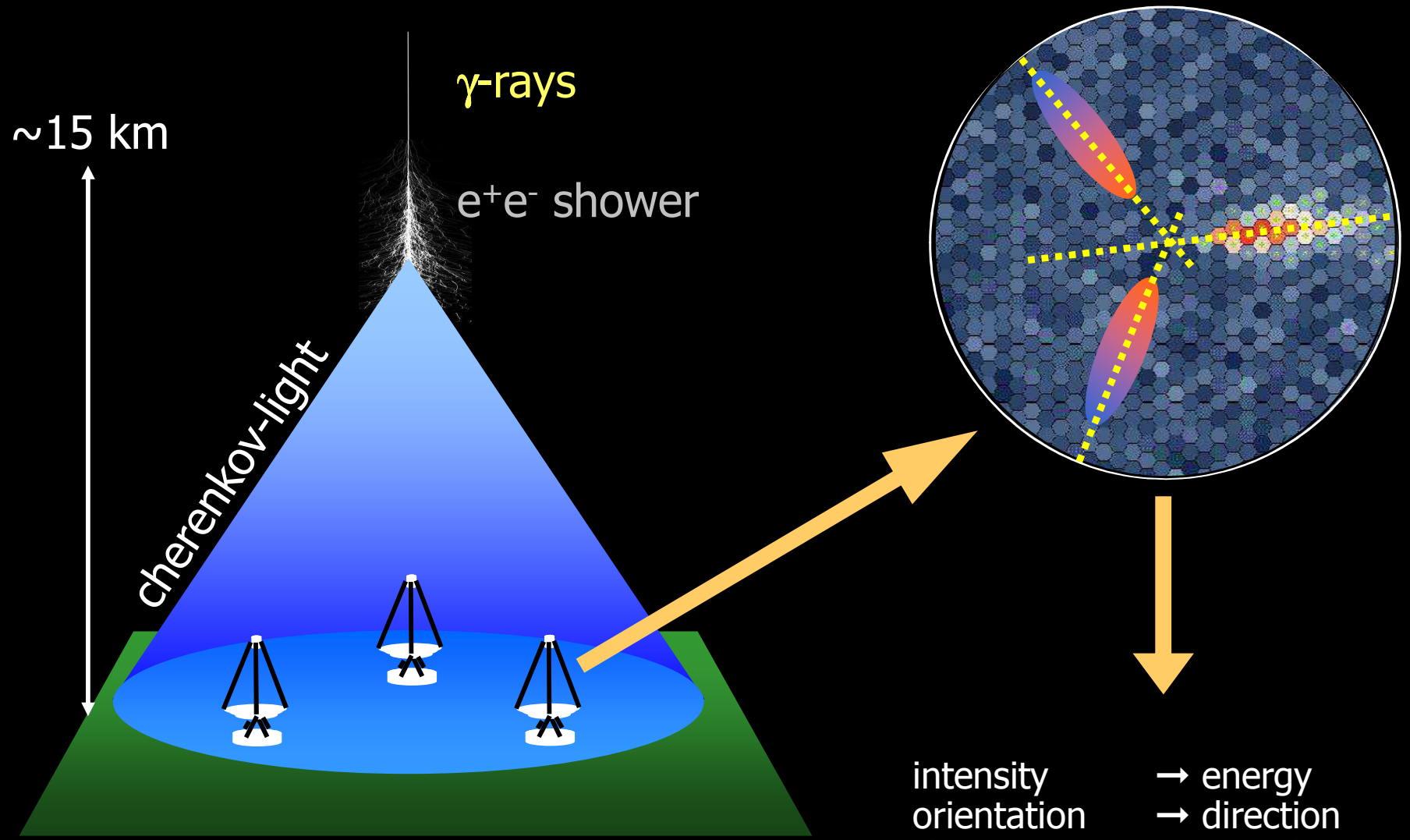
MAGIC auf La Palma

VERITAS in Arizona, USA

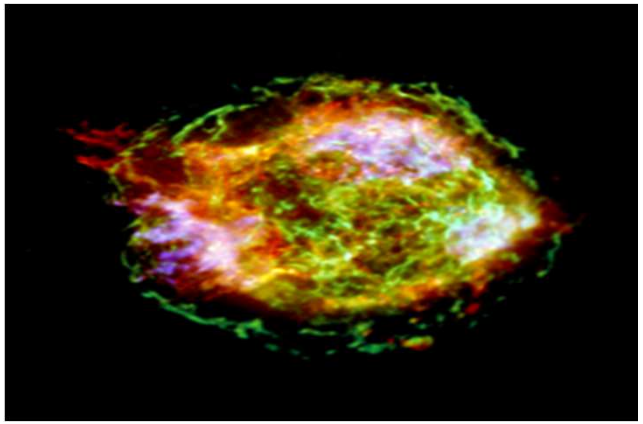
MST Prototype by DESY



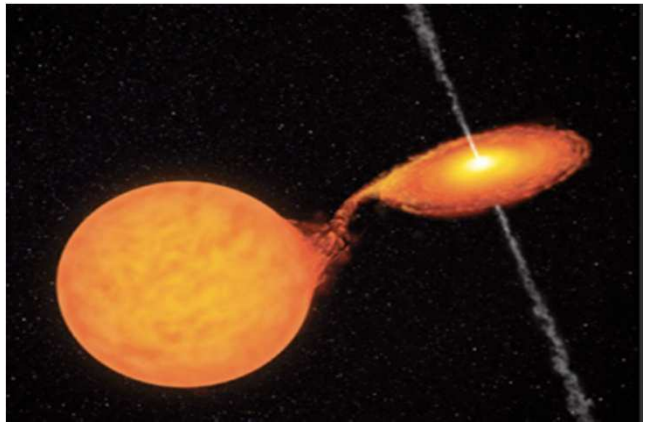
Atmospheric Cherenkov Light



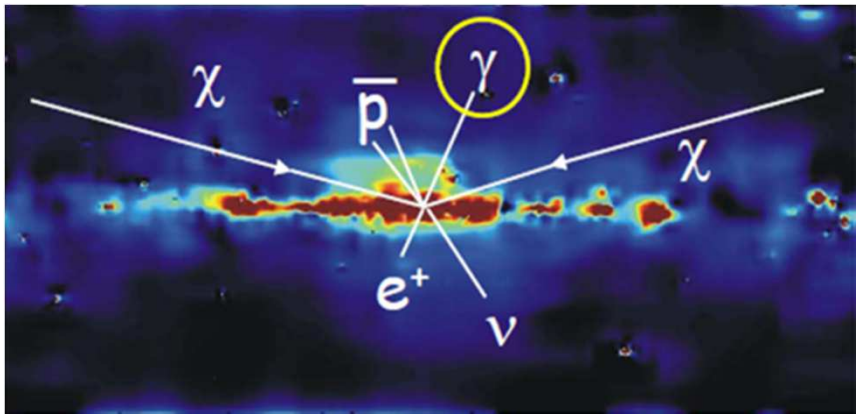
Sources of Cosmic Rays



Super Nova



Micro Quasare



Dark Matter

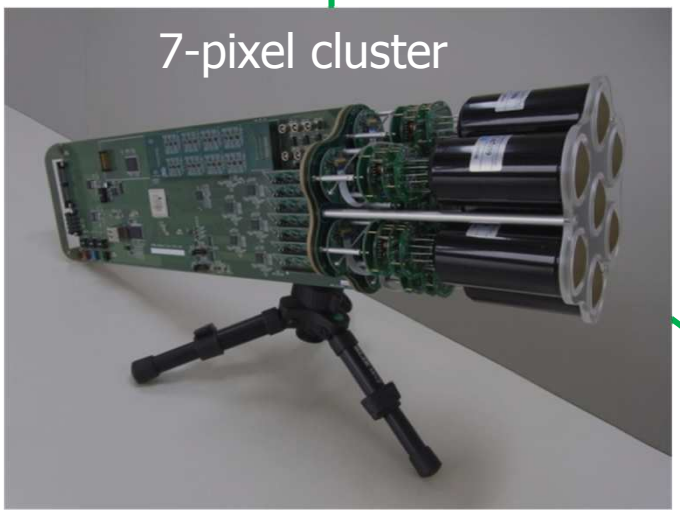
The MST (Medium Size Telescope) Camera

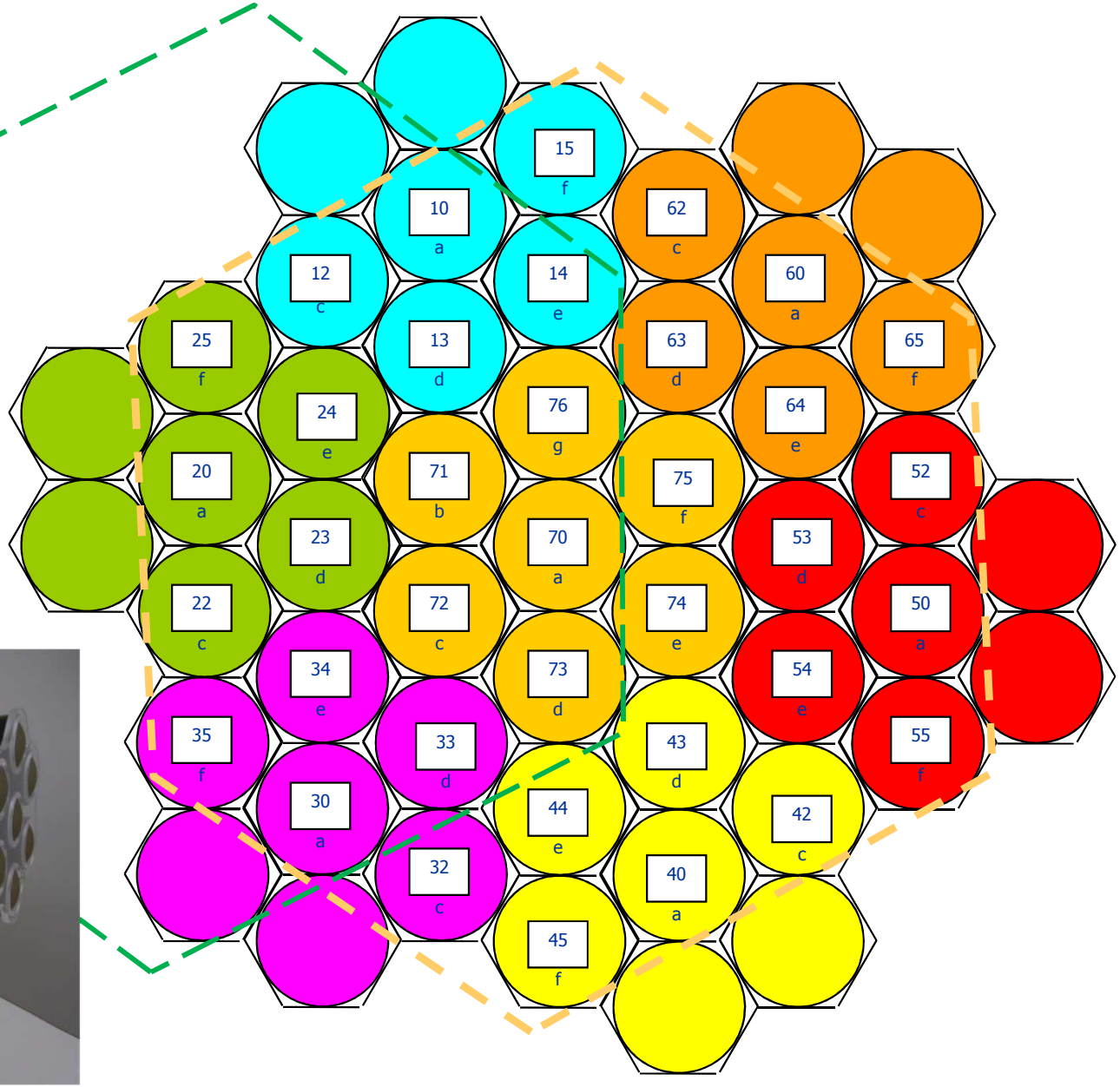
- PMT based, 265 cluster a´ 7 PMTs
- PMT-d : 38 mm (1.5 Zoll, z.B. Hamamatsu PMT R11920-100)
- Pixel-grid : 50 mm by Winston cones
- 1855 Pixel
- Size of the pixel-array : ~ 2 qm
- Weight : up to 2000 kg
- extrem light sensitive
- „shutter" time in the ns region
- self triggered

Trigger Requirements

- Design for the MST (Medium Size Telescope) Camera, „NectarCam", France
  - could also be used for LST (Large Size Telescopes), „DragonCam", Japan
- Because of the NSB (Night Sky Background), the trigger design is quite challenging
- Single pixel rate can be greater than 100 Mhz
- Basic requirements are
  - Sensitive for weak PMT signals
  - Fast
  - Low latency
  - Low power
  - Cheap
- Alternative to the „Analog Trigger" designed by Spanish colleagues
  - Based on analog sums of up to 21 pixel
  - Theoretically better for weak and noisy signals (LST)

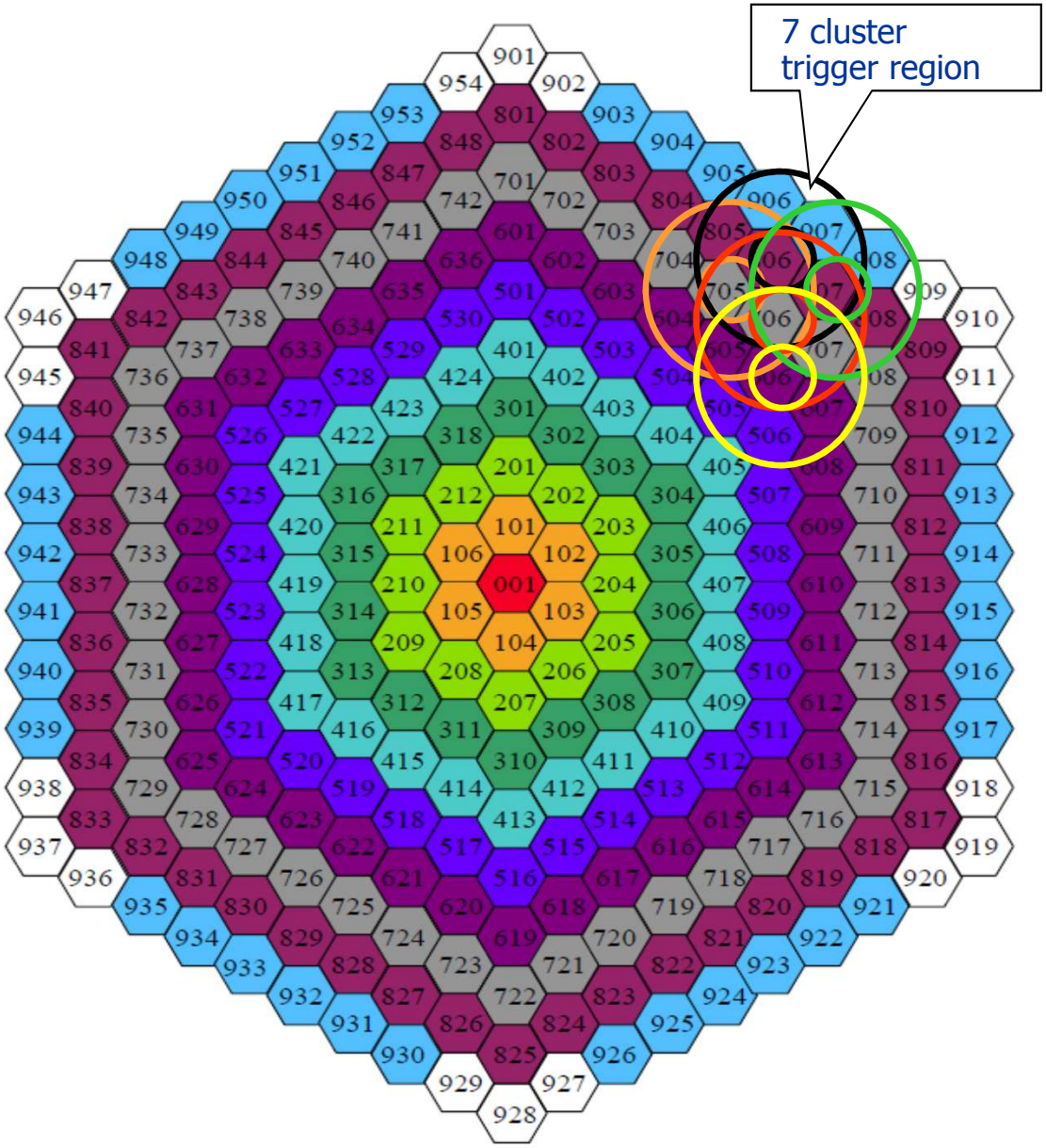
37 Pixel Trigger Region



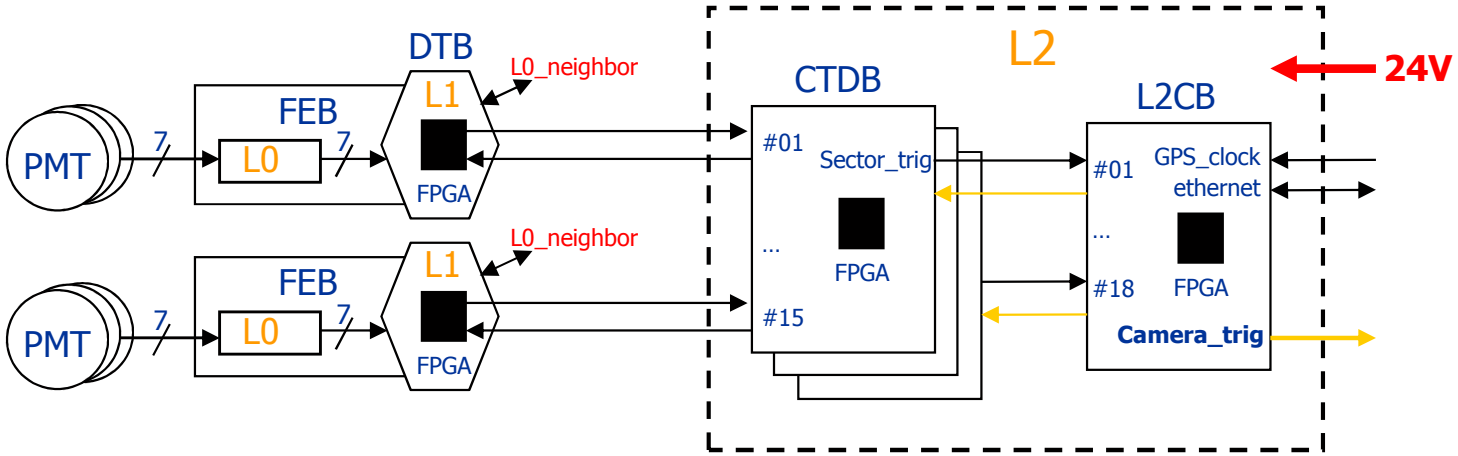


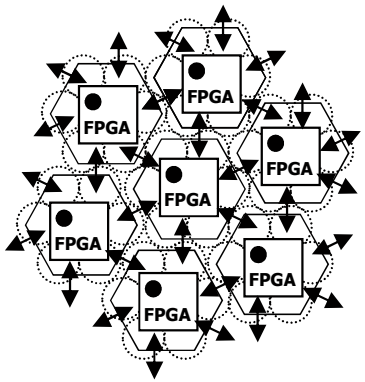
37 Pixel Trigger Regions

- clusters (not pixel !) of a MST shown
- Each heagon represents 7 pixel
- the trigger region overlaps by four pixels always



The Trigger Schema



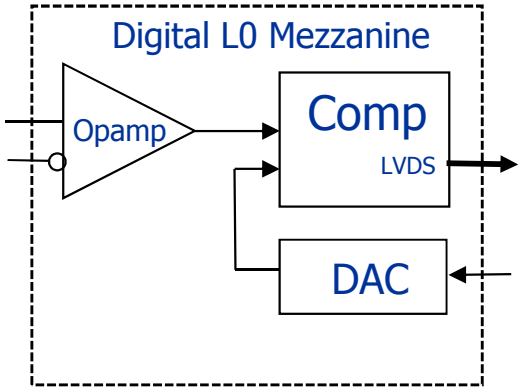


backplane connections

PMT = Photomultiplier Tube
FEB = Frontend Board
DTB = Digital Trigger Backplane
CDTB = Clock & Trigger Distribution Board
L2CB = L2 Controller Board

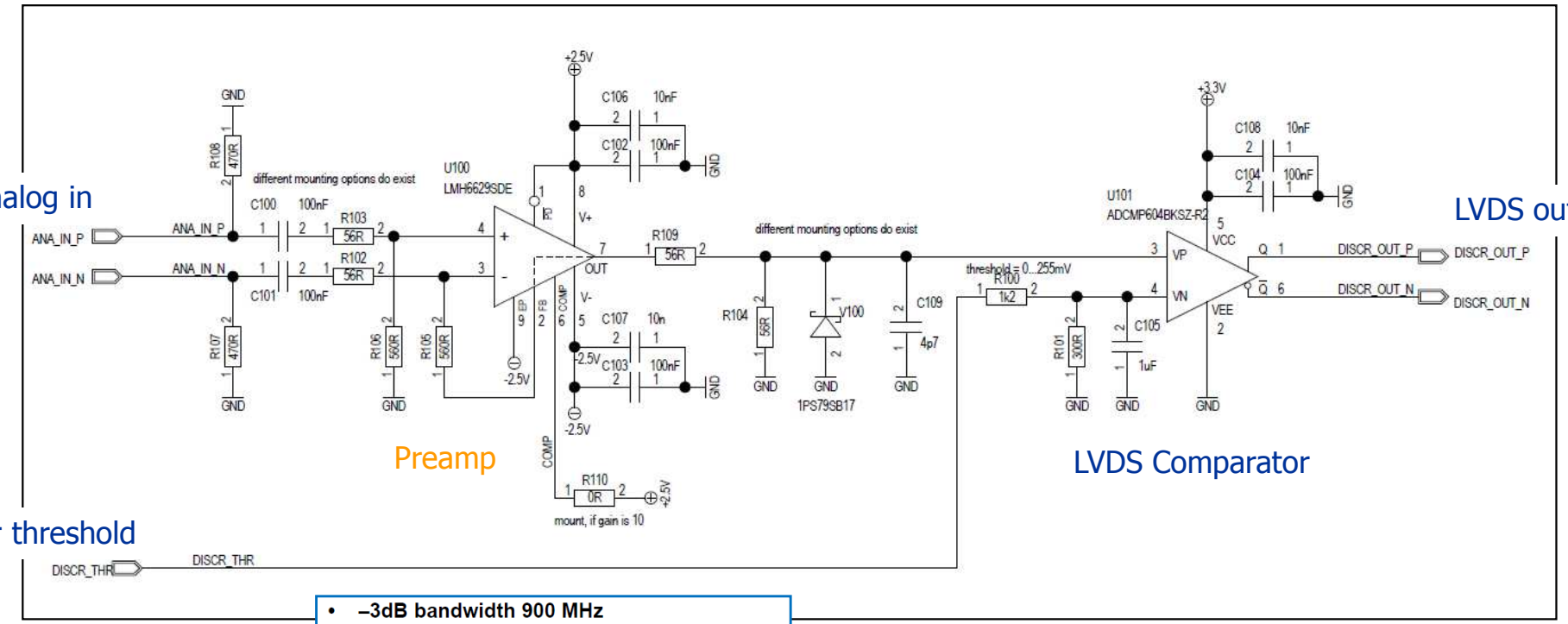
Digital Trigger L0 Mezzanine Board

- 7 channels
- Schematic simulated
- LMH6629, very low noise, low offset preamplifier



Diff. Analog in

LVDS out



Preamp

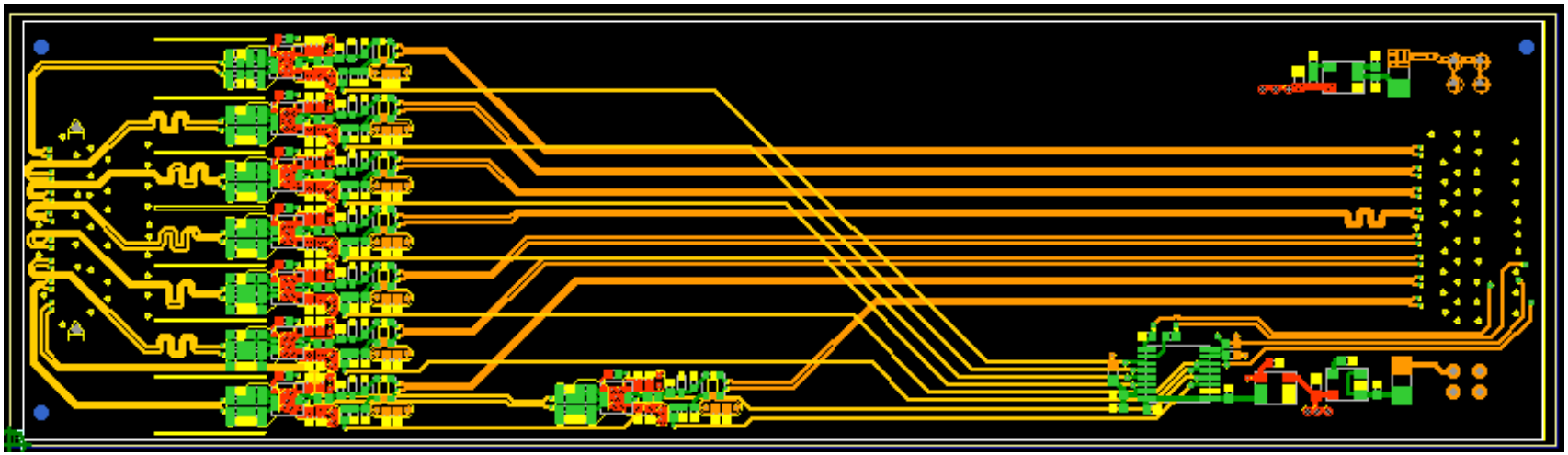
LVDS Comparator

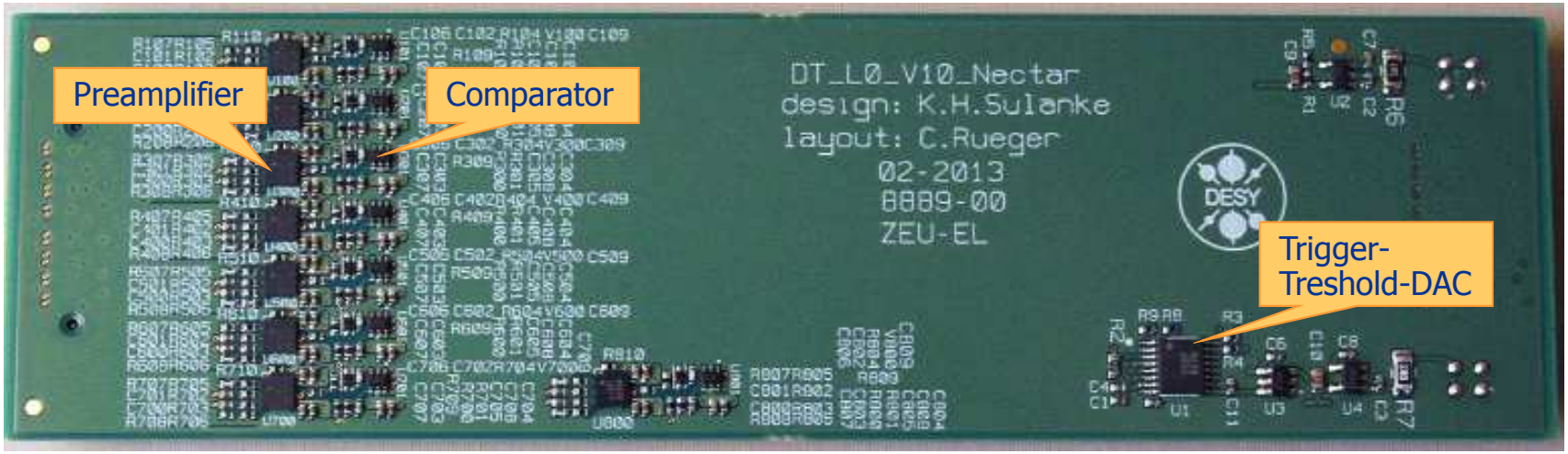
Trigger threshold

- **–3dB bandwidth 900 MHz**
- **Input voltage noise 0.69 nV/√Hz**
- **Input offset voltage max. over temperature ±0.8 mV**
- **Slew rate 1600 V/ µs**

Digital Trigger L0 Mezzanine Board

- 6 layer PCB with length-tuned signal lines



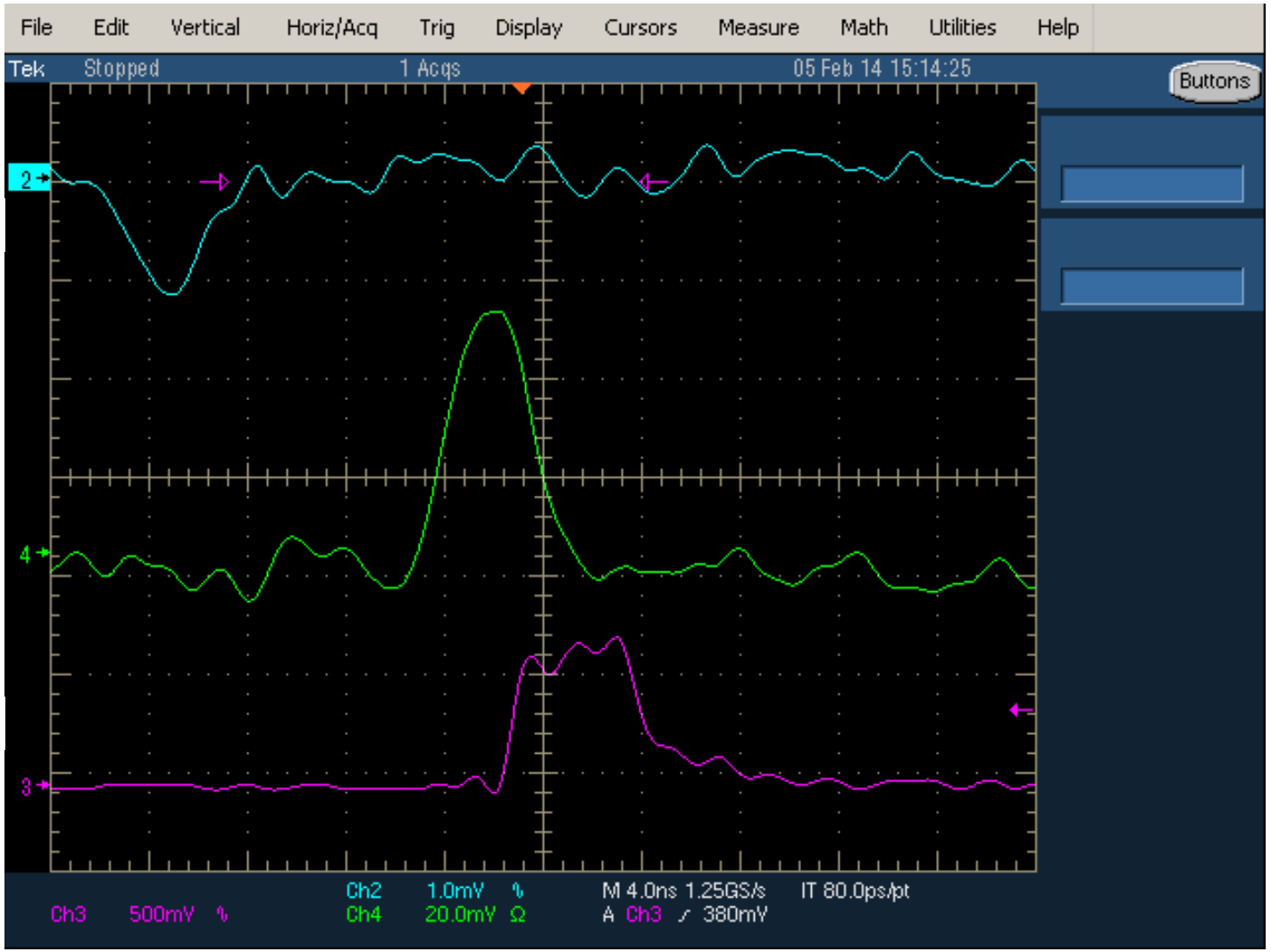


L0, minimum analog input Level

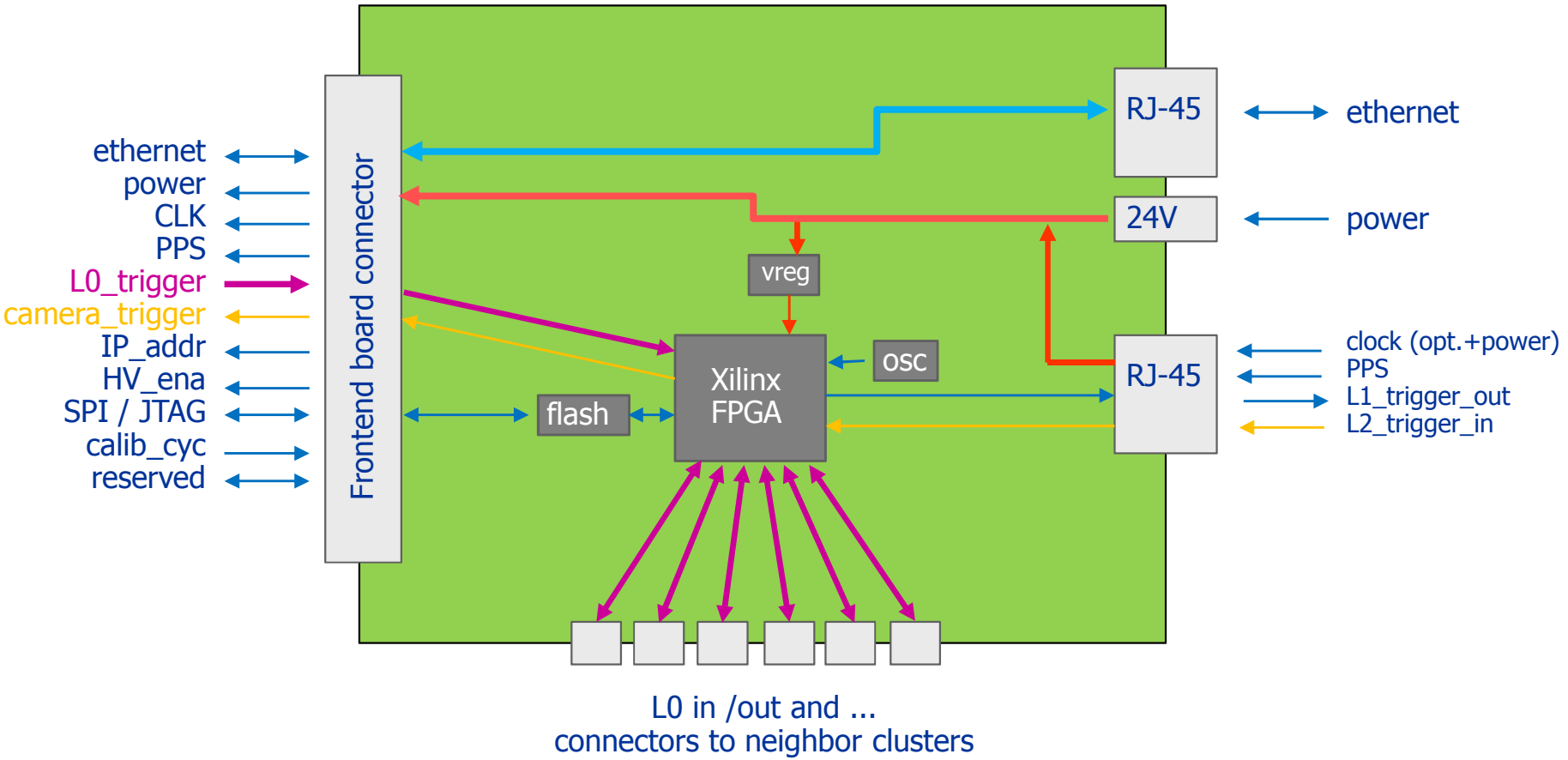
Analog_in, 1mV pk

Comp_in, gain = 27

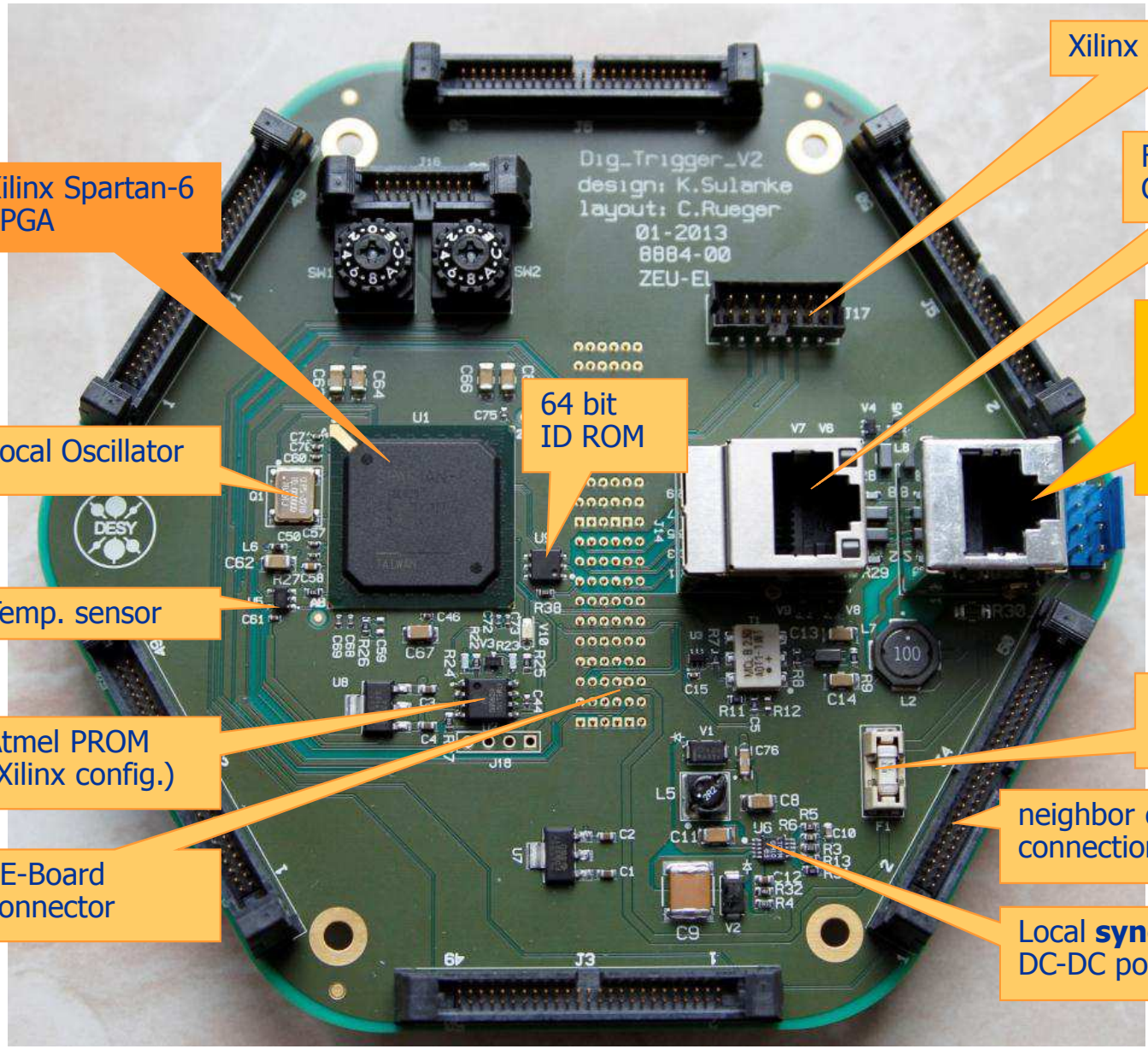
Comp_out, thr=12mV



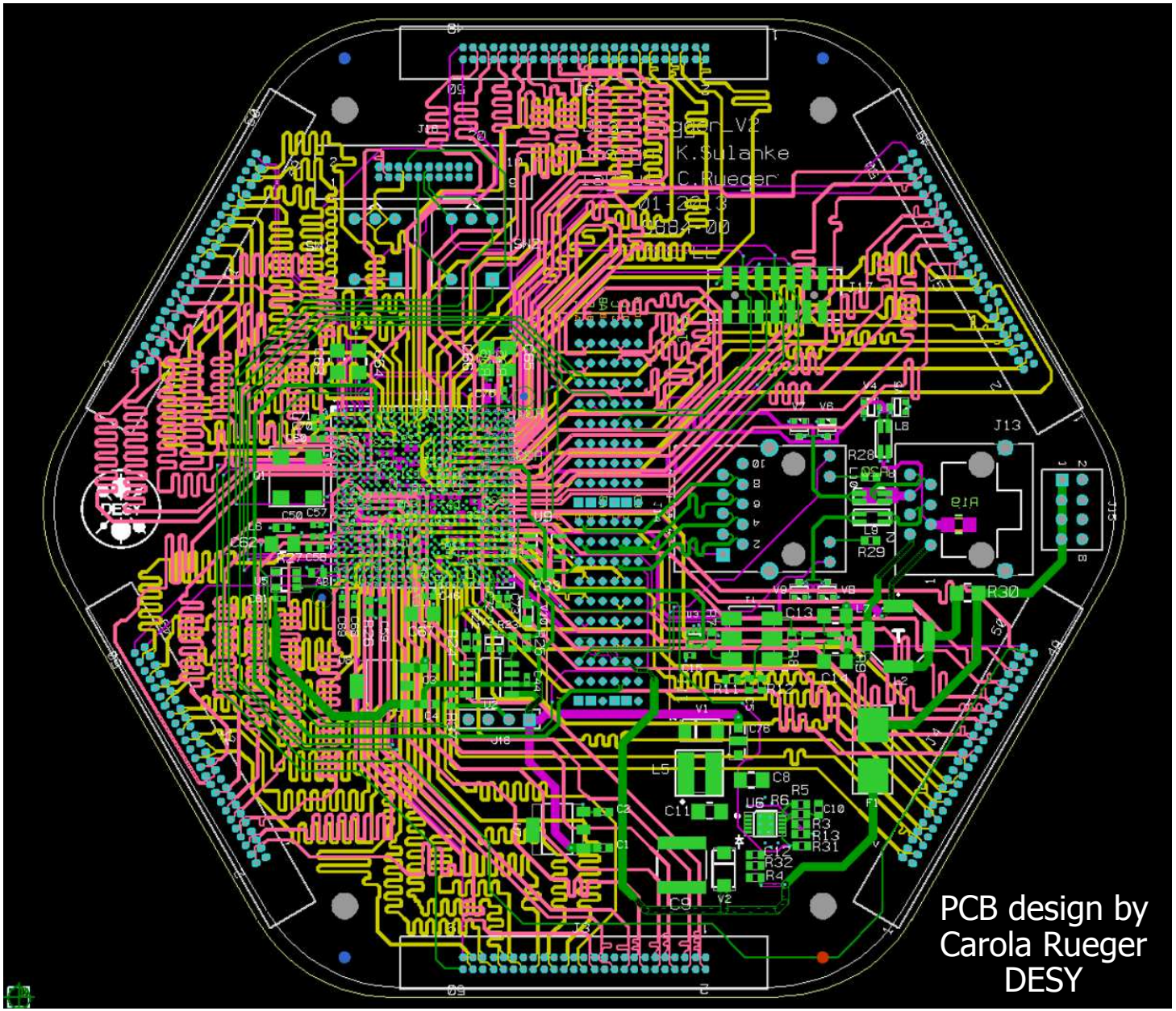
L1, Digital Trigger Backplane Rev. 2



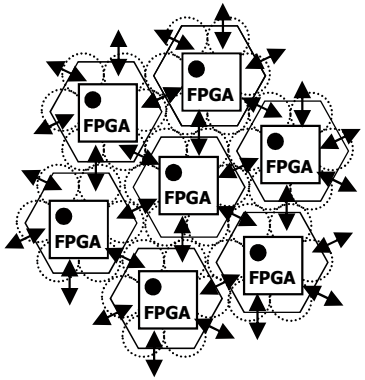
Digital Trigger Backplane, cont.

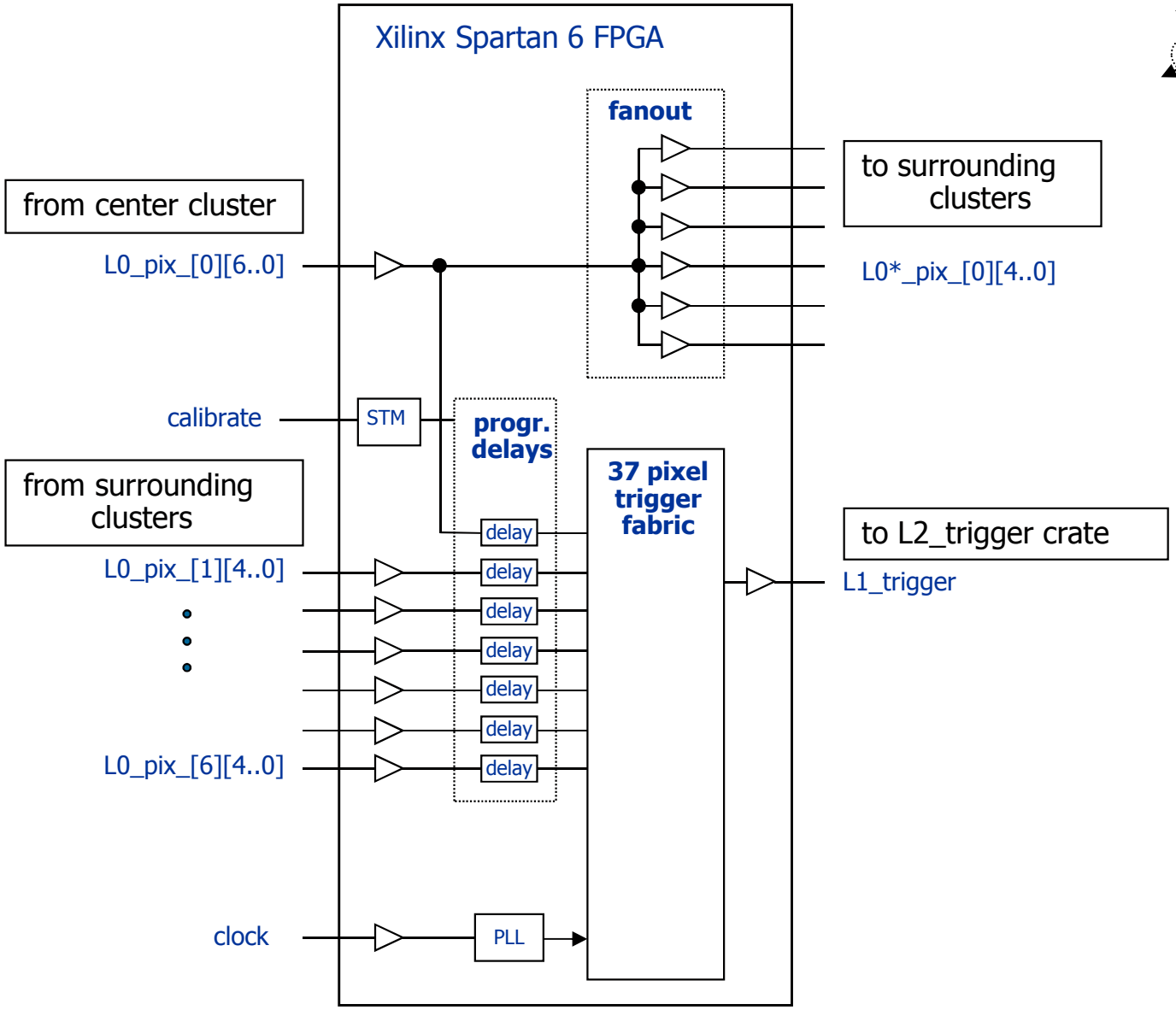


Digital Trigger Backplane, 8 Layer PCB

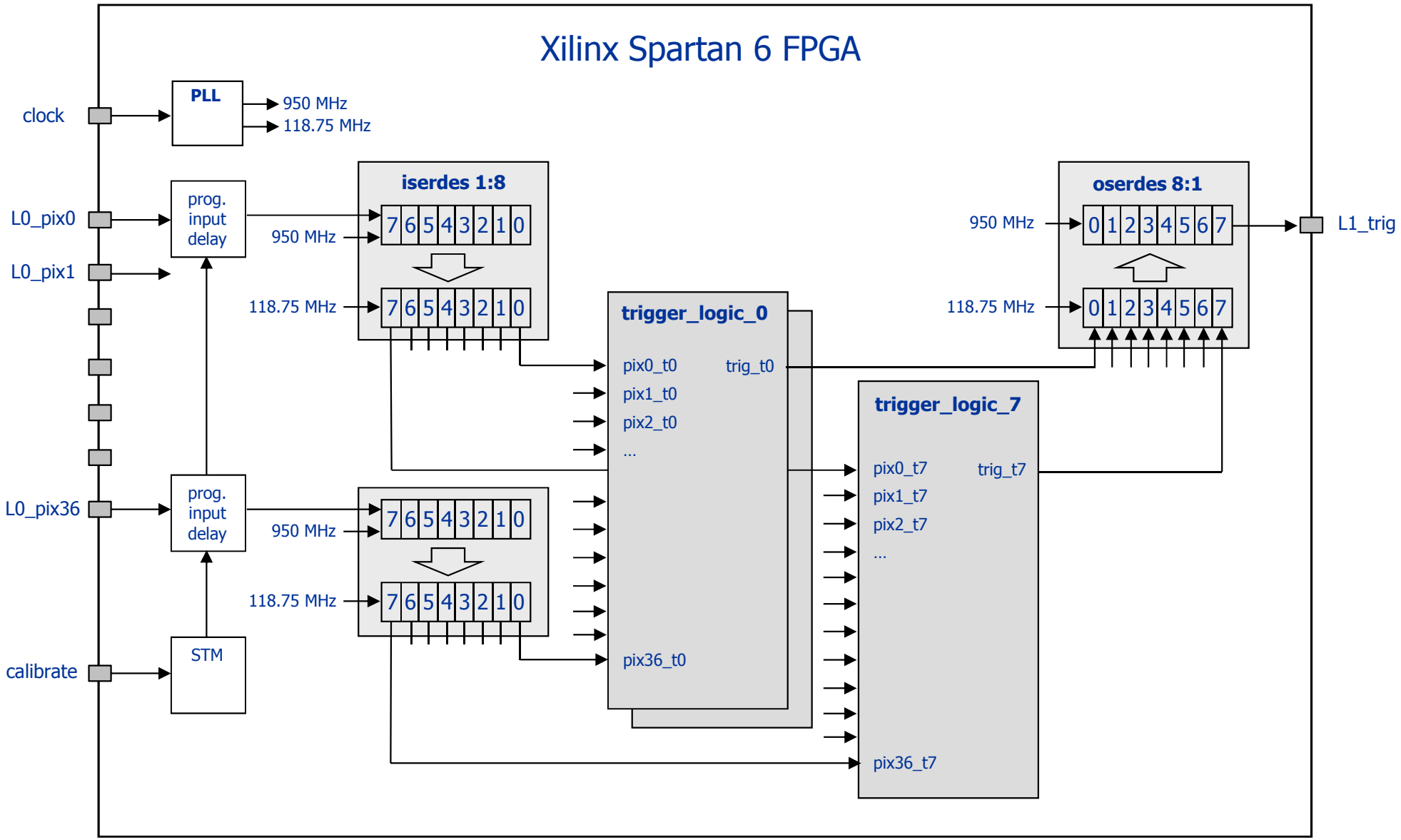


The L1-FPGA's Functionality





The L1-FPGA's Functionality, cont.

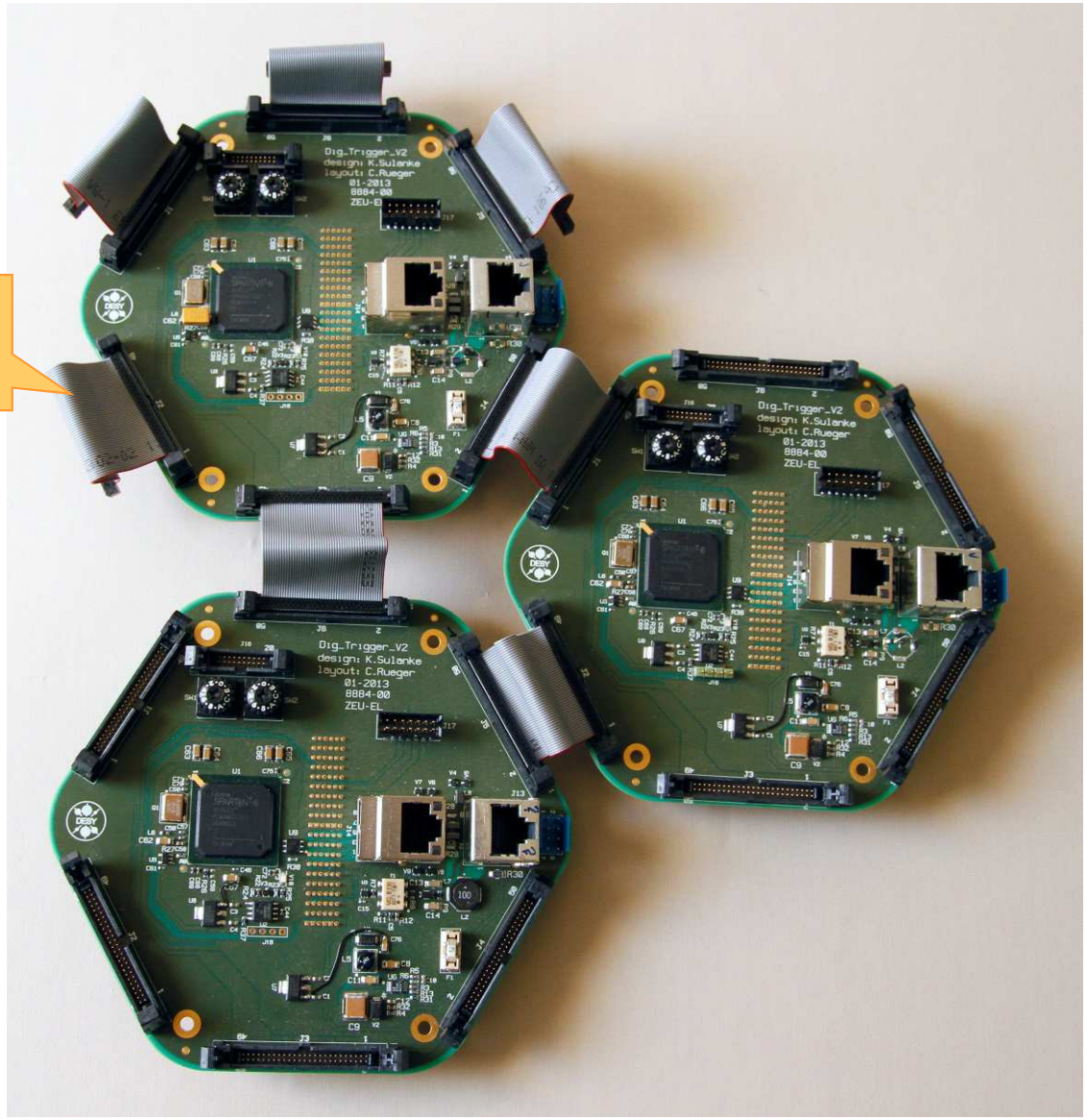


3NN Trigger Firmware

- 3NN (3 Next Neighbor) of 37 pixel
  - about 500 possible combinations
- Fully synchronous design
  - local oscillator (25 Mhz) or external clock (100 MHz)
- Trigger latency 120 ns
- Trigger time resolution 1.05 ns (950 Mhz L0-sampling rate)
- Trigger jitter +/- 1.05 ns
- Firmware automatically detects missing neighbor clusters (bit masking)

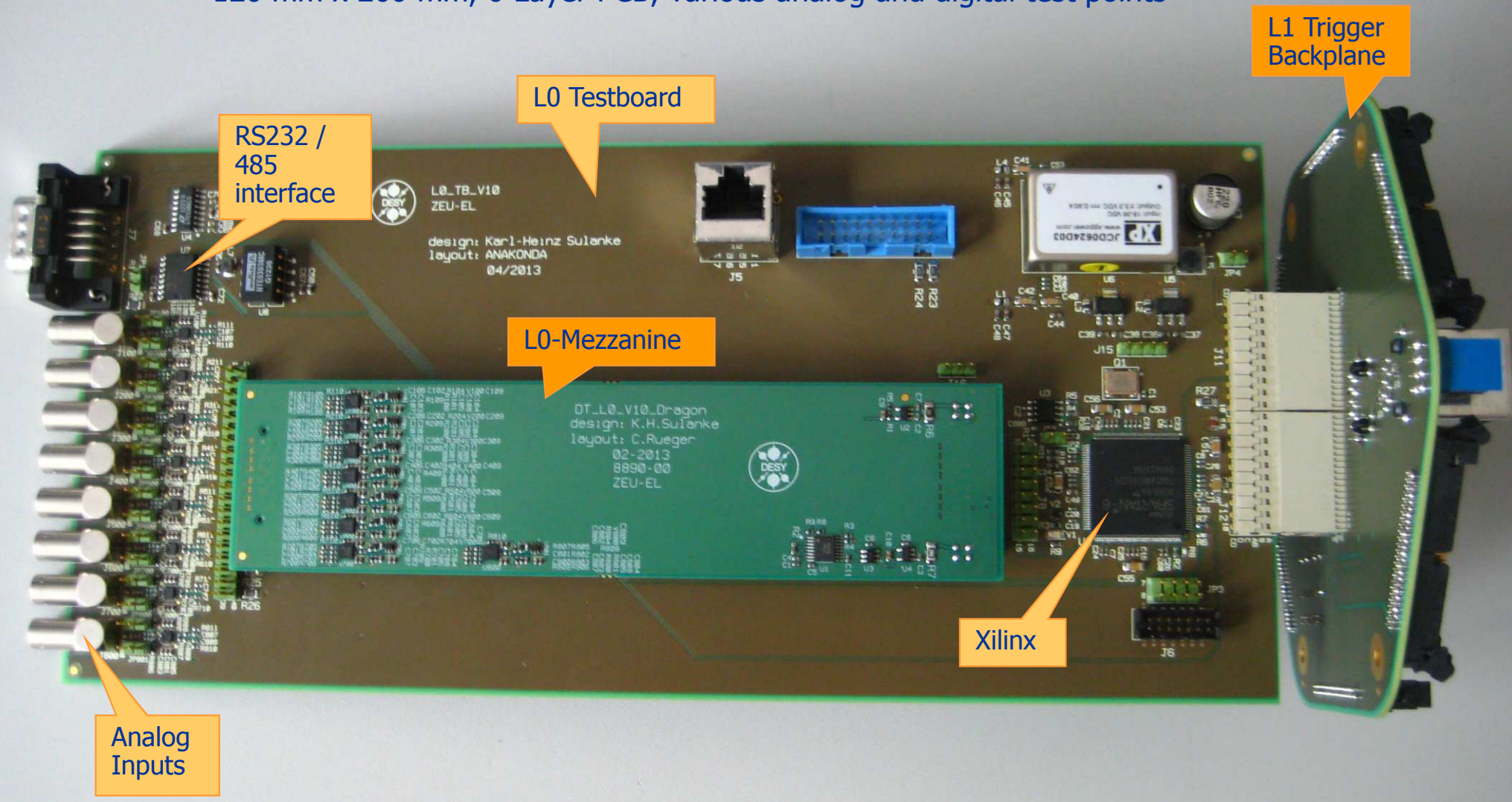
L1, Connecting the Trigger Backplanes

50 way
0.635 mm
pitch cable

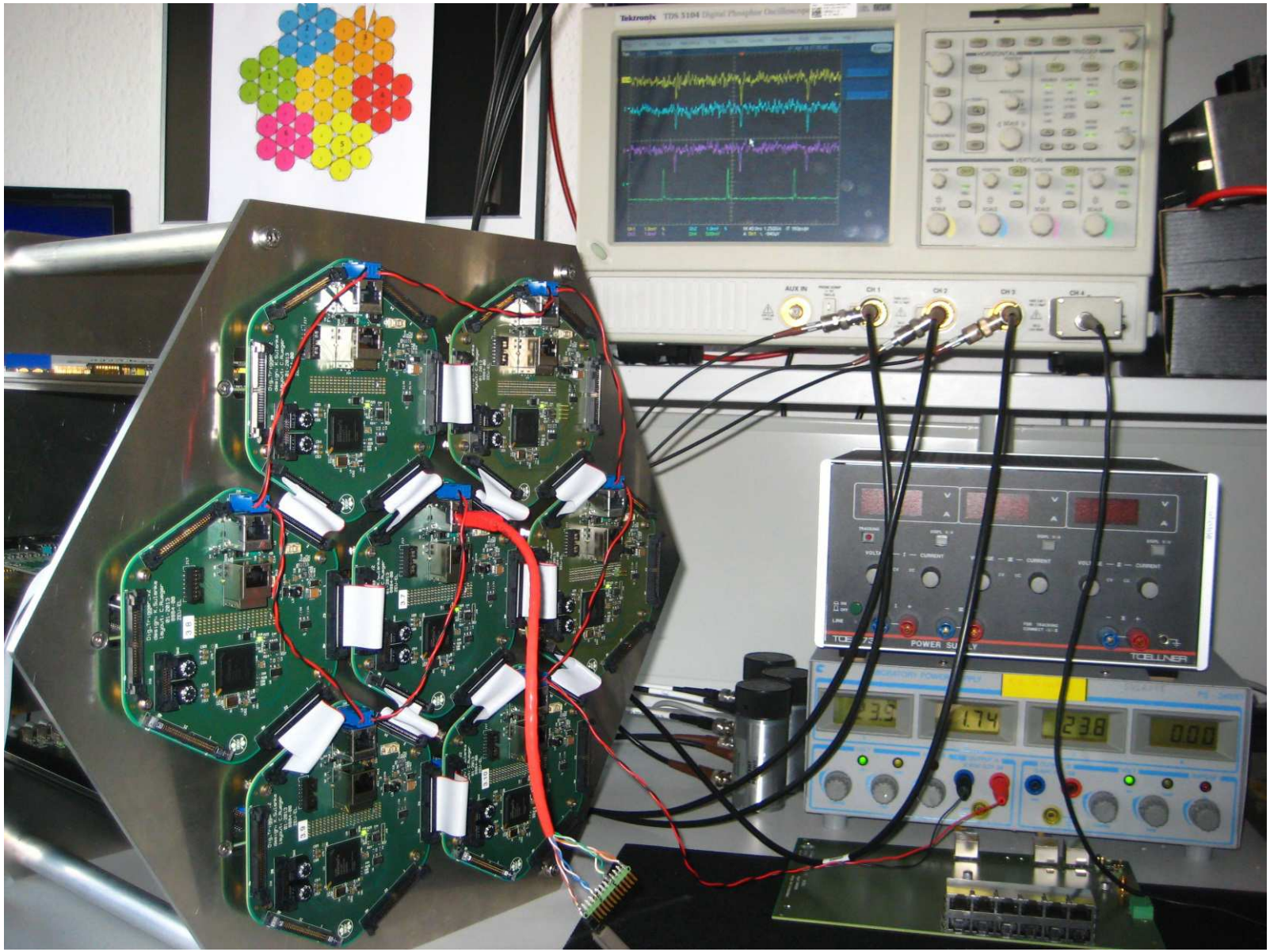


Digital Trigger Test Setup

- 120 mm x 260 mm, 6 Layer PCB, various analog and digital test points

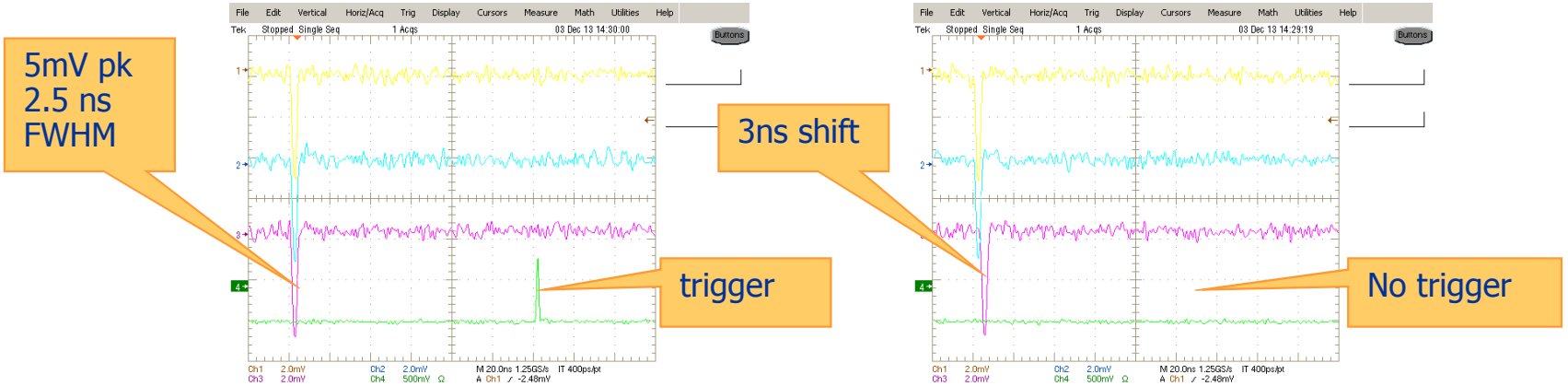


Digital Trigger Test Setup at DESY

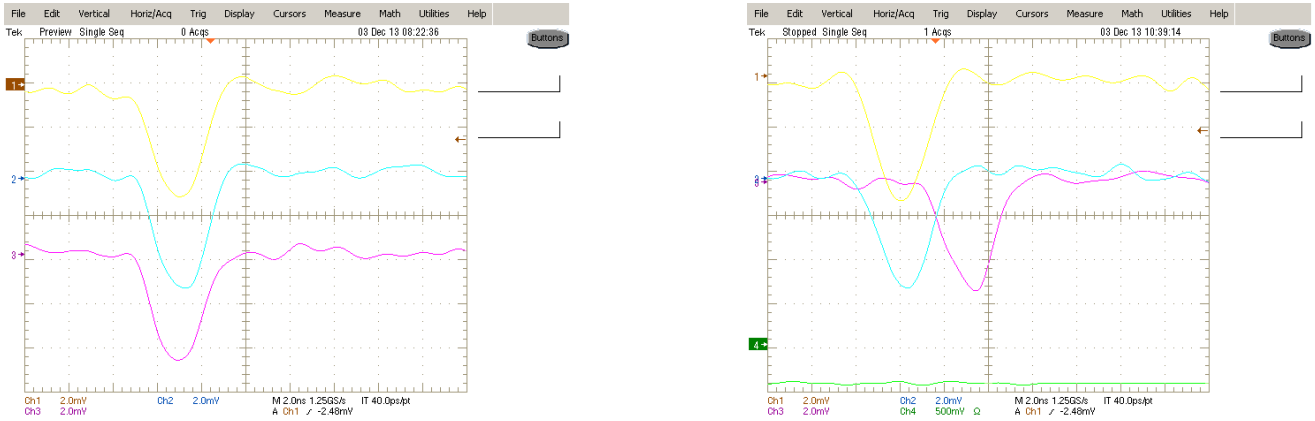


3NN Trigger Test Results

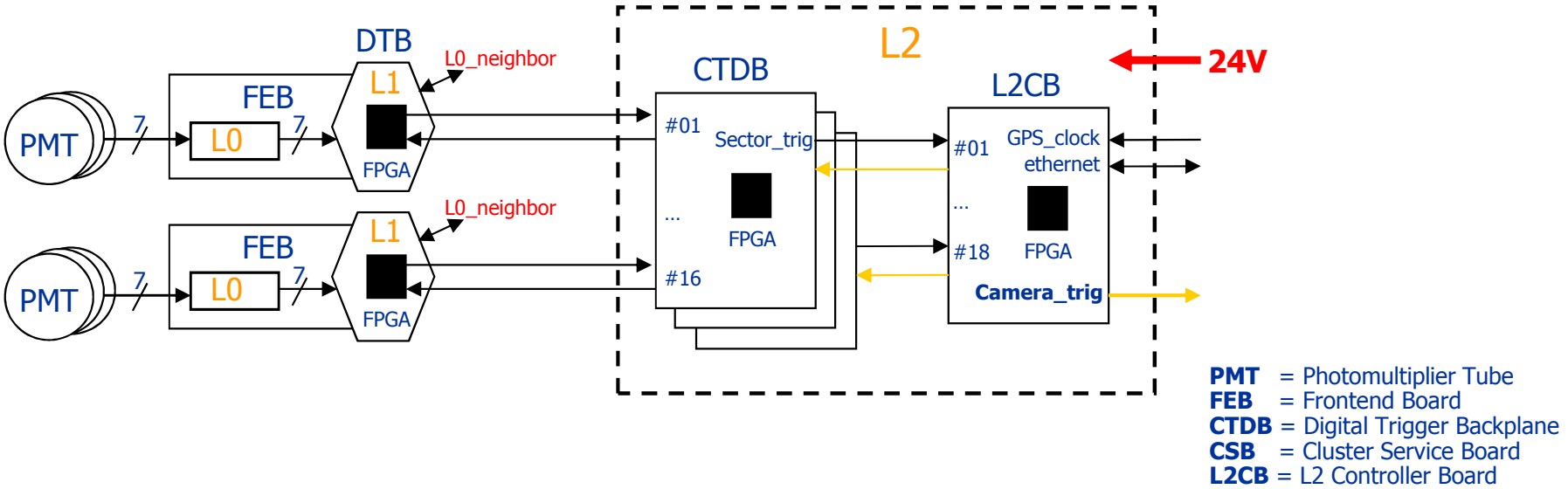
- 100% trigger and 0% trigger situation



- Analog input signals, zoomed time scale

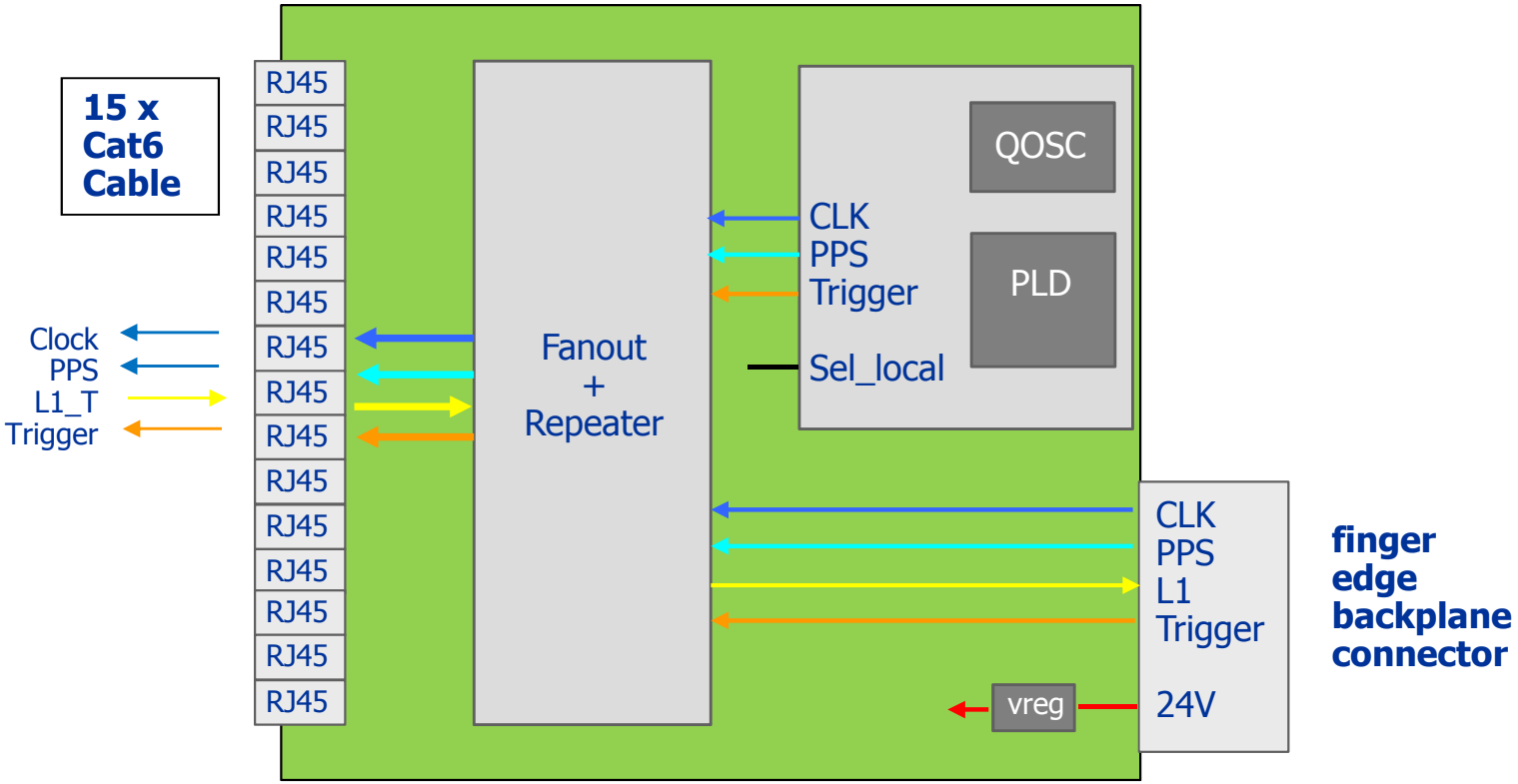


L2



- L2 still in the design phase
  - will be a crate, ~ 50 x 20 x 20 cm, ~ 11 kg
    - 18 x CTDB (Clock & Trigger DistributionBoard)
    - 1 x L2CB (L2 Controller Board)
      - Ethernet interface
      - Optical / electrical camera trigger output

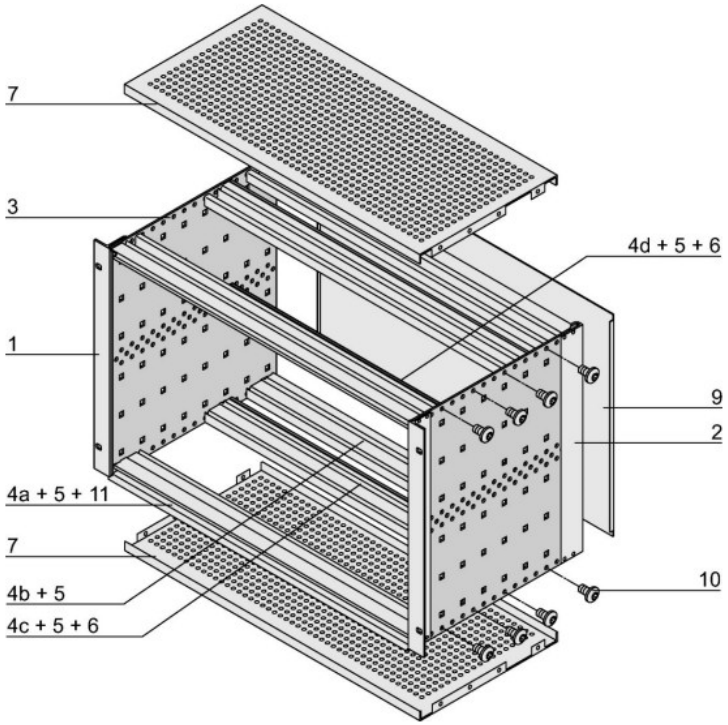
The Clock & Trigger Distribution Board (CTDB)

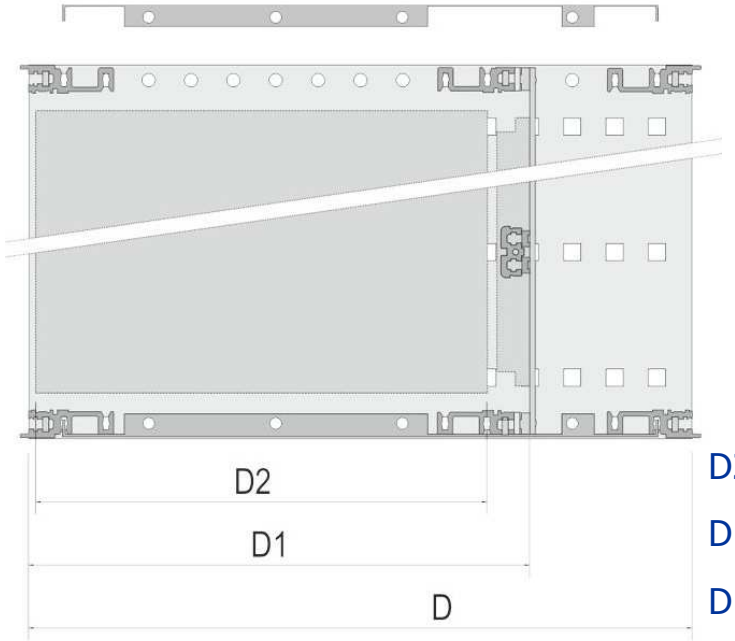


- Local mode, clk+pps+trigger by Altera PLD EPM3064, for test purposes
- Schematic design done
- Card size 160 x 233

The L2-Crate

- Schroff 24563-442
- 6 U, 84 HP (21 slots)
- Card size : 233 x 160 mm
- Preferred slot usage, see below

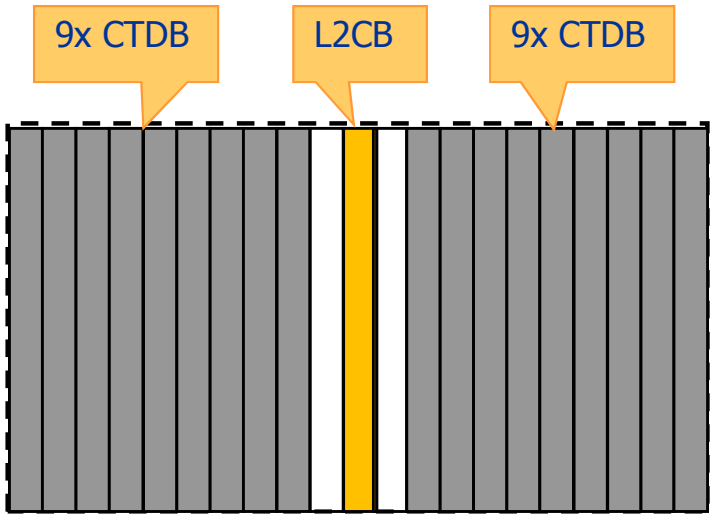




D2 = 160 mm

D1 = 175 mm

D = 235 mm



Summary

- Main advantage of the digital trigger is its flexibility concerning the trigger algorithm and the simplicity of the overall scheme
- The L0 stage performs very good (signals of 1mV are still detectable)
- First results with the L1 stage, e.g. the 3NN trigger, are encouraging
  - More sophisticated alghorithms will follow
  - E.g. a time gradient trigger
- The L2 stage will be designed and tested in 2015
  - Intermediate solution (by Axel Kretzschmann) do exist
- First camera integration tests in 2014 successful
- Not yet clear who makes it finally, the analog or the digital trigger ?

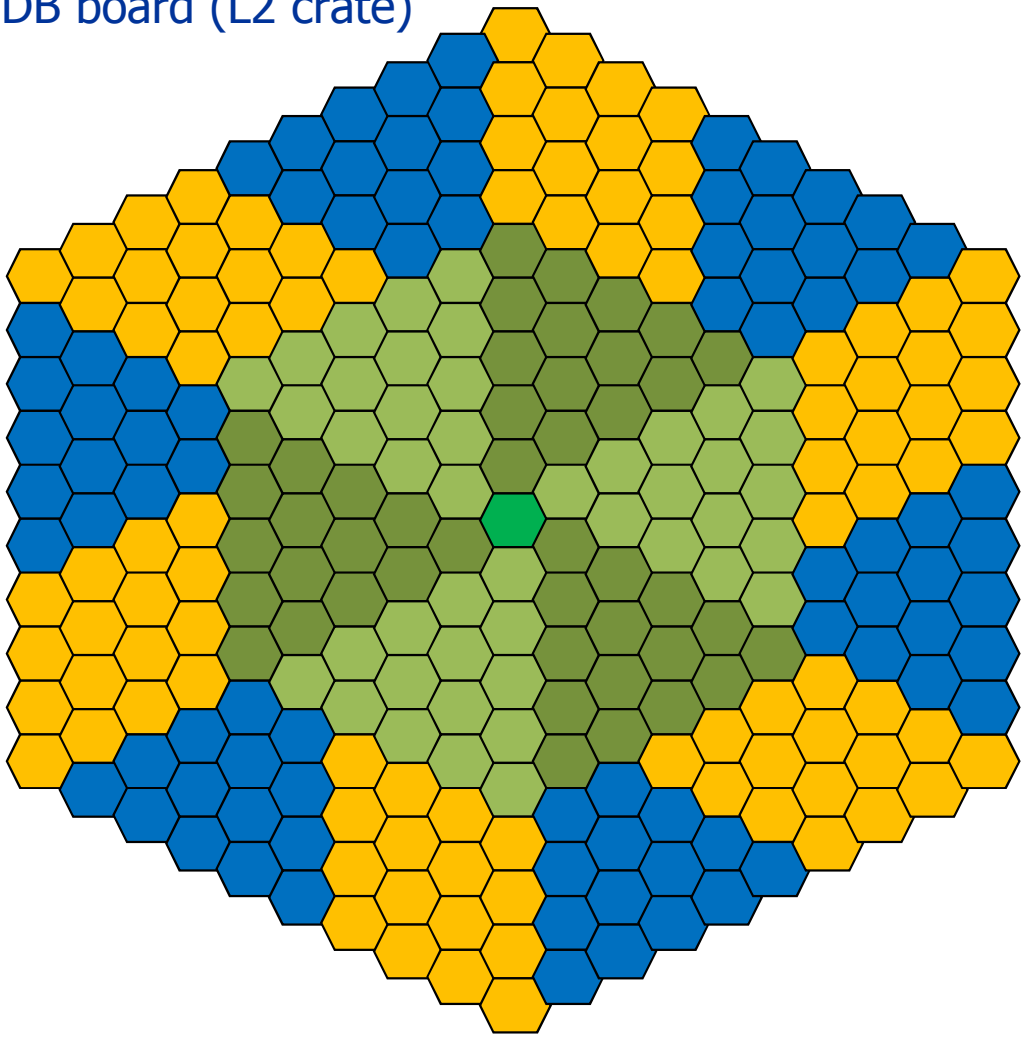
Outlook

- 19 cluster „Demonstrator" test planned in Q4 2015
  - NectarCam (MST, France)
    - Nectar chip based (analog pipeline chip)

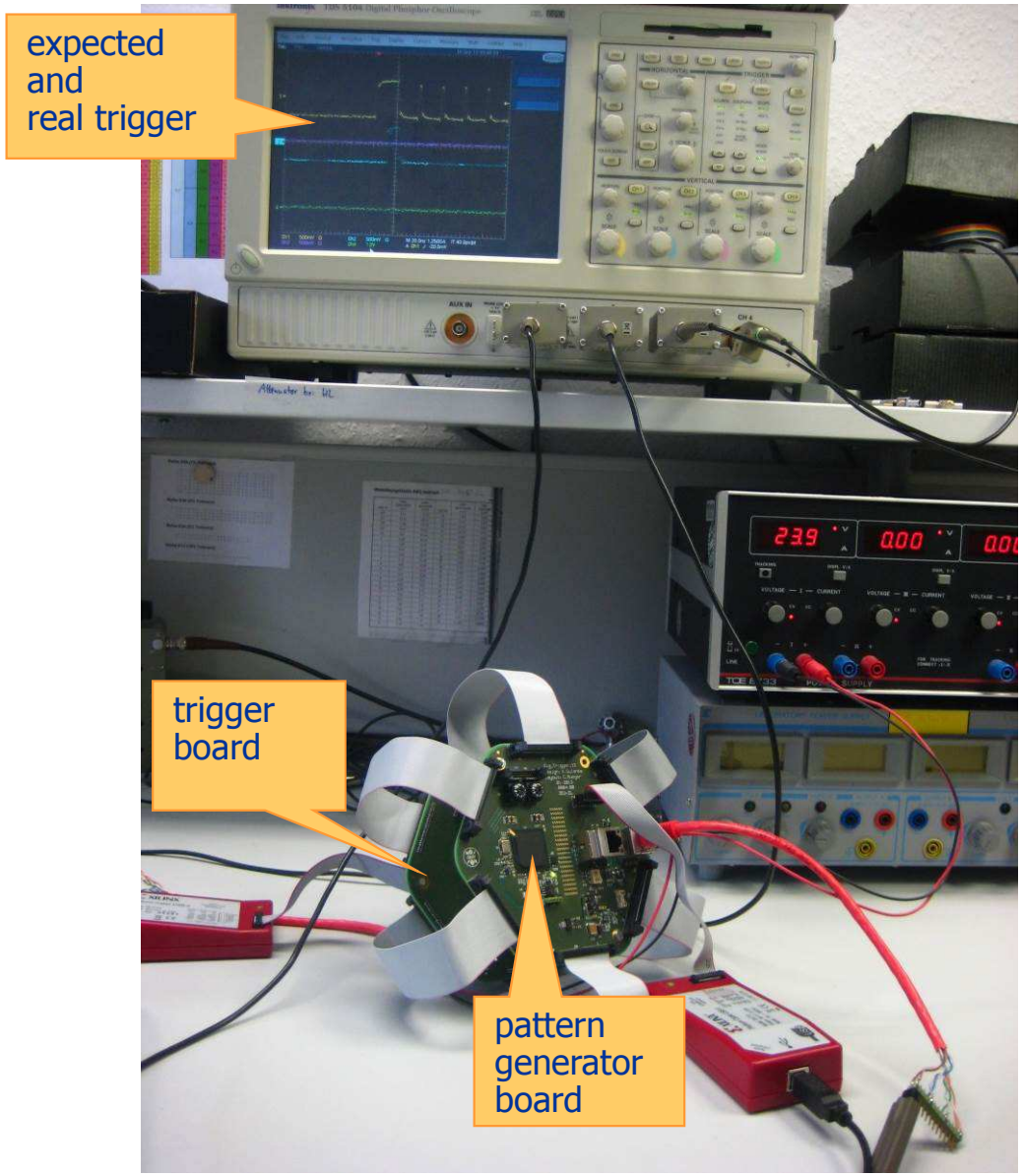
Back Up Slides

L2 Trigger Sectors, MST, Example

- 271 cluster shown (1897 pixel)
- Each sector comprises 14..16 clusters and is connected to a certain CTDB board (L2 crate)



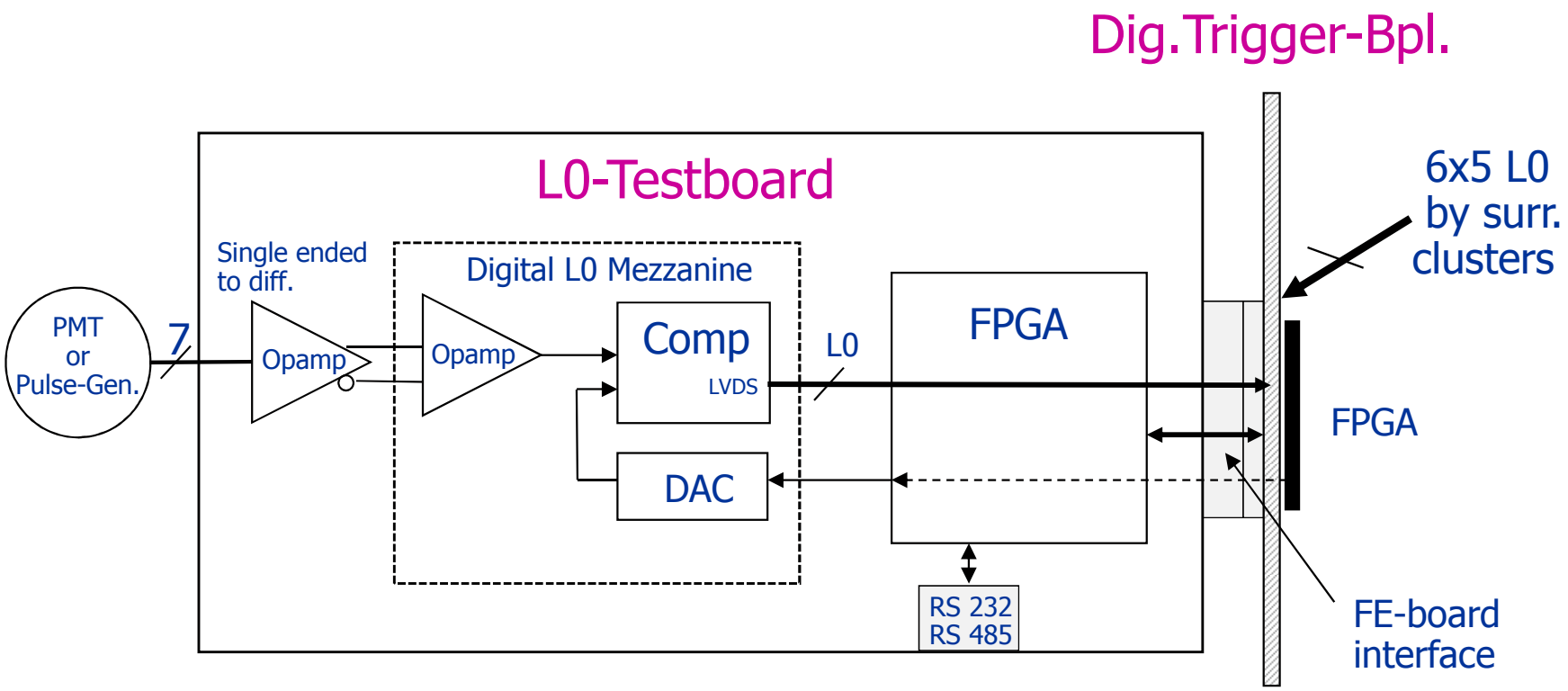
Test Setup w. Pattern Generator



- DTB used as pattern generator board
- e.g. for 3NN pattern
- time resolution is 1.05 ns

Digital Trigger Test Board

- Testing the L0 boards AND the FE-board interface of the Dig. Trigger Backplane
- Xilinx with RS232 / RS485 interface, to set the discriminator thresholds etc.



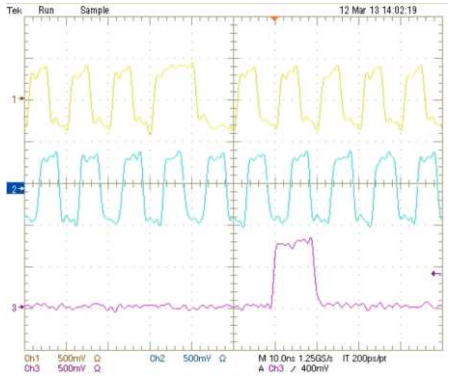
Digital Trigger Backplane, List of Key Hardware Features

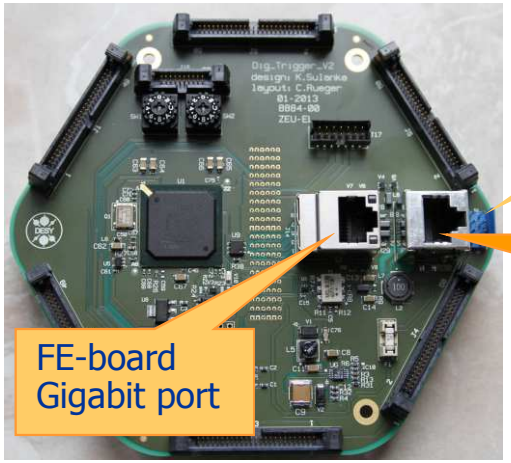
- Nominal power consumption: 1.5 W
- Weight : 95 g + 10 g cabling to neighbor clusters -> 28 kg for MST
- Automatic neighbor cluster recognition (border zone)
- Synchronous DC-DC converter (24 V to 3.0 V …)
- Local clock and external clock input (any diff. > 0.1V pk-pk)
- FPGA load by JTAG cable or PROM or remote (by FE board)
- 6 x bidirectional L0 signal connection with neighbor cluster
- Temperature sensor (allows automatic delay correction, if needed)
- adjustable 8 bit cluster position ID (for unique, position-independant, firmware)
- Gigabit ethernet pass through connection to FE-board
- RJ 45 connector as combined power and clock input (single cat5e cable)

Combined Power and Clock Input

- 24V, clock, and PPS over a single wire pair
- requires a single cat5e cable per cluster only (+ gigabit ethernet cable)
- Current spikes of 0.8 A did not influence the (recovered) clock quality

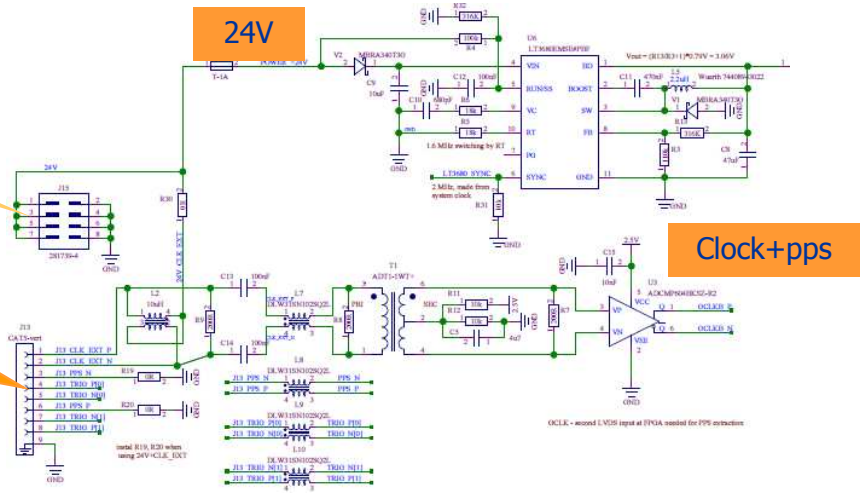
Cat5e - Wire Pair	Standard mode	Combined mode
1	Clock_in	Clock_in / PPS_in / 24V
2	PPS_in	GND
3	Trig_L1_out	Trig_L1_out
4	Trig_L2_in	Trig_L2_in





Alternative Power conn.

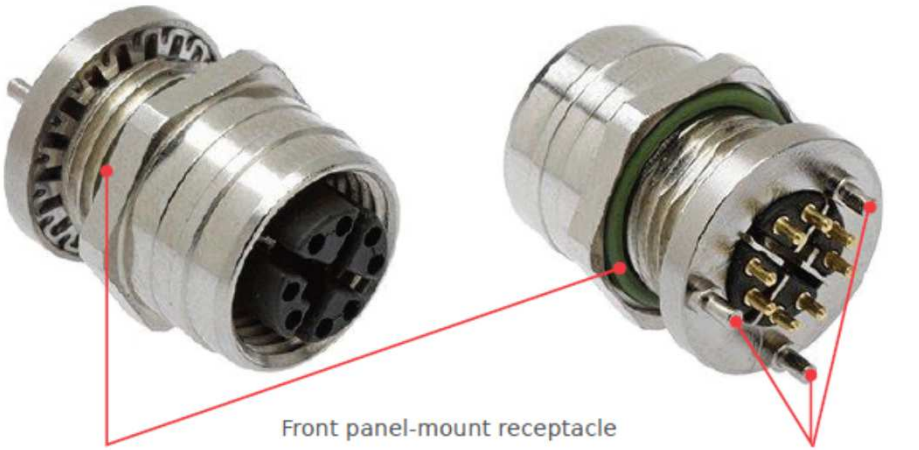
Combined Power and Clock input

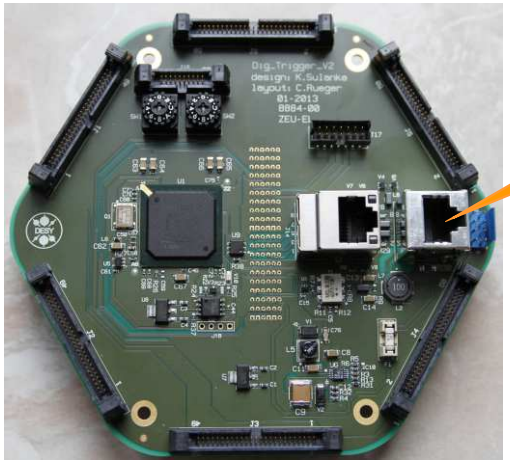


M12 Cat6 , Combined Power / Clock Input

- Instead of RJ45, more robust
- by Harting, Molex, ...

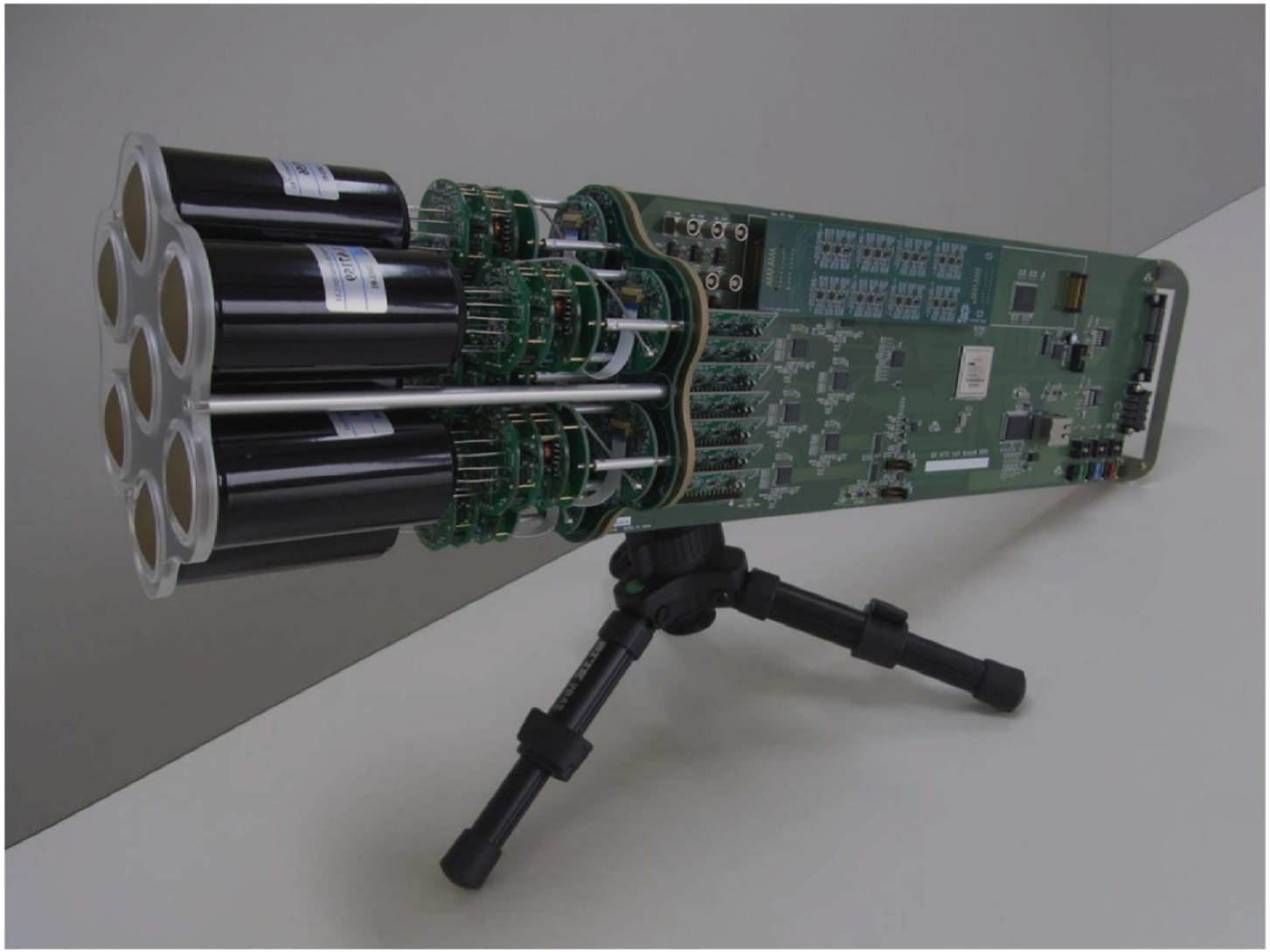
M12 Male-to-Male Cable Assemblies



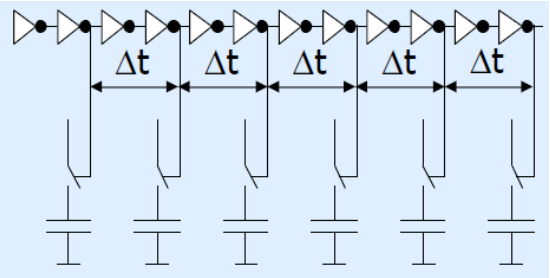


To be replaced by M12

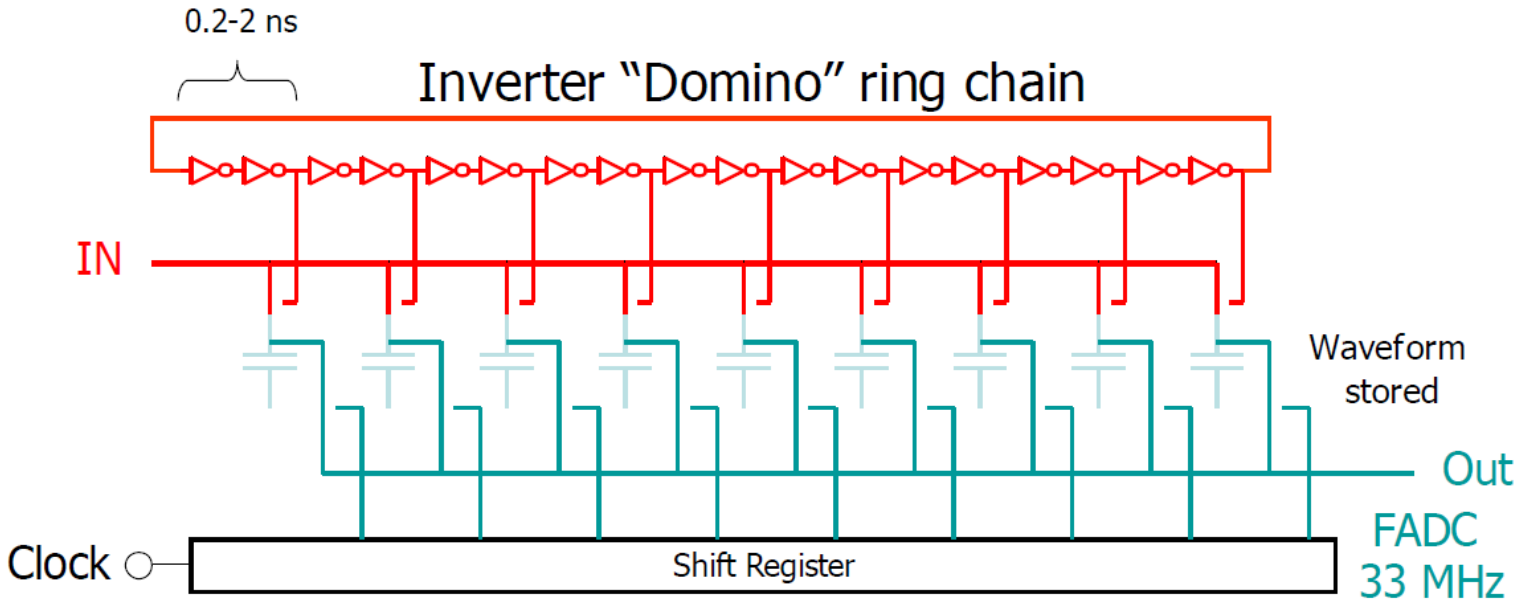
7-PMT-Cluster “DragonCam”



Analog Pipeline Chip



- 500 MHz ... 5 GHz sampling rate



"Time stretcher" GHz → MHz

Keep Domino wave running in a circular fashion and stop by trigger → Domino Ring Sampler (DRS)