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Integrated phase locked loop design

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A phase locked loop structure will be presented, which generates the sampling clock for an ADC in an on-chip pulse detection receiver.
Phase locked loops generate output clocks with the same phase as and a multiple of the frequency of a reference clock. The main blocks of a PLL are a phase frequency detector (PFD), a charge pump, a loop filter, a voltage controlled oscillator (VCO) and a frequency divider. The output clocks are generated through a four stage voltage controlled ring oscillator with 2GHz center frequency. The reference frequency is in the range of 20MHz-100MHz, so a frequency divider is necessary in the feedback path of the PLL to generate lower frequency clocks to synchronize with reference frequency. The PFD determines the phase and frequency difference between two inputs of the PLL. The phase and frequency difference is converted to a proportional current through the charge pump. The low pass filter extracts the dc amount of current to generate an appropriate control voltage for the oscillator to adjust the phase and frequency of the output clocks. In general, frequency dividers are divided into two categories of integer and fractional. Both of these frequency dividers are implemented as design alternatives for this structure. The division ratio of an integer frequency divider is a constant power of two. For some applications, in which the reference frequency changes, a fractional divider is a good option. In a fractional structure, the division ratio can be changed and is controlled by binary bits. The proposed structure is simulated in 65nm TSMC technology. Layout design currently is done for the VCO and according to post layout simulation, the VCO shows -92dB/Hz phase noise at 1MHz offset from the center frequency. The simulation results indicate 11.1mW power consumption from 1.2V supply voltage for the whole structure using integer frequency divider and 16mW power consumption using fractional divider.

Summary

A phase locked loop structure was designed in TSMC 65nm technology, which generates the sampling clock for an ADC in an on-chip pulse detection receiver. Design aspects and simulation results will be shown.

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