

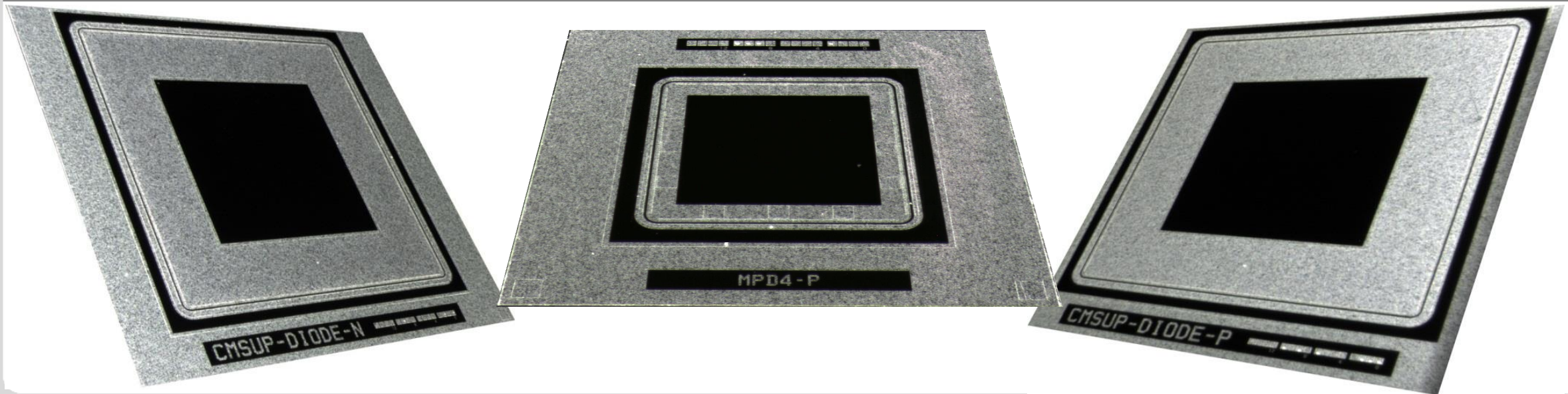
► HV-CMOS

30.09.2014

Robert Eber

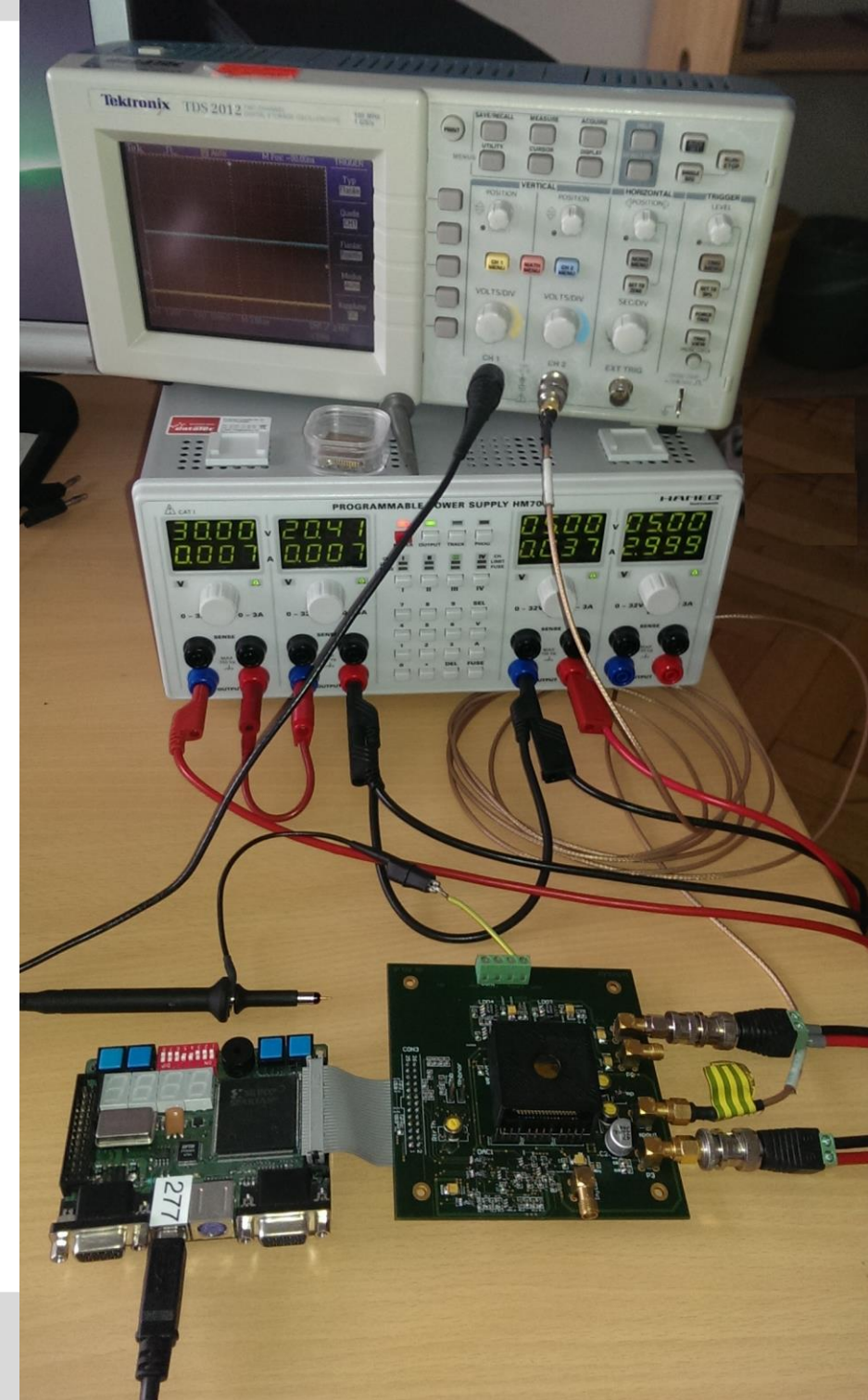
HV-CMOS

Institut für Experimentelle Kernphysik

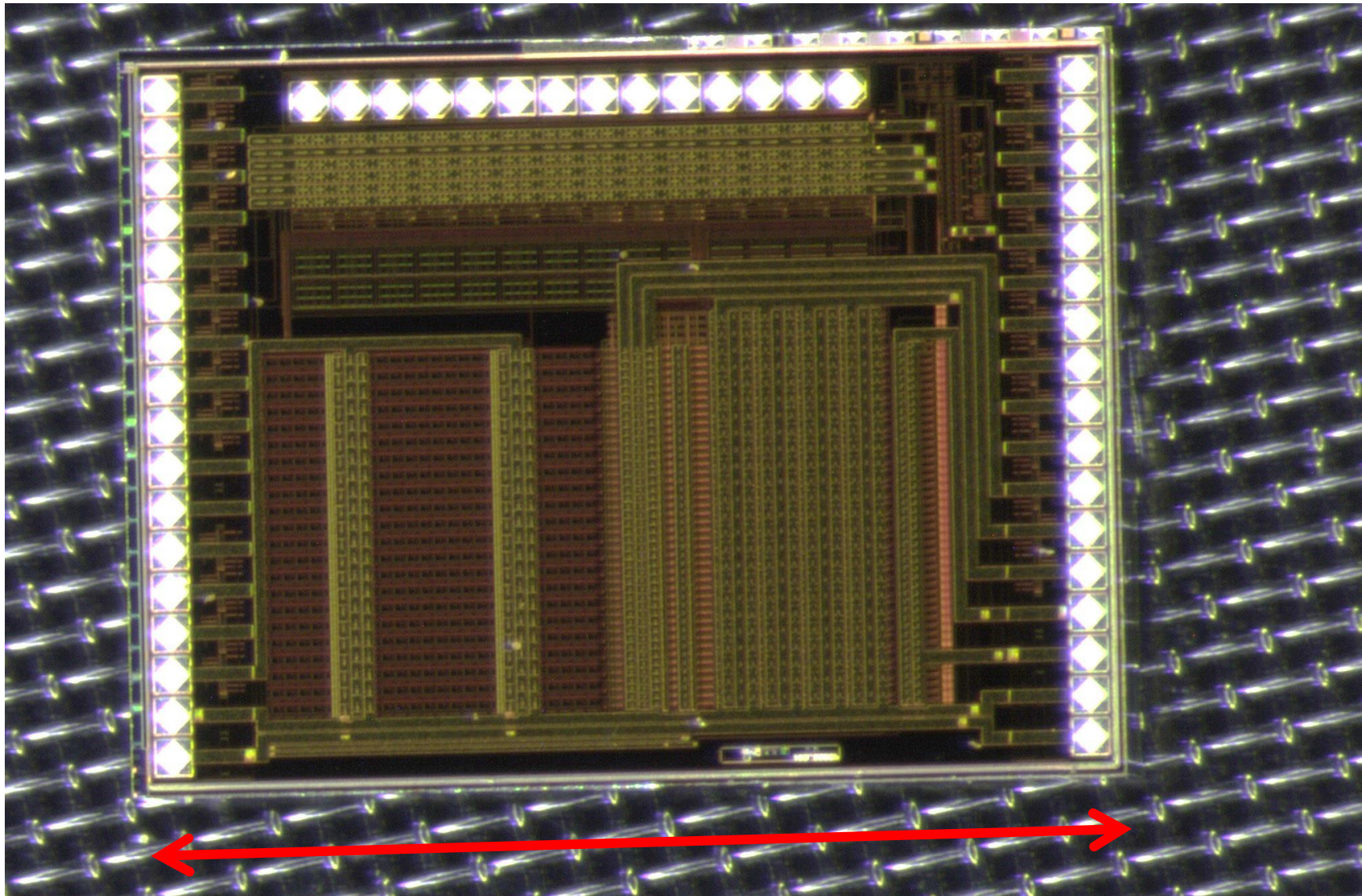


Overview of Components

- Uxibo (FPGA board, Spartan-II)
 - Readout framework provided by Ivan Peric
 - Simple wiring done for H35
- HV-Board
 - Complete assembly at KIT
- HVStripV1 Chip (HV-CMOS chip to be tested)
 - Some difficulties with bonding
 - 2 Chips available atm
- Voltage source (5V supply)
- HV source ($\sim -60\text{V}$ bias voltage)
- Oscilloscope (TEK, up to 1GHz, 5GS/s available)
- Sr-90, Fe-55 sources available



H35 Chip under the microscope

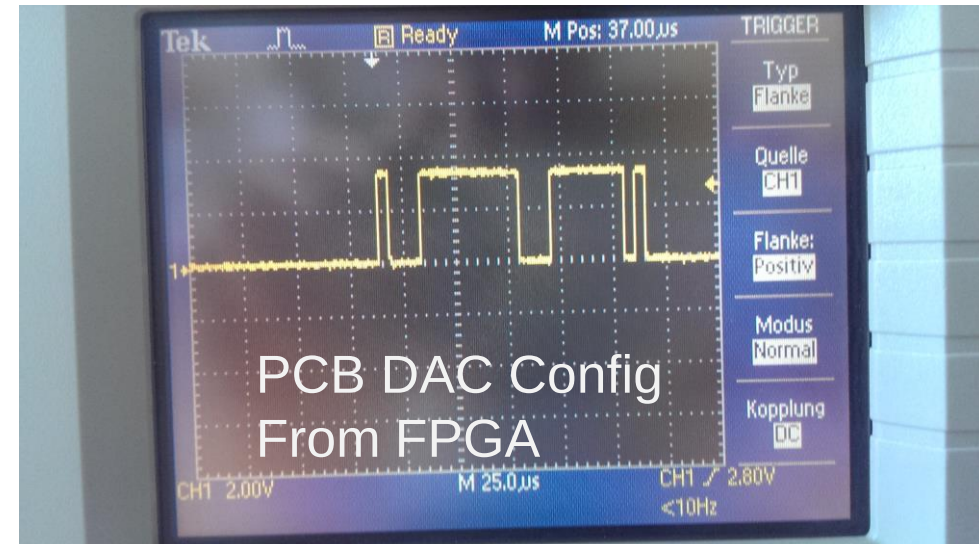


2.5mm

-
- HV-CMOS**
- MainMenu About
- ### Tests
- Test Initialize H35 Config H35 Pixel Config
- | | | | |
|------------|---|-----------|----|
| TDAC1 | 0 | BiasDac0 | 20 |
| TDAC2 | 0 | BiasDac1 | 20 |
| TDAC3 | 0 | BiasDac2 | 10 |
| ABEnB | 0 | BiasDac3 | 20 |
| ComOffNorm | 0 | BiasDac4 | 10 |
| CompOffB | 0 | BiasDac5 | 0 |
| EnLowPass | 0 | BiasDac6 | 5 |
| | | BiasDac7 | 10 |
| | | BiasDac8 | 0 |
| | | BiasDac9 | 10 |
| | | BiasDac10 | 0 |
| | | BiasDac11 | 0 |
| | | BiasDac12 | 60 |
| | | BiasDac13 | 10 |
- Configure Chip Register
- Configure PCB_Dac 1 Volt
- Analog Injection
- Hitbus Readout
- ### Log
- ```

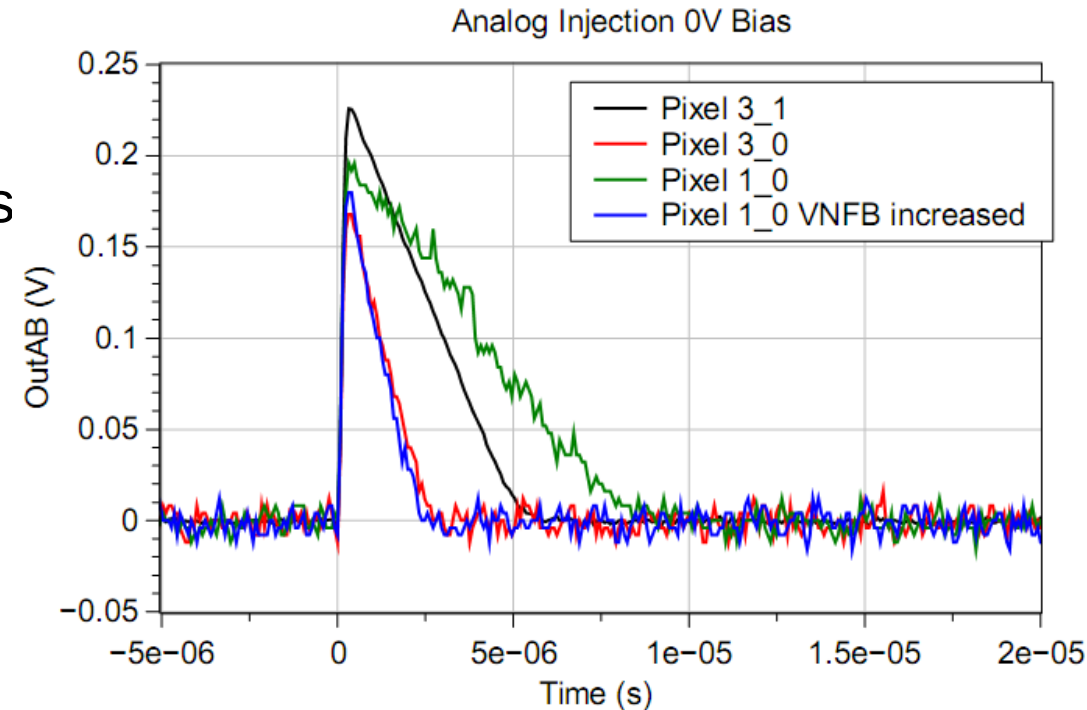
00000000000000000000
Config written into Chip and loaded.
The configured pattern is now: -----
AnaInjPattern:
00000000000000000000000000000000
10000000000000000000000000000000
Ld Pattern:
00000000000000000000000000000000
00000000000000000000000000000000
HBEEn Pattern:
11111111111111111111111111111111
01111111111111111111111111111111
DigInj Pattern:
00000000000000000000000000000000
00000000000000000000000000000000
AnaInjPattern:
00000000000000000000000000000000
10000000000000000000000000000000
Ld Pattern:
00000000000000000000000000000000
00000000000000000000000000000000
HBEEn Pattern:
11111111111111111111111111111111
01111111111111111111111111111111
DigInj Pattern:
00000000000000000000000000000000
00000000000000000000000000000000
Config written into Chip and loaded.
Set Amplitude to 1V

```

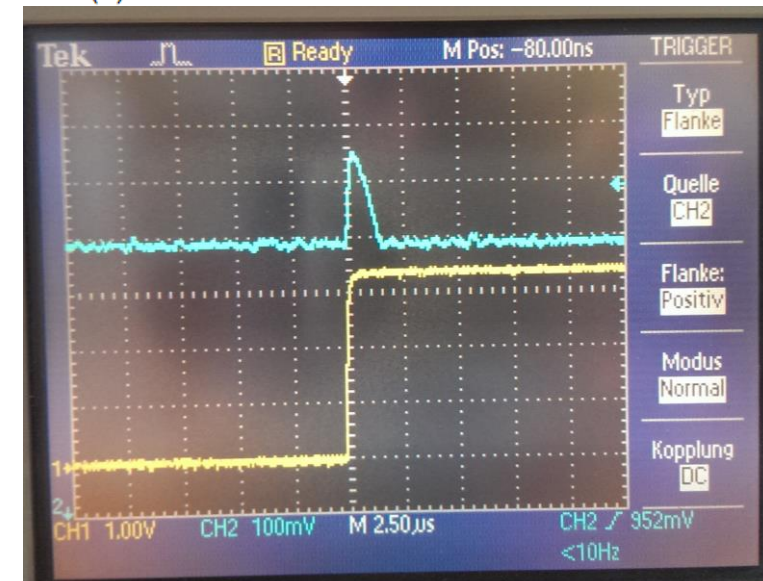


# Measurements

- Analog Injection into Pixels
- Output on OutAB

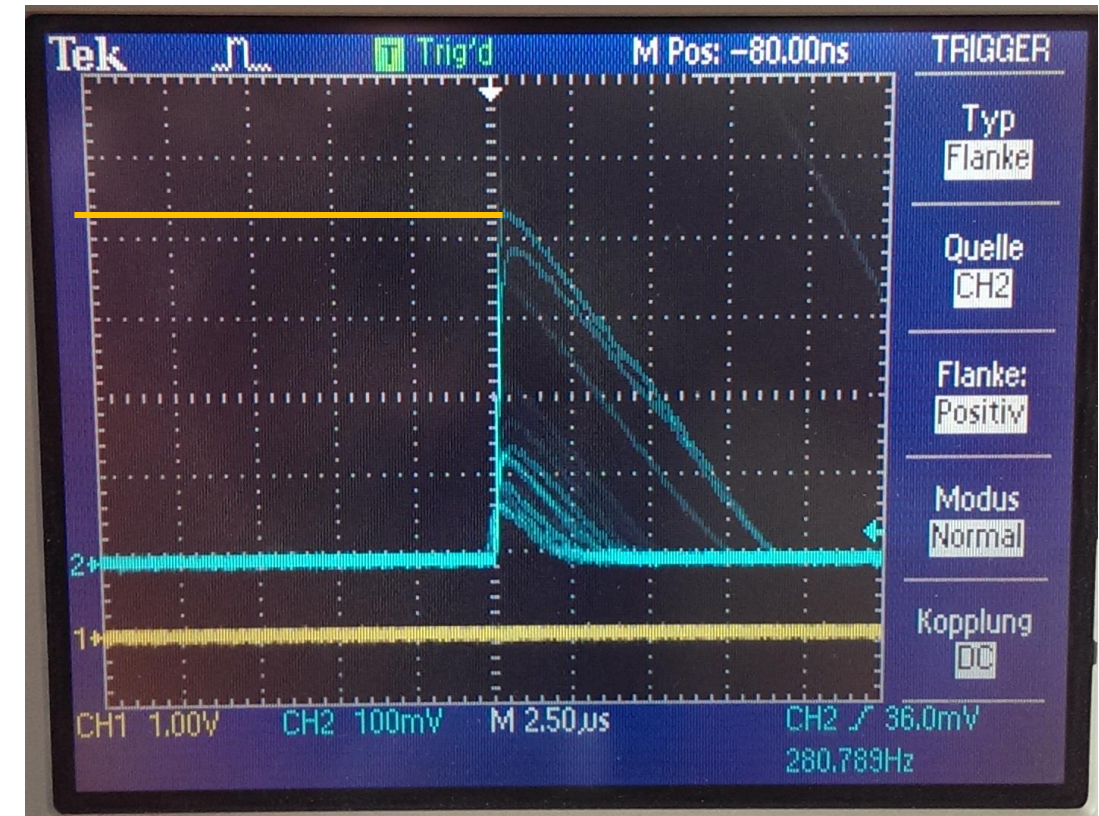
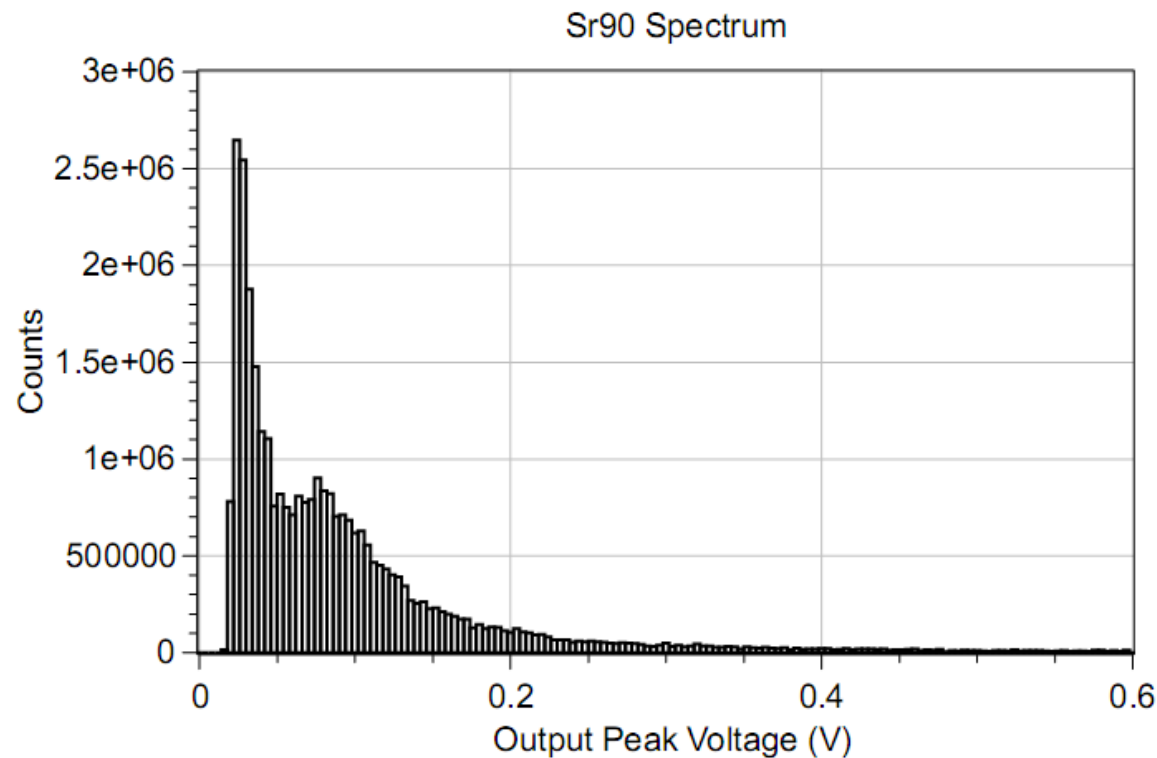


## Pattern



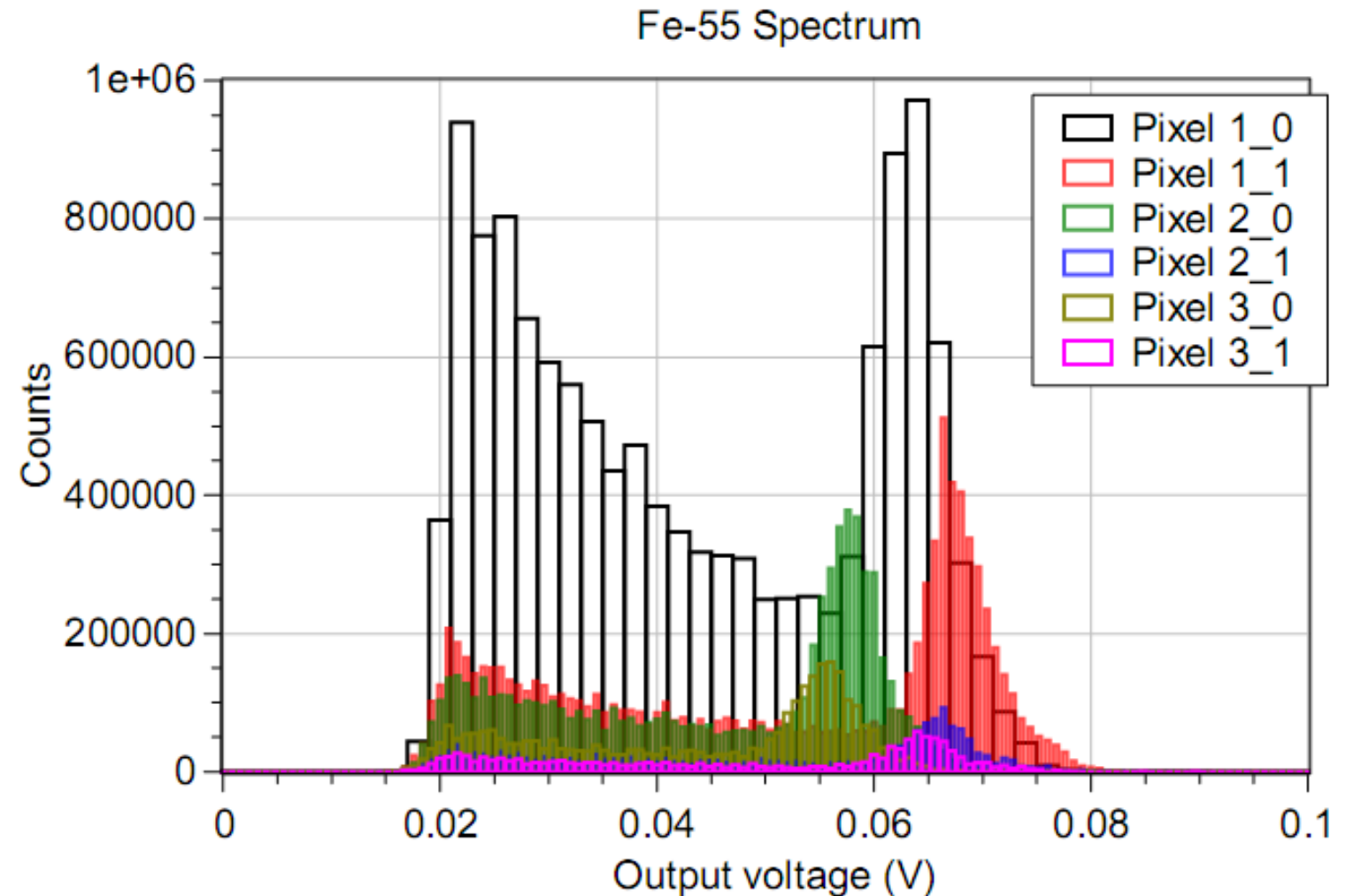
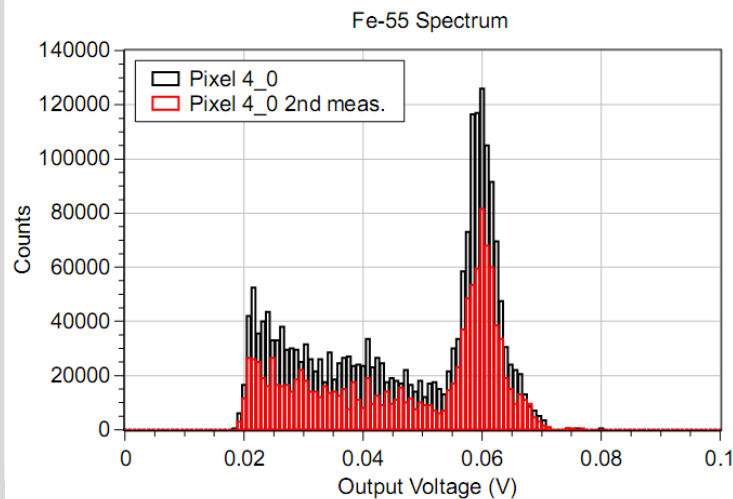
# Measurements

## ■ Test with SR-90 source (MBq)



# Measurements

- Calibration with Fe-55 source
- Bias: - 60V
- Activity: ~8MBq



# Plans

- Irradiation with X-Rays
  - X-Rays @ KIT: 60keV, 30mA, 10kGy/h
    - 60h for 600kGy (60MRad)
- Irradiation with 23MeV cyclotron protons
  - $1e15n_{eq}/cm^2$  reasonable. Preferences?
  - Also a lot of ionizing dose ( $\sim 1.5MGy$ )
- Digital readout of the chip
  - Few more steps in FPGA wiring and software configuration