DEPFET Pixel Technology

- basics and recent developments -

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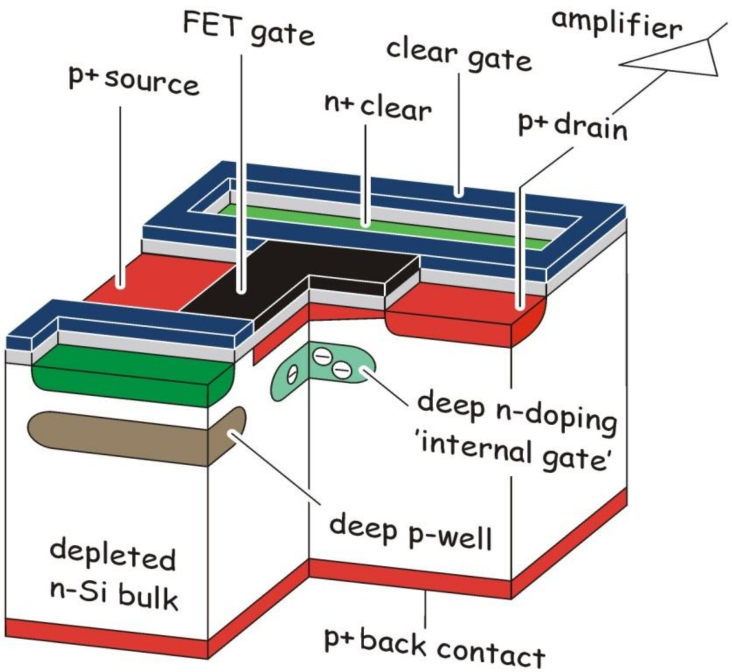
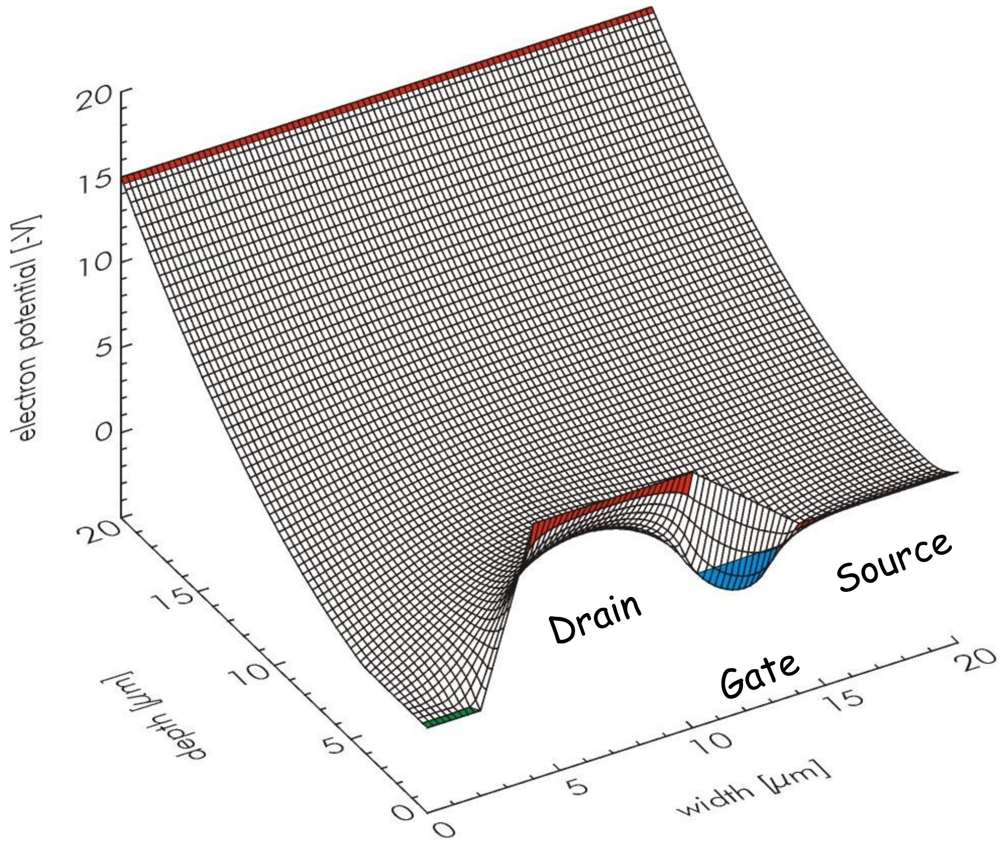
for the

DEPFET team at MPG HLL and the DEPFET Collaboration

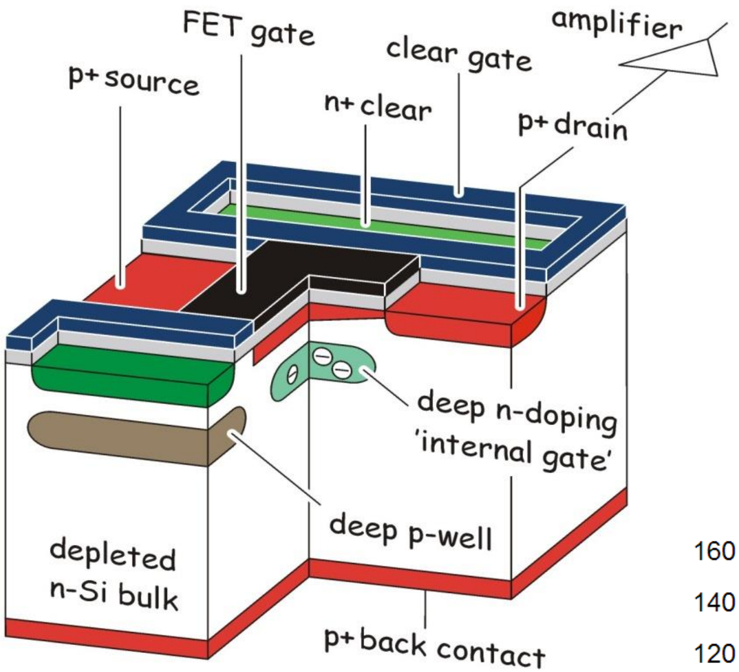
DEPFET Active Pixels

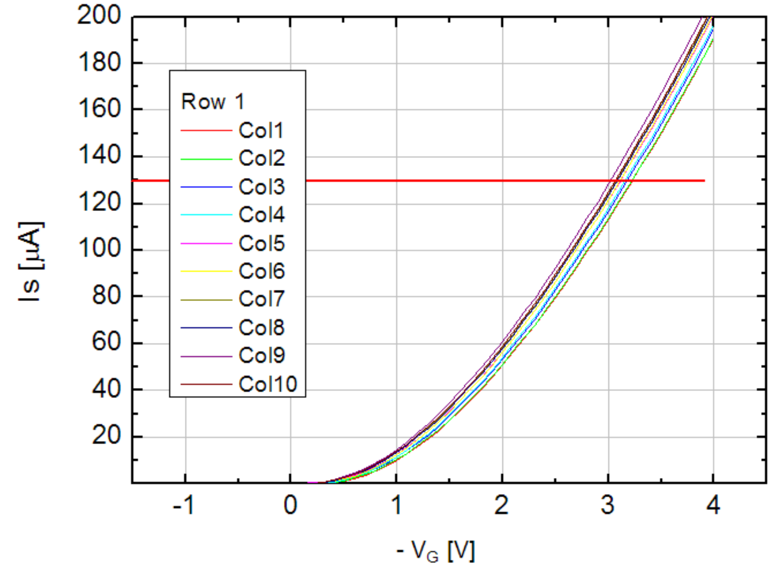


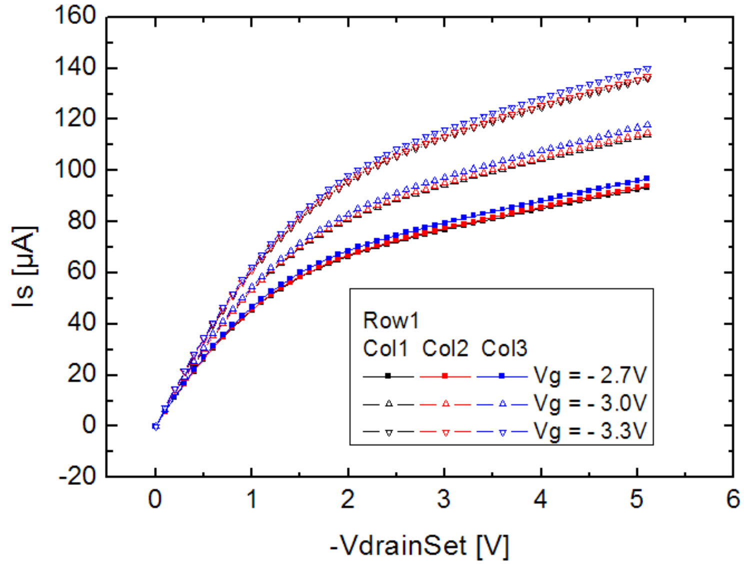


- fully depleted sensitive volume
- internal amplification
- Charge collection in "off" state, non-destructive read out on demand

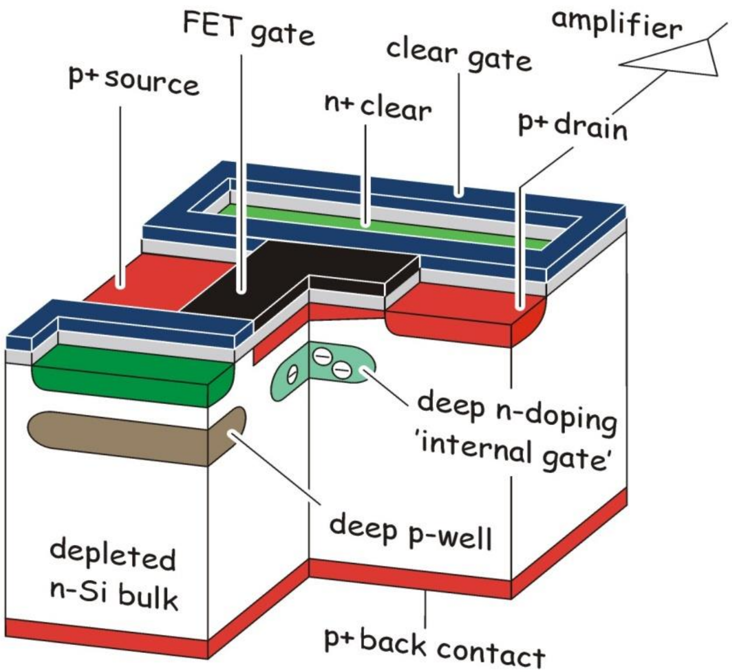
DEPFET Active Pixels

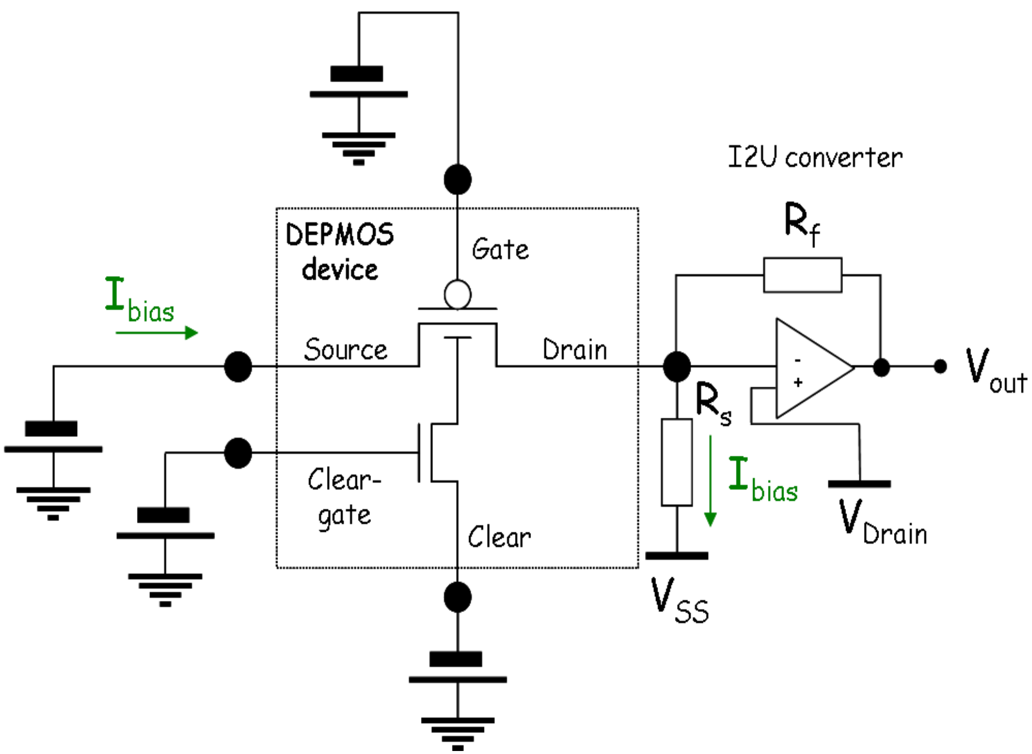




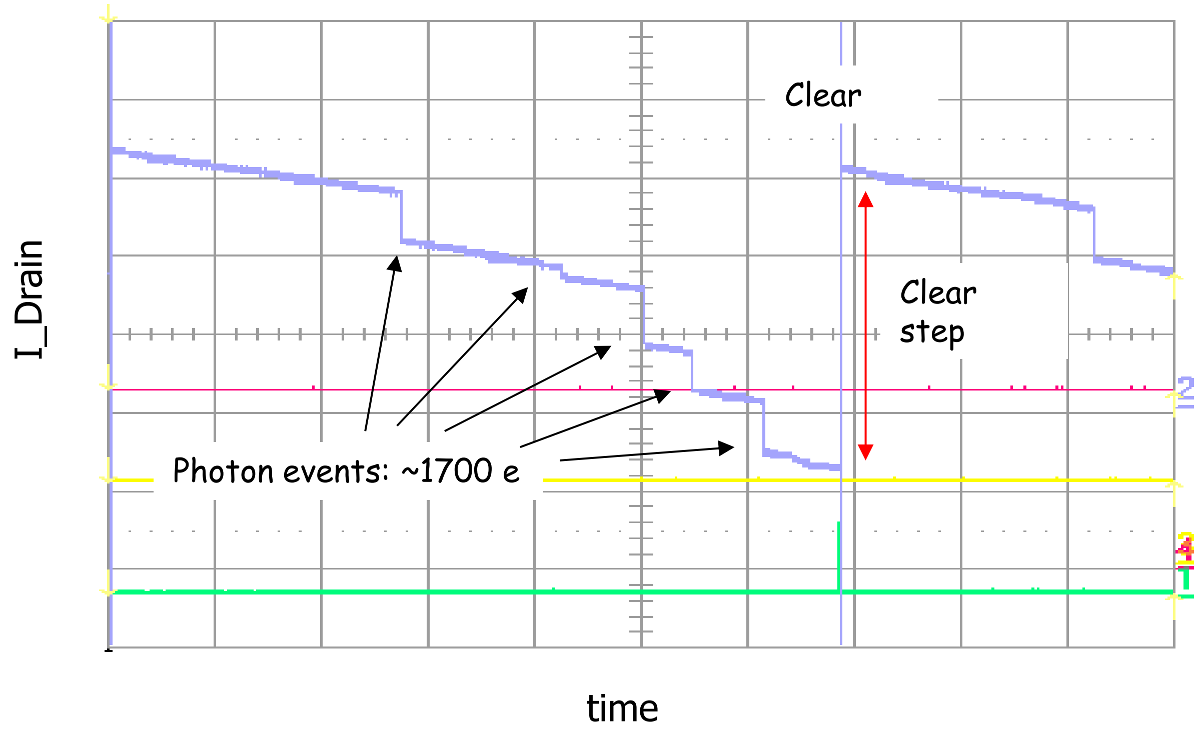


DEPFET Active Pixels





Internal Amplification

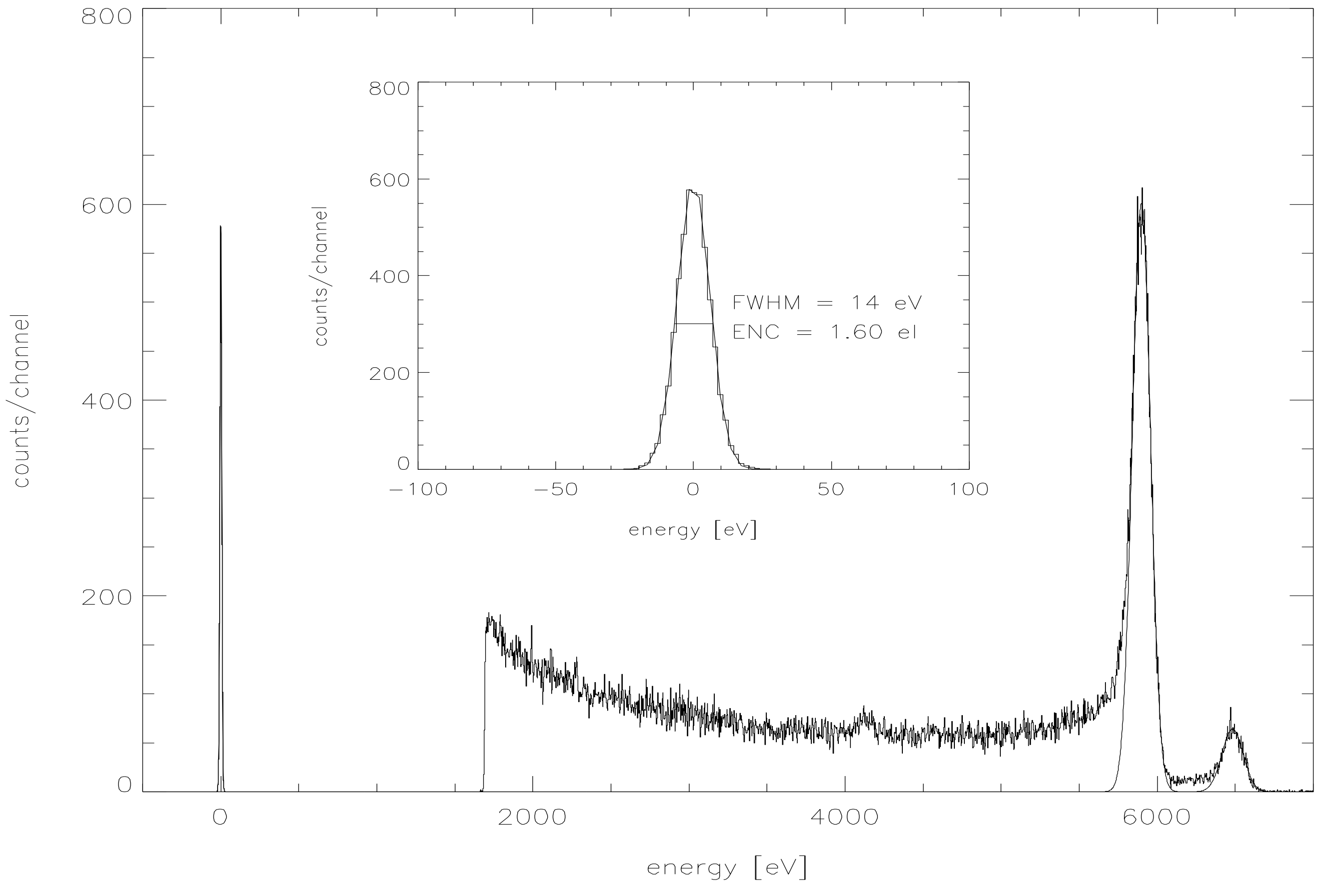


$$g_q = \frac{dI_D}{dQ} = \frac{g_m}{C_{ox}} \Rightarrow g_q \sim \frac{1}{L^{3/2}} \qquad g_q \sim I_D^{1/2} \qquad g_q \sim \frac{1}{W^{1/2}} \qquad g_q \sim t_{ox}^{1/2}$$

(Ideal transistor theory - neglecting short channel effects)

g_q for of the latest DEPFET generation (Belle II): ~0.5 nA/e

Single pixel performance – Fe55 Source

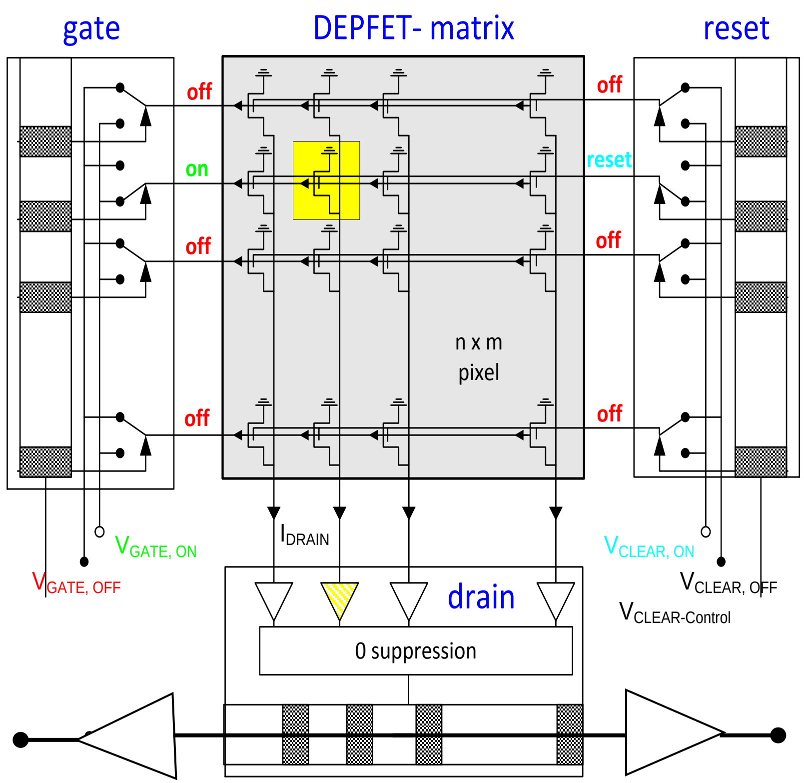


V_{thresh}≈-0.2V, V_{gate}=-2V
I_{drain}=41 μA
time cont. shaping τ=10 μs

Noise ENC=1.6 e^- (rms)

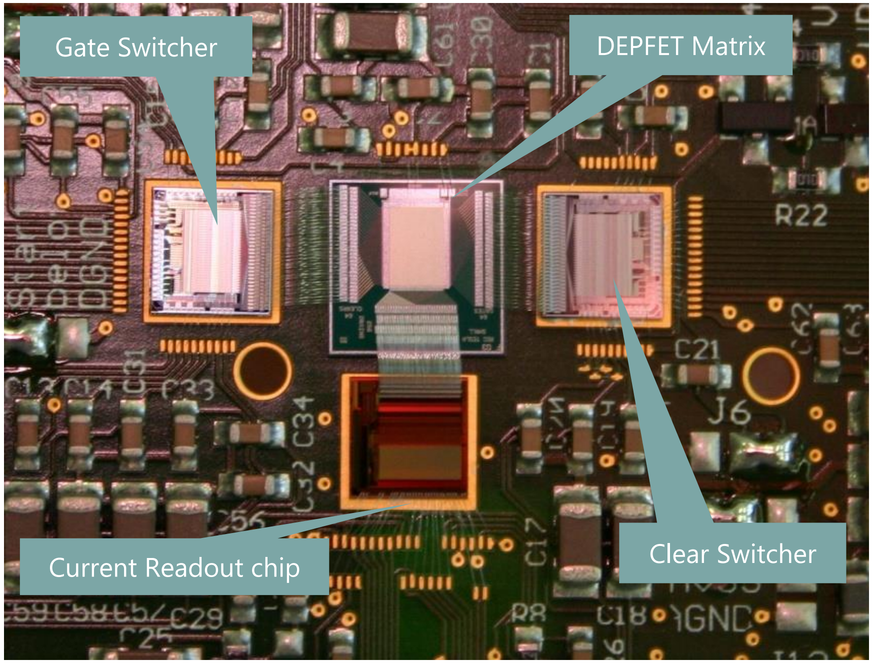
at T>23 degC

An array of DEPFETs

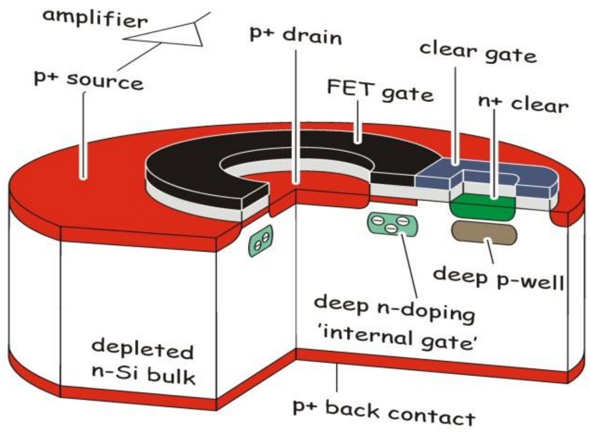


<u>Row wise read-out ("rolling shutter")</u>

- select row with external gate, read current, clear DEPFET, read current again
- two different auxiliary ASICs needed
- r/o needs time.....
- only one row active → low power consumption

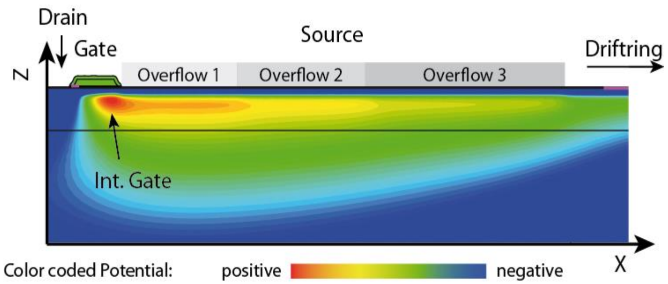


Main DEPFET Classes



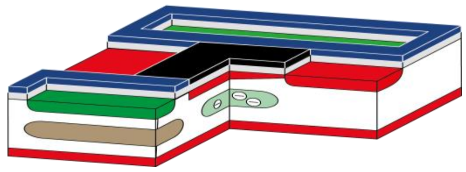
Low noise: Spectroscopic X-Ray imaging

- pixel size: 100µm, with SDD around 100s of µm
- r/o time per row: few µs
- Noise: ≈4 el ENC
- fully depleted, the thicker the better → large QE for higher E



High dynamic range, ultra-fast read-out: XFEL-DSSC

- DEPFET Sensor with Signal Compression
- pixel size: ~200 µm
- 1-to-1 bonded to r/o AISC
- frame rate in the MHz range



Thin & small & fast pixel: vertex, lowE electron detectors (TEM)

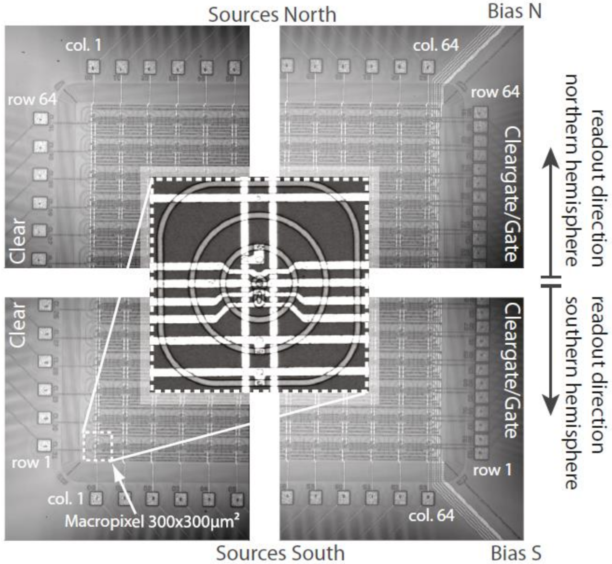
- pixel size: 20µm…75µm
- r/o time per row: 25ns-100ns
- Noise: ≈100 el ENC
- thin detectors: 50µm…75µm → still large signal: 40nA/µm for mip

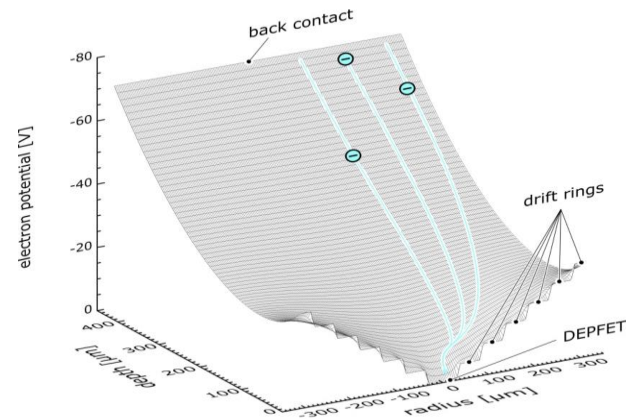
BepiColombo – MIXS instrument

:- ESA/Jaxa mission to Mercury, least explored planet in our system
:- start July 2016, eta Jan. 2024
:- 15 different instruments on board
:- MIXS: **M**ercury **I**maging **X**-ray **S**pectrometer
↳ … surface atomic composition of Mercury
↳ x-ray fluorescence map in high spatial resolution

Focal planes of MIXS:

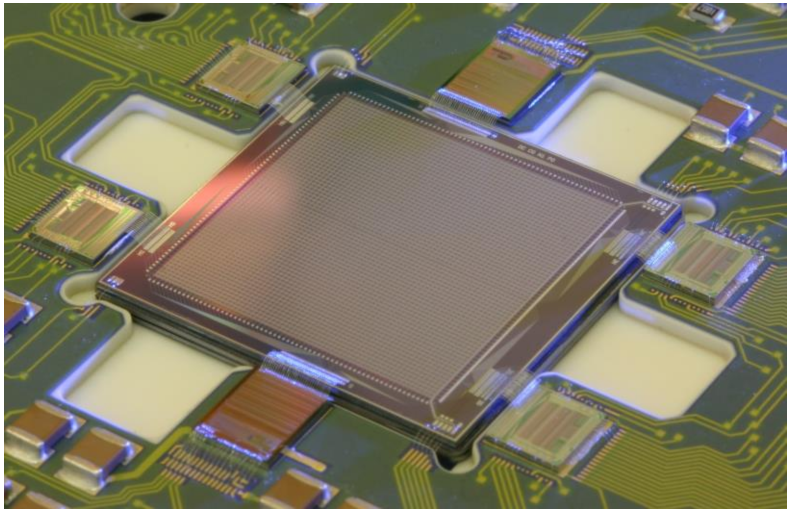
:- 2 DEPFET matrices format
↳ 1.92 x 1.92 cm^2
↳ 64 x 64 pixels
↳ 300 x 300 μm size
:- required energy resolution:
↳ 200 eV FWHM @ 1 keV
↳ QE > of 80 % @ 500 eV
:- read-out time dominated by rad. damage
↳ < 200 μs
:- Radiation tolerance
↳ ~ 20 krad TID
↳ 3 x 10^{10} 10 MeV p/cm^2 → **1.11 x 10^{11} 1 MeV n_{eq}/cm^2**



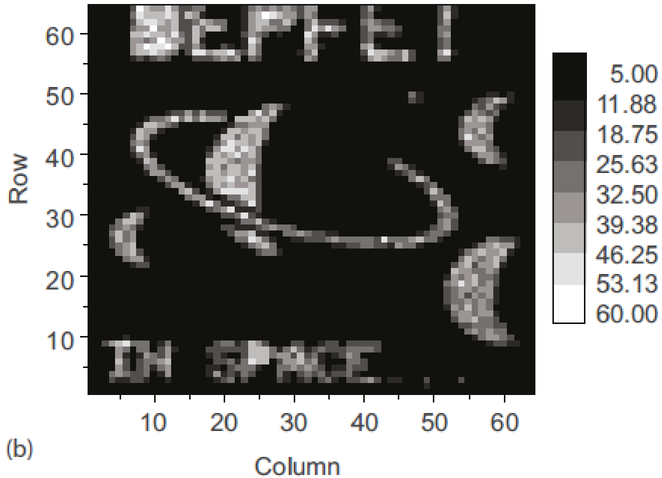


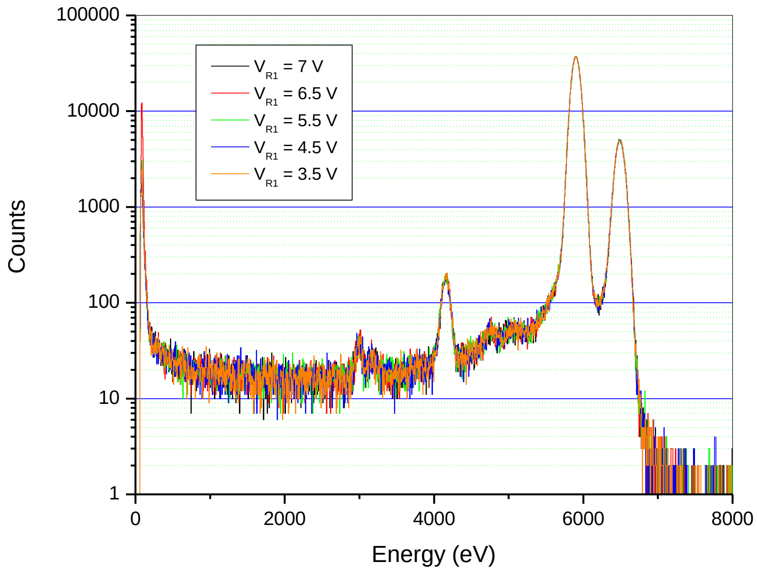
:- Status: focal plane finished, cameras being assembled and tested

Performance – Fe55



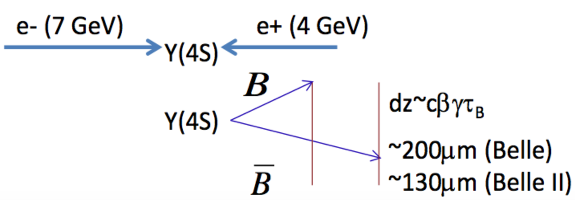
- ▷ **Operating conditions**
  - ↳ -40 °C
  - ↳ T_{row} = 5.2 µs
  - ↳ T_{frame} = 167 µs / frame
  - ↳ Framerate ~ 6 kfps
  - ↳ I_{pixel} = 125 µA
- ▷ **Noise: 4.3 e- rms**

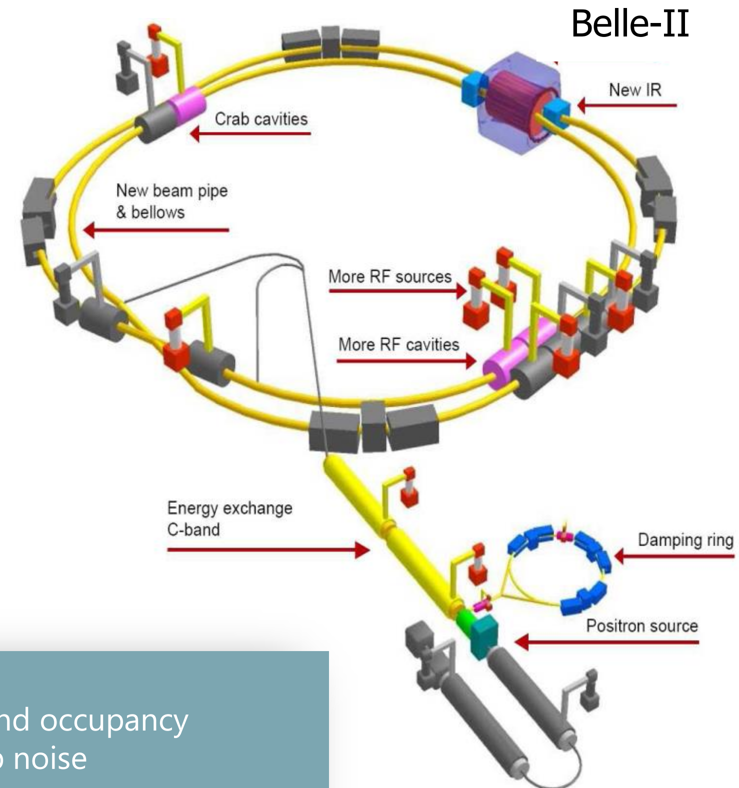




SuperKEKB and Belle II

Machine parameter	HER (KEKB)	LER (KEKB)	HER (SuperKEKB)	LER (SuperKEKB)
Vertical beam size	0.94μm	0.94μm	59nm	59nm
Beam current(mA)	1188	1637	2600	3600
luminosity($cm^{-2}s^{-1}$)	$2.1x10^{34}$		$8x10^{35}$	



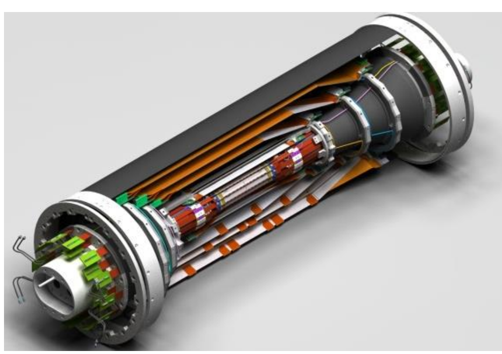


Smaller beam size & more current:

→ 40x higher luminosity, goal: $8x10^{35}$ $cm^{-2}s^{-1}$
→ probe New Physics at "intensity frontier"

→ 20x-40x higher background
- ↳ Radiation damage and occupancy
- ↳ Fake hits and pile-up noise

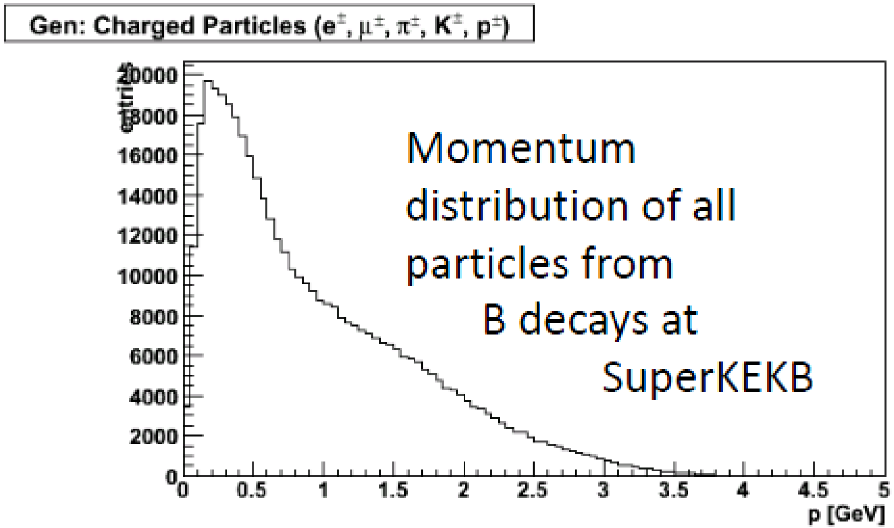
→ 10x higher event rate

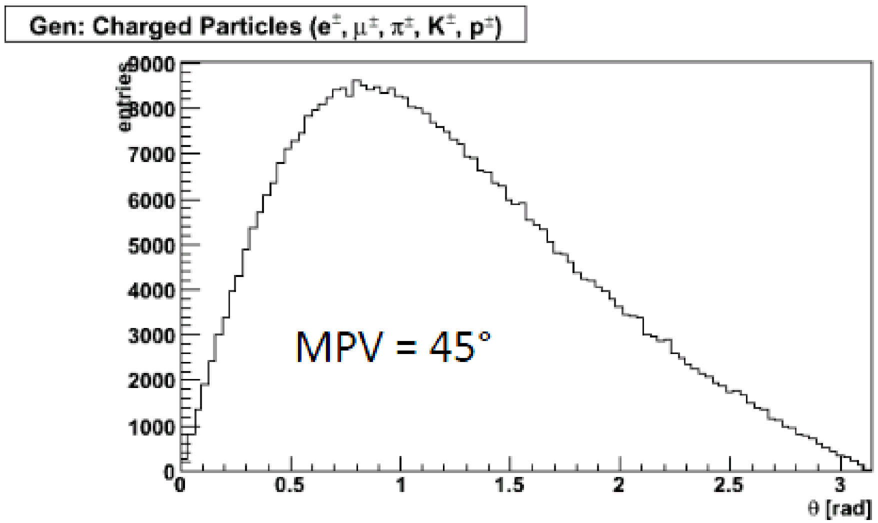


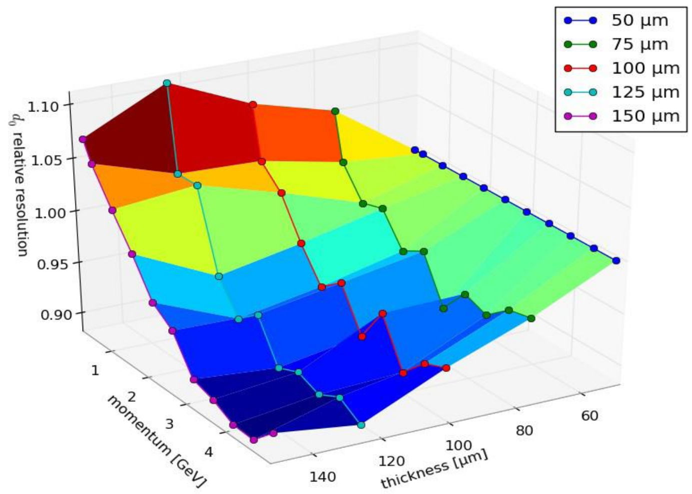
→ Detector upgrade
- ↳ Replace inner layers of the vertex detector with a pixel detector, upgrade outer layers
- ↳ …

Towards a pixel vertex detector for Belle II

Physics driven requirements



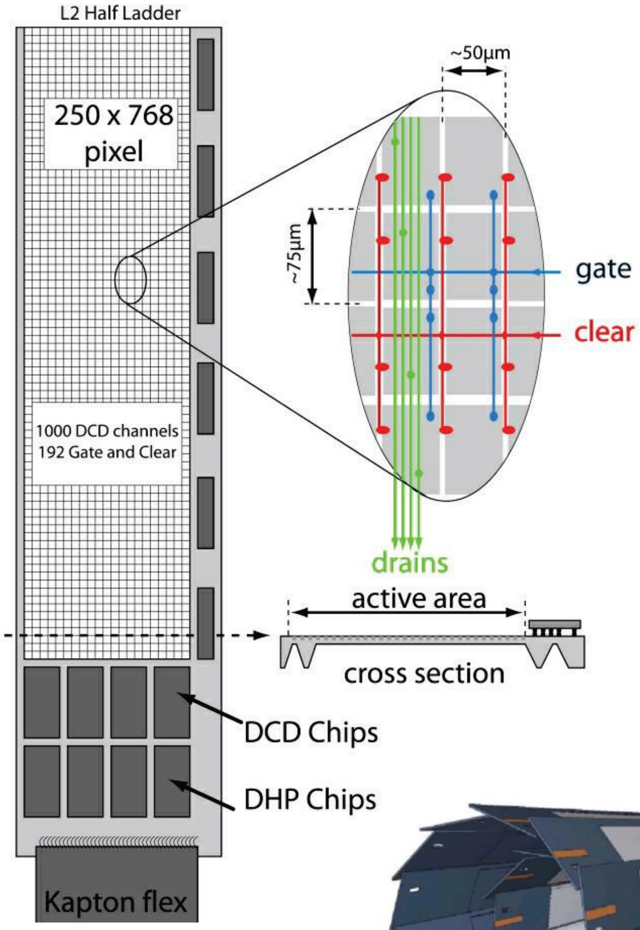




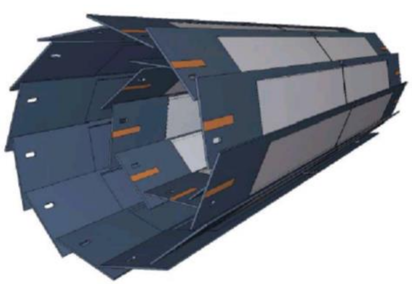
Find best technically feasible compromise:

:- for central und forward region
:- signal/noise of the sensors
:- # of r/o channels
:- occupancy
:- single point and **impact parameter res.**

The Result – Belle II PXD

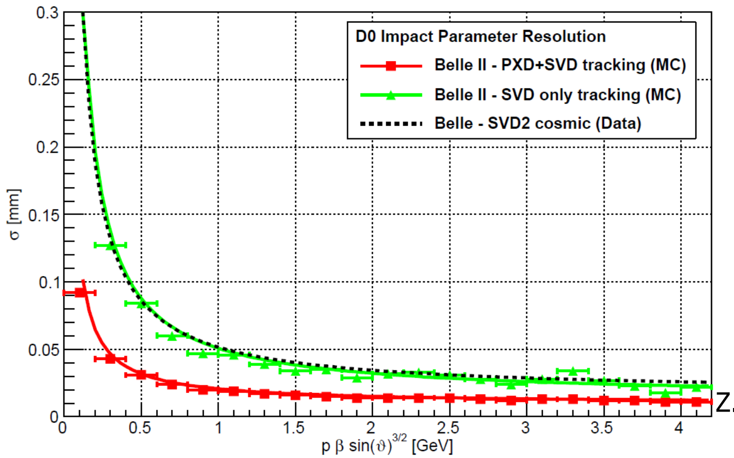


	L1	L2
# modules	8	12
Distance from IP (cm)	1.4	2.2
Thickness (µm)	75	75
#pixels/module	768x250	768x250
#of address and r/o lines	192x1000	192x1000
Total no. of pixels	3.072×10^6	4.608×10^6
Pixel size (µm²)	55x50 60x50	70x50 85x50
Frame/row rate	50kHz/10MHz	50kHz/10MHz
Sensitive Area (mm²)	44.8x12.5	61.44x12.5



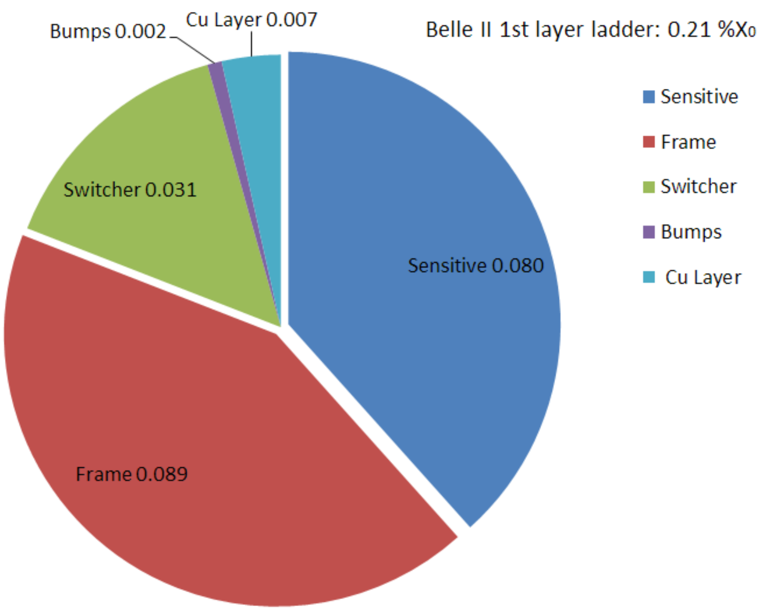
Angular coverage 17°<θ < 155°

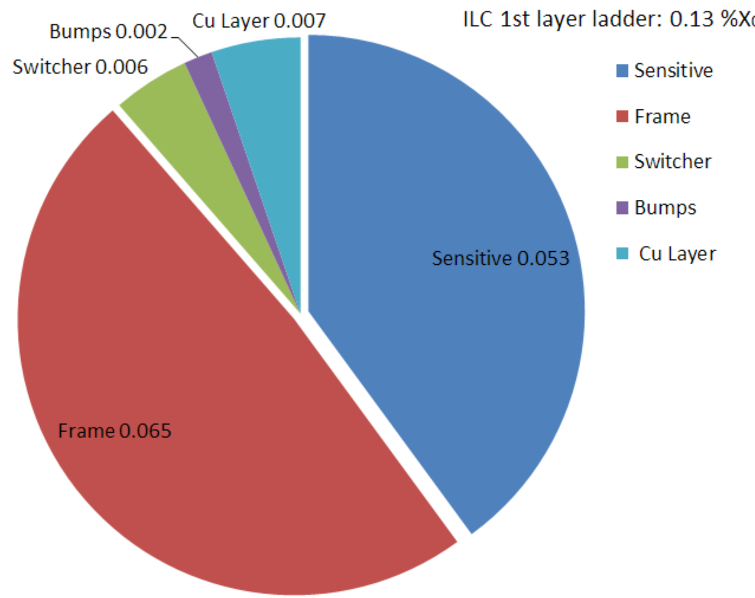
vertex resolution significantly improved



Z. Drasal

Reducing material in the barrel region





	Belle II	ILC
Frame thickness	525 µm	400µm
Sensitive layer	75 µm	50µm
Switcher thickness	500µm	75µm
Cu layer	only on periphery	only on periphery
Total	0.21 %X0	0.13 %X0

→ less material with small modifications/improvements of module technology within reach

DEPFET all-silicon module

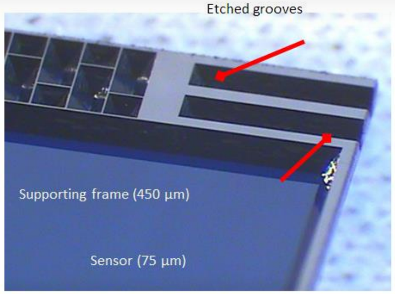
DCDB (Drain Current Digitizer)
Analog front-end

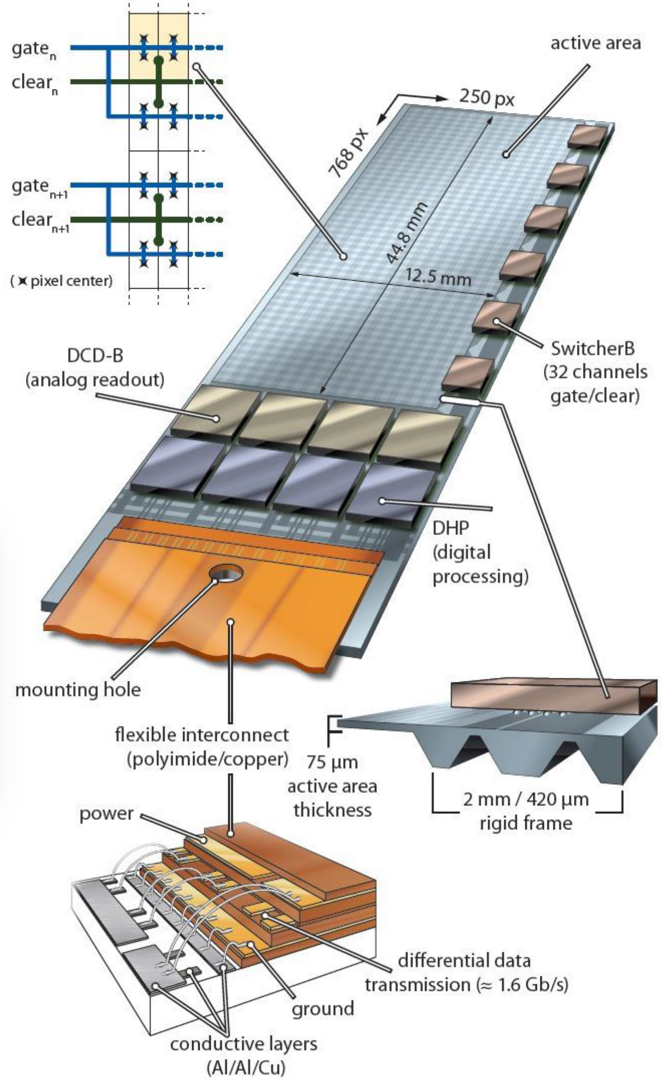
Amplification and digitization of DEPFET signals.

- 256 input channels
- 8-bit ADC per channel
- 92 ns sampling time
- new version w/ 50ns sampling time under test
- UMC 180 nm

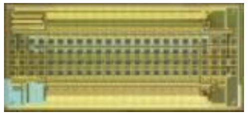
Key to low mass vertex detectors

→ **highest integration!**
↳ Thin sensor area
↳ EOS for r/o ASICs
↳ Thin (perforated) frame w/ steering ASICs



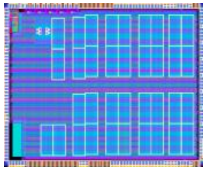


SwitcherB - Row Control



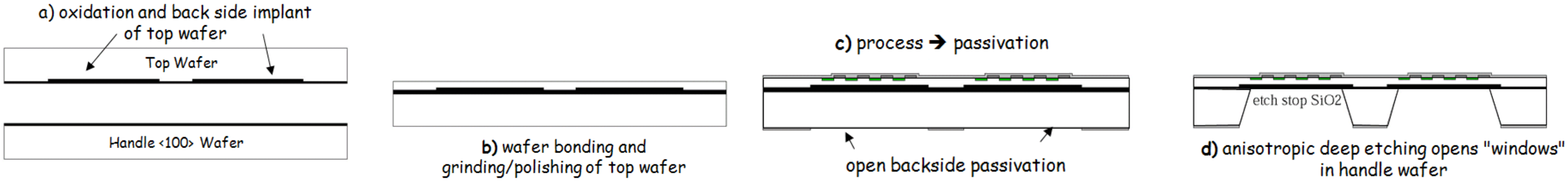
AMS/IBM HVCMOS 180 nm
- Size 3.6 × 1.5 mm^2
- Gate and Clear signal
- 32x2 channels
- Fast HV ramp for Clear

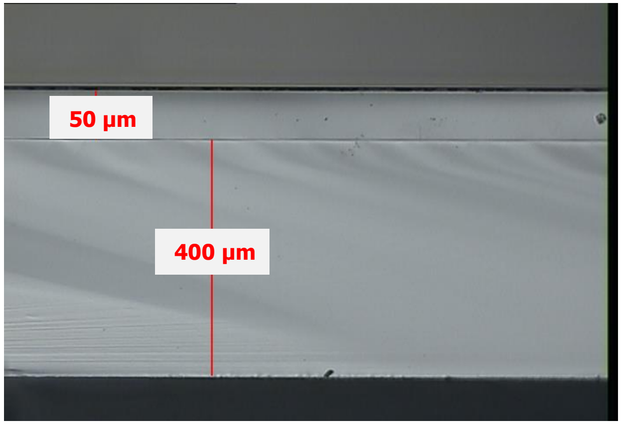
DHP (Data Handling Processor)
First data compression



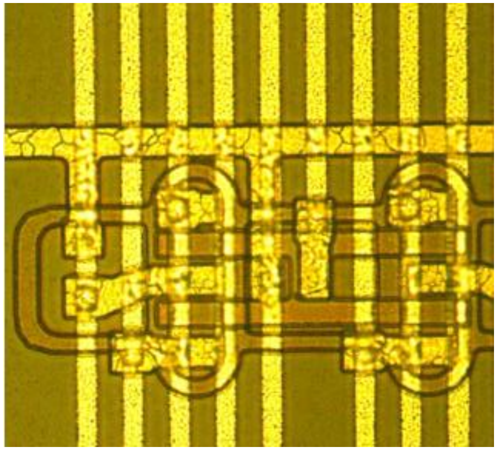
IBM CMOS 90 nm (TSMC 65 nm)
- Size 4.0 × 3.2 mm^2
- Stores raw data and pedestals
- CM and pedestal correction
- Data reduction (zero suppression)
- Timing and trigger control
- Drives data link

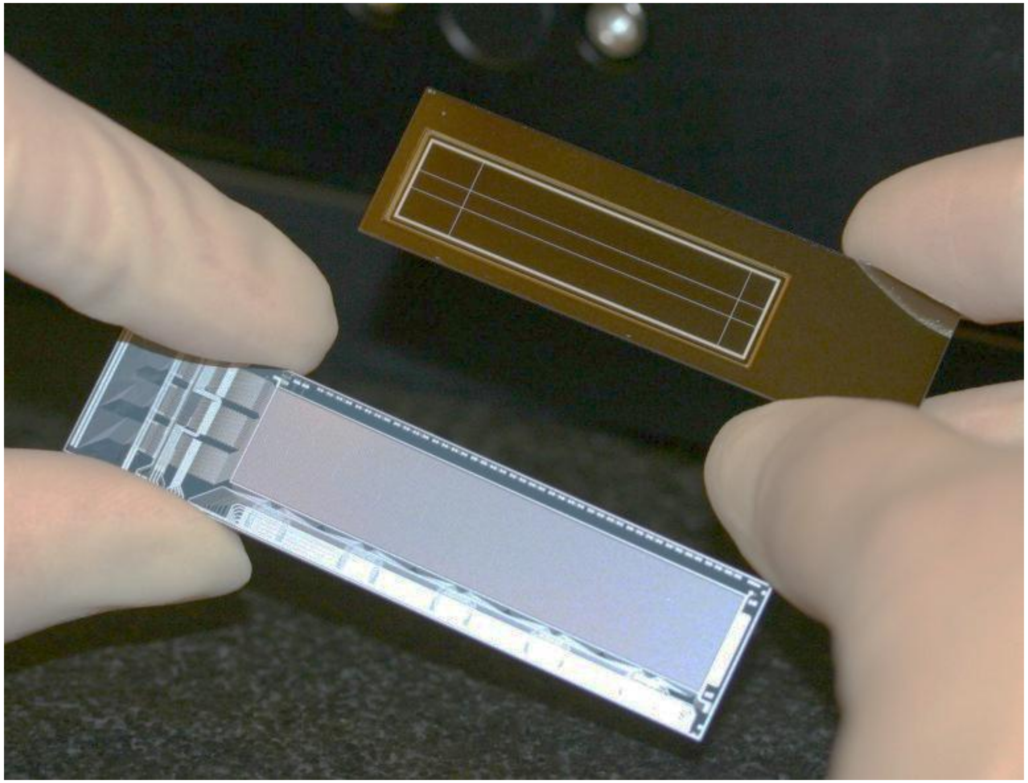
DEPFET Prototype Fabrication and “Thinning” – PXD6



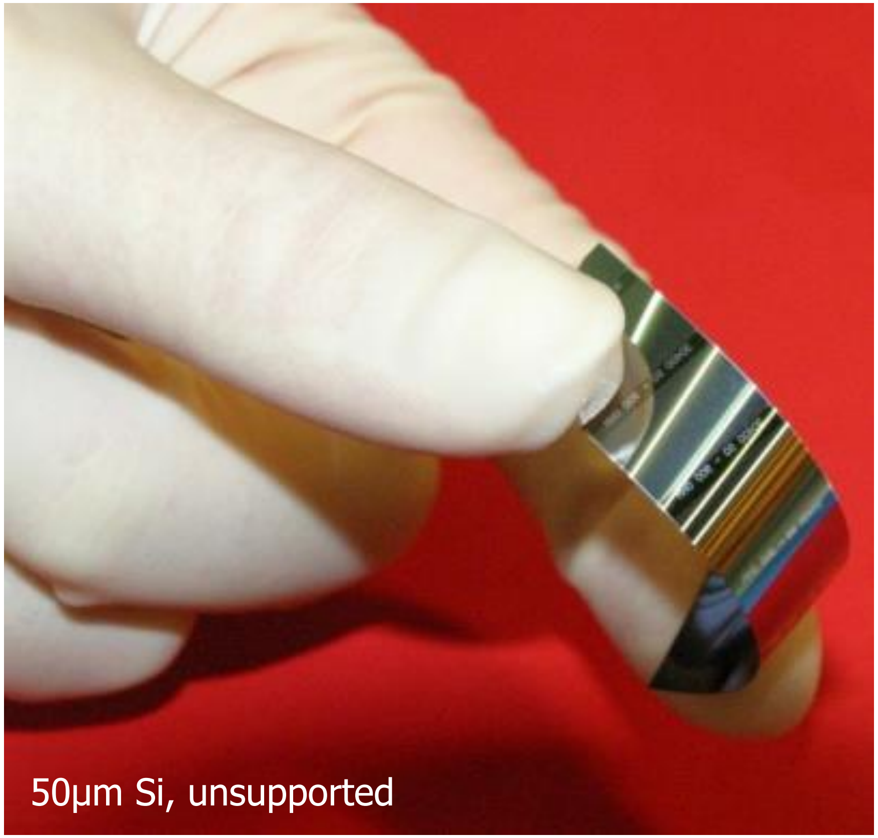


Top side of prototype run





All-Silicon Module


50µm Si, unsupported

- Half-ladders (modules) are laser-cut
- Modules are supported by a monolithic silicon frame
- Two inner (outer) modules are assembled to inner (outer) ladders


50µm Si in Silicon frame

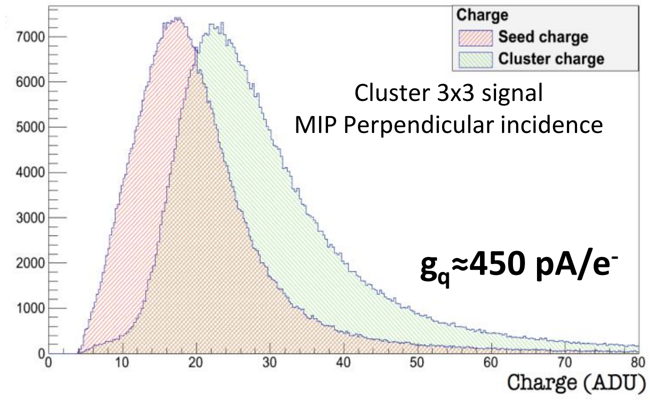
Sensor and r/o electronics: Beam tests with the full system

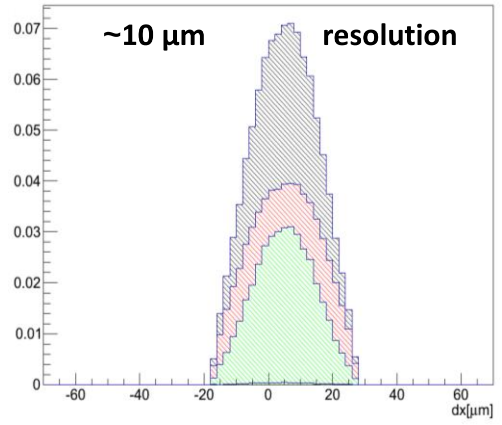
PXD6 Belle II design

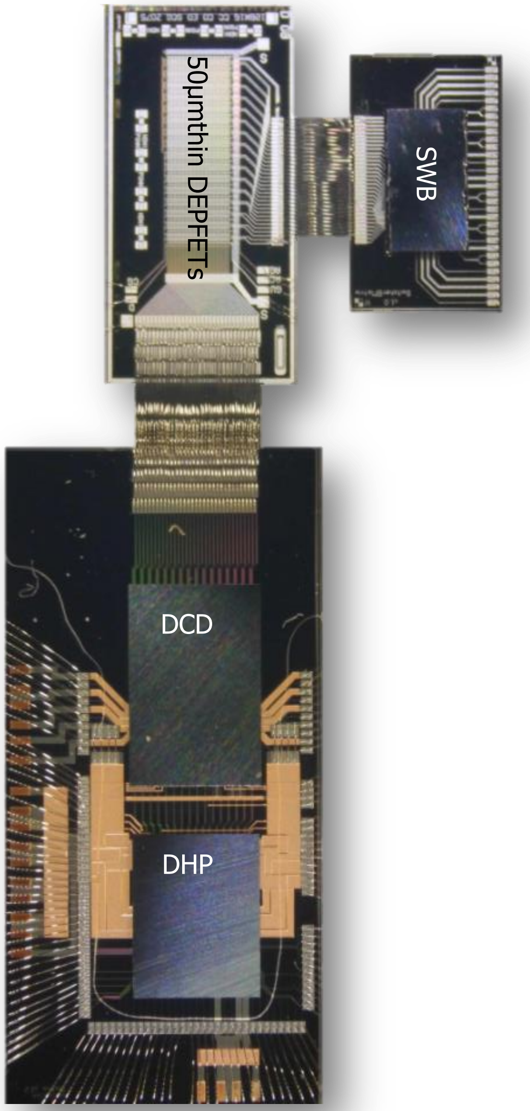
- Thin (**50** µm) sensor 32x64 pixels
- Pitch 50x75 µm^2

- SwitcherB and DCDB at full speed
- Belle II prototype power supply
- DCDB readout at 320 MHz → **100 ns row time**

- 99% Efficiency
- S/N for MIPs: 20-40 depending on gate length







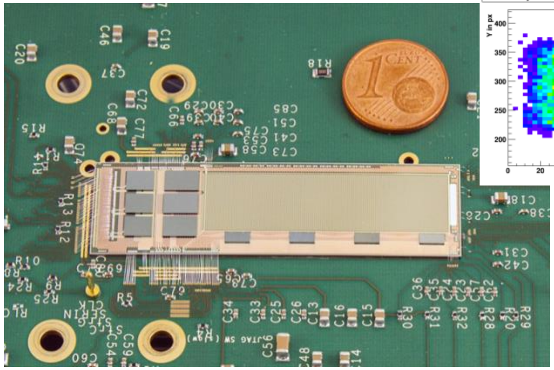
Towards a real ladder

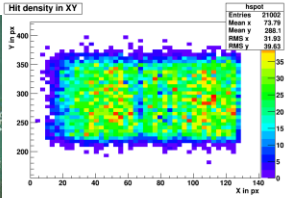
Transition from test systems to integrated modules

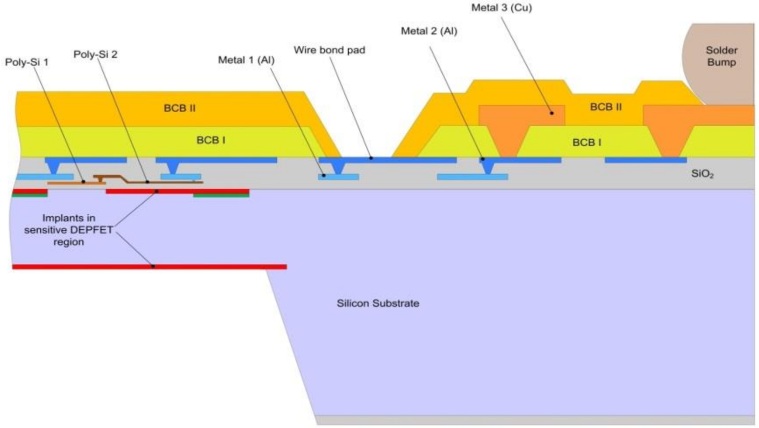
» PCB for the various matrices ….. "hybrids"

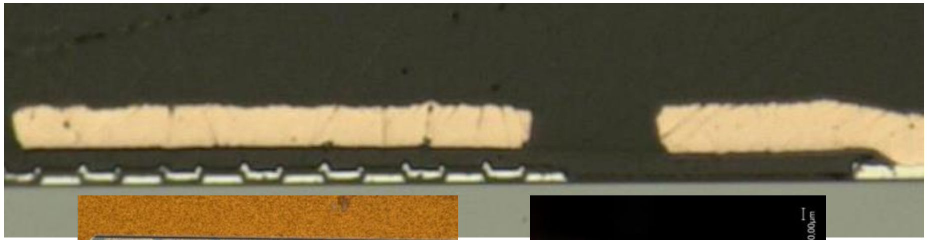
» first bump bonded chip on PXD6 prototype matrices
- ↳ 2 metal layers, not the final geometry, simple 3rd metal
- ↳ need still support PCB for I/O
- ↳ not perforated balcony

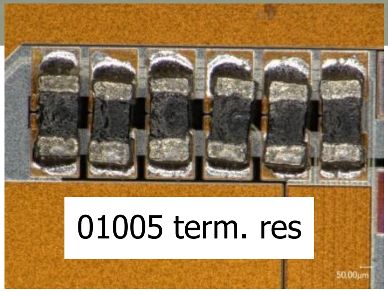
» Belle-II PXD Module (two modules form a ladder)
- ↳ **three metal layers, Cu as LM only on periphery**
- ↳ MCM: 4 DCD, 4 DHP, 6 Switchers → ~3000 bonds/module
- ↳ **Cu as UBM, bumps partly on thinned perforated frame**
- ↳ passive components soldered to substrate
- ↳ I/O and power over Kapton cable

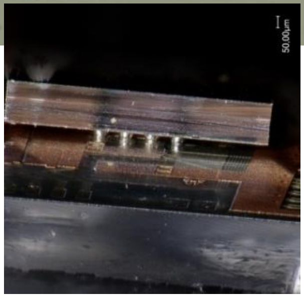




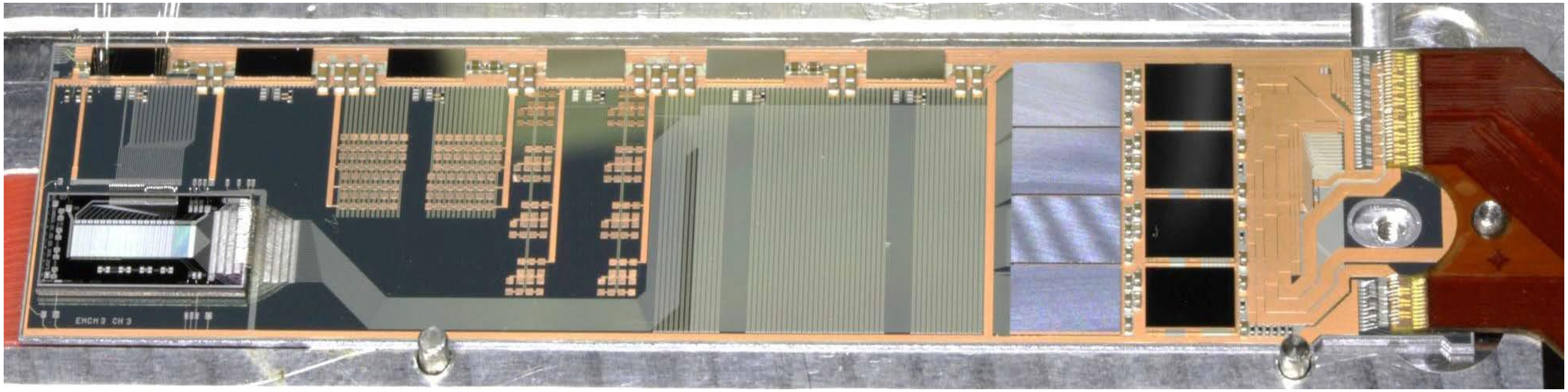


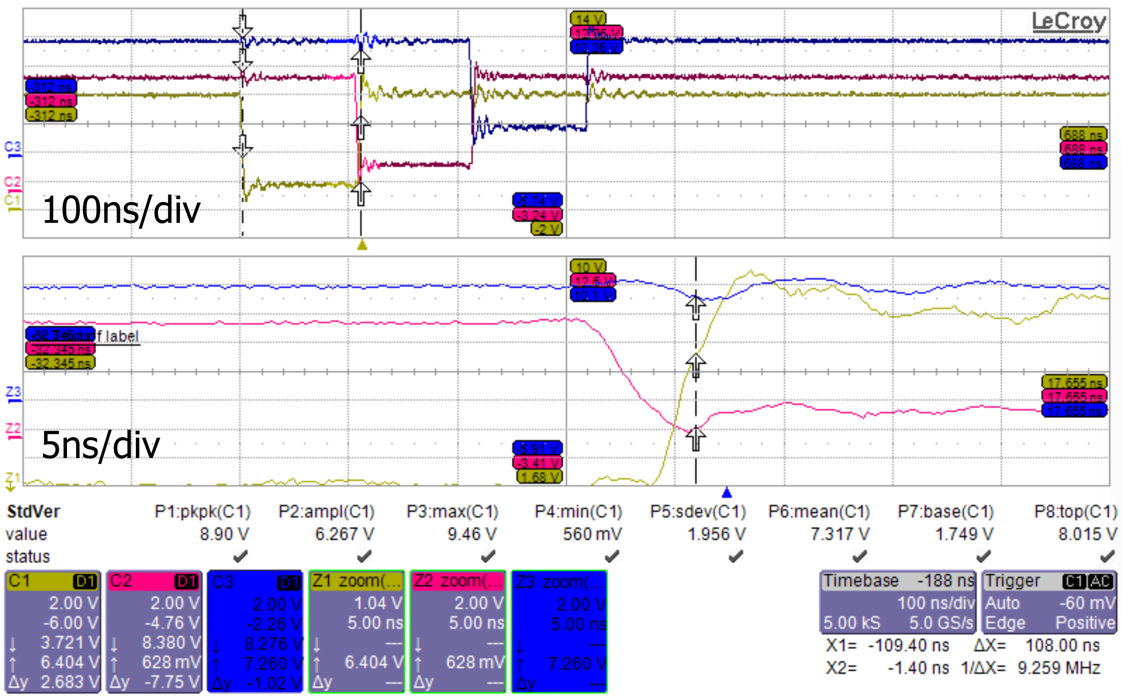






Test vehicle E-MCM





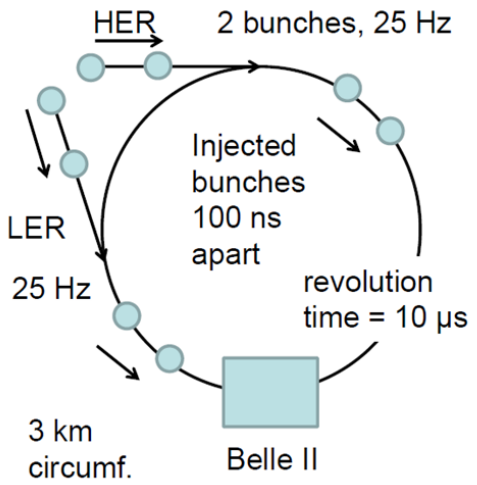
Extensive test program

- Interconnect technology
- Powering, control, DAQ
- Signal integrity, timing …
- …

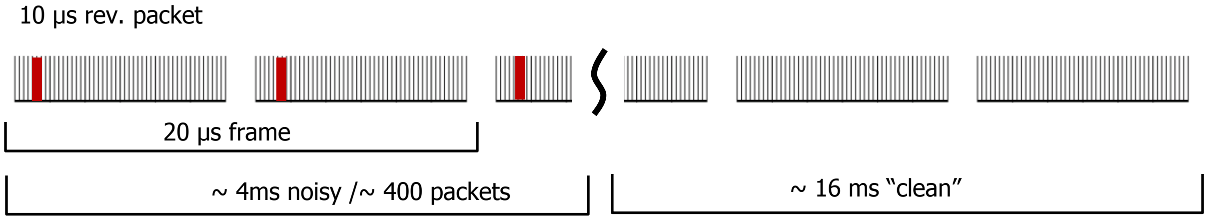
Lessons learned applied to final module layout

→ PXD pilot production launched!

The SuperKEKB injection noise issue



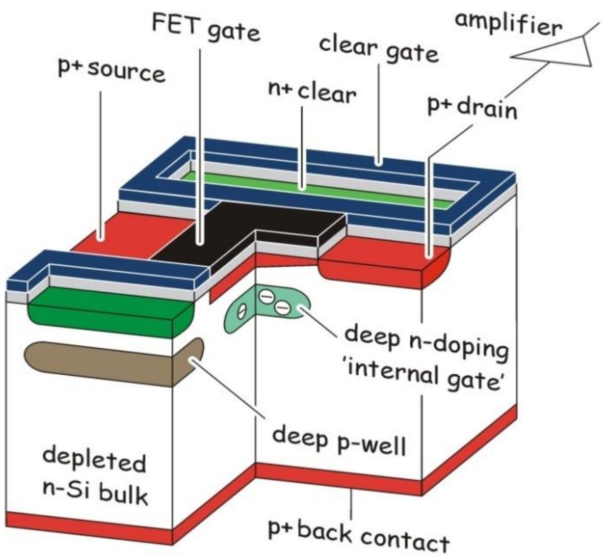
10µs packets with 2503 bunches , 200 ns gap in-between (TDR)



- » continuous injection → ~ 400 revolutions with two noisy bunches (100ns apart) every 20 ms
- » DEPFET integrates two trains, these noisy bunches would blank the frames → 20% loss of data

- » the best solution: gate the DEPFET during the passage of the noisy bunches
- » 100ns gate, with some rise and fall times, twice per frame … is this possible?

Blinding the DEPFET



normal operation

- charge collection mode
  - *ext. gate* off (positive), *clear* in off state (close to Ø)
  - generated e- drift into internal gate (most positive potential)
  - clear is shielded by depleted deep p-well (negative space charge)

- read mode
  - *ext. gate* on (negative), *clear* off
  - sensor is still sensitive

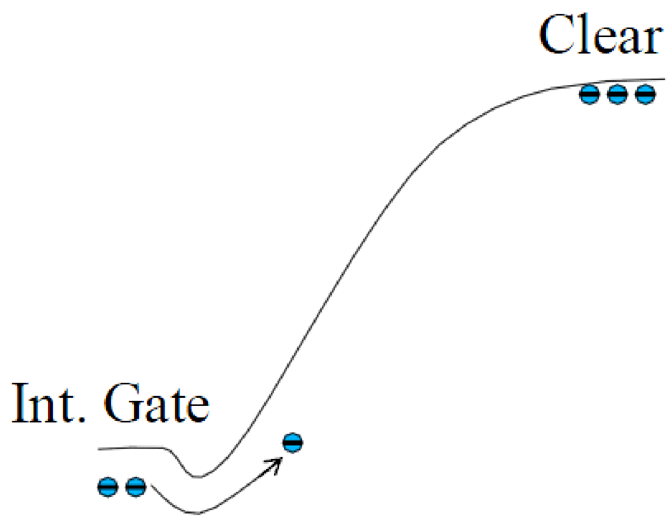
- clear mode
  - *ext. gate* on (negative), *clear* on (positive 15..20V)
  - internal gate drained to *clear*, as well as all charges coming from bulk

→ clear mode is basically already the blind mode, bulk generated charge drifts directly into clear

→ how "blind" is this mode, how much charge goes into the internal gate, if *clear* is positive?

→ how can signal charge stored in the internal gate be preserved during blind mode?

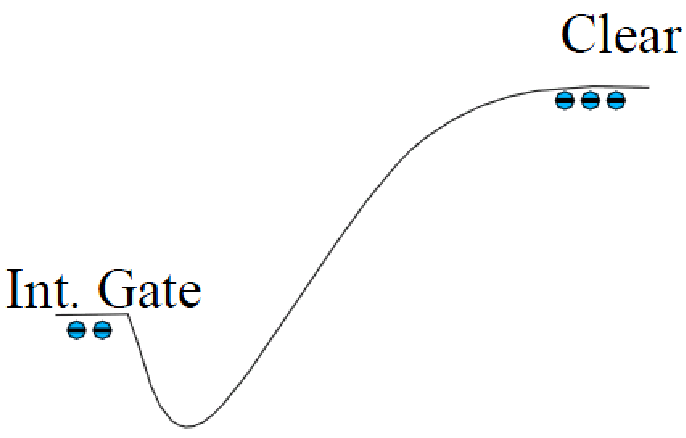
Incomplete Clear (this time on purpose!!)



normal clear

» implantations and ext. voltages carefully adjusted

» signal charge overcomes by thermionic emission a well defined potential barrier and drifts to clear



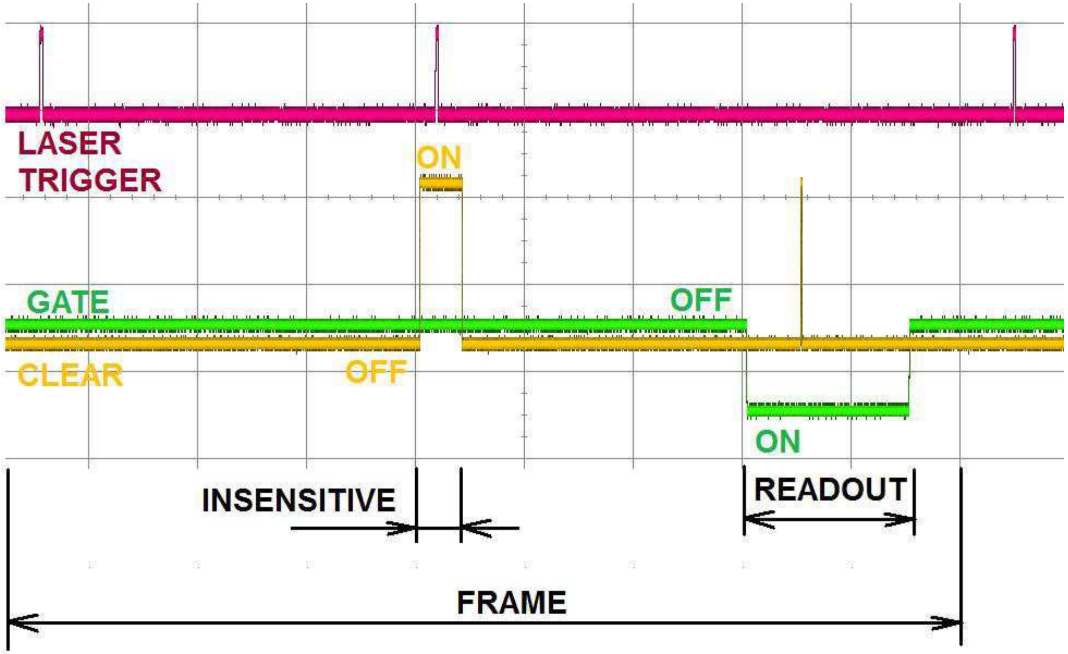
suppressed clear

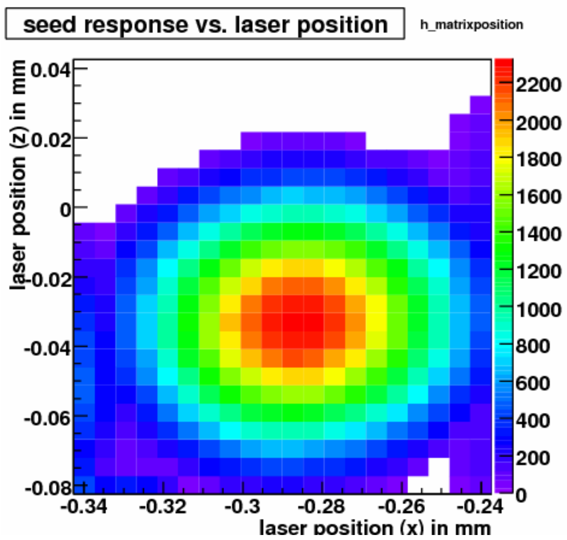
» positive voltage on ext. gate (more off)
   » cap. coupling of int. gate, also more positive

» potential barrier for signal charge to high
   » even for high clear voltages, no clearing possible

→ applying the clear pulse and keeping the DEPFET in off state conserves the charge in the int. gate
→ clear is positive: new charge drifts directly to clear

experimental confirmation

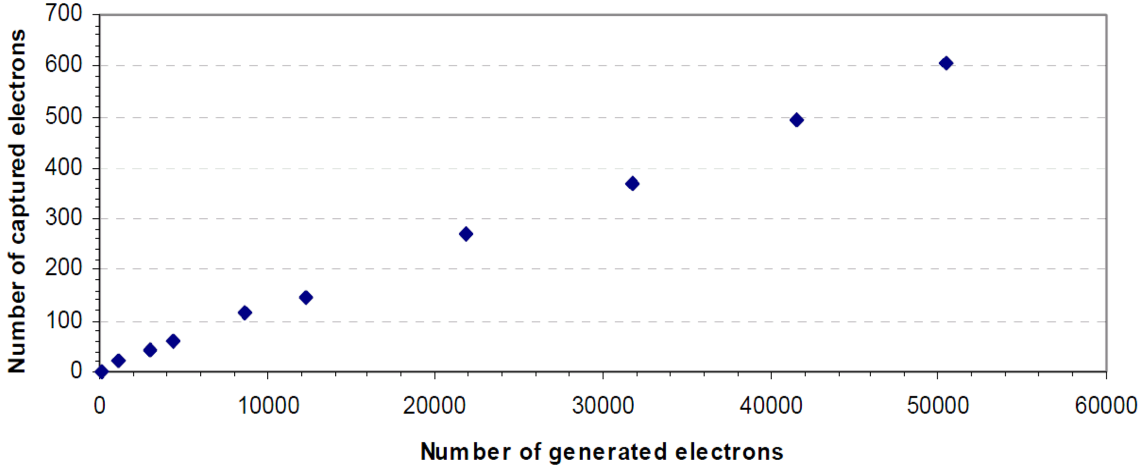




experiment:

- PXD6 matrix, 450 µm thick, installed in mini-matrix test setup
- irradiation from the back, Laser 660 nm
- laser spot in the center of the pixel → worst case scenario for blind mode

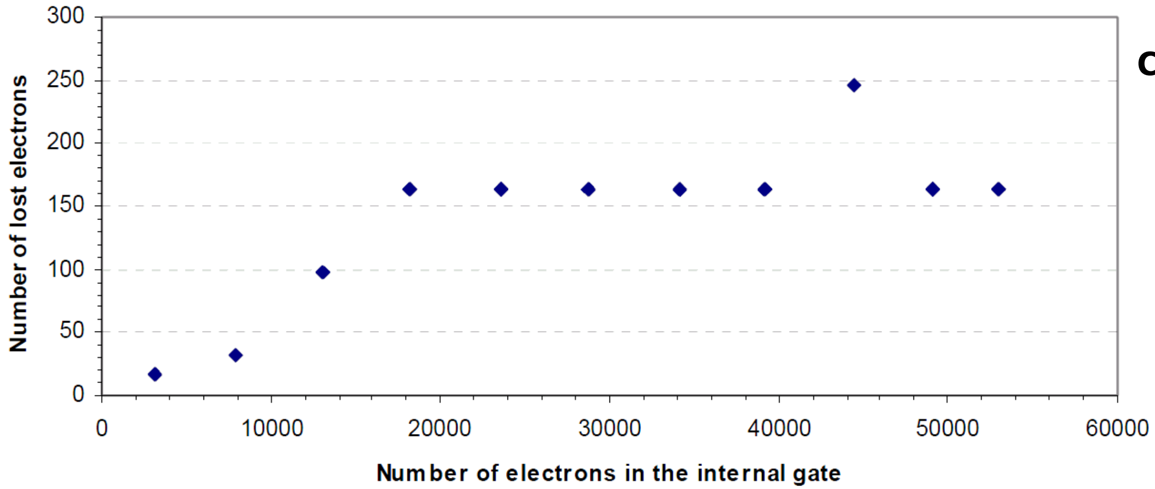
results



Charge generation in blind mode

Vgate=6V, Vclear=20.4V

~ 1% of generated charge make it into the internal gate



Charge preservation during blind mode

Vgate=6V, Vclear=20.4V

the loss of charge is <200e-

for small signal charges (~10000e-,)
the loss of signal charge is on noise level

Jan Scheirich, Prague

In Summary

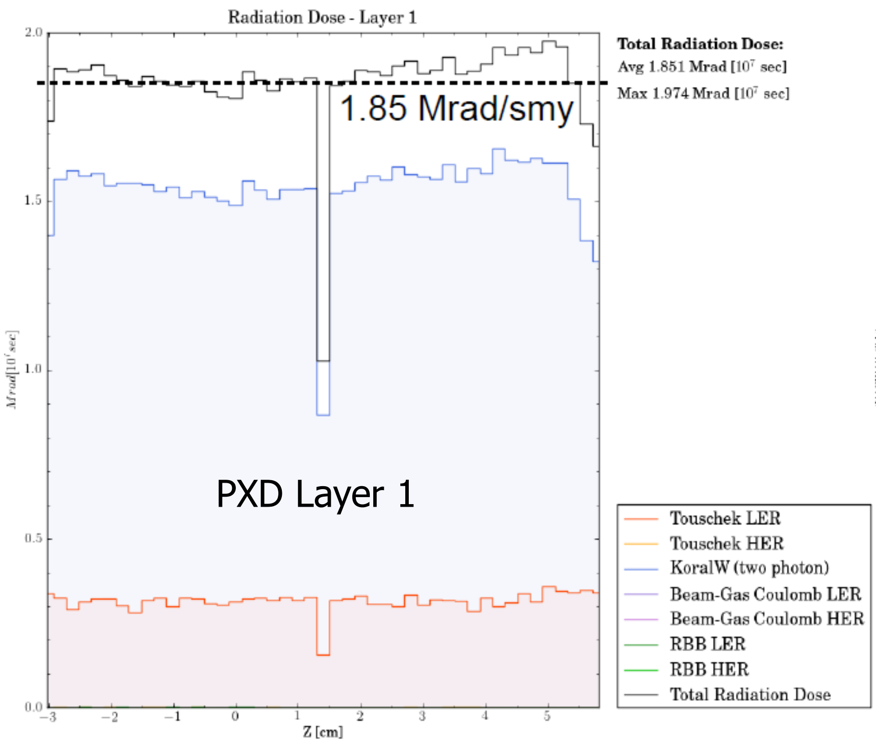
- There is no such thing like “the DEPFET” – sensor cell is always optimized for spec. application
  - ↳ pixel size 20μm → ~mm
  - ↳ shaped response (linearity, charge handling capability..)
  - ↳ special operation modes
    - » electronic shutter to make the cell insensitive
    - » double DEPFET structures for dead time free read-out
    - » multiple read-out for noise reduction
    - » …

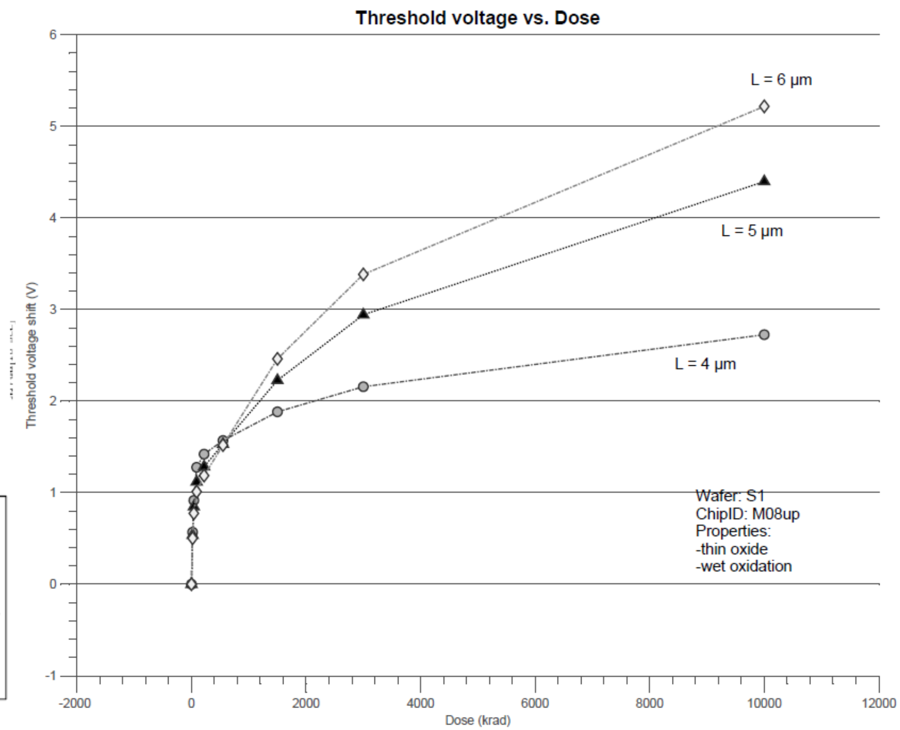
- Main applications are
  - ↳ spectroscopic x-ray imaging
  - ↳ high precision vertexing
  - ↳ new fields emerging: direct electron detectors

- Biggest DEPFET project as of today: Belle II PXD
  - ↳ all process modules: front-end + thinning + three metals ready
  - ↳ pilot batch started
  - ↳ ….. exicting times …. ☺

Thank you for your attention!!

Belle II Background – rad. damage - TiD





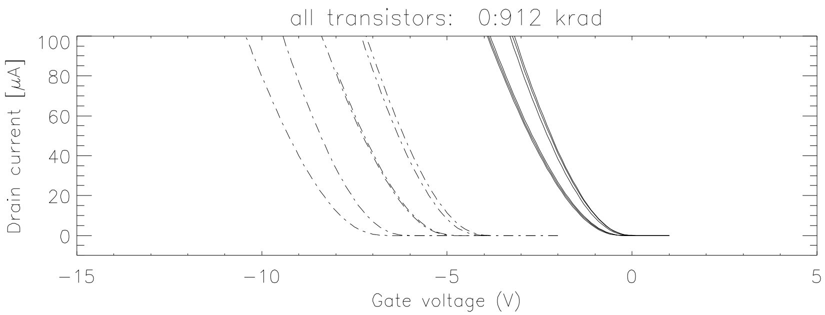
Total ionizing dose:

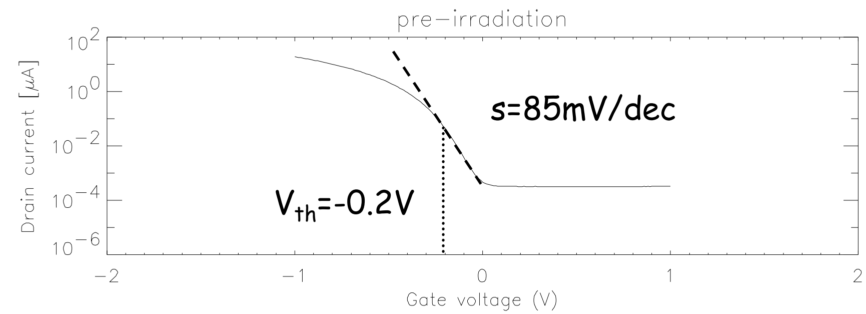
- ▷ L1 ~2 Mrad/smy
- ▷ L2 ~0.6 Mrad/smy
- ▷ Fairly uniform over Z

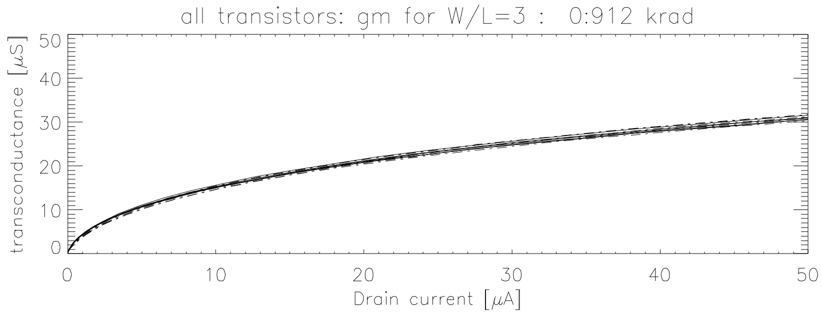
Effect on DEPFET:

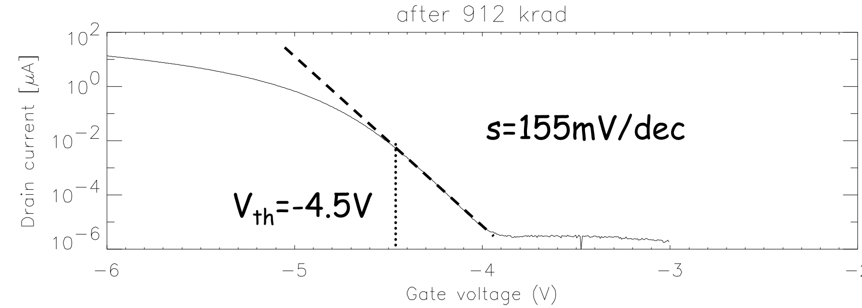
- ▷ ΔVth after 10Mrad ~5V
  - ↳ uniformity of response to radiation?
- ▷ ASICs to allow for additional pedestal variation

Irradiation effects (after ≈1Mrad ^{60}Co)

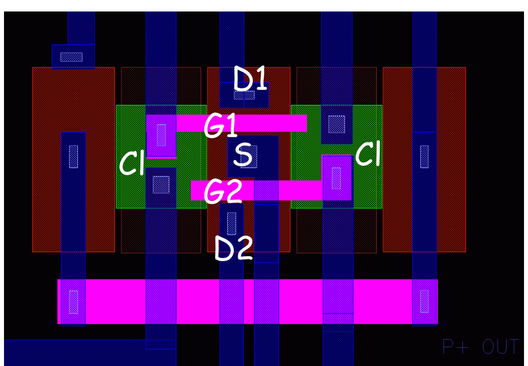








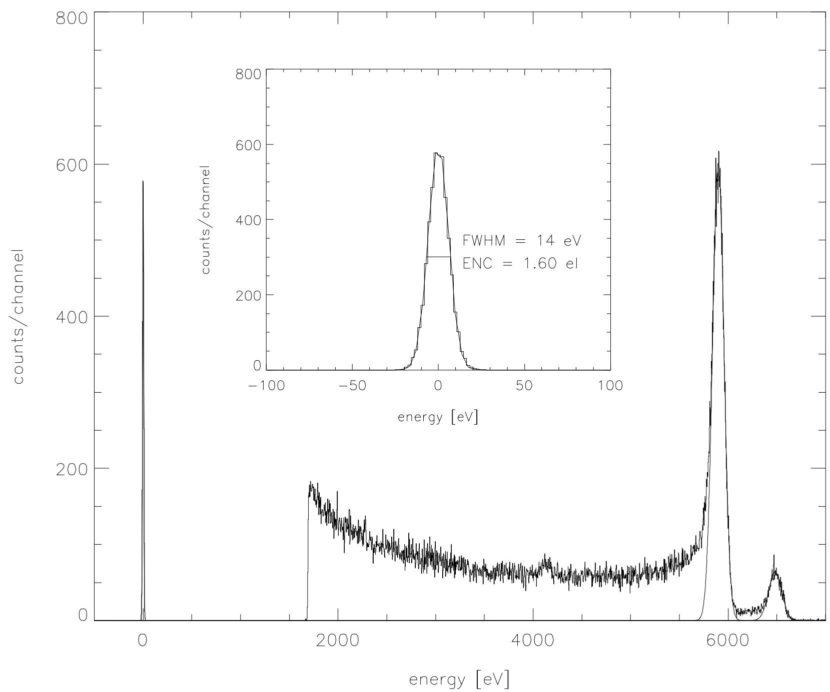
No change of g_m but increased interface trap density (912 krad → $\Delta N_{it} \approx 7 \cdot 10^{11}$ cm^{-2})



Open questions:

- Noise contributions after irrad.?
- Internal amplification g_q?
- Leakage current?

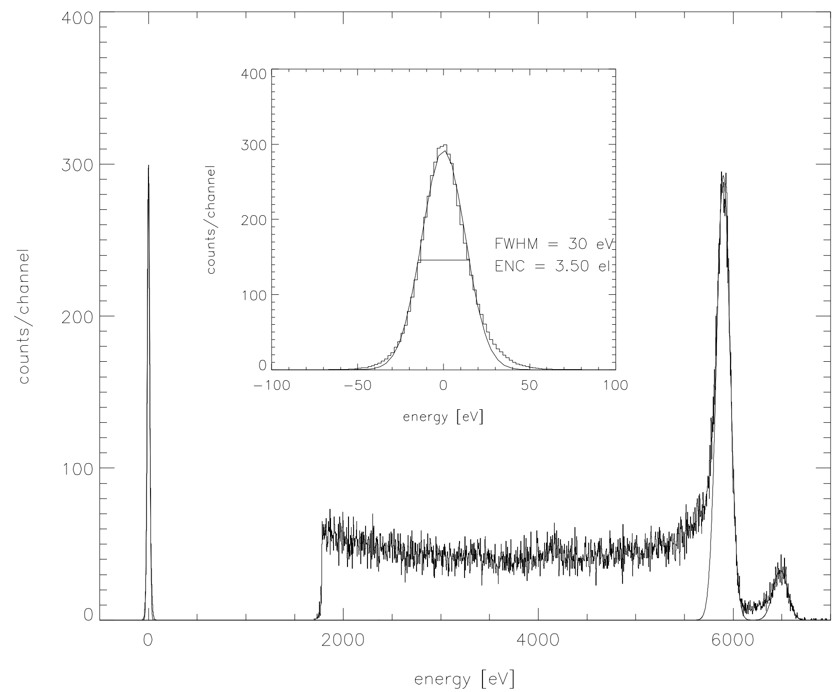
^{55}Fe Spectrum (before and after ≈1Mrad ^{60}Co)



non-irradiated
V_{thresh}≈-0.2V, V_{gate}=-2V
I_{drain}=41 μA
time cont. shaping τ=10 μs

Noise ENC=1.6 e^- (rms)

at T>23 degC

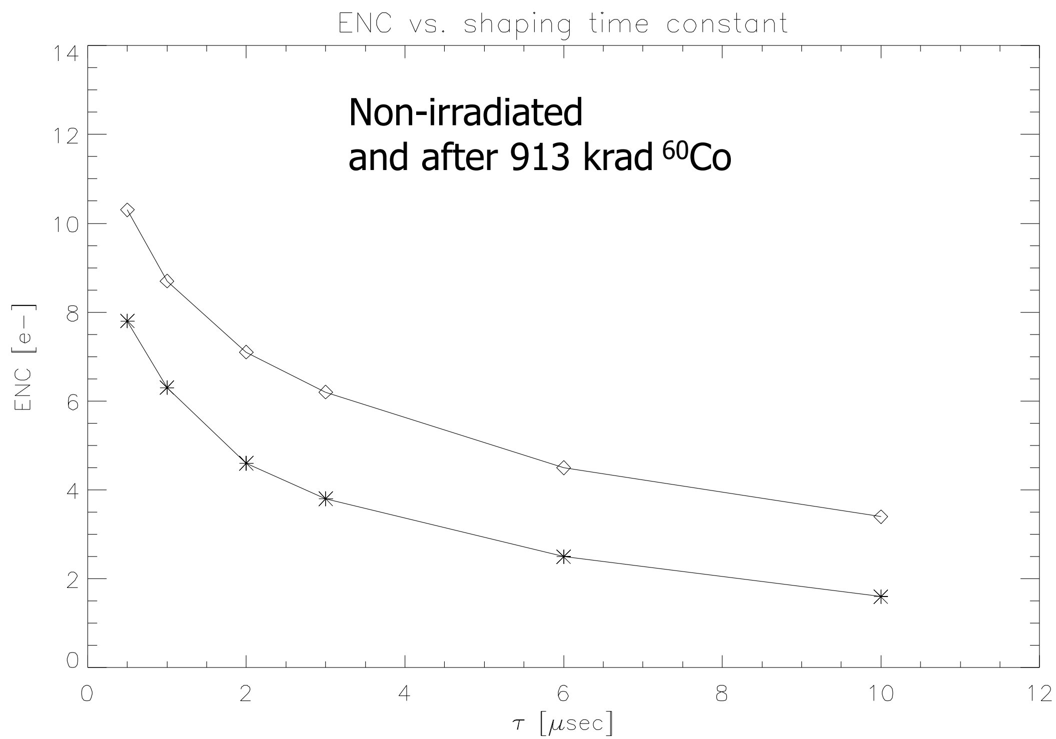


912 krad ^{60}Co
V_{thresh}≈-4.0V, V_{gate}=-6.0V
I_{drain}=40 μA
time cont. shaping τ=10 μs

Noise ENC=3.5 e^- (rms)

at T>23 degC

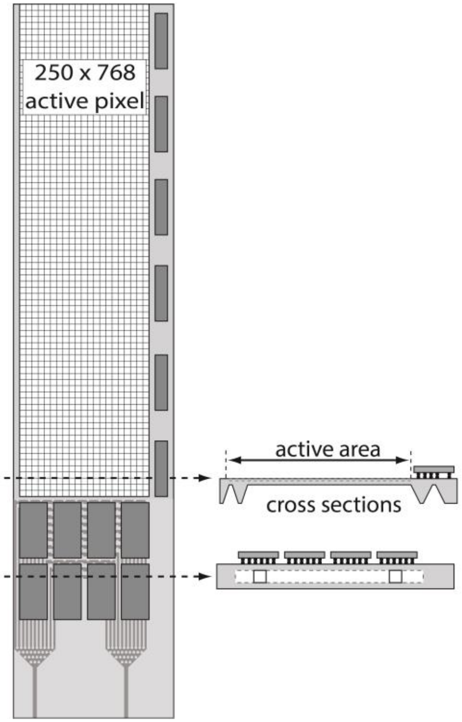
Noise vs. shaping time τ

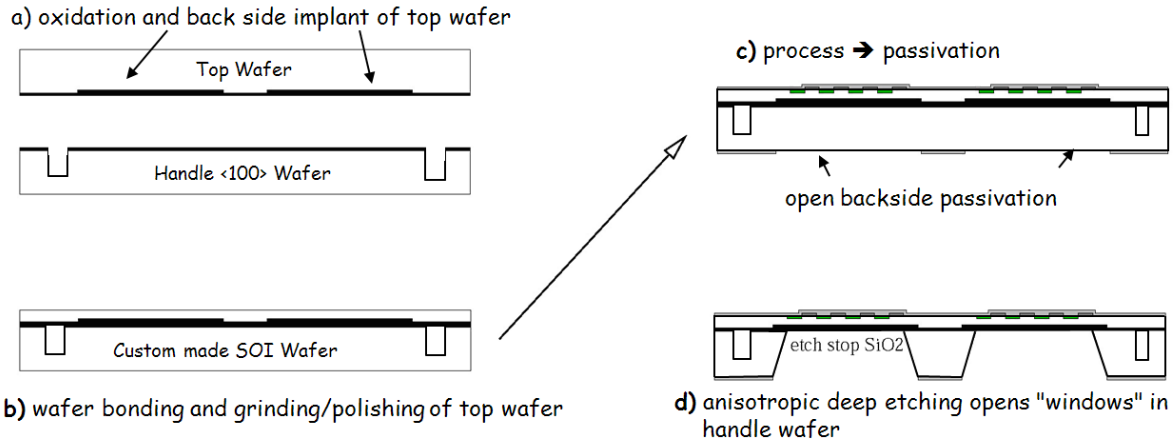


$$ENC = \sqrt{\alpha \frac{2kT}{g_m} C_{tot}^2 A_1 \frac{1}{\tau} + 2\pi a_f C_{tot}^2 A_2 + q I_L A_3 \tau}$$

Therm. noise | 1/f | I_L

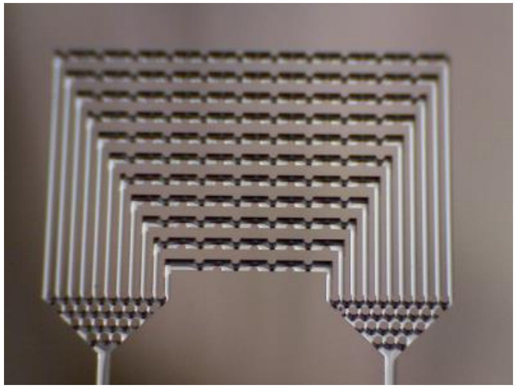
Integrated micro-channels



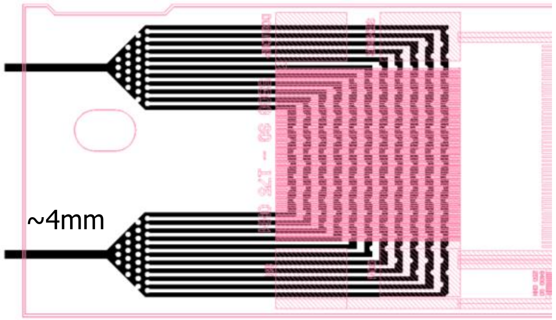


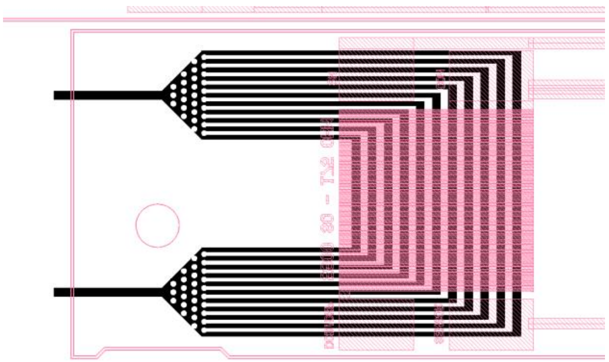
A spin-off of SOI approach : thinned all-silicon module with integ. cooling

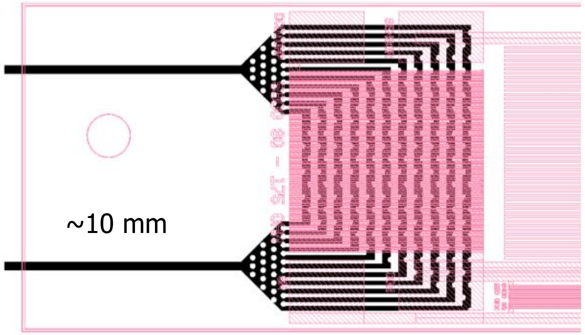
:- most heat generated by read-out ASICs
:- idea: integrate channels into handle wafer beneath the ASICs
:- channels etched before wafer bonding → cavity SOI (C-SOI)
:- full processing on C-SOI, thinning of sensitive area
:- micro-channels accessible only after cutting (laser)

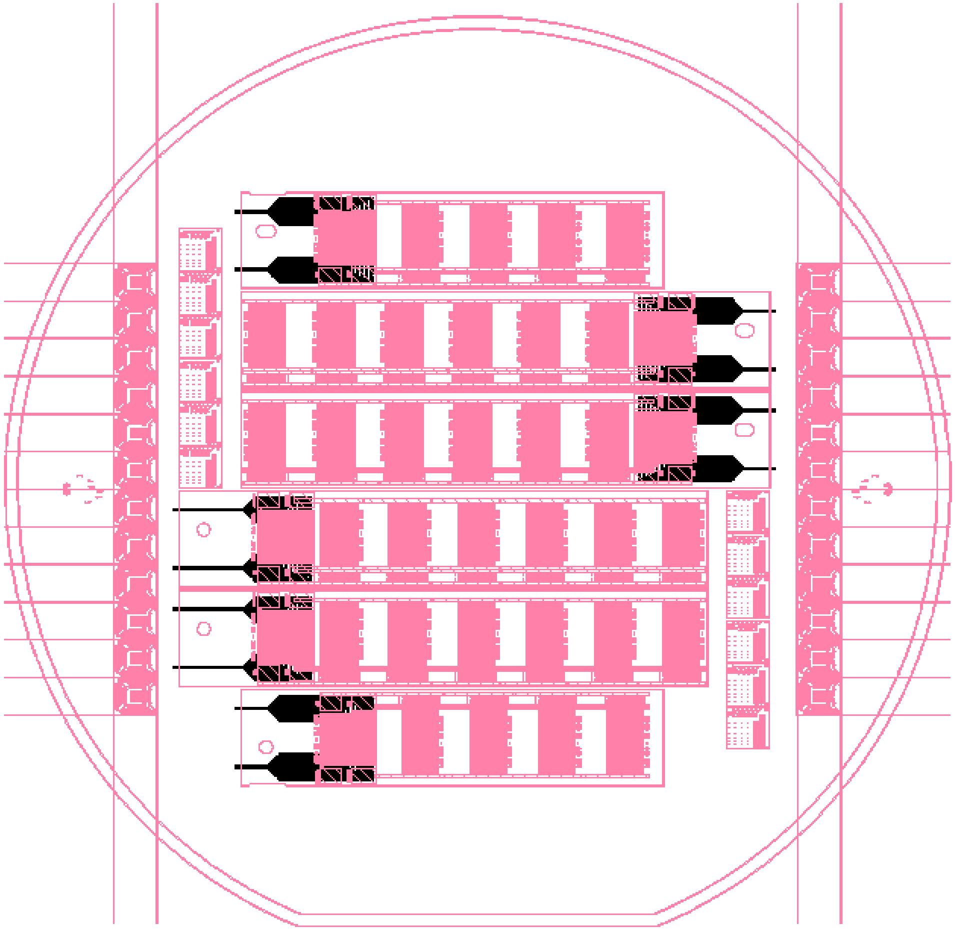


First feasibility study

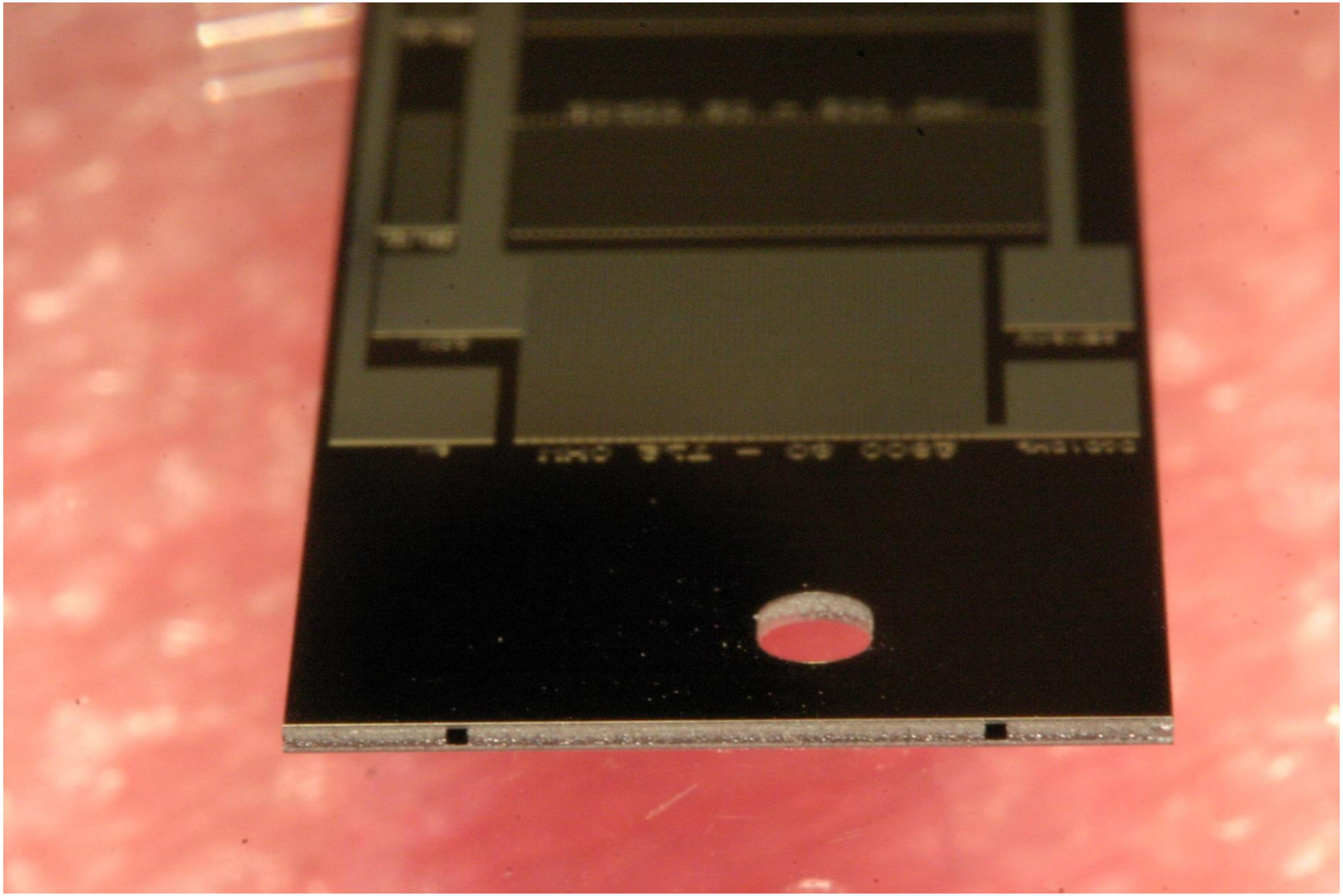






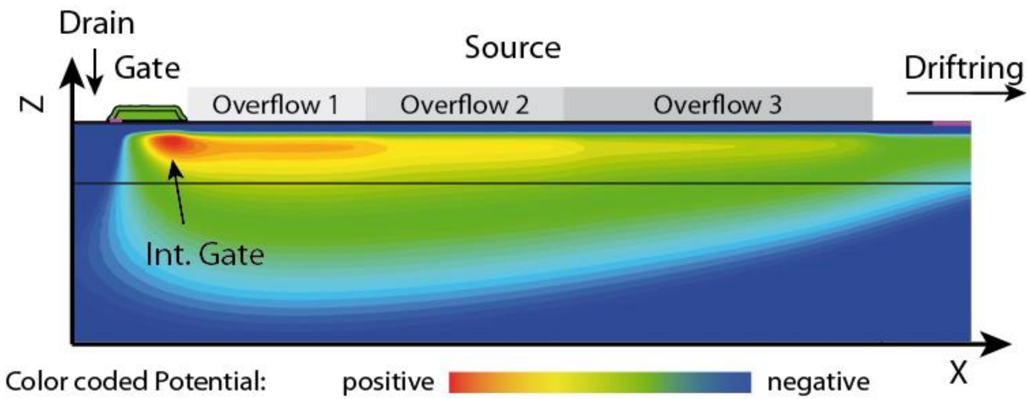


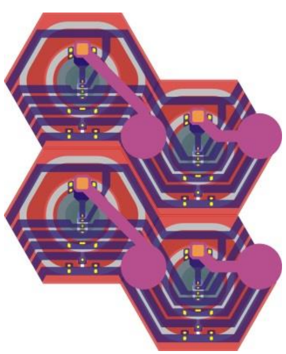
First thermal samples for testing

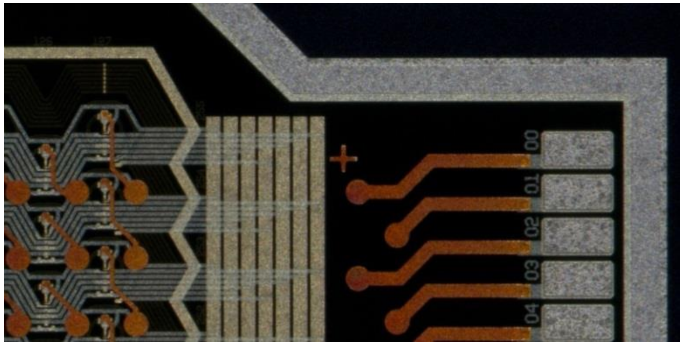


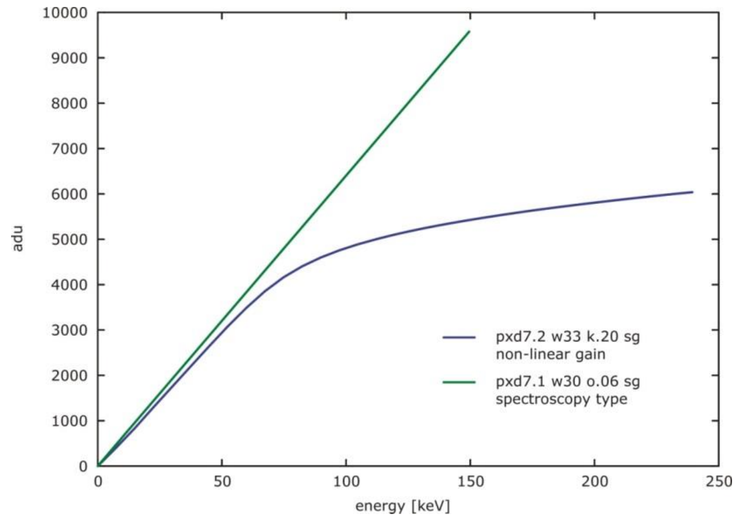
DEPFET Sensor with Signal Compression - DSSC

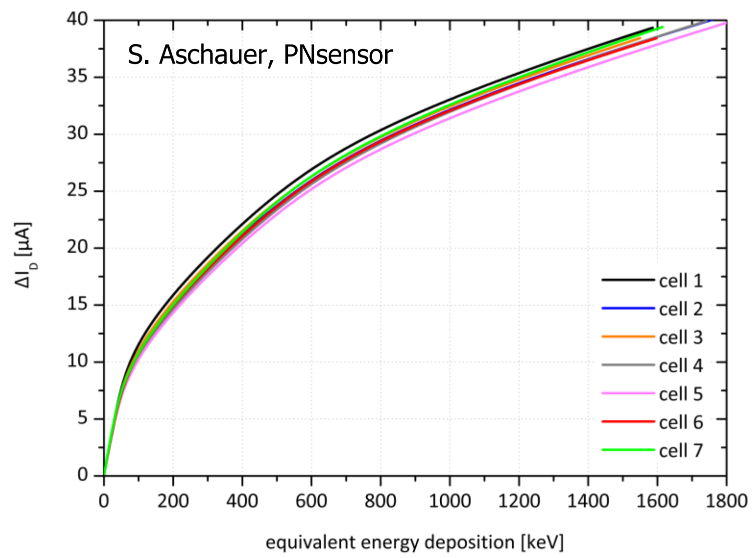
- The internal gate extends into the region below the source
- Small signals collected directly below the channel
  - ↳ Most effective, large signal
- Large signals spill over into the region below the source
  - ↳ Less effective, smaller signal
- staggered potential inside internal gate by varying impl. doses



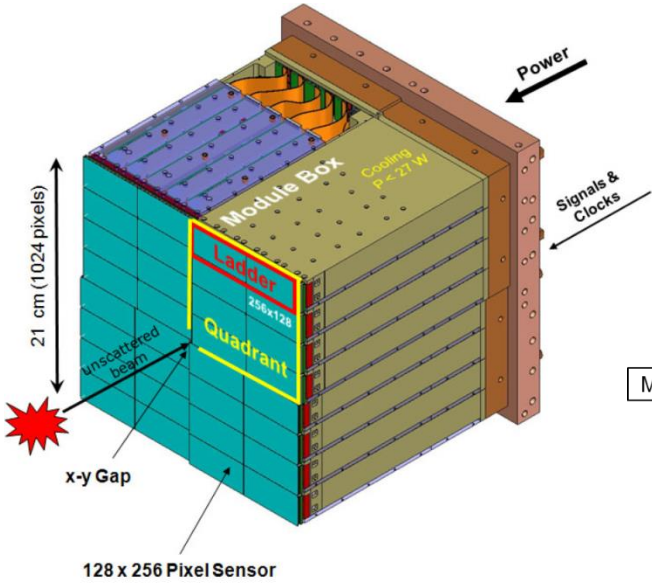


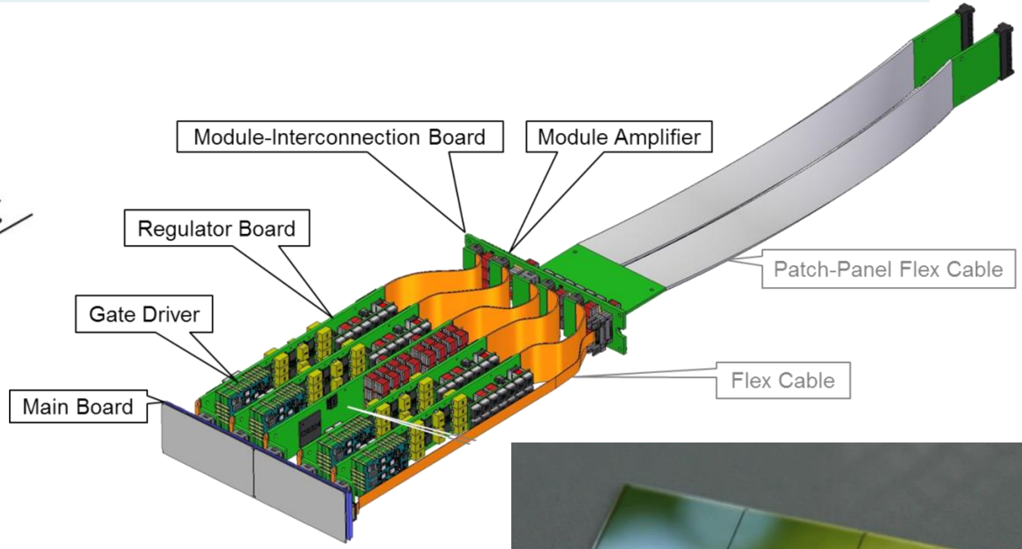


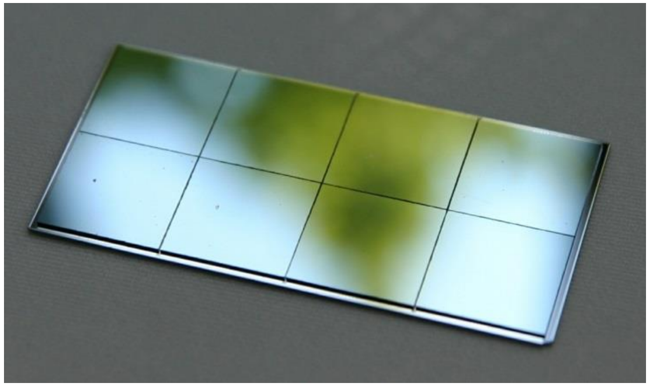


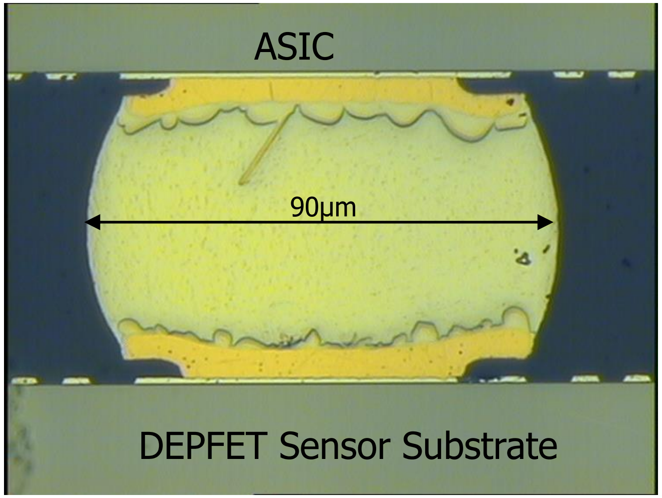


full parallel read-out – 1Mpix at 4.5MHz frame rate







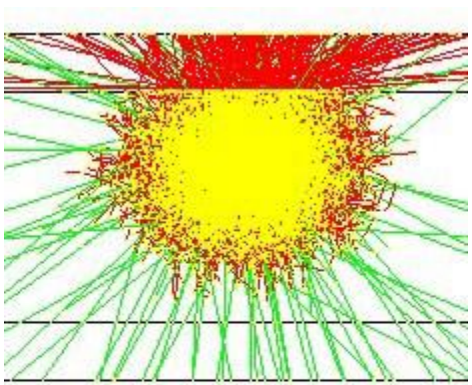


- ▷ 8 chips, 1.5x1.4 cm², 33000 bumps in total per half-ladder
- ▷ Low force, back side free, bump bonding on special jigs
- ▷ **Hybrid pixel sensor with active pixels**

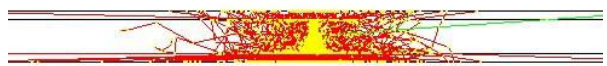
Scaling the thickness - µ-mechanics

Why thin(ner) sensors?

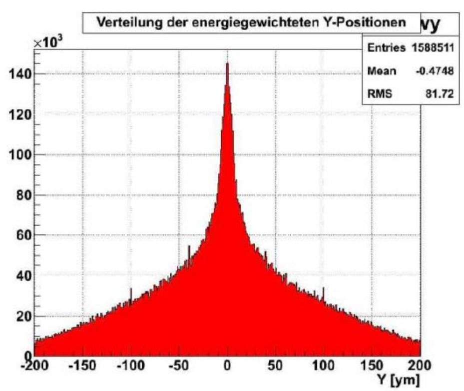
- ▷ High precision vertexing
  - ↳ Belle II, ILC → Carlos' talk
- ▷ LowE electron detectors (300keV primaries)
  - ↳ Position resolution drastically improved

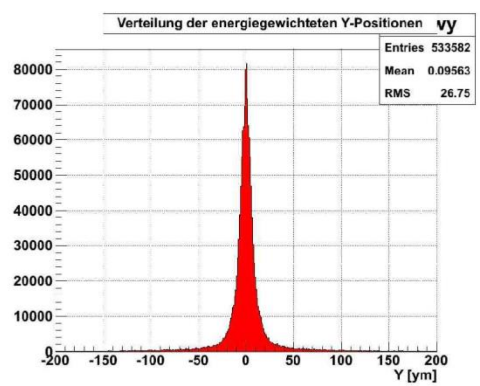


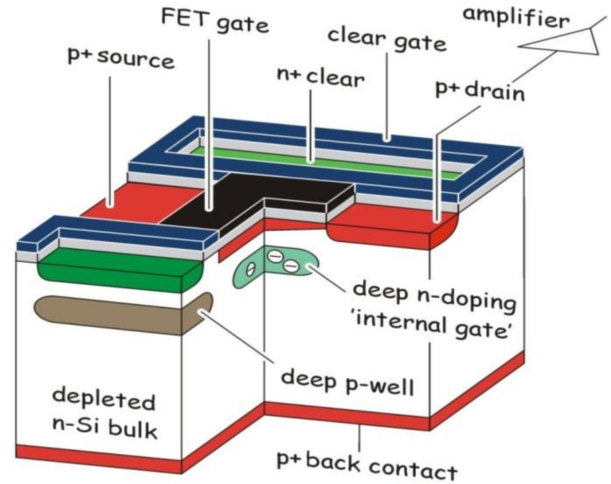
450 µm



50 µm







450µm

↓

75, 50, 20 … µm