Development of CMOS Pixel Sensors for HIGH-PRECISION Vertexing & Tracking Devices

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Terascale Workshop, Berlin 6th of March 2015

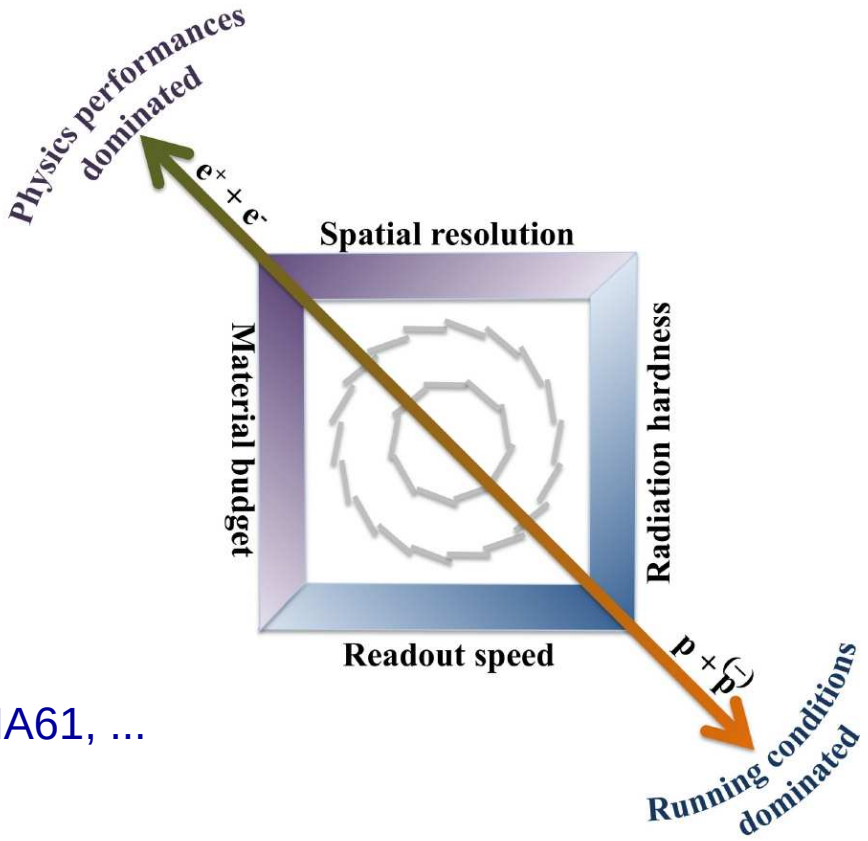
Contents

SOURCES : Talks at CPIX-14 + VERTEX-14 + FEE-14 + TWEPP-13/14 + LHCC/ALICE

SLIDES : M.Deveaux, L.Greiner, Ch.Hu-Guo, M.Keil, M.Mager, L.Musa, F.Morel, D.Muenstermann, I.Peric, F.Reidt, W.Snoeys

Motivation for Developing CMOS Sensors

Quadrature of the Vertex Detector



- **CPS development triggered by need of**
  very high granularity & low material budget

- **Applications exhibit much milder running conditions than pp/LHC**

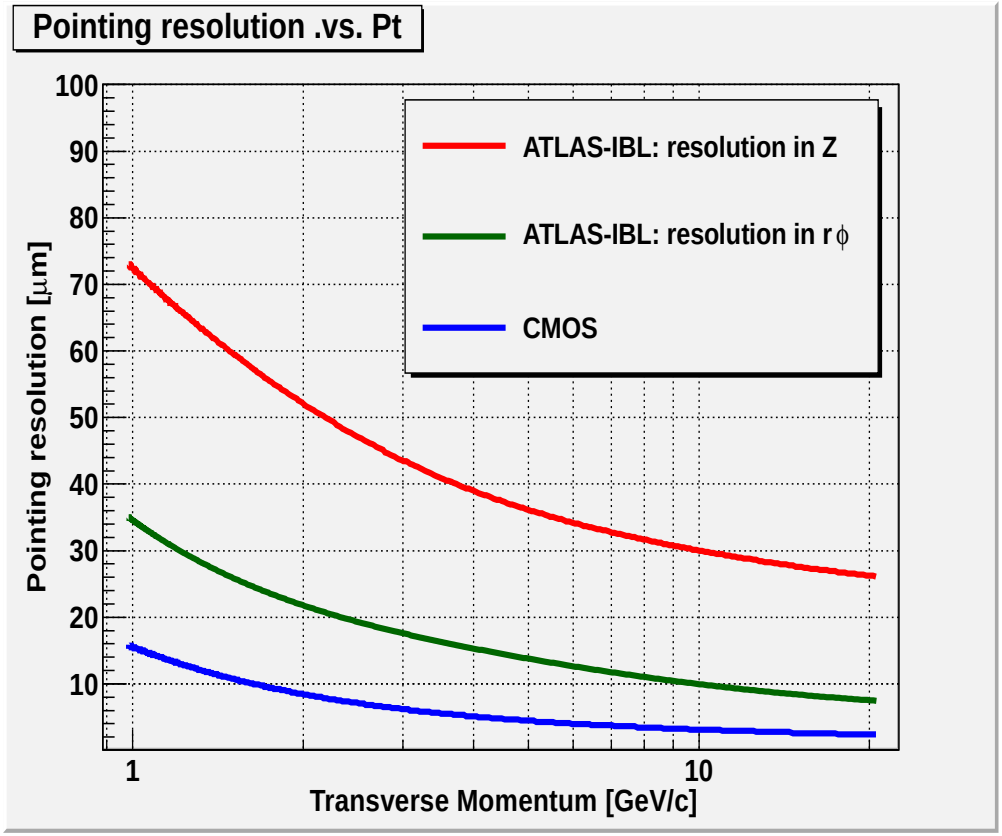
  ⇒ **Relax speed & radiation tolerance specifications**

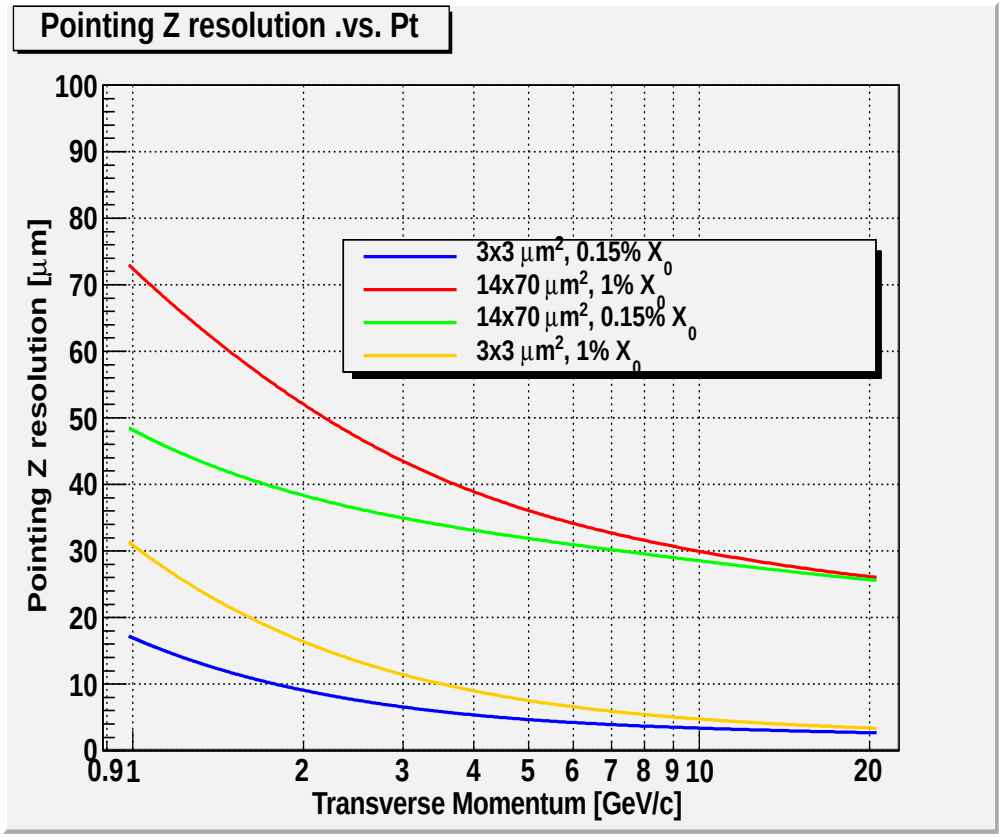
- **Increasing panel of existing, foreseen or potential application domains :**
  - **Heavy Ion Collisions :** STAR-PXL, ALICE-ITS, CBM-MVD, NA61, ...
  - **e^+e^- collisions :** ILC, BES-3, ...
  - **Non-collider experiments :** FIRST, NA63, Mu3e, PANDA, ...
  - **High precision beam telescopes** adapted to medium/low energy electron beams :

    ↪ few μm resolution achievable on DUT with EUDET-BT (DESY), BTF-BT (Frascati), ...

Example of Application : ILC Vertex Detector

- **Goal :** $\sigma_{sp} \lesssim 3\ \mu m$ **in both directions with** $\lesssim$ **0.15 % X$_0$ / layer**
- **Comparison:** σ_{sp} = 3x3 μm^2 & 0.15 % X$_0$ against **14x70** μm^2 **& 1.0 % X$_0$**



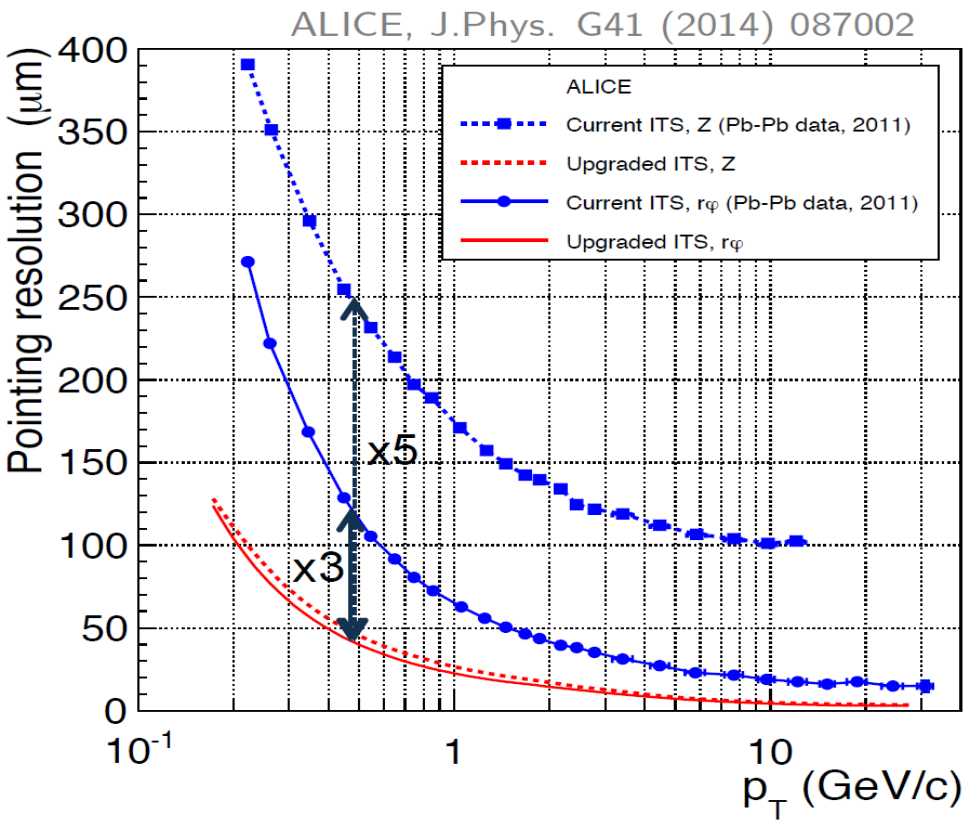


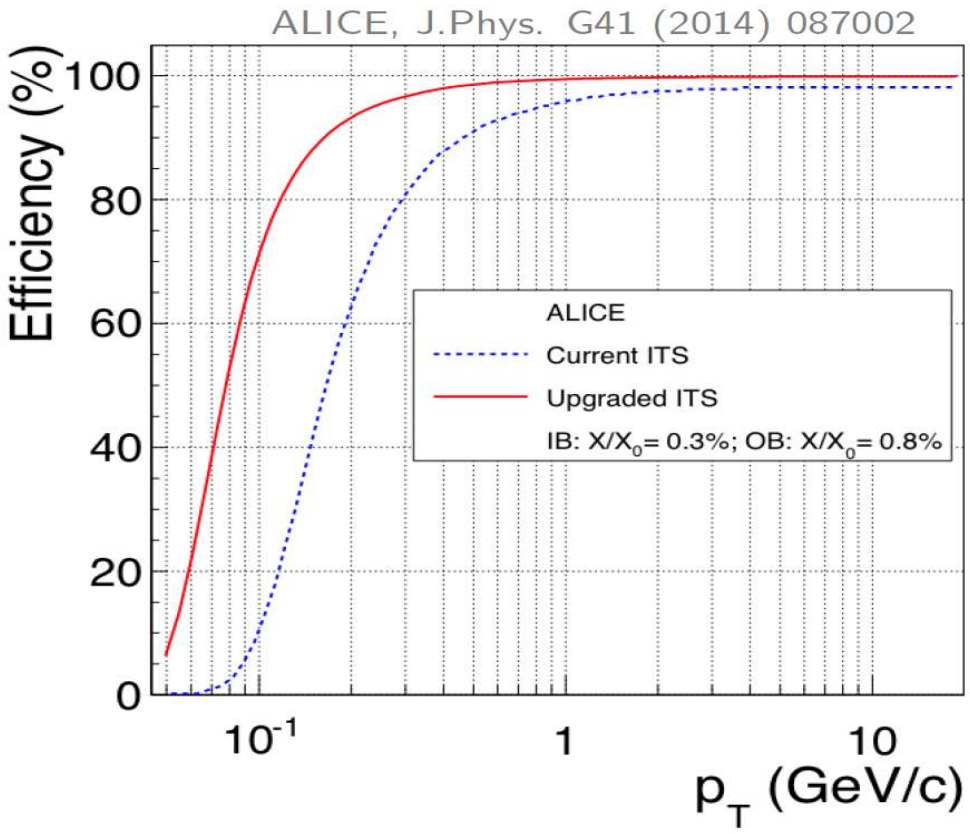
Example of Application : Upgrade of ALICE-ITS

- **ALICE Inner Tracking System (ITS) foreseen to be replaced during LS2/LHC**

  ↪ higher luminosity, improved charm tagging

- **Expected improvement in pointing resolution and tracking efficiency**





Long Term R&D

- *R&D activity of CPS initiated in 1999 for future subatomic physics experiments*
- *First contact for STAR PXL took place in Year 2000 during the workshop Vertex-2000*

VERTEX 2000
9th International Workshop on Vertex Detectors
Sleeping Bear Dunes
National Lakeshore, Michigan, U.S.A.
September 10-15, 2000

First Announcement

Submission of Proceedings

Referees

Registration

Workshop Program

Presen

Pictur

Comm

Accom

Travel

Attend

Attendee Arrival Information

A new Inner Vertex Detector for STAR

H. Wieman
Vertex 2000

1

MONOLITHIC ACTIVE PIXEL SENSORS FOR A LINEAR COLLIDER

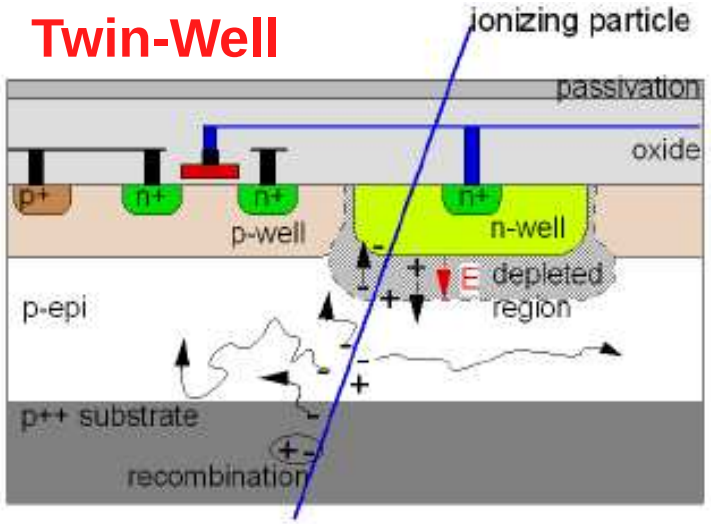
(Marc WINTER - IReS (Strasbourg))
on behalf of IReS+LEPSI coll.

- Physics Motivations
- Principle of Operation of M.A.P.S.
- Characteristics of 1st MAPS prototype
- Beam test Results (preliminary)
- Outlook

CMOS Pixel Sensors: Main Features

- **Prominent features of CMOS pixel sensors :**
  - high granularity $\Rightarrow$ excellent (micronic) spatial resolution
  - signal generated in very thin (15-40 μm) epitaxial layer
    - $\hookrightarrow$ resistivity may be $\gg$ 1 k$\Omega \cdot cm$
  - signal processing μ-circuits integrated on sensor substrate
    - $\Rightarrow$ impact on downstream electronics and syst. integration ($\Rightarrow$ cost)

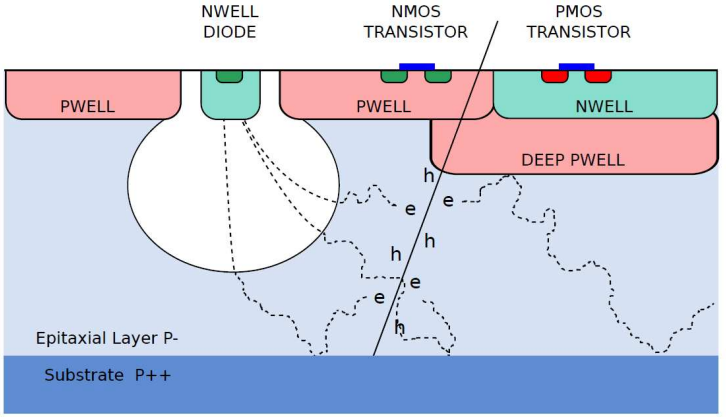
Twin-Well



- **CMOS pixel sensor technology has the highest potential :**

$\Rightarrow$ R&D largely consists in trying to exploit potential at best with accessible industrial processes

$\hookrightarrow$ manufacturing param. not optimised for particle detection: wafer/EPI characteristics, feature size, N(ML), ...



Quadruple-Well

- **Read-out architectures :**
  - 1st generation : rolling shutter (synchronous) with analog pixel output (end-of-column discri.)
  - 2nd generation : rolling shutter (synchronous) with in-pixel discrimination
  - 3rd generation : data driven (asynchronous) with in-pixel discrimination
  - ...

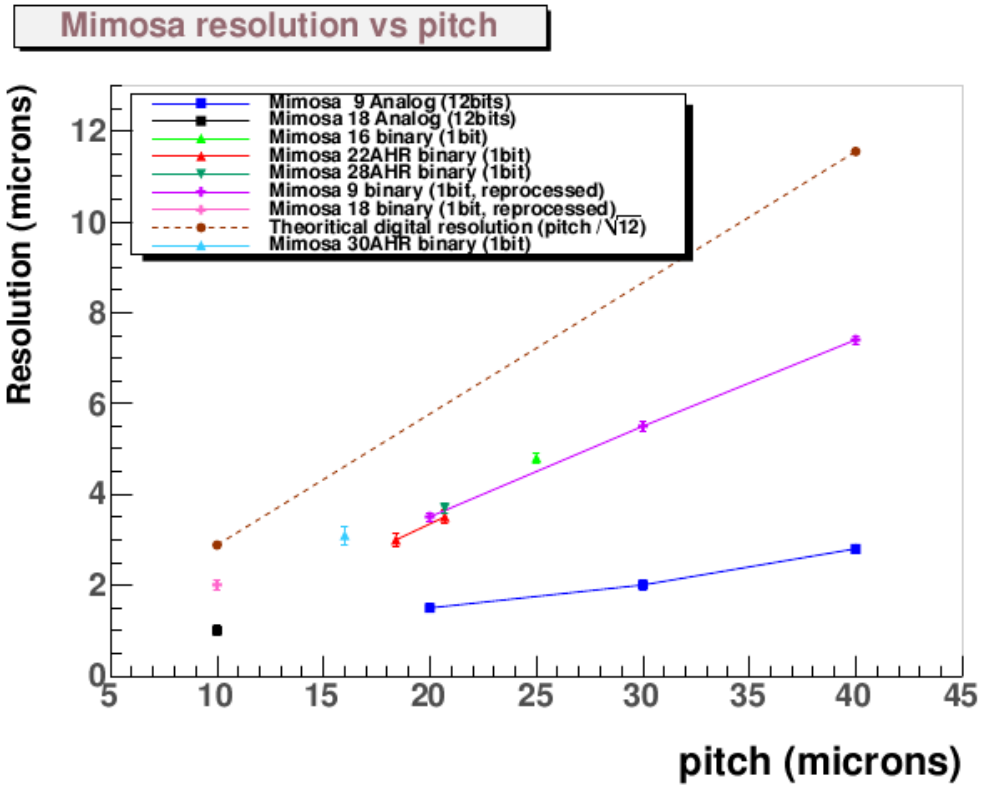
Measured Spatial Resolution

- **Several parametres govern the spatial resolution :**
  - pixel pitch
  - epitaxial layer thickness and resistivity
  - sensing node geometry & electrical properties
  - signal encoding resolution

  $\Rightarrow$ σ_{sp} fct of pitch $\oplus$ SNR $\oplus$ charge sharing $\oplus$ ADCu, ...

- **Impact of pixel pitch (analog output) :**

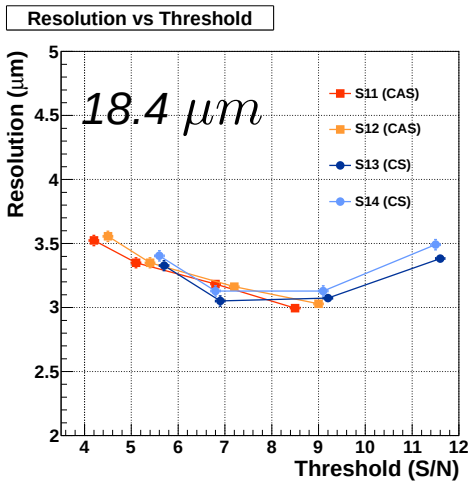
  $\sigma_{sp} \sim 1\ \mu m$ (10 μm pitch) $\rightarrowtail$ $\lesssim 3\ \mu m$ (40 μm pitch)

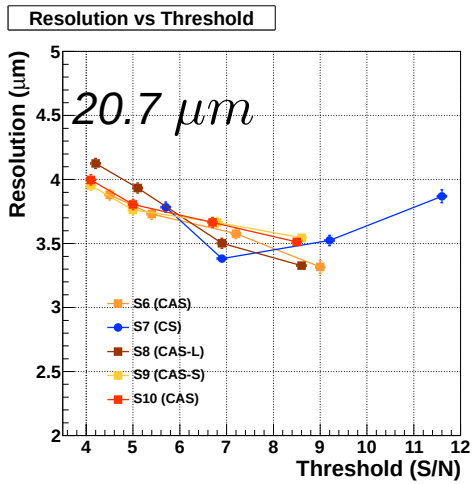


- **Impact of charge encoding resolution :**

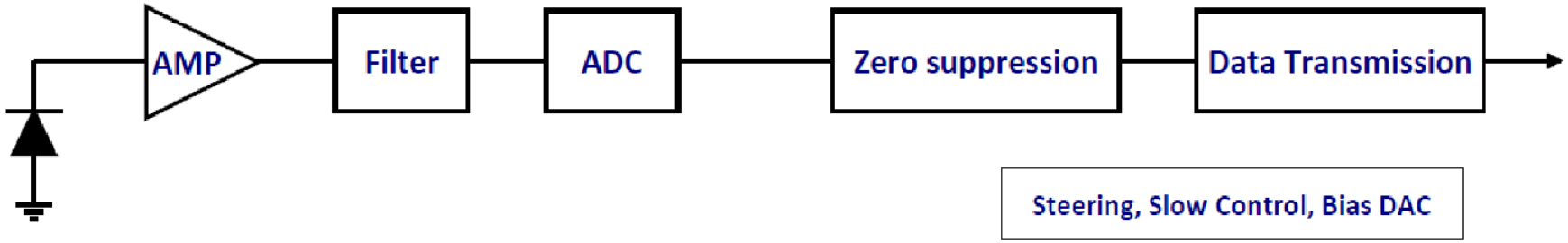
  ▷ ex. of 20 μm pitch $\Rightarrow$ σ_{sp}^{digi} = pitch/$\sqrt{12} \sim 5.7\ \mu m$

Nb of bits	12	3-4	1
Data	*measured*	*reprocessed*	*measured*
σ_{sp}	$\lesssim 1.5\mu m$	$\lesssim 2\mu m$	$\lesssim 3.5\mu m$





Example of Application : Upgrade of ALICE-ITS



- **Typical components of read-out chain :**
  - **AMP :** In-pixel low noise pre-amplifier
  - **Filter :** In-pixel filter
  - **ADC :** Analog-to-Digital Conversion : 1-bit ≡ discriminator
    ↪ may be implemented at column or pixel level
  - **Zero suppression :** Only hit pixel information is retained and transfered
    ↪ implemented at sensor periphery (usual) or inside pixel array
  - **Data transmission :** O(Gbits/s) link implemented on sensor periphery

- **Read-Out alternatives :**
  - **Synchronous :** rolling shutter architecture
  - **Asynchronous :** data driven architecture

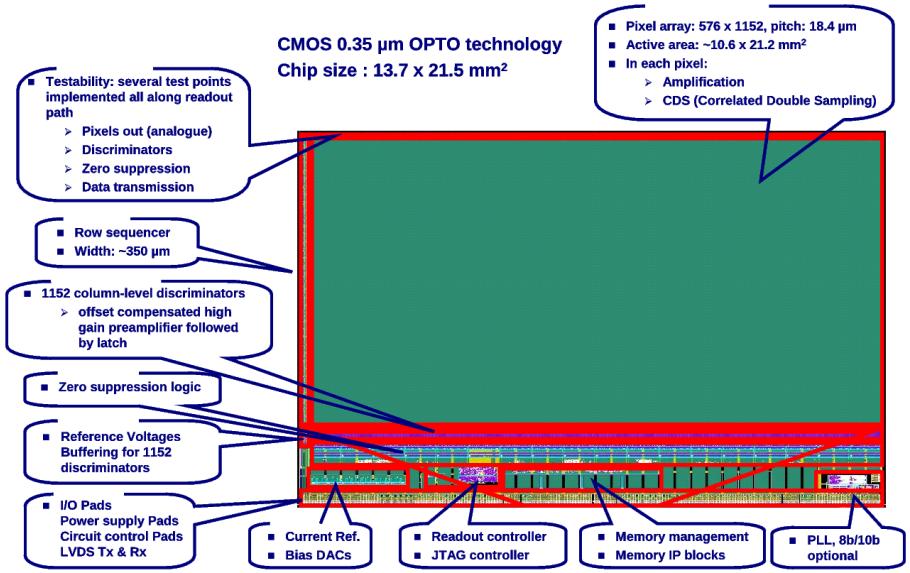
- **Rolling shutter : best approach for twin-well processes**

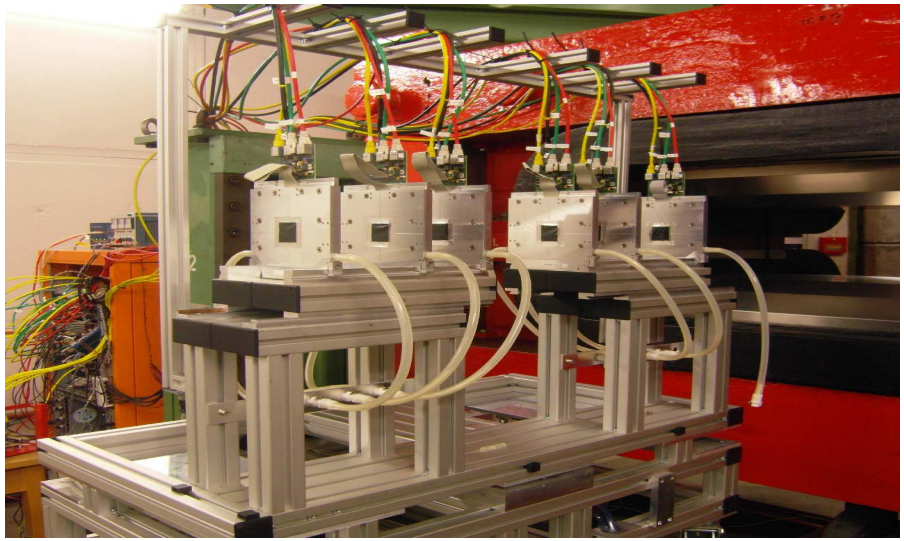
↪ trade-off between performance, design complexity, pixel dimensions, power, ...

↪ MIMOSA-26 (EUDET), MIMOSA-28 (STAR), ...

CMOS Pixel Sensors: Established Architecture

- **Main characteristics of MIMOSA-26 sensor equipping EUDET BT :**
  - 0.35 μm process with high-resistivity epitaxial layer
    (coll. with IRFU/Saclay)
  - column // architecture with in-pixel amplification (cDS)
    and end-of-column discrimination, followed by $\emptyset$
  - binary charge encoding
  - active area: 1152 columns of 576 pixels (21.2$\times$10.6 mm^2)
  - pitch: 18.4 $\mu m \rightarrowtail$ $\sim$ 0.7 million pixels
    - $\triangleright$ charge sharing $\Rrightarrow$ $\sigma_{sp} \sim$ 3.-3.5 μm
  - t$_{r.o.} \lesssim$ 100 μs ($\sim$10^4 frames/s)
    - $\hookrightarrow$ suited to $>$10^6 part./cm^2/s
  - JTAG programmable
  - rolling shutter architecture
    - $\Rrightarrow$ full sensitive area dissipation $\cong$ 1 row
      - $\triangleright$ $\sim$ 250 mW/cm^2 power consumption (fct of N$_{col}$)
  - thinned to 50 μm (yield $\sim$ 90 %)

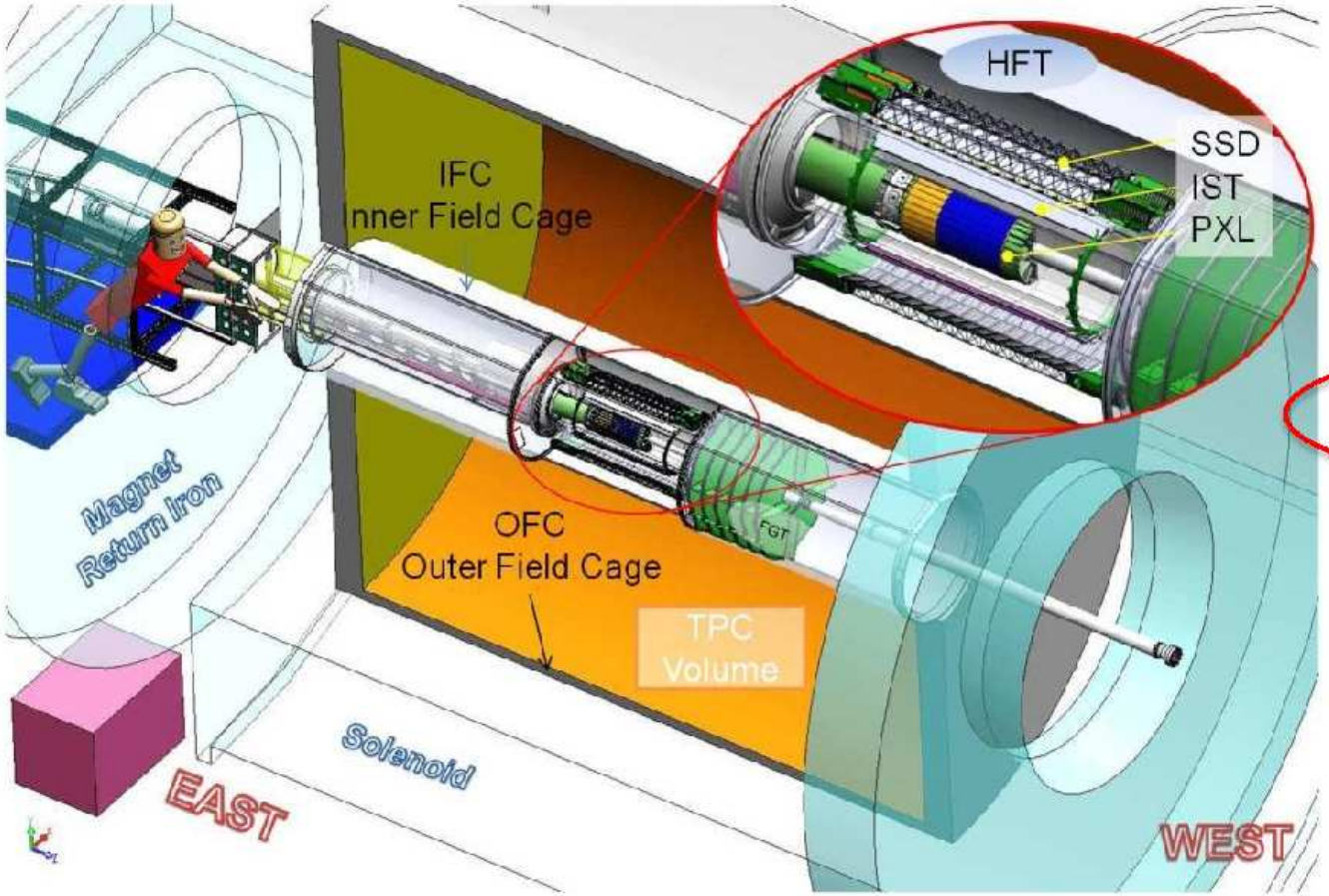




- **Various applications :** VD demonstrators, NA63, NA61, FIRST, oncotherapy, dosimetry, ...

PXL in STAR Inner Detector Upgrades

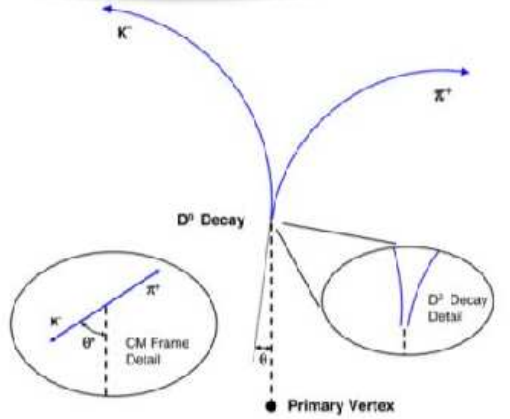
STAR HFT



TPC – Time Projection Chamber
(main tracking detector in STAR)

HFT – Heavy Flavor Tracker

- SSD – Silicon Strip Detector
  - r = 22 cm
- IST – Inner Silicon Tracker
  - r = 14 cm
- PXL – Pixel Detector
  - r = 2.8, 8 cm



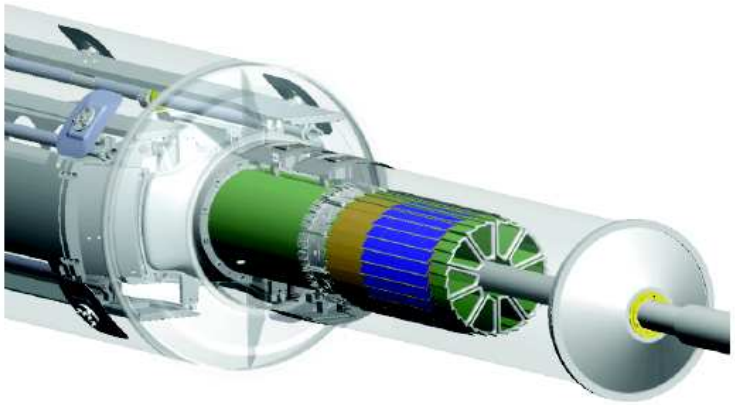
Direct topological reconstruction of
Charm – displaced verticies

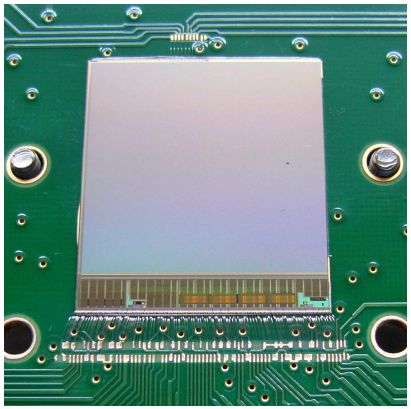
We track inward from the TPC with graded resolution:

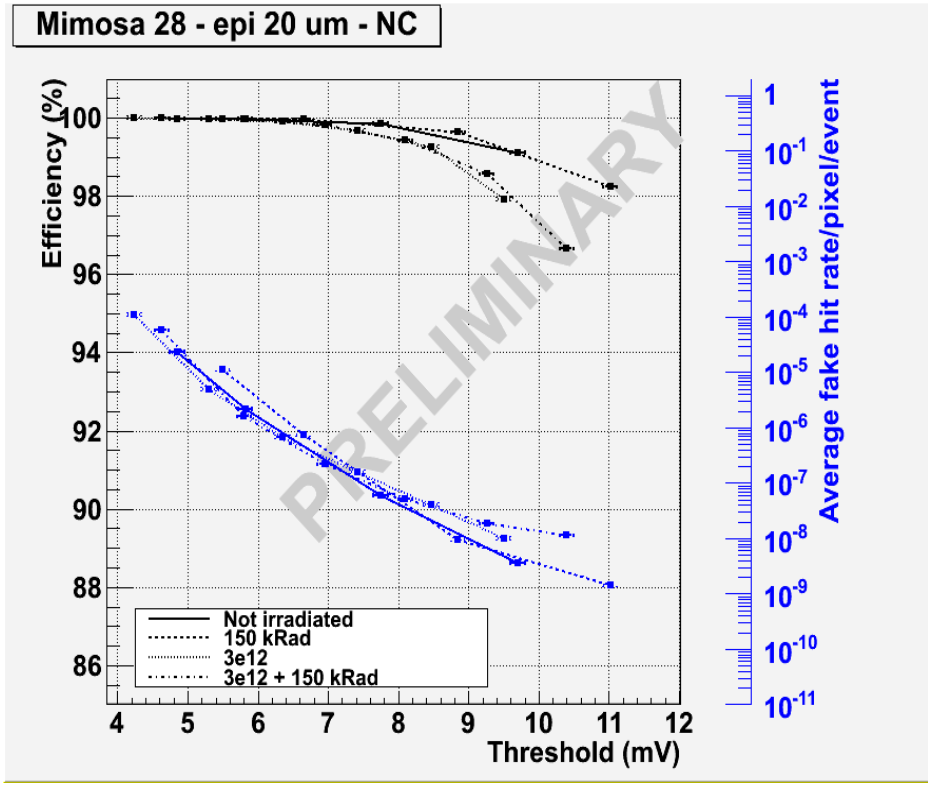
L. Greiner
(CPIX-14)

State-of-the-Art: MIMOSA-28 for the STAR-PXL

- **Main characteristics of ULTIMATE ($\equiv$ MIMOSA-28):**
  - 0.35 μm process with high-resistivity epitaxial layer
  - column // architecture with in-pixel cDS & amplification
  - end-of-column discrimination & binary charge encoding
  - on-chip zero-suppression
  - **active area: 960 colums of 928 pixels (19.9$\times$19.2 mm^2)**
  - **pitch: 20.7 $\mu m \longmapsto \sim$ 0.9 million pixels**
    $\hookrightarrow$ **charge sharing $\Rrightarrow$ $\sigma_{sp} \gtrsim$ 3.5 μm**
  - JTAG programmable
  - **t$_{r.o.}$ $\lesssim$ 200 μs ($\sim$ 5$\times$10^3 frames/s) $\Rrightarrow$ suited to $>$10^6 part./cm^2/s**
  - 2 outputs at 160 MHz
  - **$\lesssim$ 150 mW/cm^2 power consumption**





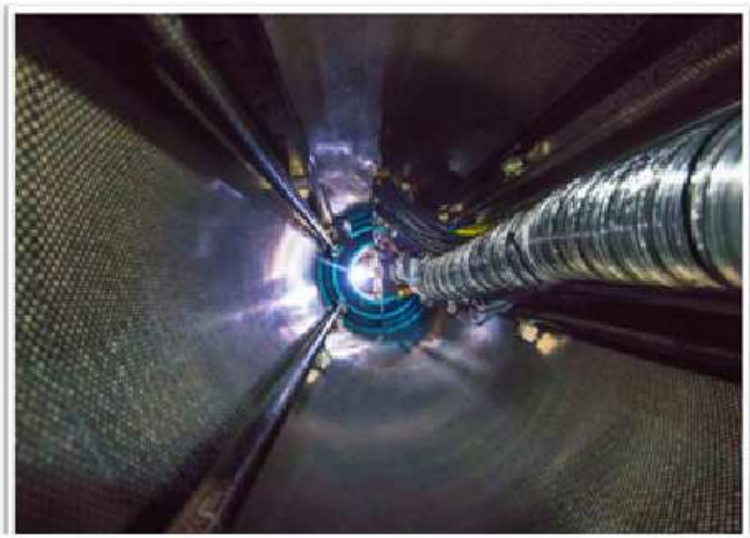


$\triangleright\triangleright\triangleright$ **Sensors FULLY evaluated/validated :** (50 μm thin)

- N $\lesssim$ 15 e$^-$ ENC at 30-35°C
- ϵ_{det}, fake & σ_{sp} as expected
- **Rad. tol. validated (3$\cdot$10^{12}n$_{eq}$/cm^2 & 150 kRad at 30°C)**
- All specifications were met $\Rrightarrow$ 2 detectors of 40 ladders constructed

$\triangleright\triangleright\triangleright$ **1st physics data taking : March to June 2014 $\mapsto$ measured $\sigma_{ip}(p_T)$ match requirements**

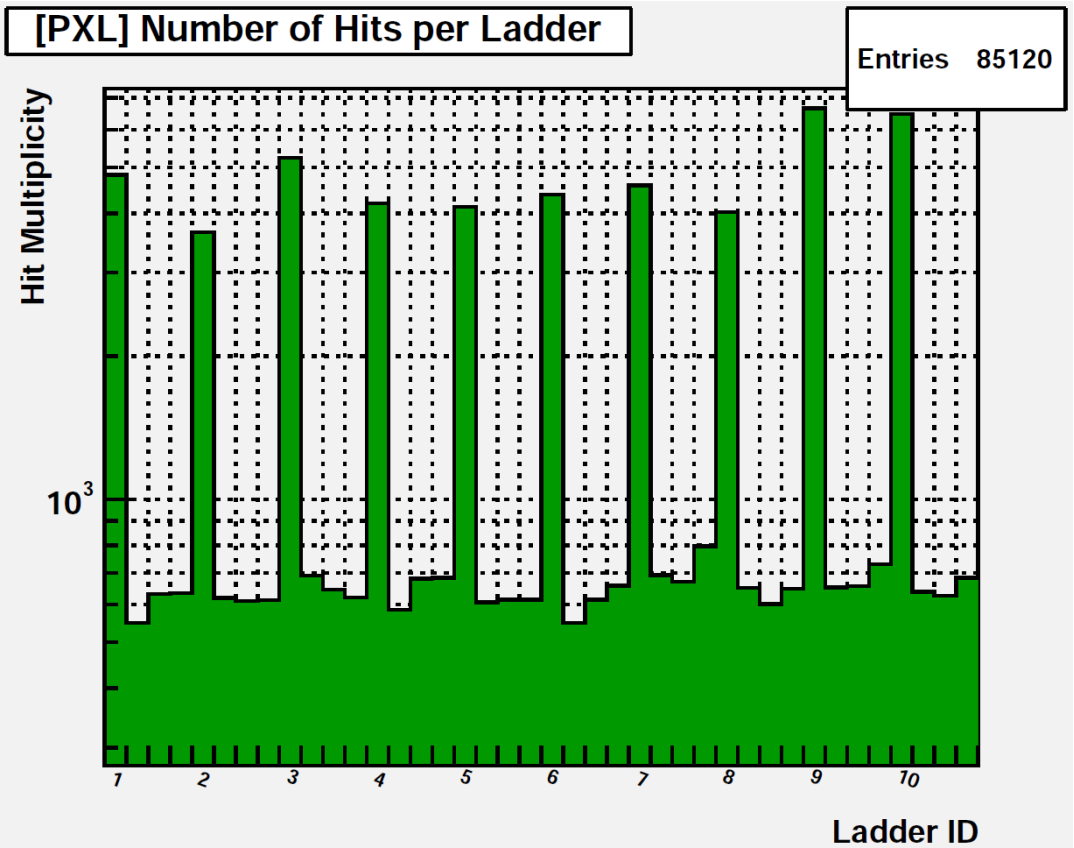
State-of-the-Art : STAR-PXL



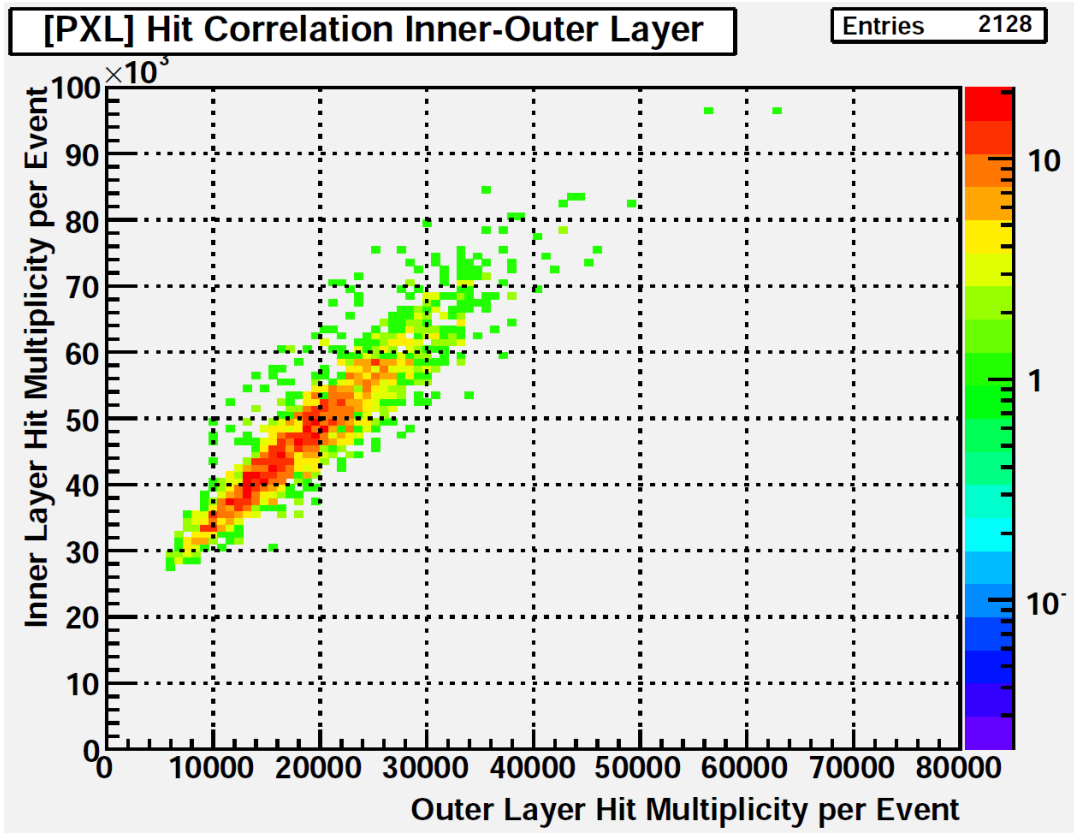
Validation of CPS for HEP (25/09/14 : DoE final approval, based on vertexing performance assessment)

Preliminary Results of STAR-PXL Run : Hit multiplicity

- **Hit pixel multiplicity per ladder (≡ 10 chips) and per layer** **(courtesy of STAR collaboration)**



Nb(hit pixels / ladder)

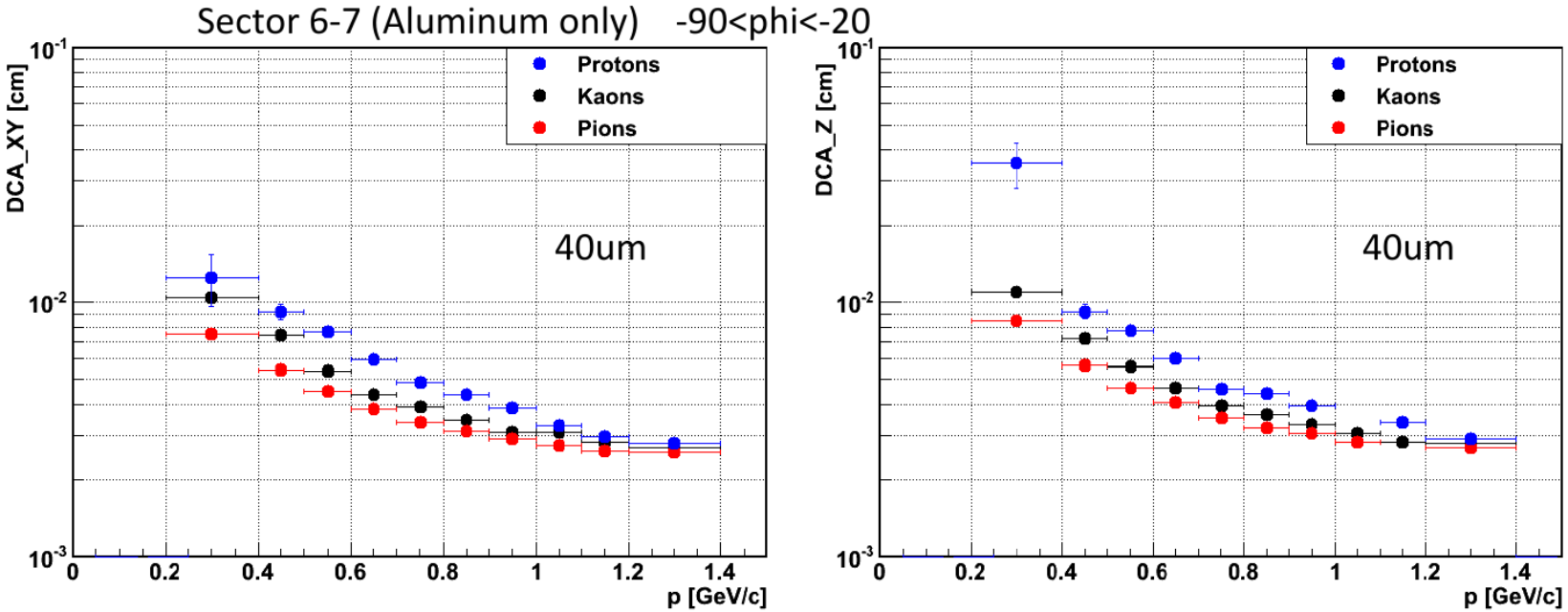


Pixel rate / ladder : Inner vs Outer layer

⇒ **Inner barrel sensors see O(100) hits (≡ 4 pixels) per frame**

Preliminary Results of STAR-PXL Run

- **Benchmark : measured impact parametre resolution for 700-800 MeV/c kaons :**
  - Figure (courtesy of STAR collaboration) displays resolutions on DCA in RΦ and Z
  - Data collected with low luminosity (clean TPC environment)
  - Tracks traversing the ladders equipped with Al traces
  - Results are still **PRELIMINARY**



⇛ **40 μm obtained for 700-800 MeV/c kaons in both directions, as expected**

Next Challenge : ALICE-ITS Upgrade

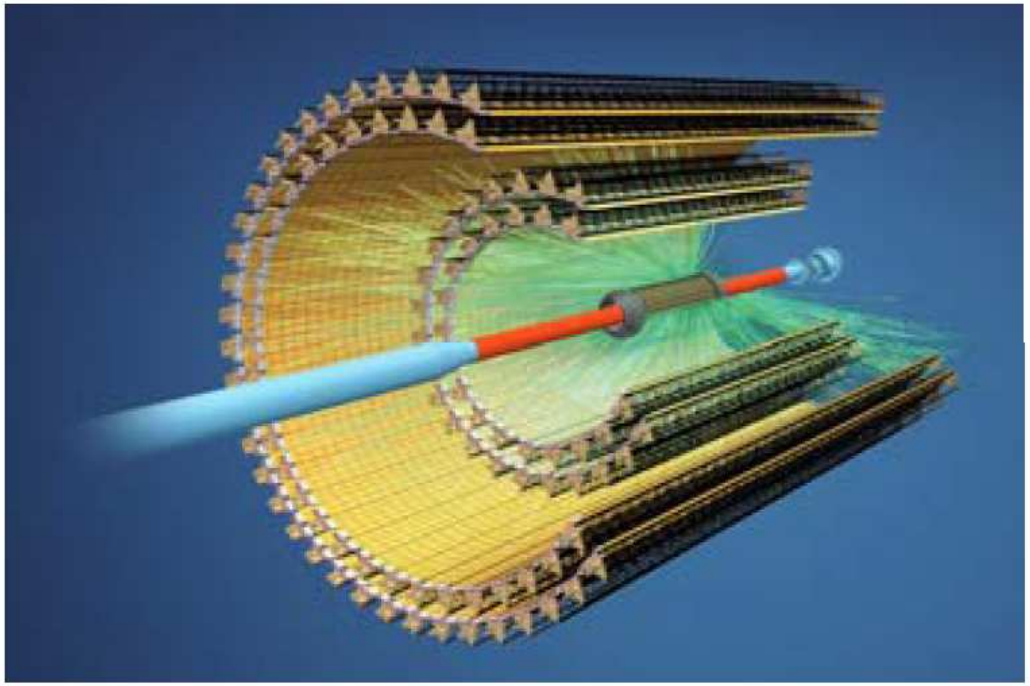
- Upgrade of ITS **entirely based on CPS** :
  - Present geometry: 6 layers

    HPS x 2 / Si-drift x 2 / Si-strips x 2
  - Future geometry : 7 layers $\longmapsto$ $\longmapsto$ $\longmapsto$

    all with CPS ($\sim$ 25-30 $\cdot$ 10^3 chips)

    $\Rrightarrow$ 1st large tracker (10 m^2) using CPS
  - ITS-TDR approved March 2014 :

    Pub. in J.Phys. G41 (2014) 087002



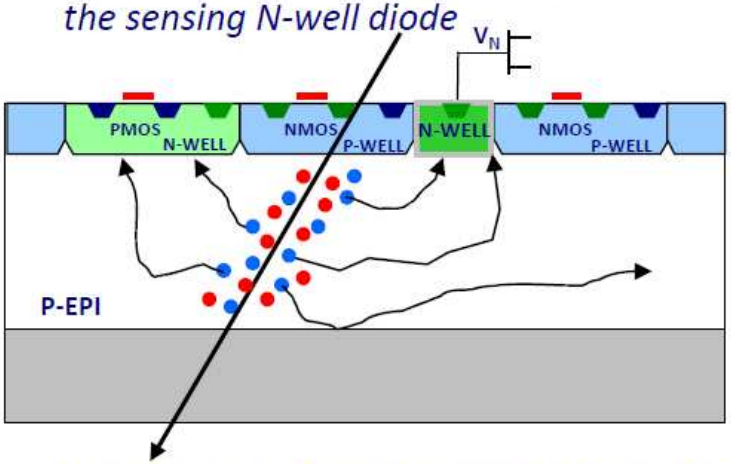
- **Requirements for ITS inner and outer barrels compared to specifications of STAR-PXL chip :**

	σ_{sp}	$t_{r.o.}$	Dose	Fluency	T_{op}	Power	Active area
STAR-PXL	$< 4\ \mu m$	$< 200\ \mu s$	150 kRad	3·10^{12} n_{eq}/cm^2	30-35°C	160 mW/cm^2	0.15 m^2
ITS-in	$\lesssim 5\ \mu m$	$\lesssim$ **30** μs	**700 kRad**	**1·10^{13} n_{eq}/cm^2**	30°C	$<$ 300 mW/cm^2	0.17 m^2
ITS-out	$\lesssim 10\ \mu m$	$\lesssim$ **30** μs	15 kRad	4·10^{11} n_{eq}/cm^2	30°C	$<$ **100 mW/cm^2**	$\sim$ **10 m^2**

$\Rrightarrow$ **0.35 μm CMOS process (STAR-PXL) marginally suited to read-out speed & radiation tol.**

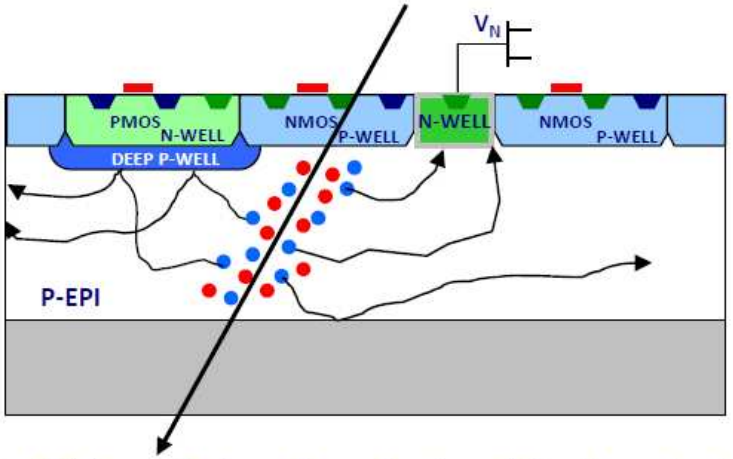
CMOS Process Transition : STAR-PXL ⟼ ALICE-ITS

- *Twin well process: 0.6-0.35 µm*
  - *Use of PMOS in pixel array is not allowed because any additional N-well used to host PMOS would compete for charge collection with the sensing N-well diode*

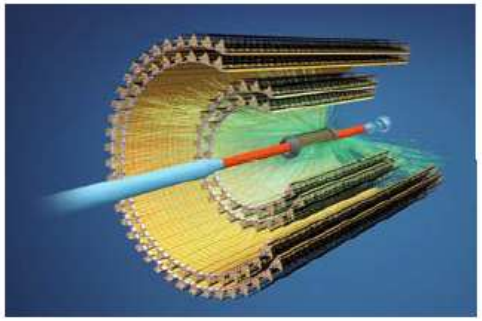


  - *Limits choice of readout architecture strategy*
  - *Already demonstrate excellent performances*
    - *STAR PXL detector: MIMOSA28 are designed in this AMS-0.35 µm process*
      - ✓ $\varepsilon_{eff} > 99.5\%$, $\sigma < 4$ µm
    - *1st CPS based VX detector at a collider experiment*

- *Quadruple well process (deep P-well): 0.18 µm*
  - *N-well used to host PMOS transistors is shielded by deep P-well*
  - *Both types of transistors can be used*

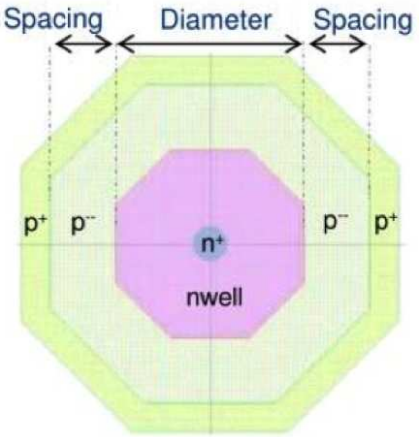


  - *Widens choice of readout architecture strategies*
    - *Ex. ALICE ITS upgrade: 2 sensors R&D in // using TOWER CIS 0.18 µm process (quadruple well)*
      - *Synchronous Readout R&D:*
        - ✓ *proven architecture = safety*
      - *Asynchronous Readout R&D: challenging*

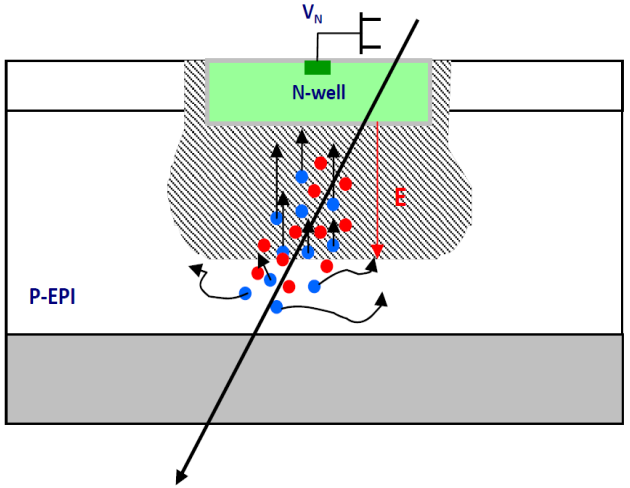


Sensing Node & VFEE Optimisation

- **General remarks on sensing diode :**
  - should be small because : $V_{signal} = Q_{coll}/C$; Noise $\sim$ C ; $G_{PA} \sim 1/C$
  - BUT should not be too small since $Q_{coll} \sim$ CCE (important against NI irradiation)



- **General remarks on pre-amplifier** connected to sensing diode :
  - should offer high enough gain to mitigate downstream noise contributions
  - should feature input transistor with minimal noise (incl. RTS)
  - should be very close to sensing diode (minimise line C)

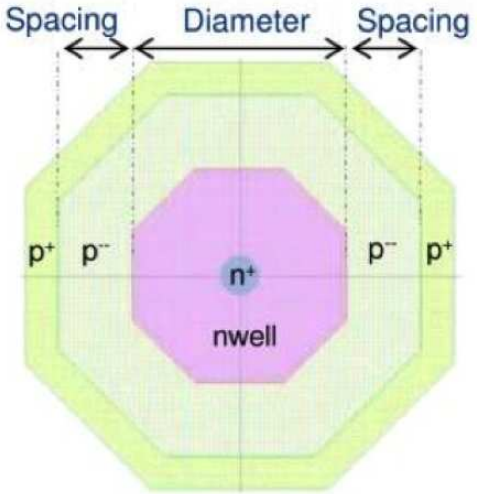


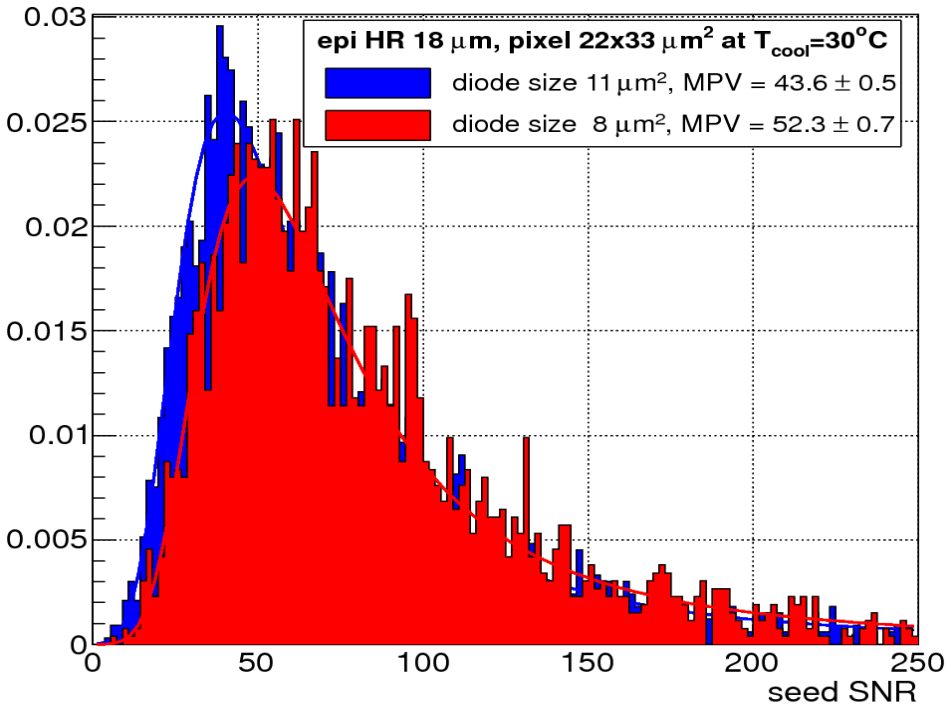
- **General remarks on depletion voltage :**
  - apply highest possible voltage on sensing diode
    preserving charge sharing $\mapsto \sigma_{sp}$
  - alternative : backside/reverse biasing

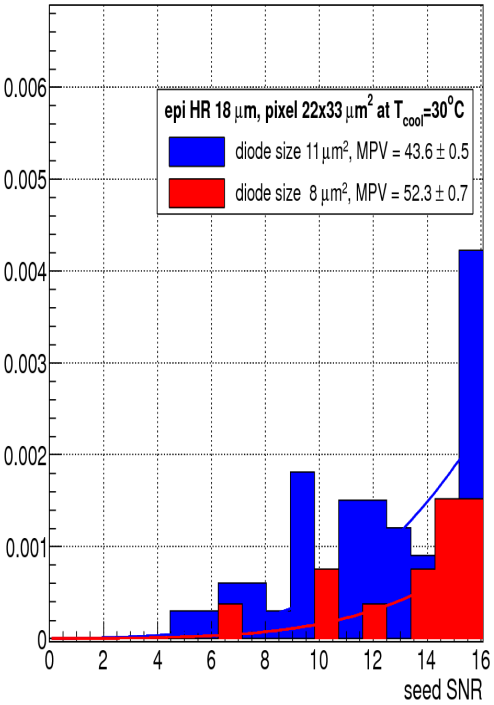
$\Rightarrow$ **Multiparametric trade-off to be found,**
based on exploratory prototypes rather than on simulations

Charge Sensing Element ⟼ Optimal SNR

- **Influence of sensing diode area**





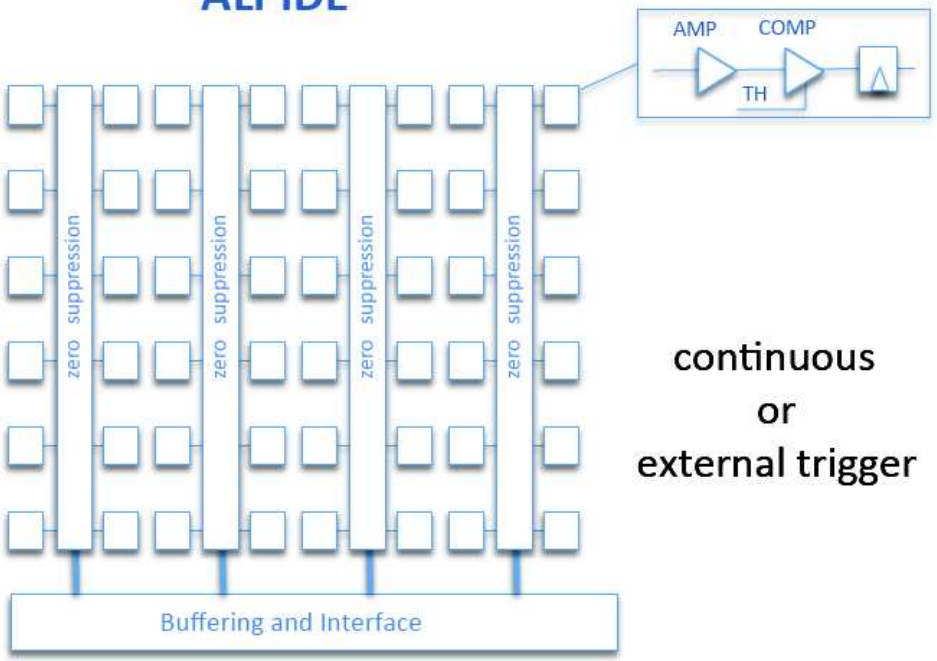


- **Benefit from reducing the sensing diode area**
  - sensing diode cross-section varied from 10.9 μm^2 to 8 μm^2 underneath 10.9 μm^2 large footprint

    ↪ suppresses low SNR tail ⟼ enhances detection efficiency (and mitigates effect of fake rate)

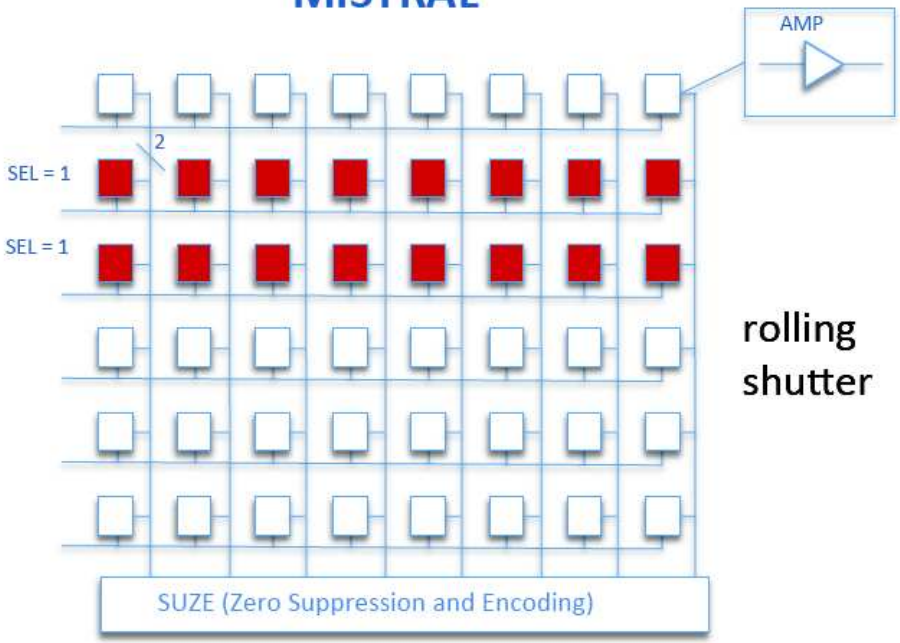
ITS Pixel Chip – two architectures

ALPIDE



continuous
or
external trigger

MISTRAL



rolling
shutter

Pixel pitch	28μm x 28μm
Event time resolution	~2μs
Power consumption	39mW/cm^2
Dead area	1.1 mmx30mm

Pixel pitch	36μm x 64μm
Event time resolution	~20μs
Power consumption$^{(*)}$	97mW/cm^2
Dead area	1.7 mm x 30mm

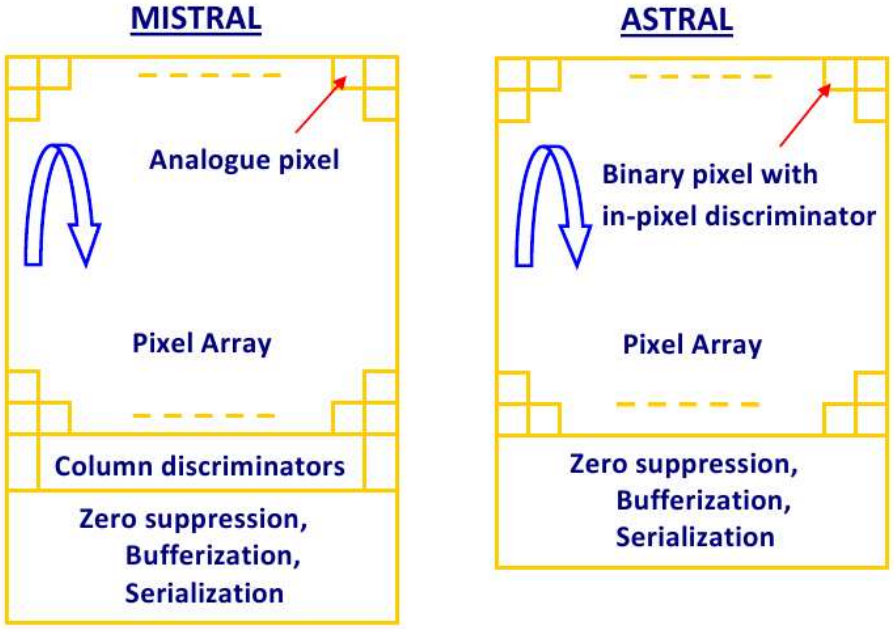
ALPIDE and MISTRAL-O have same dimensions (15mm x 30mm), identical physical and electrical interfaces: position of interface pads, electrical signaling, protocol

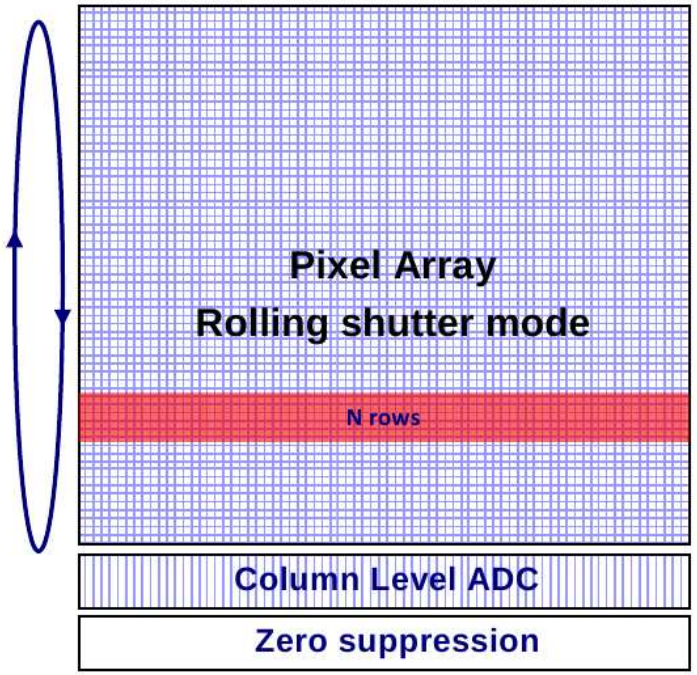
L. Musa
(LHCC 03/03/15)

$^{(*)}$ might further reduce to 73mW/cm^2

Synchronous Read-Out Architecture : Rolling Shutter Mode

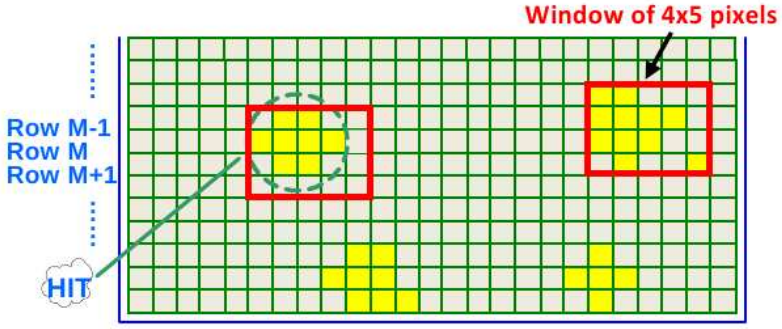
- *Design addresses 3 issues:*
  - *Increasing S/N at pixel-level*
  - *A to D Conversion: at column-level (MISTRAL)*
    at pixel-level (ASTRAL)
  - *Zero suppression (SUZE) at chip edge level*





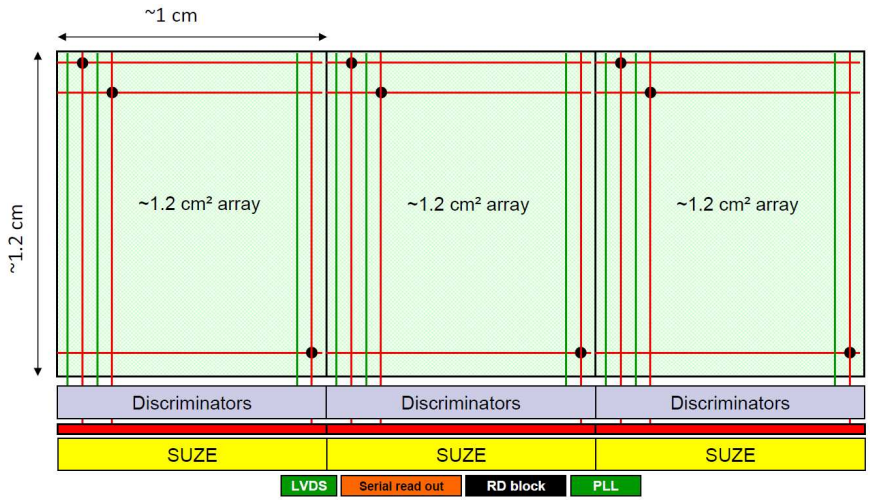
- *Power vs speed:*
  - *Power: only the selected rows (N=1, 2, …) to be read out*
  - *Speed: N rows of pixels are read out in //*
    - *Integration time = frame readout time*

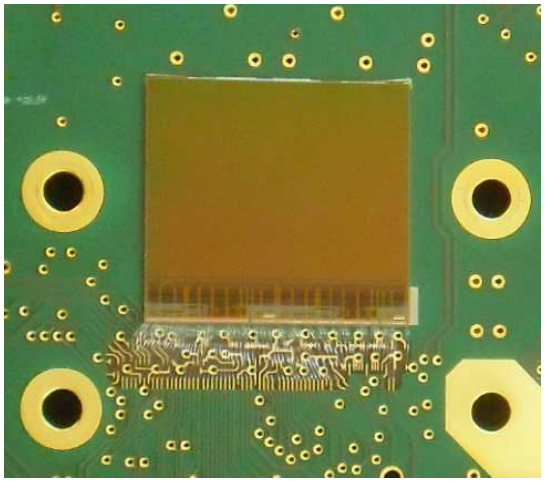
$$t_{\text{int}} = \frac{(\text{Row readout time}) \times (\text{No. of Rows})}{N}$$

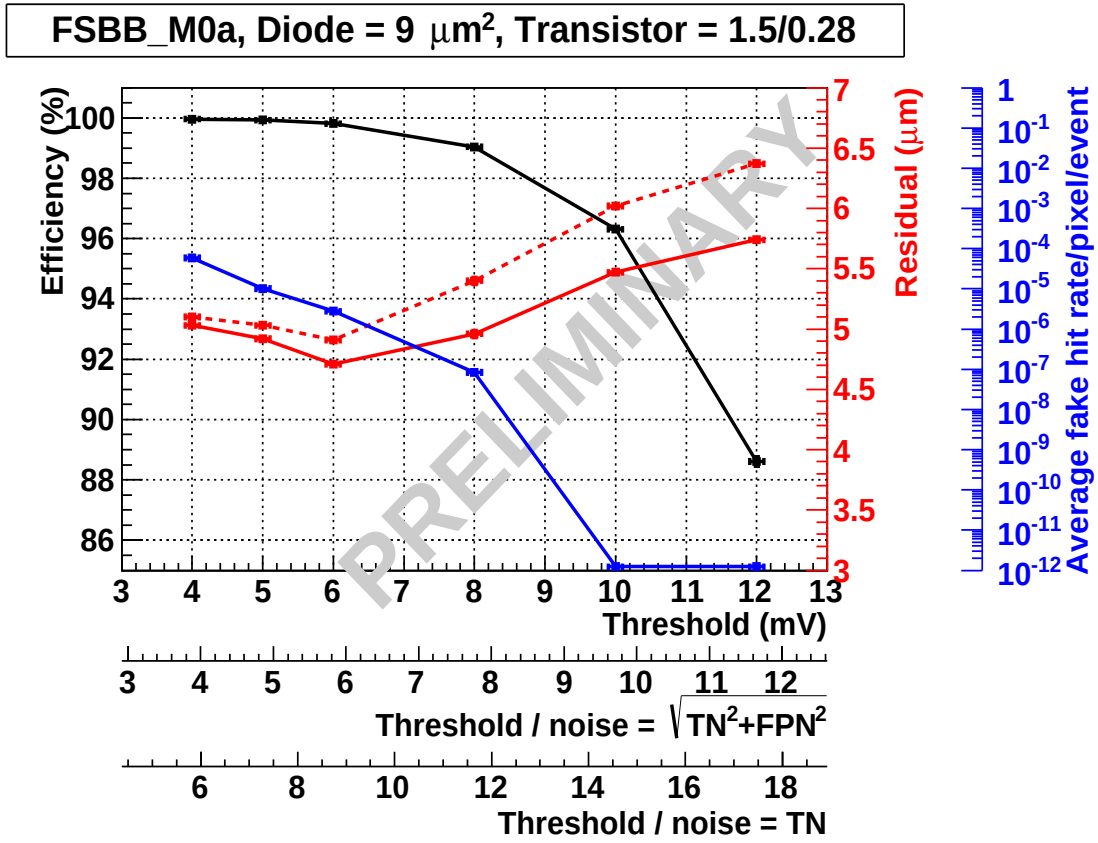


Detection Performances of MISTRAL Building Block

- ϵ_{det}, fake rate, σ_{res} vs Discriminator Threshold : Noise averaged over 11 thinned sensors







- **MISTRAL-O composed of 3-4 identical Full Scale Building Blocks operated in parallel & multiplexed at their outputs**
  (prototype pixel dim. : 22 x 33 μm^2)

- **Beam tests with a few GeV electrons (DESY)**

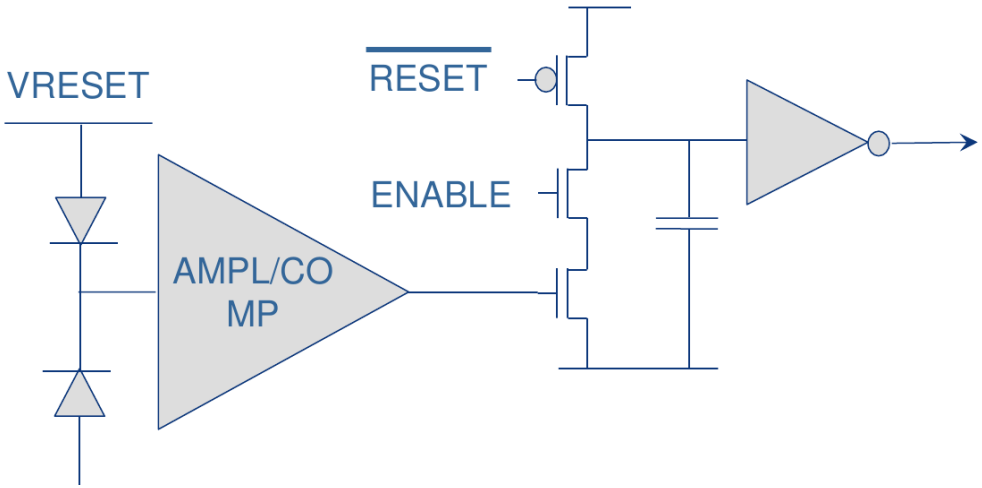
  ↪ **Valid threshold range ∼ 7–12 TN (T = 30°C)**

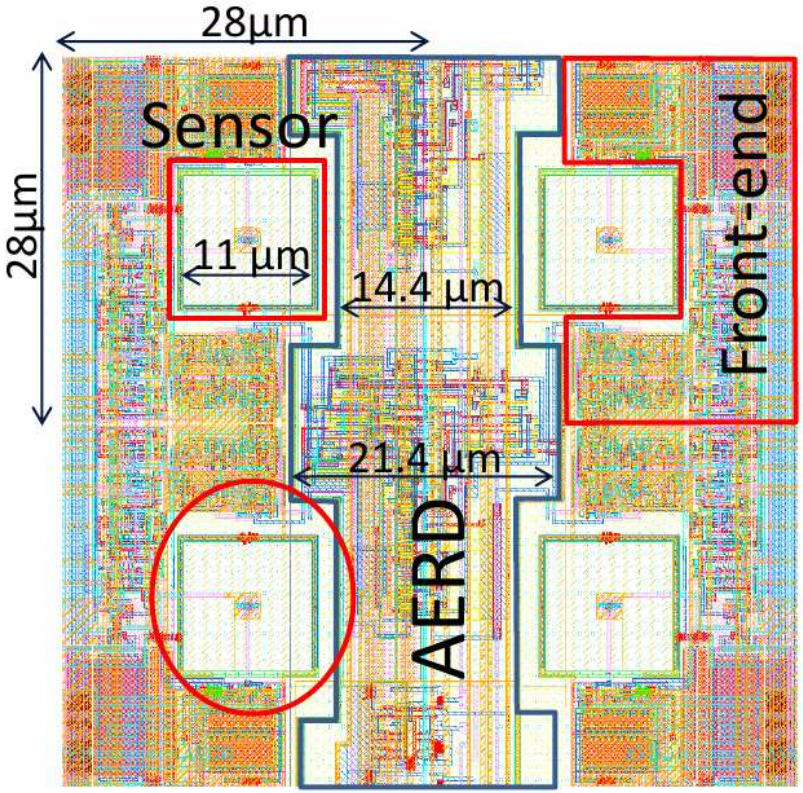
  - $\epsilon_{det} > 99\ \%$ and $\sigma_{sp} \lesssim 5\ \mu m$
  - Fake rate ($\equiv$ noise fluctuations) $< 10^{-5}$

Asynchronous Read-Out Architecture : ALPIDE (Alice PIxel DEtector)

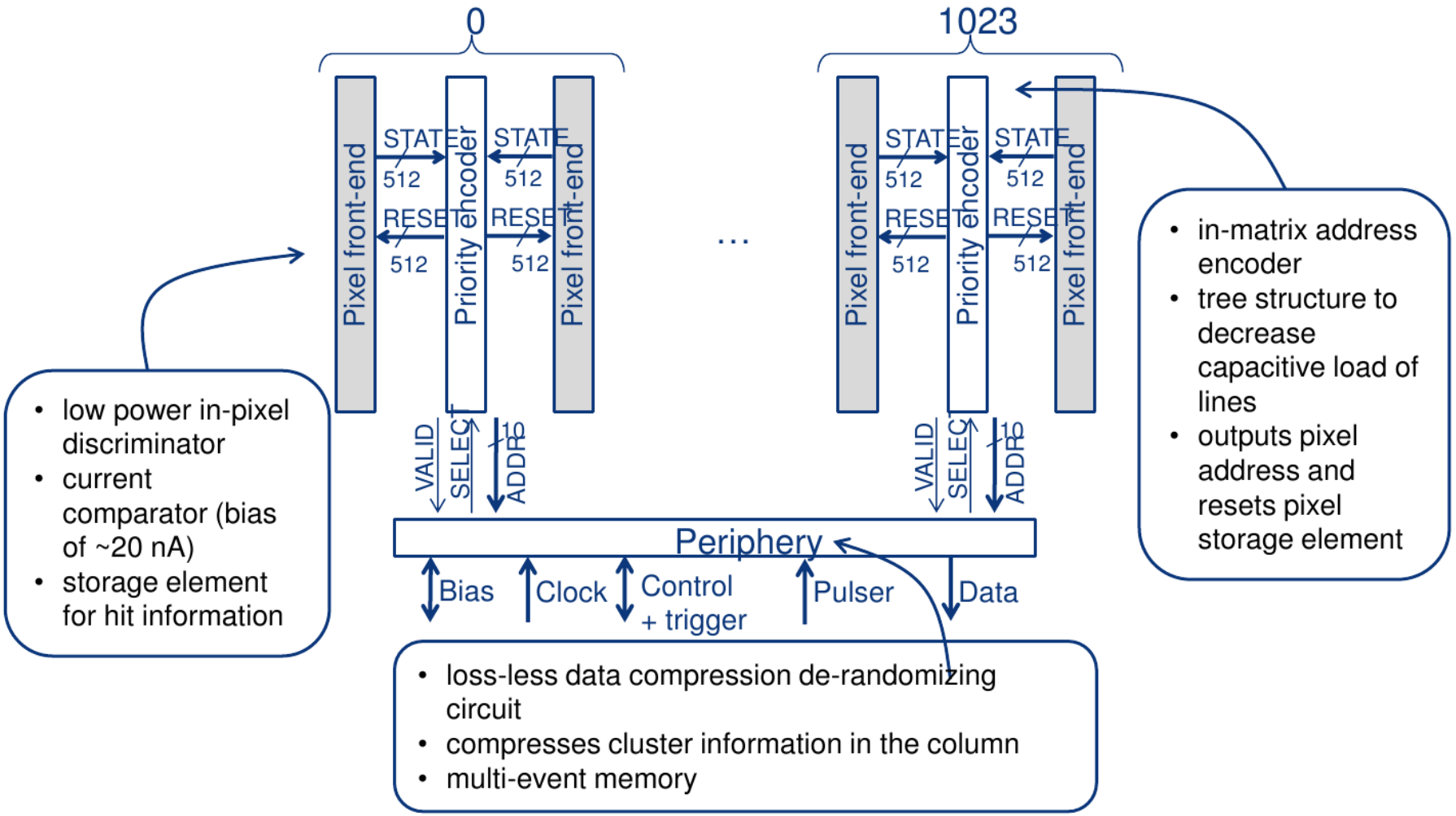
- **Design concept similar to hybrid pixel read-out architecture**
  exploiting availability of TJsc CIS quadruple well process : pixel hosts N- & P-MOS transistors

- **Each pixel features a continuously power active**
  - low power consumming analogue front end (P $<$ 50 nW/pixel)
    based on a single stage amplifier with shaping / current comparator
    - amplification gain $\sim$ 100
    - shaping time $\sim$ few μs
  - Data driven read-out of the pixel matrix
    $\Rrightarrow$ only zero-suppressed data are transfered to periphery



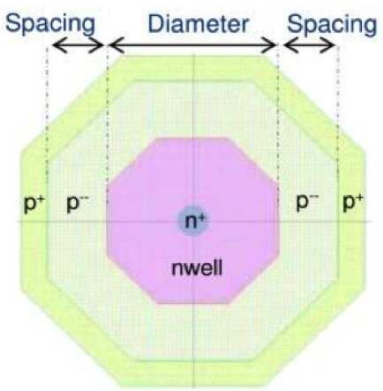


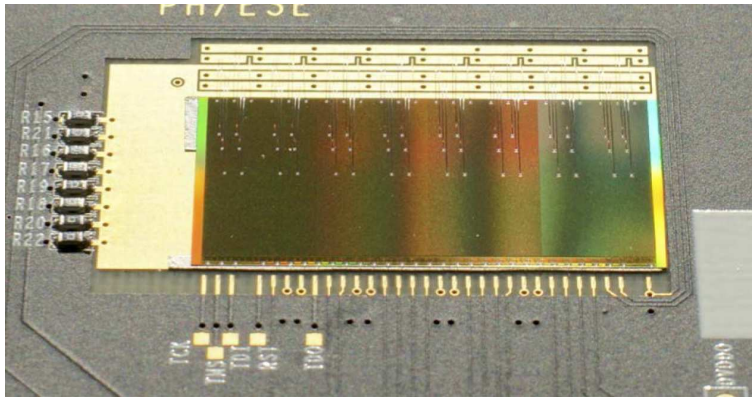
Asynchronous Read-Out Architecture : ALPIDE

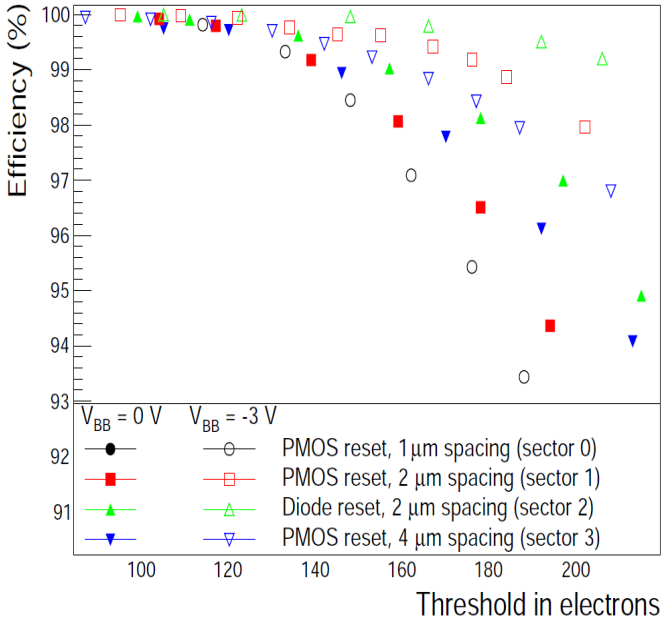


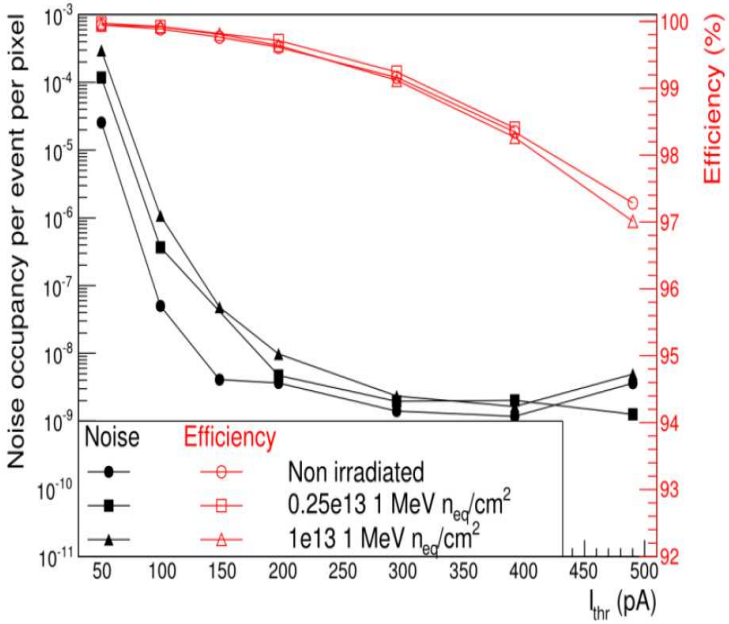
ALPIDE Detection Performance Assessment

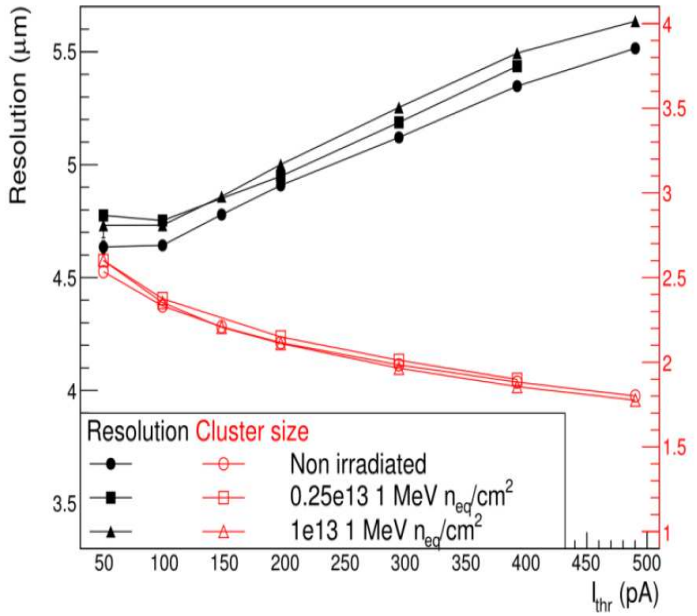
- **ALPIDE-1 beam tests (5–7 GeV pions) :**
  - Final sensor dimensions : 15 mm $\times$ 30 mm
  - About 0.5 M pixels of 28 $\mu m \times 28\ \mu m$
  - 4 different sensing node geometries
  - Possibility of reverse biasing the substrate
    - ↪ default : - 3 V
  - Possibility to mask pixels (fake rate mitigation)
    - ↪ default : $\lesssim$ O(10^{-3}) masked pixels





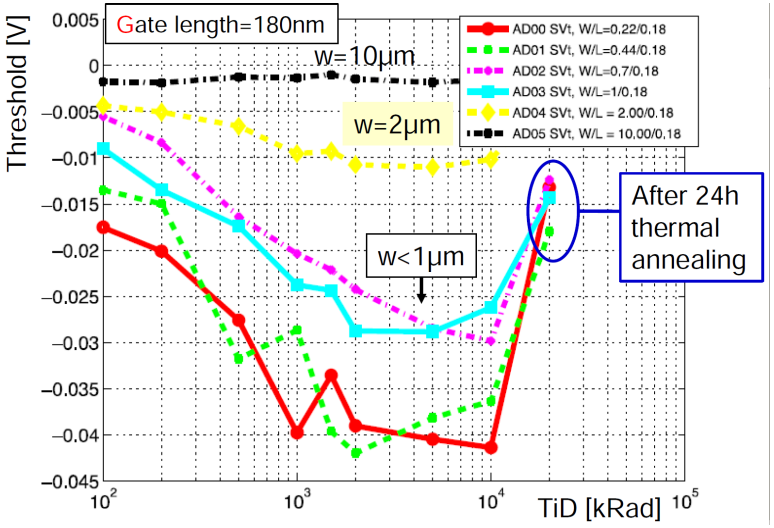




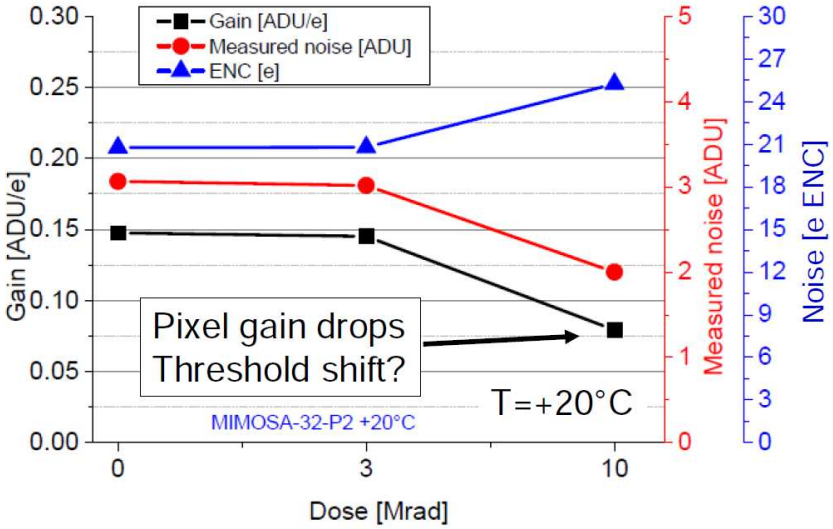


Tolerance to Ionising Radiation

- **Studies of 0.18 μm transistors exposed to TID $\geq$ 10 MRad**
  - measurements performed (+20°C) :
    leakage current & threshold shift
  - increase of leakage current remains small
  - threshold shifts remain small if W $\gtrsim 2\mu m$
    and are recoverable with thermal annealing



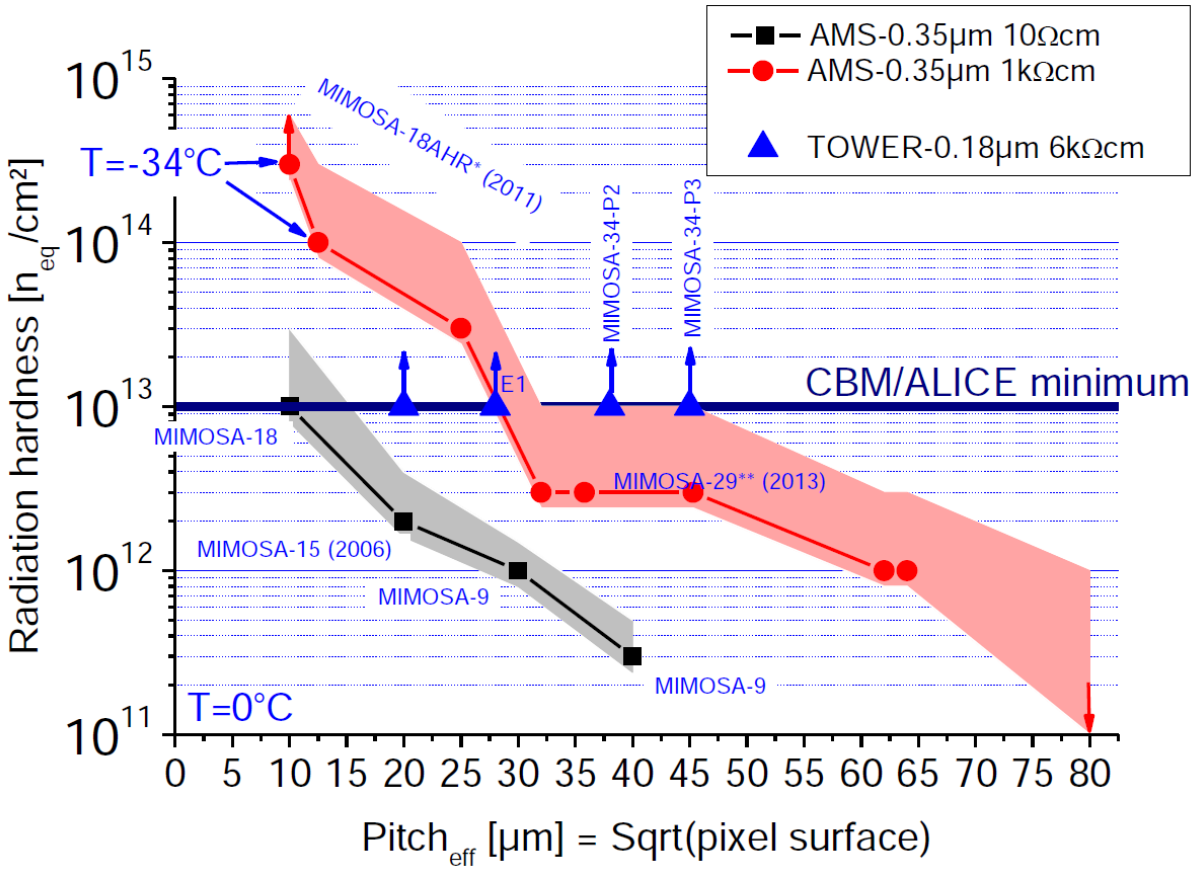
- **Studies of sensing node in 0.18 μm process at +20°C :**
  - Pixel gain drops $>$ 5 MRad (threshold shift ?)
    ↪ but SNR seems acceptable up to 10 MRad
  - Well known remedies seem efficient up to $\gtrsim$ 10 MRad :
    short integration time, low temperature, ELT with guard rings
  - Potential pb : space available in high resolution pixels



Tolerance to Non-Ionising Radiation

- **Main parametres governing the tolerance to NI radiation :**
  - epitaxial layer : thickness and resistivity
  - sensing node : density, geometry, capacitance, depletion voltage
  - operating temperature
  - read-out integration time

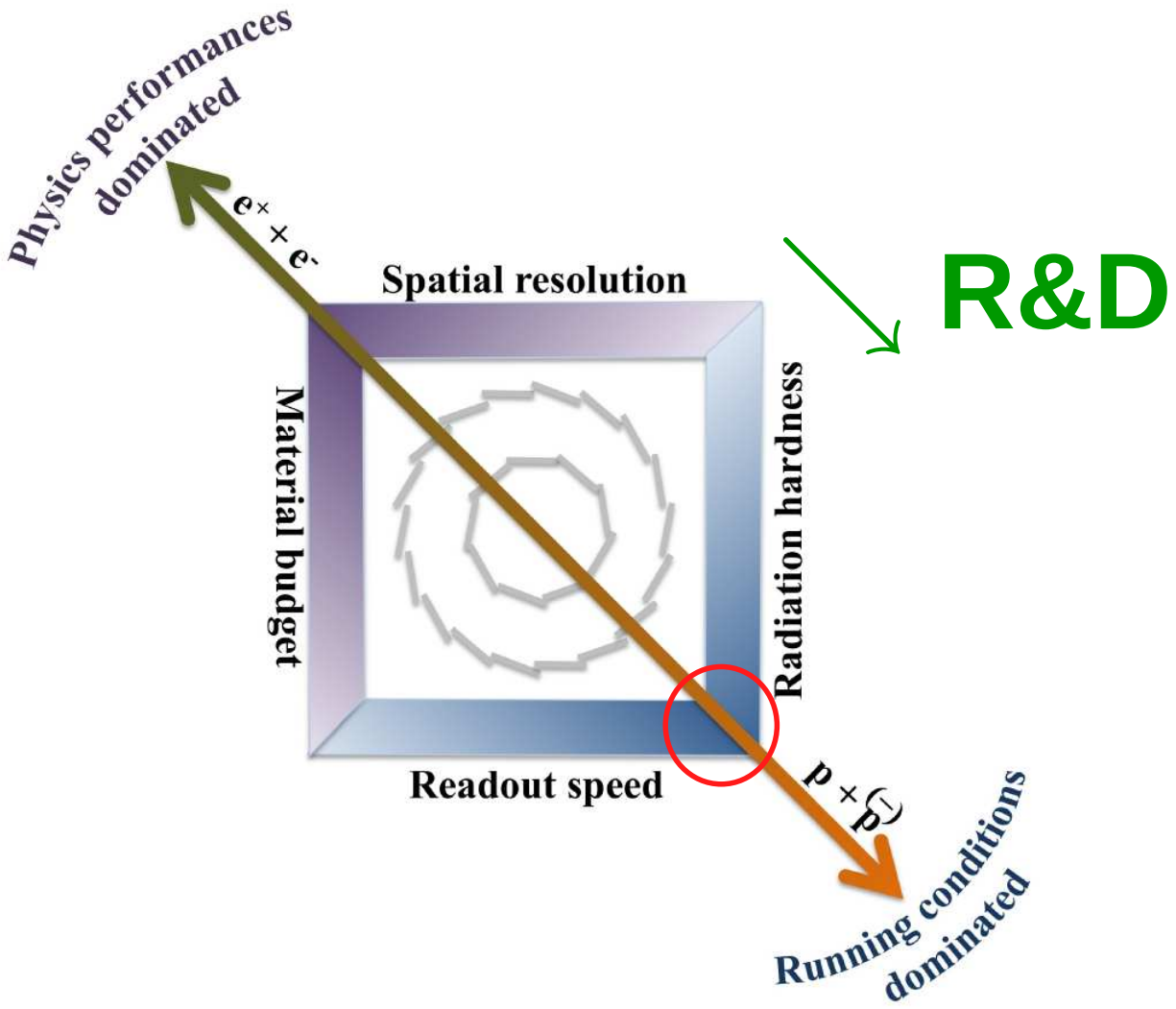
- **Most measurements performed with chips manufactured in two CMOS processes :**
  - 0.35 μm with low & high resistivity epitaxy
  - 0.18 μm with high & resistivity epitaxy (mainly 18 & 20 μm thick)



- **Clear improvement with 0.18 μm process w.r.t. 0.35 μm process**
  - ALICE-ITS requirement seems fulfiled : 700 kRad & $10^{13} n_{eq}/cm^2$ at T = +30°C
  - Fluences in excess of $10^{14} n_{eq}/cm^2$ seem within reach
    - $\Rightarrow$ requires global optimisation of design & running parametres

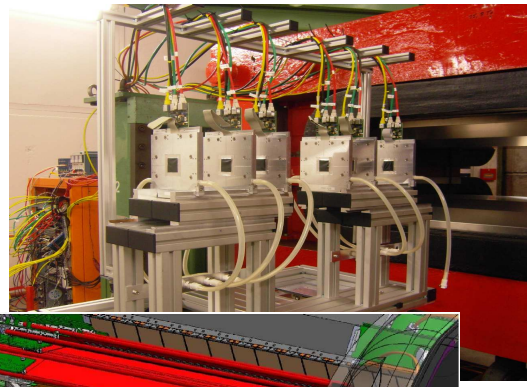
Forthcoming Challenges

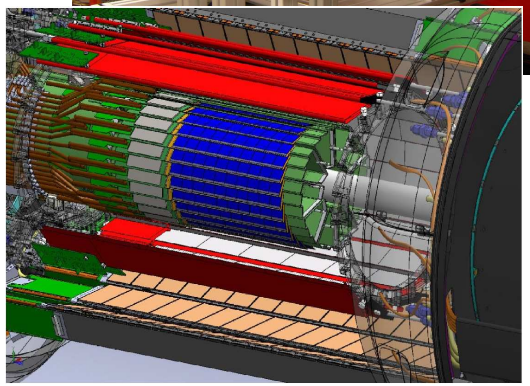
How to reach the bottom right corner of the ”Quadrature” ?



Improving Speed and Radiation Tolerance

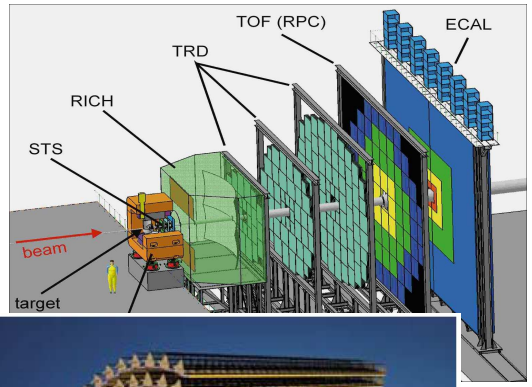
O(10^2) μs

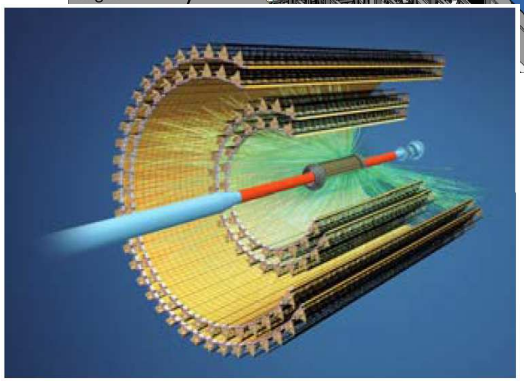




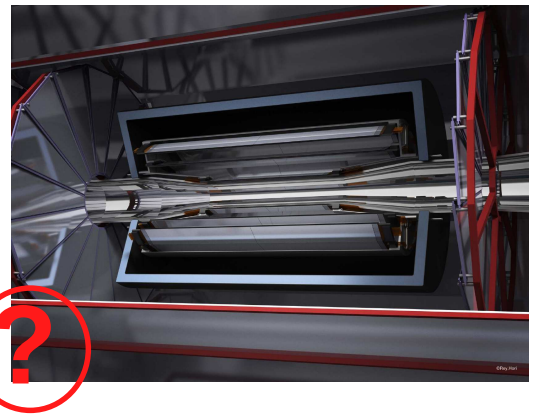
How to improve speed & radiation tolerance while preserving 3-5μm precision & $< 0.1\%\ X_0$?

O(10) μs





O(1) μs



?

EUDET/STAR ⟶ **ALICE/CBM** ⟶ **?X?/ILC**

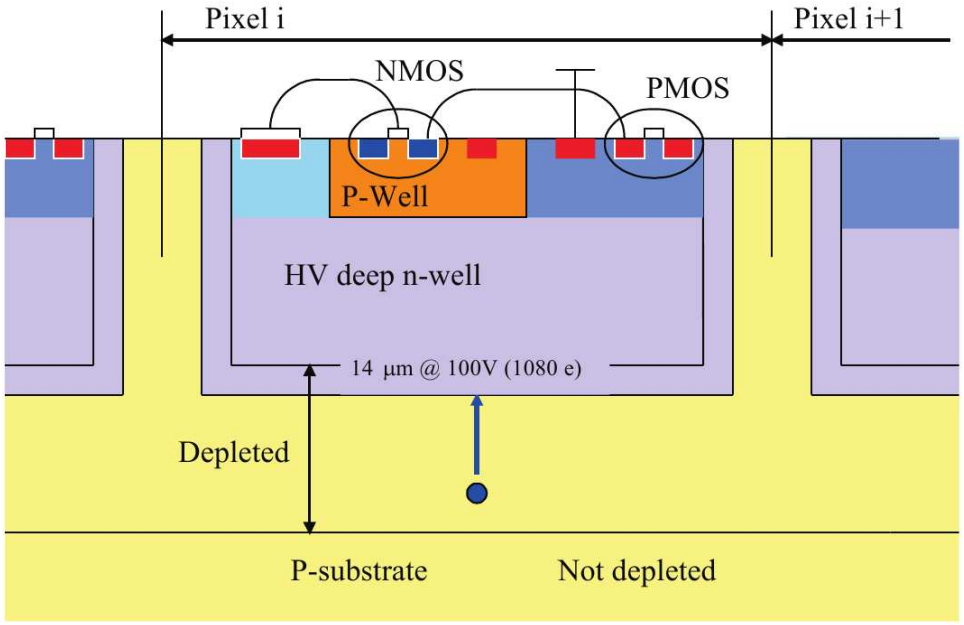
2010/14 ⟶ 2015/2019 ⟶ $\gtrsim$ 2020

Further Perspectives of Performance Improvement

- **Expected added value of HV-CMOS :**
  - Benefits from extended sensitive volume depletion :
    - faster charge collection
    - higher radiation tolerance
  - Not bound to CMOS processes using epitaxial wafers

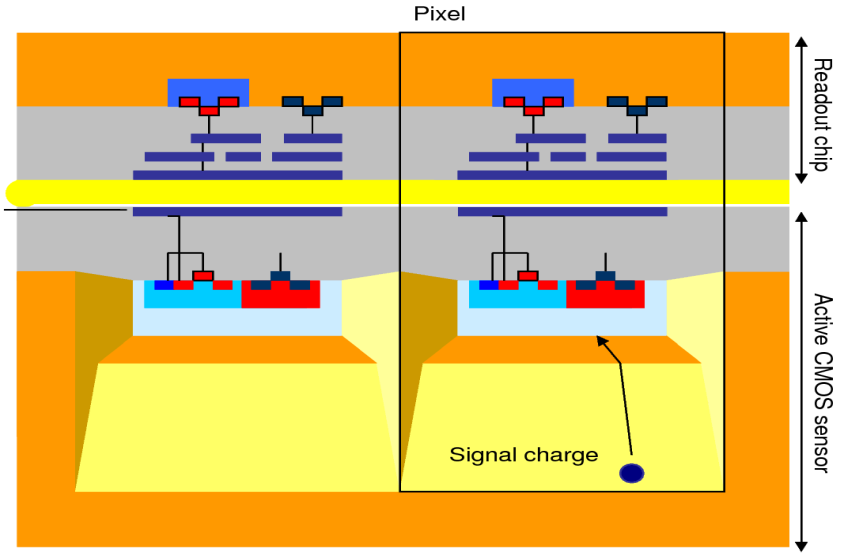
    ⇛ easier access to VDSM ($<$ 100 nm) processes

    ⇛ higher in-pixel micro-circuit density



- **Questions :**
  - minimal pixel dimensions vs $\sigma_{sp} \lesssim 3\ \mu m$?
  - uniformity of large pixel array, yield ?

- **Attractive possible evolution : 2-tier chips**
  - signal sensing & processing functionnalities distributed over 2 tiers interconnected at pixel level (capa. coupling)
  - combine 2 different CMOS processes if advantageous : 1 optimal for sensing, 1 optimal for signal processing
  - benefit : small pixel ⟼ resolution, fast response, data compression, robustness ?
  - challenge : interconnection technology (reliability, cost, ...)



CONCLUSION

- **CPS have demonstrated that they can provide the spatial resolution and material budget required for numerous applications**

- **CPS are suited for vertex detectors ($\ll$ 1 m^2)**
  - $\hookrightarrow$ **attractive features for tracking devices ($\gg$ 1 m^2), incl. cost (!)**

- **Forthcoming & Upcoming challenges :**
  - **Large active area :** ALICE-ITS $\equiv$ 10 m^2 to cover with 20-30,ooo sensors
  - **Radiation tolerance :** $\gtrsim$ 10 MRad & $\gtrsim$ 10^{14} n_{eq}/cm^2 (e.g. CBM at SIS-300)
  - **Read-out speed :** $\lesssim$ 1 μs (e.g. ILC vertex detector & tracker)

- **Perspectives :**
  - HV-CPS but exposed to challenges if small pixels and very low power consumption are required
    - $\hookrightarrow$ VDSM processes ?
  - 2-tier sensors $\equiv$ (sensing + ampli) $\oplus$ (sparsification + data transfer)
    combining 2 CMOS processes at pixel level
    - $\hookrightarrow$ still an R&D ...

CMOS Pixel Sensors (CPS): A Long Term R&D

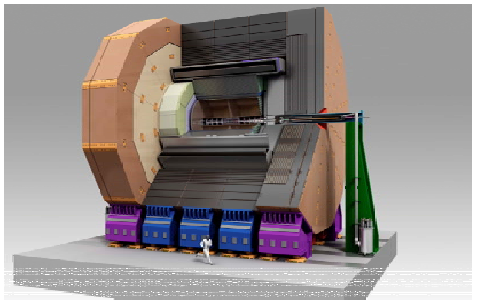
- ***Ultimate objective: ILC, with staged performances***
  - *CPS applied to other experiments with intermediate requirements*

EUDET 2006/2010

Beam Telescope

ILC >2020

International Linear Collider



EUDET (R&D for ILC, EU project)

STAR (Heavy Ion physics)

CBM (Heavy Ion physics)

ILC (Particle physics)

HadronPhysics2 (generic R&D, EU project)

AIDA (generic R&D, EU project)

FIRST (Hadron therapy)

ALICE/LHC (Heavy Ion physics)

EIC (Hadron physics)

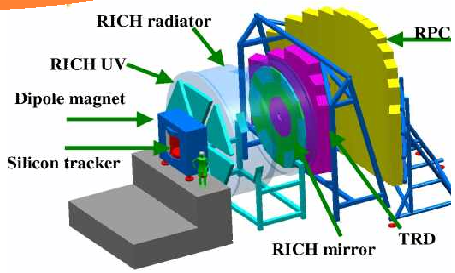
CLIC (Particle physics)

BESIII (Particle physics)

...

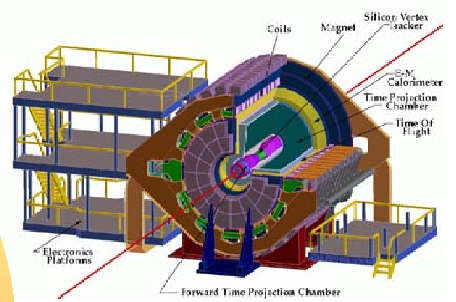
CBM >2018

Compressed Baryonic Matter



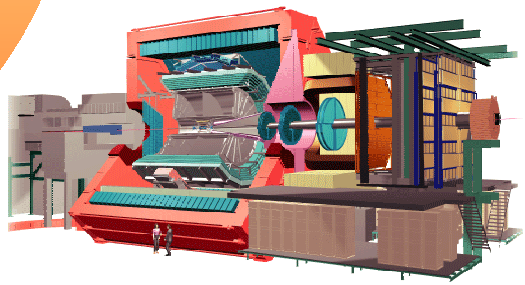
STAR 2013

Solenoidal Tracker at RHIC

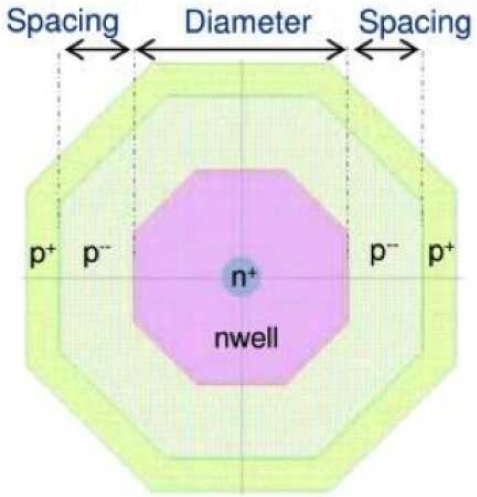


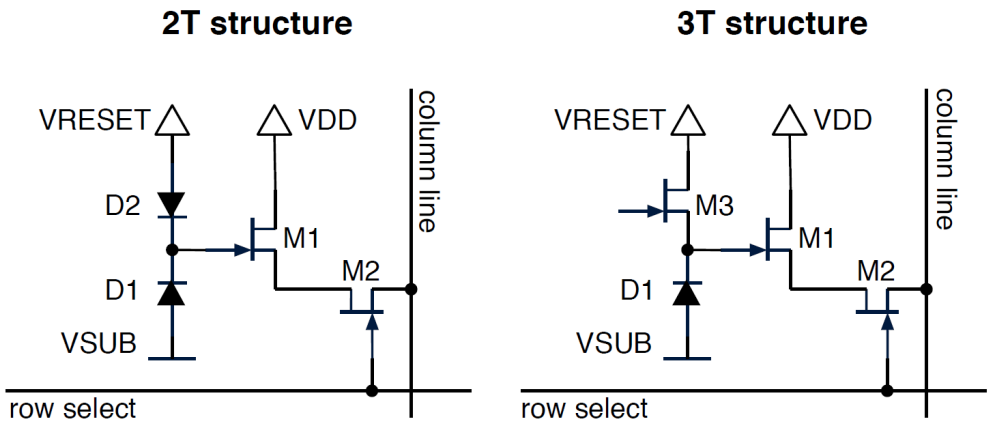
ALICE 2018

A Large Ion Collider Experiment



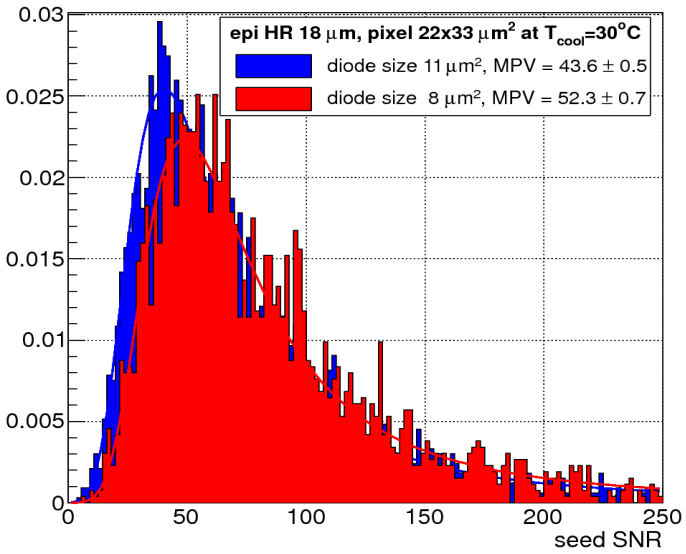
Charge Sensing Element ↦ Optimal SNR

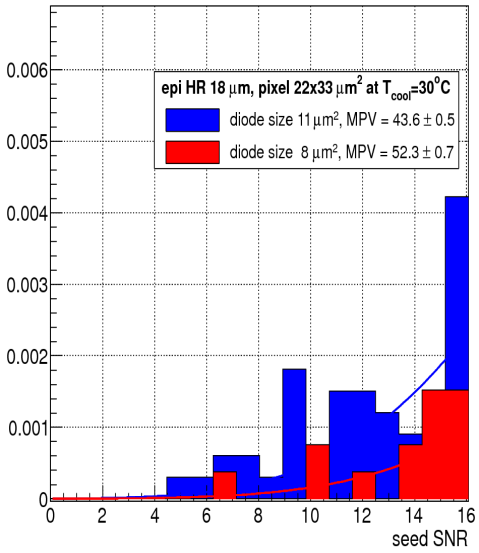




- **Influence of sensing diode area**
  - Optimum sensing diode geometry between
    - the smallest for the sake of C, N, G_{PA}
    - but not too small to preserve CCE (rad. tol.)
  - 10.9 μm^2 large sensing diode
  - 8 μm^2 cross-section sensing diode underneath 10.9 μm^2 large footprint

    ↪ Improves SNR ↦ Detection efficiency

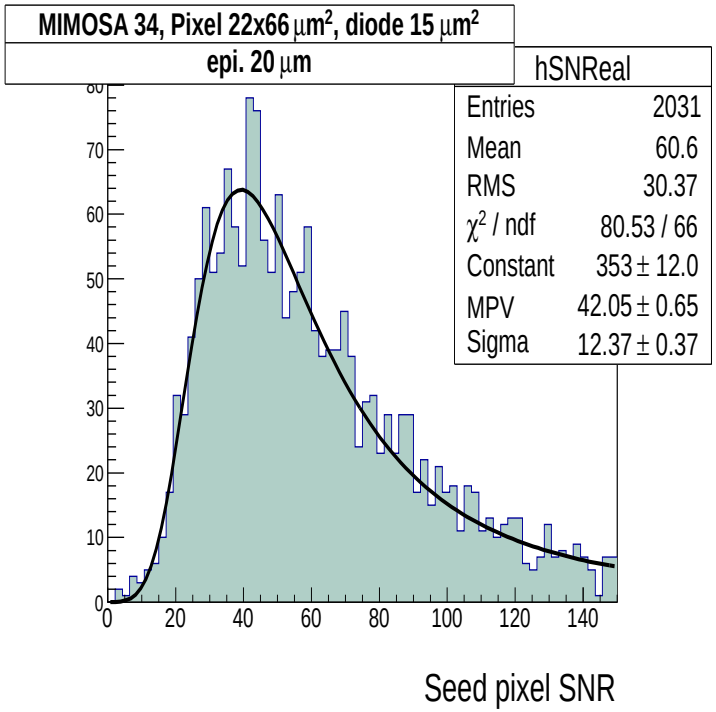


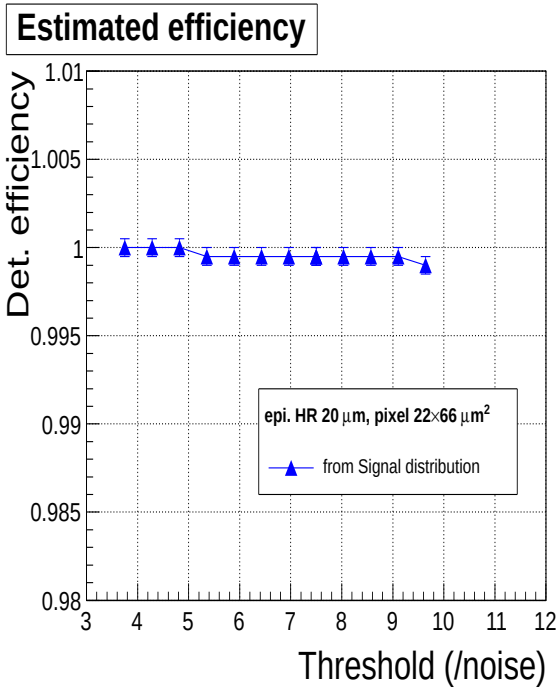


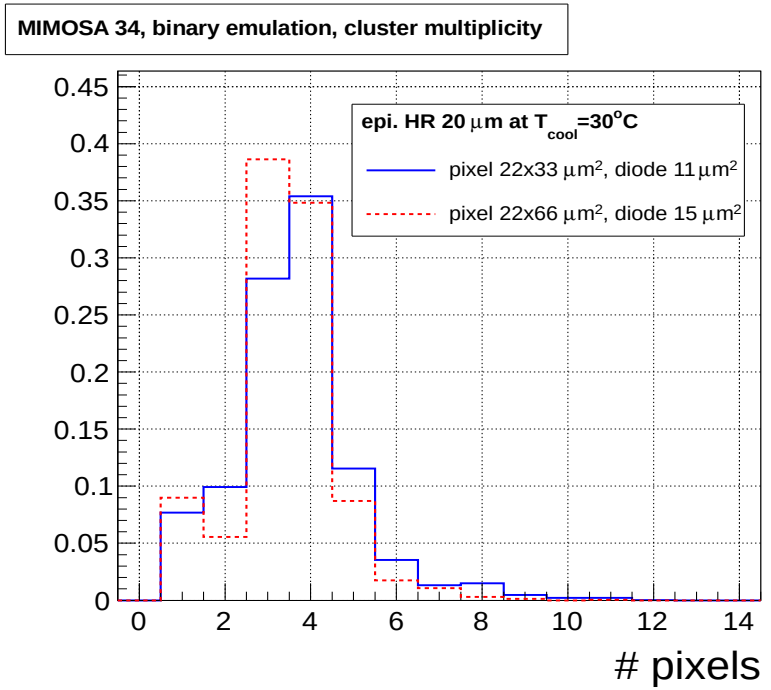
Large Pixels for Outer Layers ?

- **Motivation for LARGE pixels :** reduced power (& read-out time) in case of alleviated spatial resolution requirement

  ↪ adequate for L3-6 (also required rad. tol. alleviated)







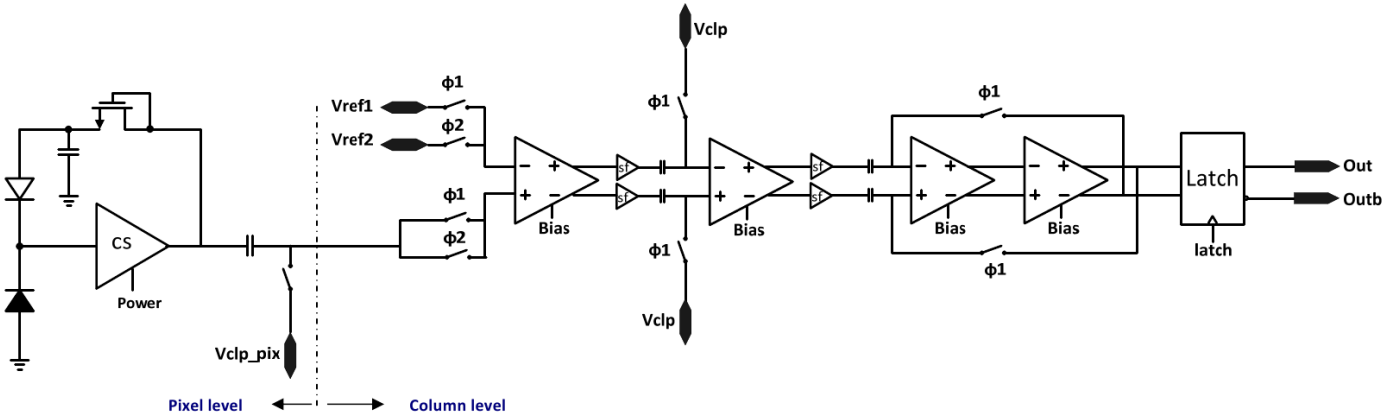
- **Difficulty :** keep high CCE (all over the pixel) without substantial (capacitive) noise increase and gain loss

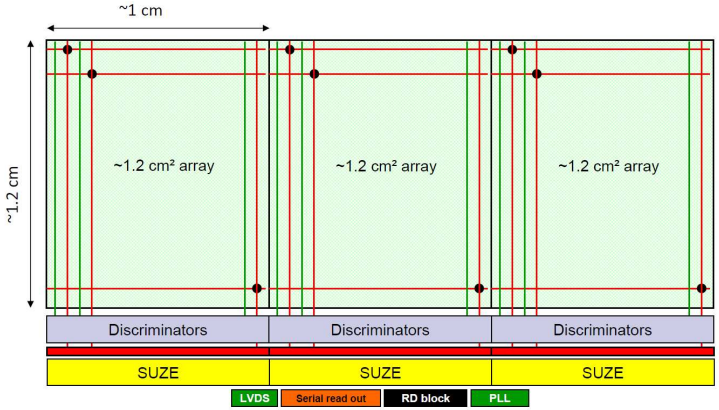
- **Results :** tests with 4.4 GeV electrons, no in-pixel CDS

  - SNR(MPV) $\simeq 42.1 \pm 0.7 \Rightarrow \quad \epsilon_{det} \simeq 100$ %
  - cluster multiplicity (22×66) $\simeq$ cluster multiplicity (22×33) $\simeq$ 3 (mean)

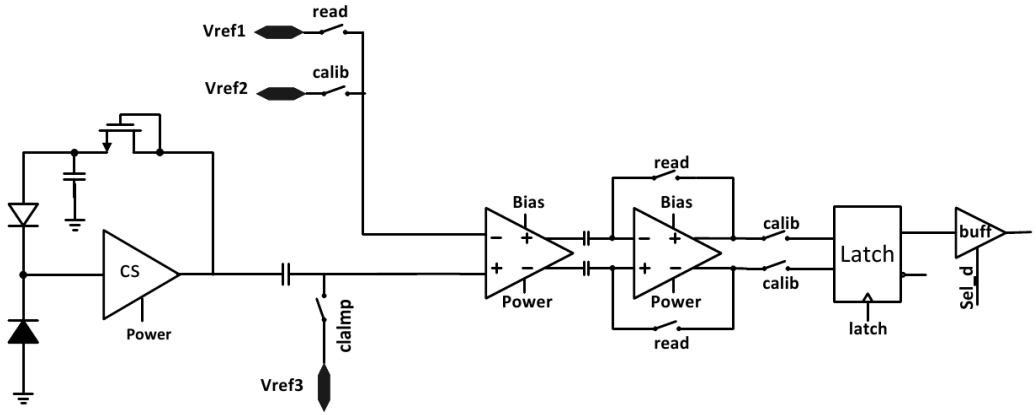
MISTRAL & ASTRAL : Schematics & Layouts

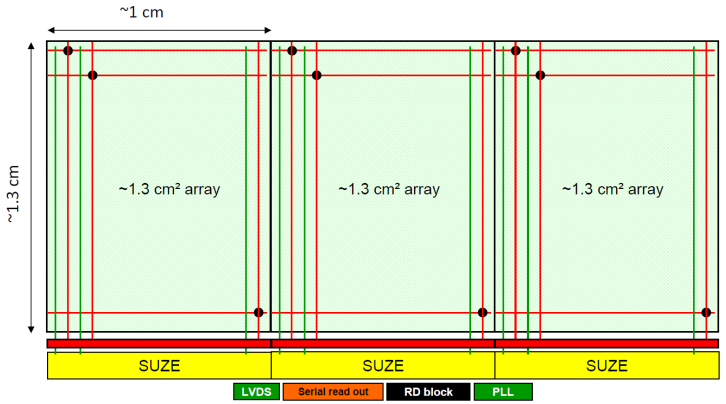
- **MISTRAL :** rolling shutter with 2-row read-out **& end-of column discriminators**





- **ASTRAL :** rolling shutter with 2-row read-out (≡ MISTRAL) **& in-pixel discriminators**



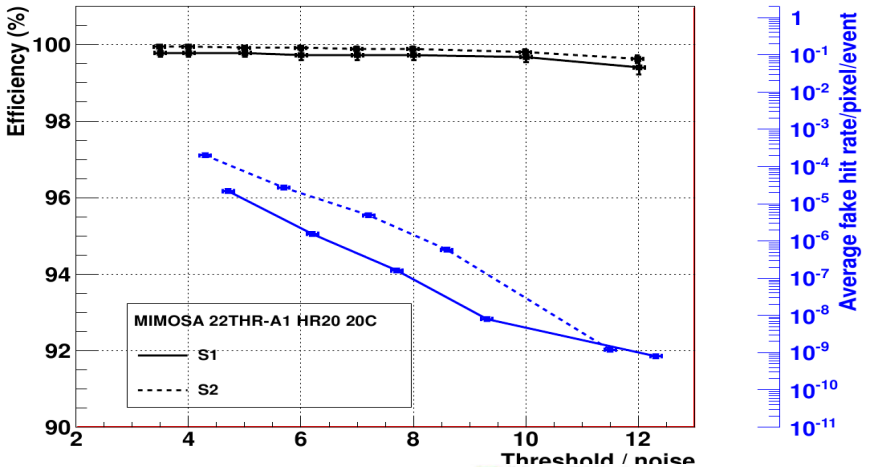


- **1st Full Scale Building Blocks (FSBB) fab. in Spring ’14 ⟼ FSBB-M0 tests ± completed**

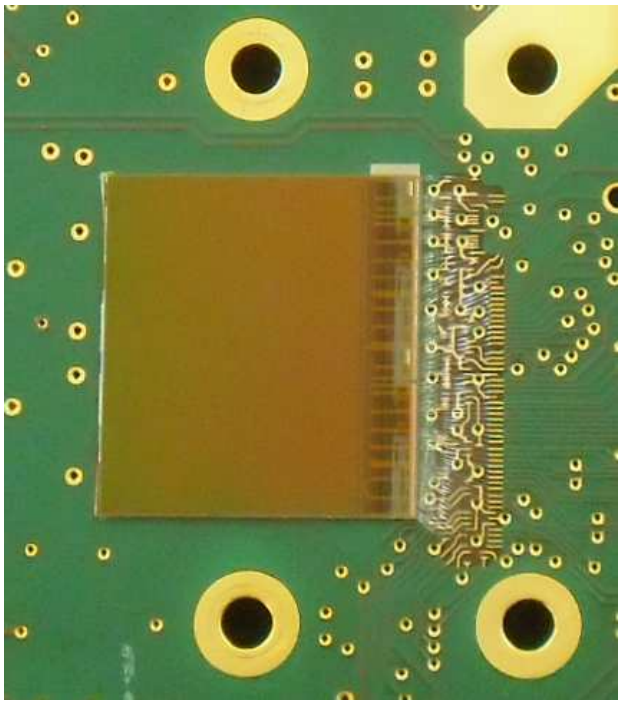
MISTRAL Architecture Validation

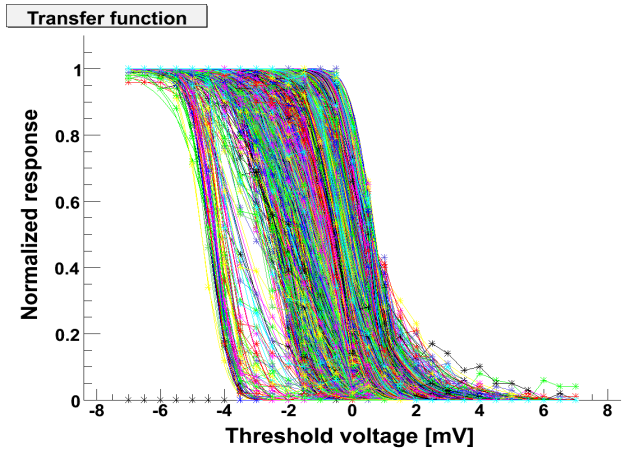
- **1st step : Separate validation of each element composing signal sensing & processing chain :**
  - Pixel array with 1-row read-out (1 discri./column)
  - Pixel array with 2-row read-out (2 discri./column)
  - Zero suppression circuitry with output buffers

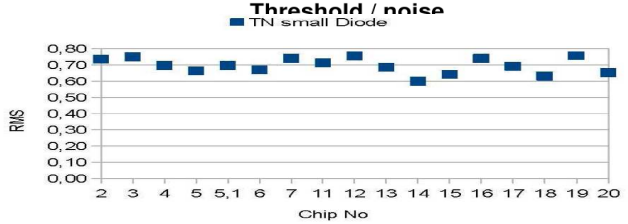
⟼

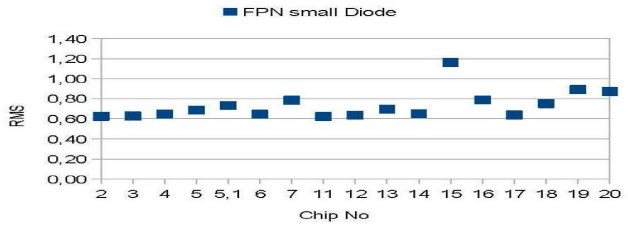


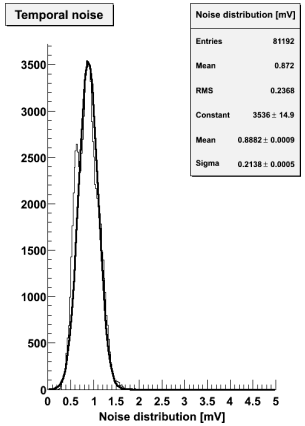
- **2nd step : FSBB-M**
  ≃ **1/3 of MISTRAL :**

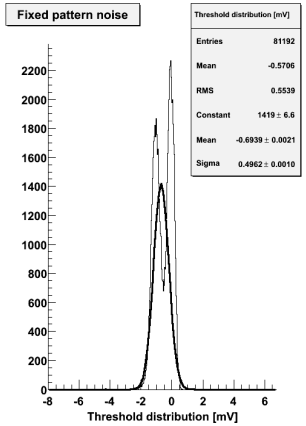










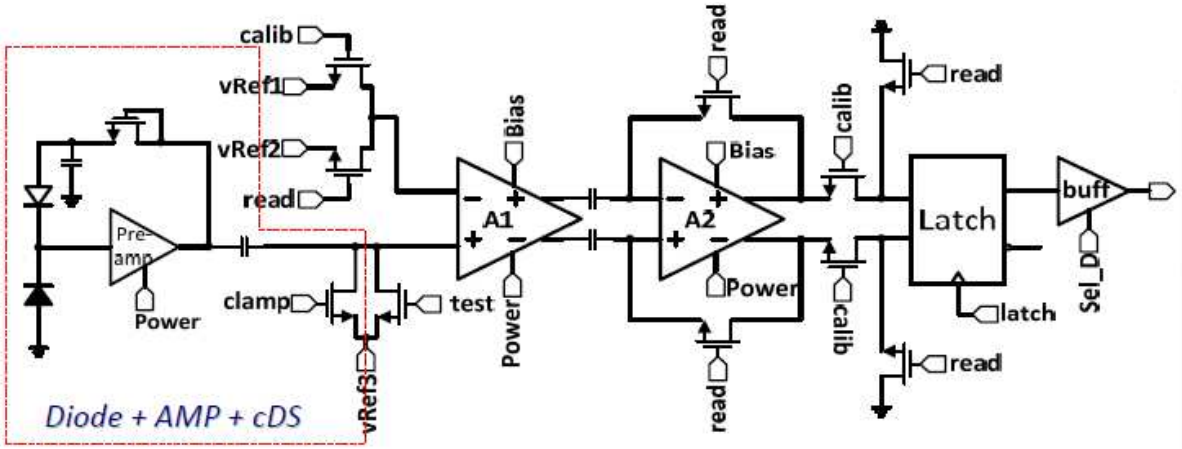


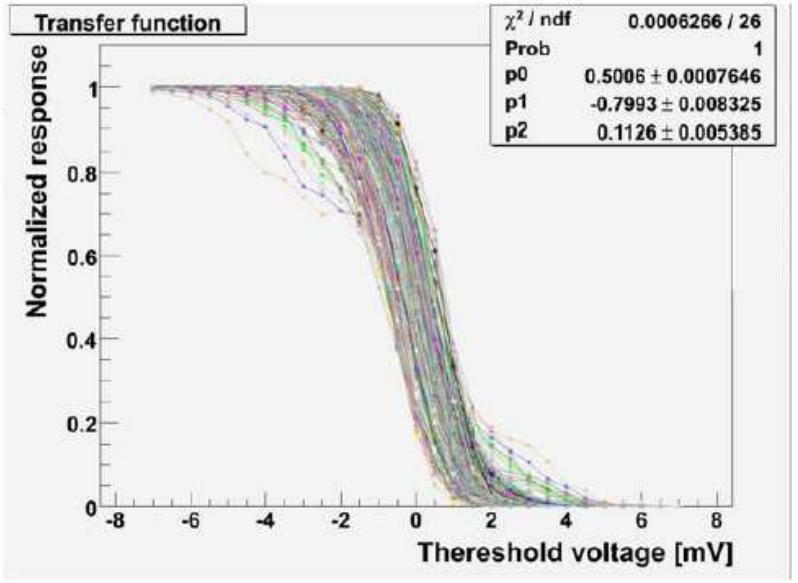
TN ≃ 0.87 mV FPN ≃ 0.55 mV

(total noise ≃ 15-20 e⁻ ENC)

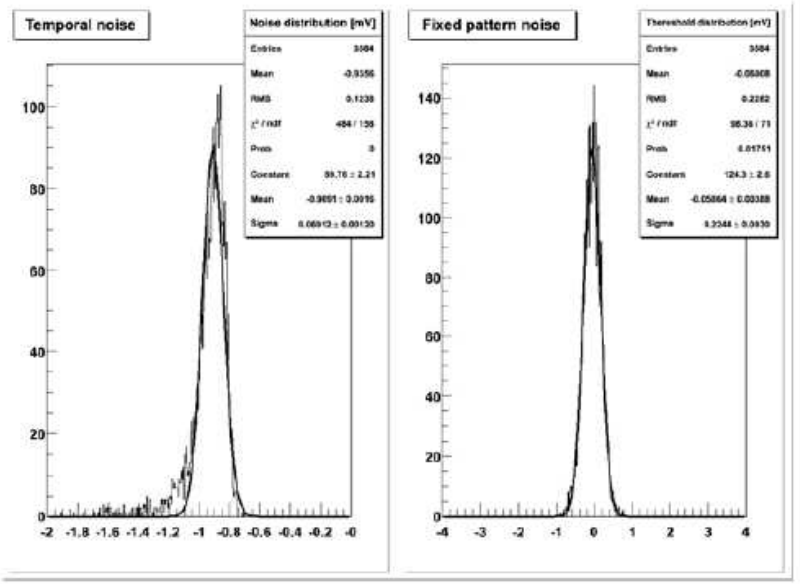
threshold		fake rate
4 mV	11870	1.4 10e-5
5 mV	3584	4.35 10e-6
6 mV	1092	1.32 10e-6
7 mV	406	4.96 10e-7
8 mV	236	2.86 10e-7

Synchronous Read-Out Architecture : In-Pixel Discrimination



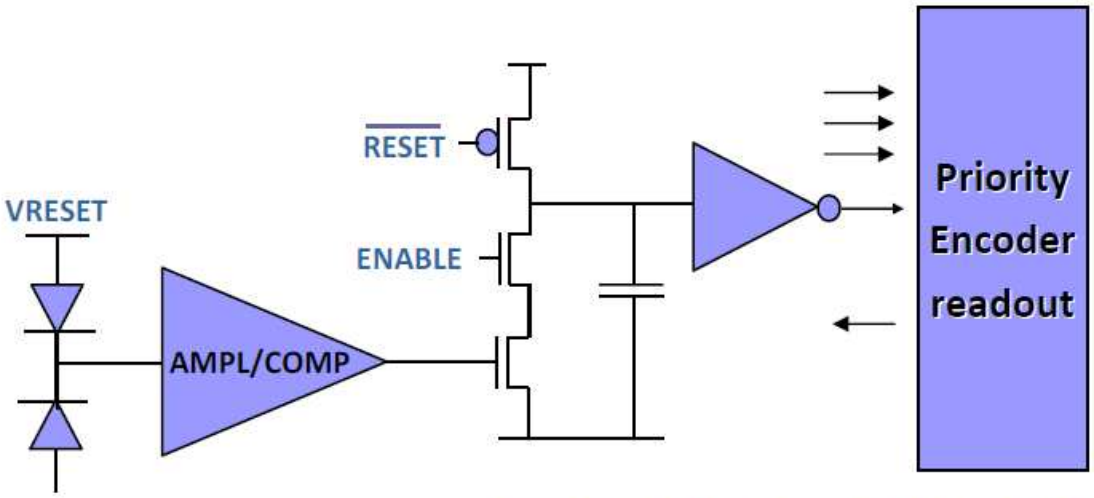


- *To provide adequate performance within small pixel*
  - *Structure selection: speed & power & offset mitigation vs area*
    - *Differential structure: preferable in mixed signal design*
    - *Two auto-zero amplifying stages + dynamic latch*
      - ✓ *OOS (Out Offset Storage) for the first stage and IOS (Input Offset Storage) for the second*
    - *Gain and power optimized amplifier*
  - *Very careful layout design to mitigate cross coupling effects*
  - *Conversion time: 100 ns; current: ~14 µA/discriminator*
- *Test results of in-pixel discriminator:*
  - *Discriminators alone: TN ~ 0.29 mV, FPN ~ 0.19 mV*
  - *Discriminators + FEE: TN ~ 0.94 mV, FPN ~ 0.23 mV*

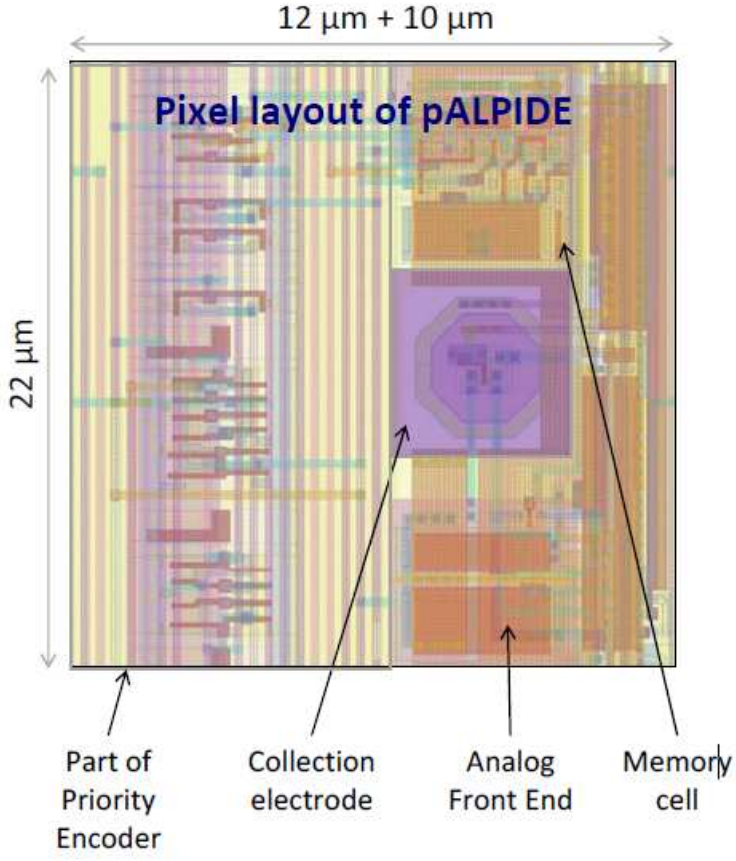


Asynchronous Read-Out Architecture : ALPIDE (Alice PIxel DEtector)

- *Design concept similar to hybrid pixel readout architecture thanks to availability of Tower CIS quadruple well process: both N & P MOS can be used in a pixel*
- *Each pixel features a continuously power active:*
  - *Low power consumption analogue front end (Power < 50 nW/pixel) based on a single stage amplifier with shaping / current comparator*
    - *High gain ~100*
    - *Shaping time few µs*
  - *Dynamic Memory Cell, ~80 fF storage capacitor which is discharged by an NMOS controlled by the Front-End*
- *Data driven readout of the pixel matrix, only zero-suppressed data are transferred to the periphery*

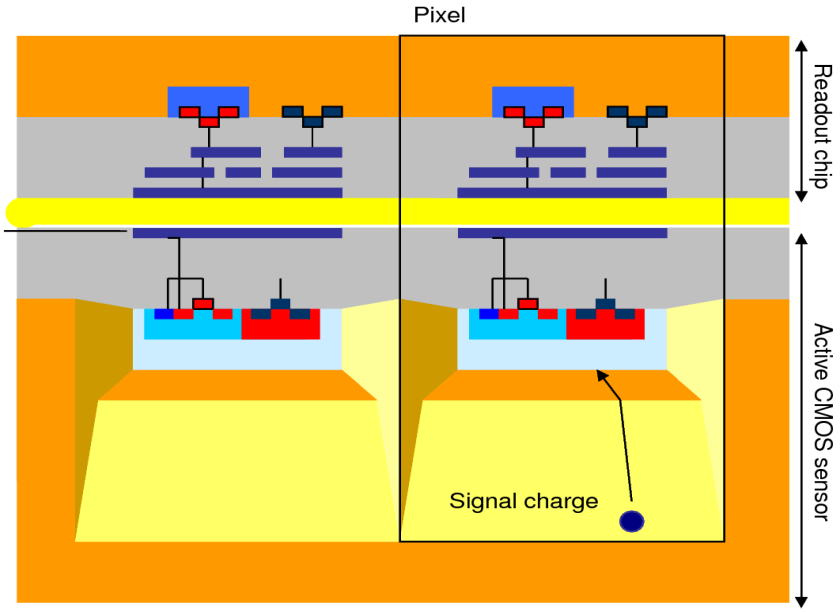


Courtesy of W. Snoeys / TWEPP-2013



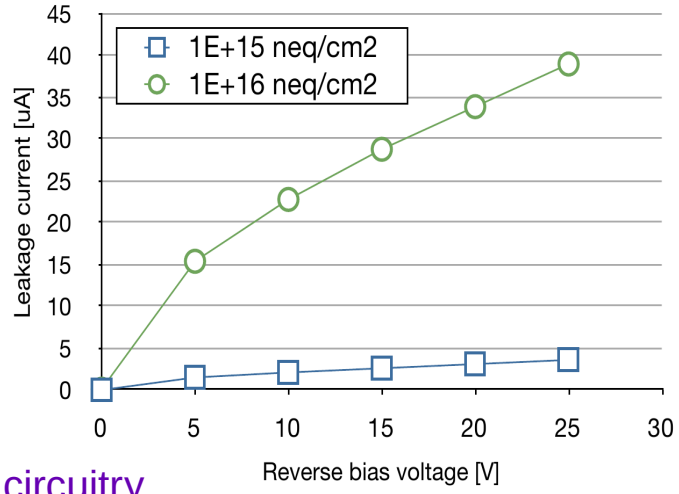
Perspectives : 2-Tier HV-CPS

- **Attractive possible evolution : 2-tier chips**
  - signal sensing & processing functionnalities distributed over 2 tiers interconnected at pixel level (capa. coupling)
  - combine 2 different CMOS processes if advantageous : 1 optimal for sensing, 1 optimal for signal processing
  - benefit : small pixel ⟼ resolution, fast response, data compression, robustness ?
  - challenge : interconnection technology (reliability, cost, ...)



Ivan Peric: CPIX14, Bonn, 2014

- **On-going R&D : ATLAS upgrade for HL-LHC**
  - HV2FEI4 chip ≡ sensitive HV-CPS tier (180 nm process) interconnected to FEI4 ROC (130 nm process)
  - radiation tolerance test results encouraging, threshold dispersion ?
  - promising perspective : high-resistivity EPI (≅ ALICE-ITS)



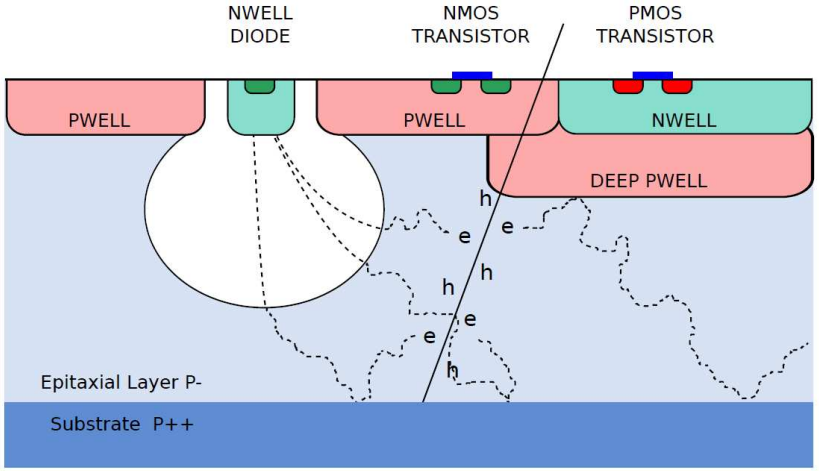
- **Other applications envisaged/foreseen :**
  - ATLAS strip like read-out
  - CLIC vertex detector
  - Mu3e experiment : analog pixel read-out with remote signal processing circuitry

Boundaries of the CPS Development

- **New fabrication process :**
  - Expected to be radiation tolerant enough
  - Expected to allow for fast enough read-out
  - Larger reticule ($\lesssim$ 25 mm $\times$ 32 mm)

STAR-PXL	**ALICE-ITS**	added-value
0.35 μm	**0.18** μm	speed, TID, power
4 ML	6 ML	speed. power
twin-well	quadruple-well	speed, power
EPI 14/20 μm	EPI 18/40 μm	SNR
EPI $\gtrsim$ 0.4 k$\Omega \cdot cm$	EPI $\sim$ 1 - 8 k$\Omega \cdot cm$	SNR, NITD

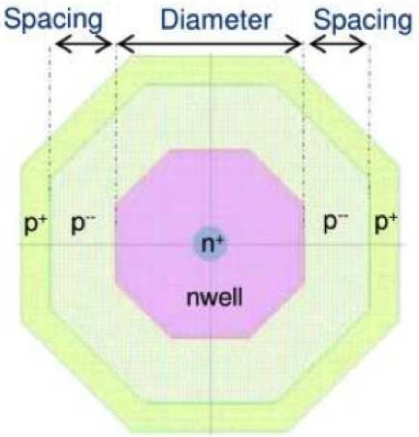
- **Drawbacks of smaller feature size**
  - 1.8 V operating voltage (instead of 3.3 V)
    $\Rrightarrow$ reduced dynamics in signal processing circuitry and epitaxy depletion voltage
  - increased risk of Random Telegraph Signal (RTS) noise



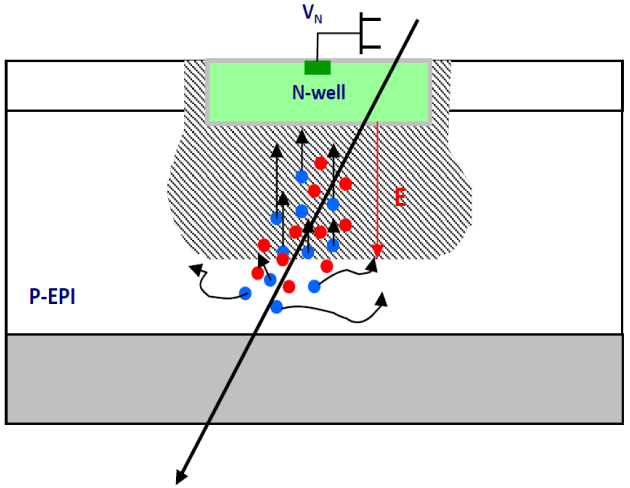
- **Consequences of the large surface to cover**
  - good fabrication yield required $\Rrightarrow$ sensor design robustness
  - mitigate noisy pixels (data transmission band width)
  - sensor operation should be stable along 1.5 m ladder (voltage drop !)
  - minimal connections to outside world (material budget)
    $\Rrightarrow$ impacts sensor periphery (slow control, steering parametres, ...)

Sensing Node & VFEE Optimisation

- **General remarks on sensing diode :**
  - should be small because : V_{signal} = Q_{coll}/C ; Noise $\sim$ C ; $G_{PA} \sim$ 1/C
  - BUT should not be too small since $Q_{coll} \sim$ CCE (important against NI irradiation)



- **General remarks on pre-amplifier** connected to sensing diode :
  - should offer high enough gain to mitigate downstream noise contributions
  - should feature input transistor with minimal noise (incl. RTS)
  - should be very close to sensing diode (minimise line C)



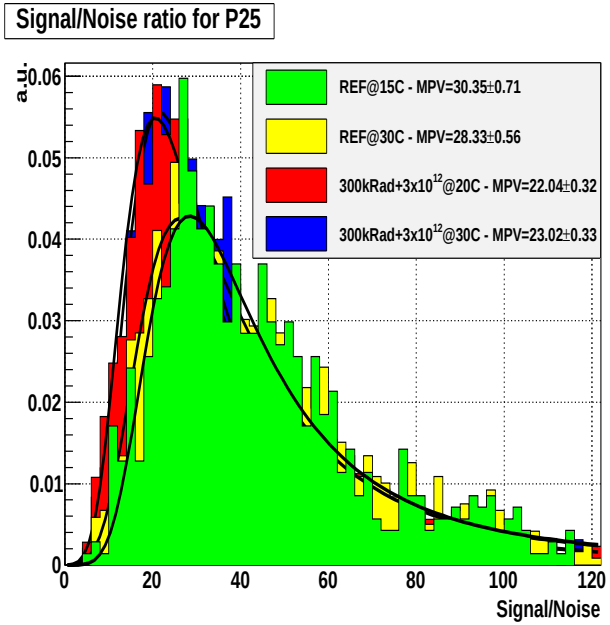
- **General remarks on depletion voltage :**
  - apply highest possible voltage on sensing diode
    preserving charge sharing $\mapsto \sigma_{sp}$
  - alternative : backside biasing

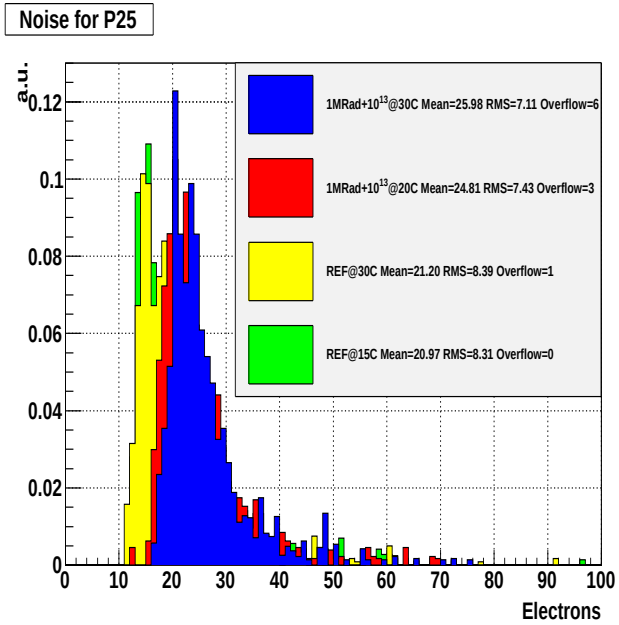
$\Rightarrow$ **Multiparametric trade-off to be found,**
based on exploratory prototypes rather than on simulations

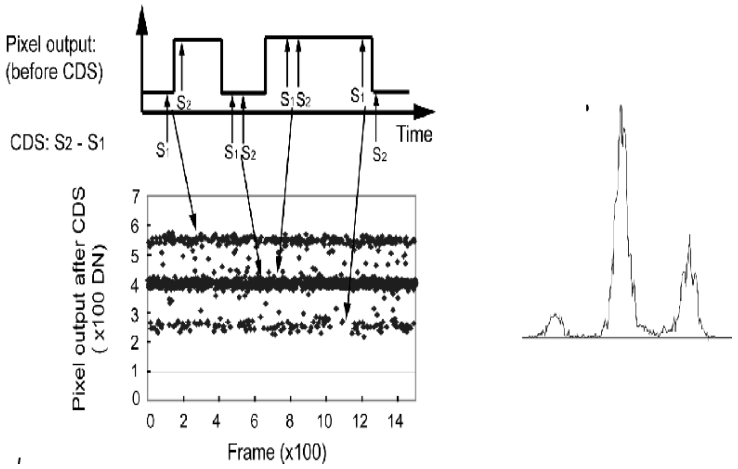
Outcome of 2012 Exploration of the 0.18 μm Process

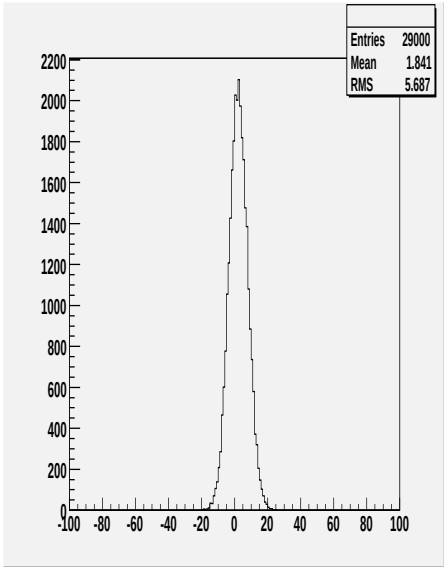
- STEPS VALIDATED IN 2012 :
  - ✳ Several in-pixel amplifier variants lead to satisfactory SNR & det. eff. ($20 \times 20\ \mu m^2$) incl. after 1 MRad & $10^{13} n_{eq}/cm^2$ at 30°C
  - ✳ Results pres. at VCI-2013 (J. Baudot)

- CALL FOR IMPROVEMENT :
  - ✳ **Pixel circuitry noise :**
    tail due few noisy pixels
    ↪ **attributed to RTS noise**
    ⇛ required optimising T geometries

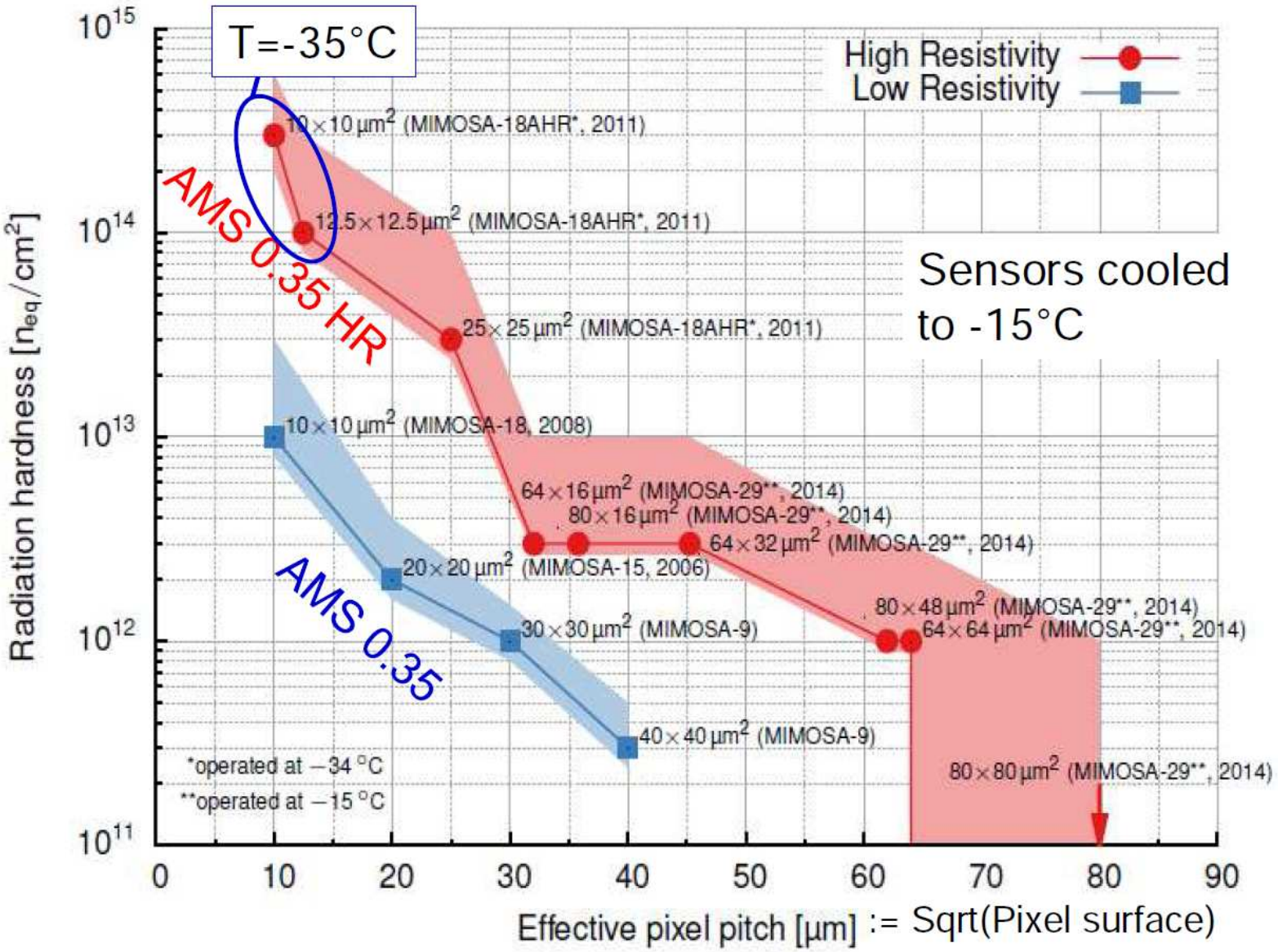








Established knowledge on radiation tolerance



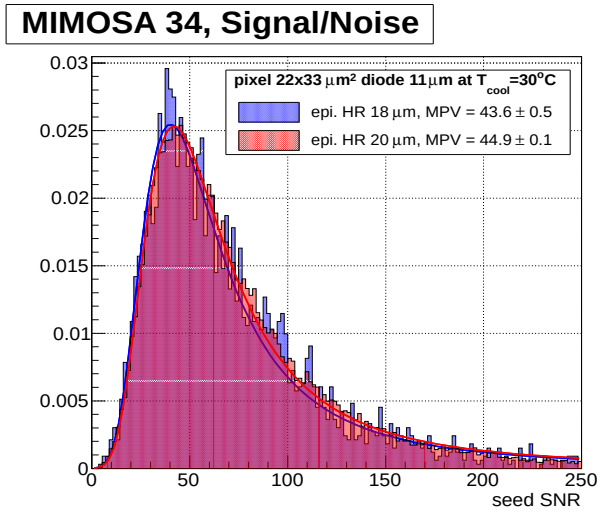
Sensors: IPHC Strasbourg
M. Deveaux, D. Doering, S. Strohauer, CBM/IKF Frankfurt

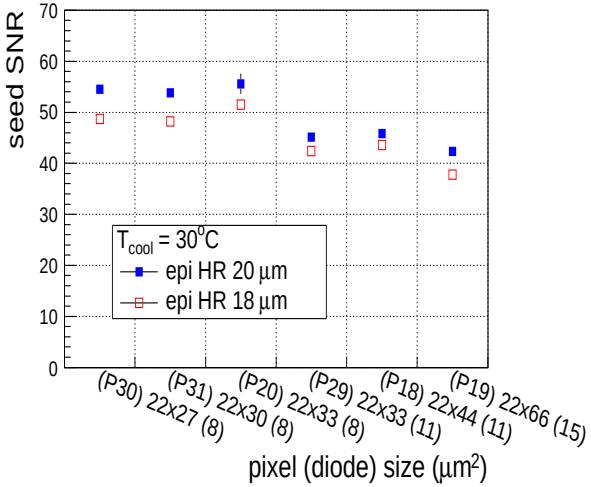
Pixel Optimisation : Epitaxial Layer and Sensing Node

- **Pixel charge coll. perfo. for HR-18 & VHR-20 (no in-pixel CDS) :**
  - SNR distributions $\longmapsto$ MPV & low values tail
  - $22 \times 33\ \mu m^2$ (2T) pixels at 30°C

$\Rightarrow$ **Results :**

- only $\sim$ 0.1 % of cluster seeds exhibit SNR $\lesssim$ 7–8
- SNR(VHR-20) $\sim$ 5-10% higher than SNR(HR-18)

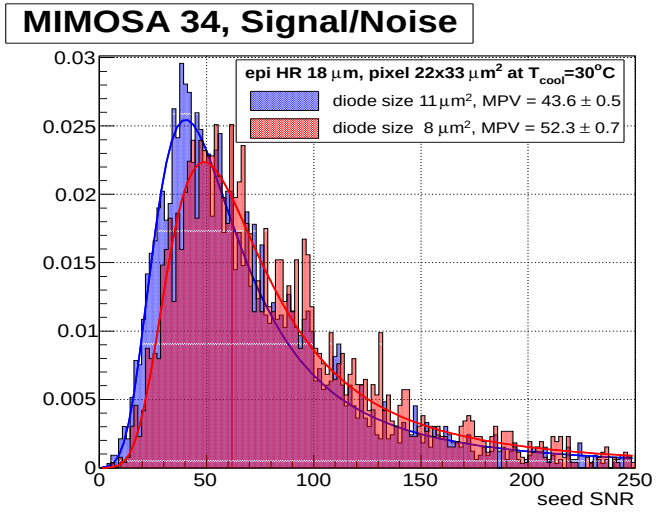


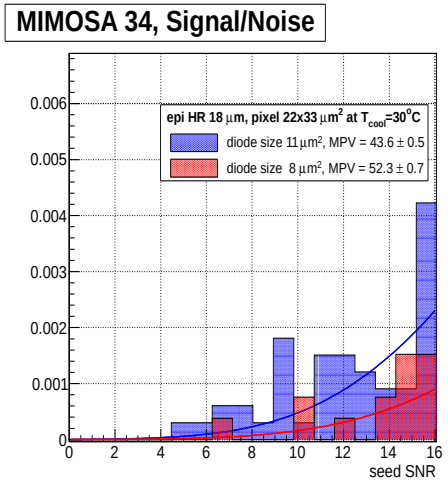


- **Pixel charge coll. perfo. for 2 diff. sensing nodes:**
  - 10.9 μm^2 large sensing diode
  - 8 μm^2 cross-section sensing diode
    underneath 10.9 μm^2 large footprint

$\Rightarrow$ **Results :**

- 8 μm^2 diode features nearly 20% higher SNR(MPV)
  & much less pixels at small SNR (e.g. SNR $<$10)
  $\hookrightarrow$ $Q_{clus} \simeq$ 1350/1500 e^- for 8/10.9 μm^2
  $\Rightarrow$ marginal charge loss with 8 μm^2 diode
- radiation tolerance to 250 kRad & $2.5 \cdot 10^{12}$ n_{eq}/cm^2 at 30°C OK





In-Pixel Pre-Amp & Clamping : SNR of Pixel Array

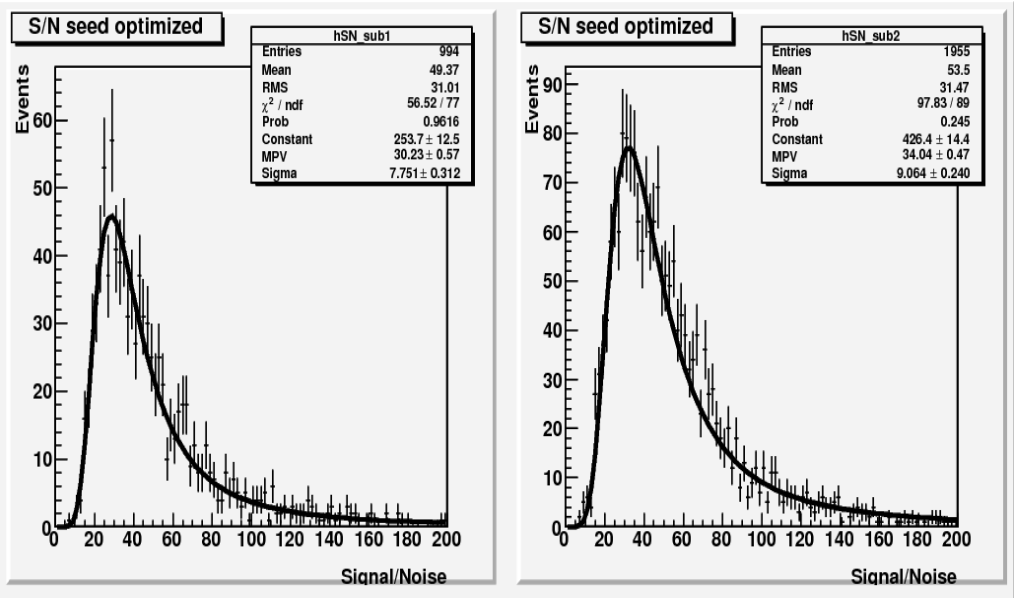
- MIMOSA-22THRa1 exposed to $\sim$ 4.4 GeV electrons (DESY) in August 2013

- Analog outputs of 8 test columns (no discri.)

  $\hookrightarrow$ SNR with HR-18 epitaxy, at T=30°C

  ⁂ Noise determination with beamless data taking

  ⁂ Ex: S2 (T gate L/W=0.36/1 μm against RTS noise)
  S1 (T gate L/W=0.36/2 μm against RTS noise)



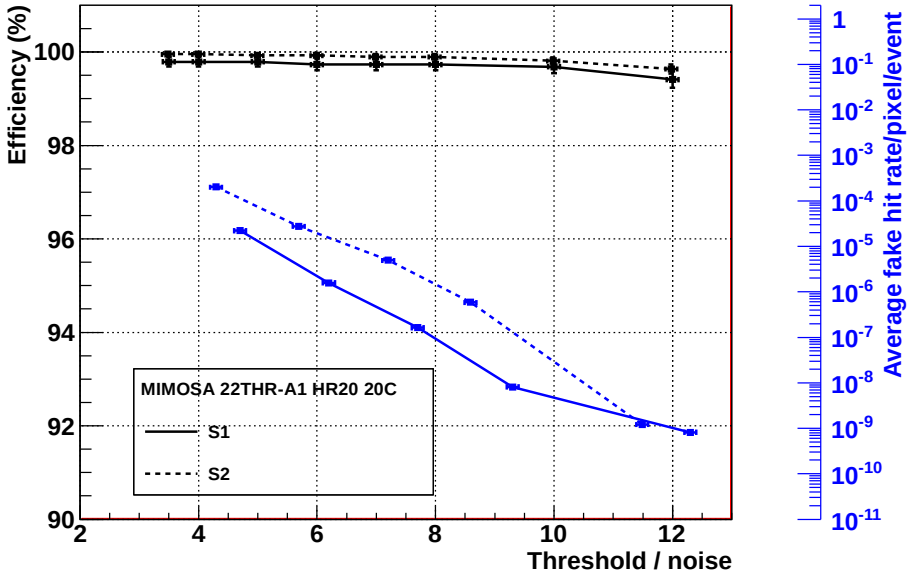
- Results :

  ⁂ Charge collected in seed pixel $\simeq$ 550 e$^-$

  ⁂ Detection efficiency of S1 & S2 $\gtrsim$ 99.5%
  while Fake rate $\lesssim$ O(10^{-5}) for
  Discrimination Thresholds in range $\sim$ 5N $\rightarrowtail$ $>$ 10N

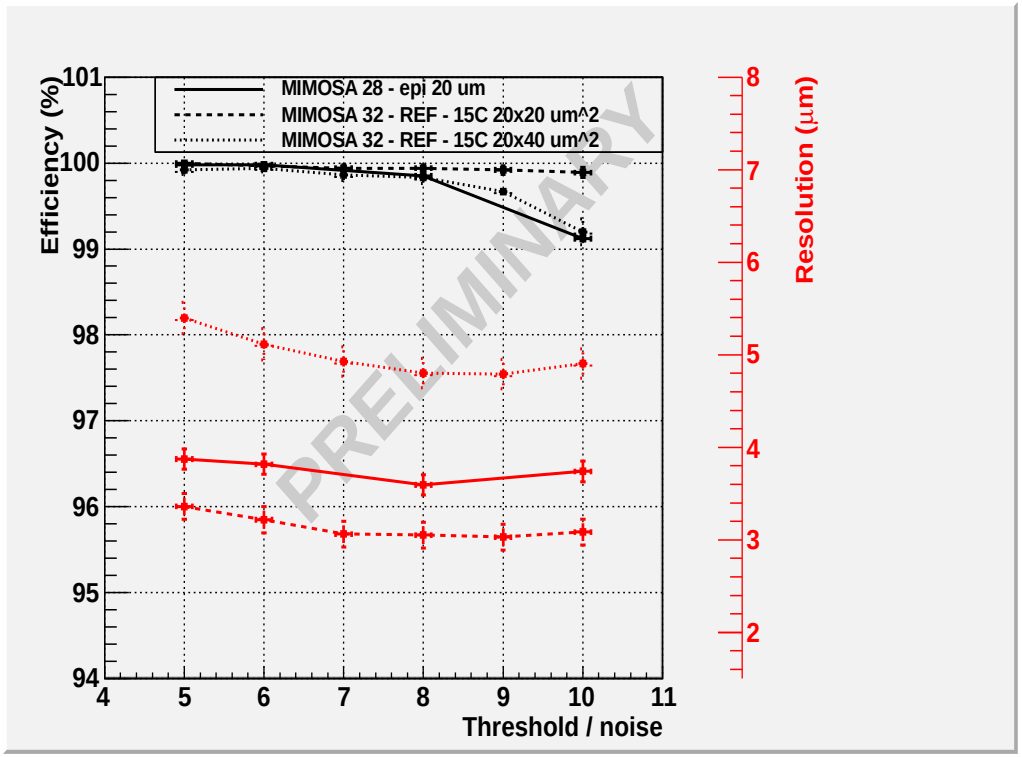
  ⁂ Mitigation of Fake Hits due to RTS
  noise fluctuations confirmed

  ⁂ A few 10^{-3} residual inefficiency may come
  from BT-chip association missmatches
  and non-optimised cluster algorithme



Spatial Resolution

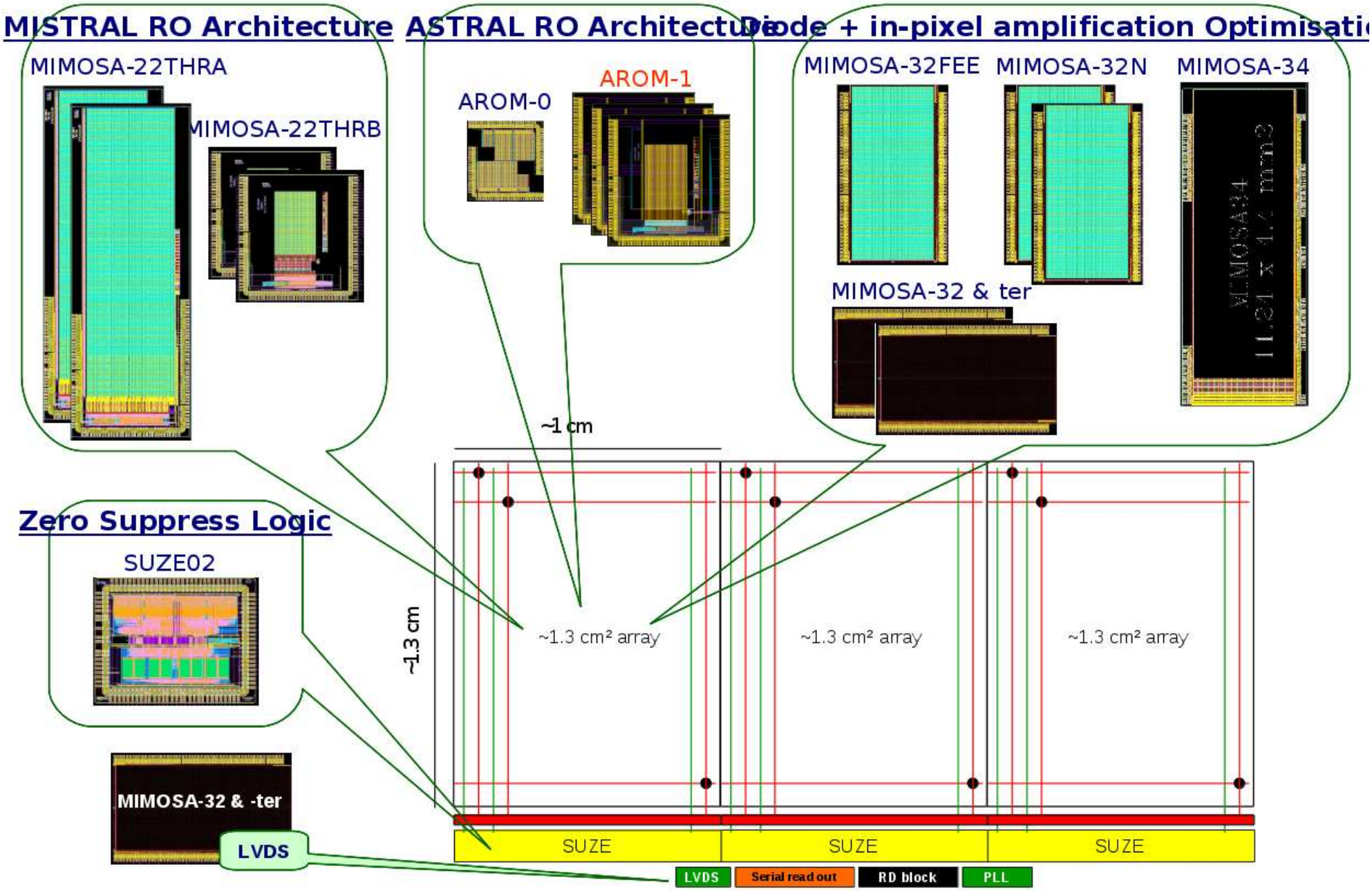
- **Beam test (analog) data used to simulate binary charge encoding :**
  - ✳ Apply common SNR cut on all pixels using <N>
    - ↪ simulate effect of final sensor discriminators
  - ✳ Evaluate single point resolution (charge sharing) and detection efficiency vs *discriminator threshold* for 20x20; 22x33; 20x40; 22x66 μm^2 pixels



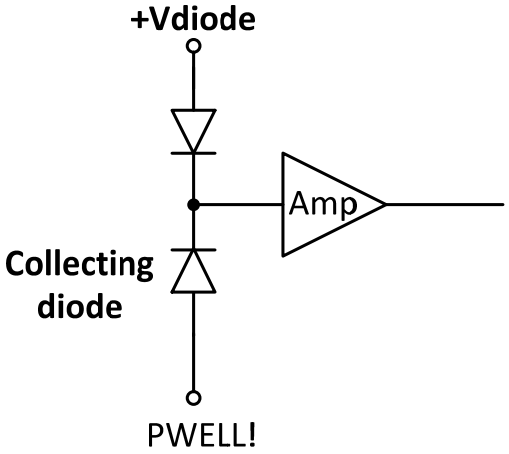
- **Comparison of 0.18 μm technology ($> 1\ k\Omega \cdot cm$) with 0.35 μm technology ($\lesssim 1\ k\Omega \cdot cm$)**

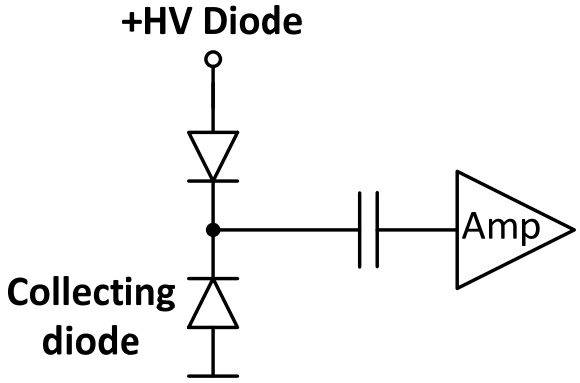
Process ▷	0.35 μm		0.18 μm			
Pixel Dim. [μm^2]	18.4×18.4	20.7×20.7	20×20	22×33	20×40	22×66
$\sigma_{sp}^{bin}[\mu m]$	3.2 ± 0.1	3.7 ± 0.1	3.2 ± 0.1	~ 5	5.4 ± 0.1	~ 7

CPS fabricated in 2012/13 in 0.18 μm Process



Depleting the sensitive layer





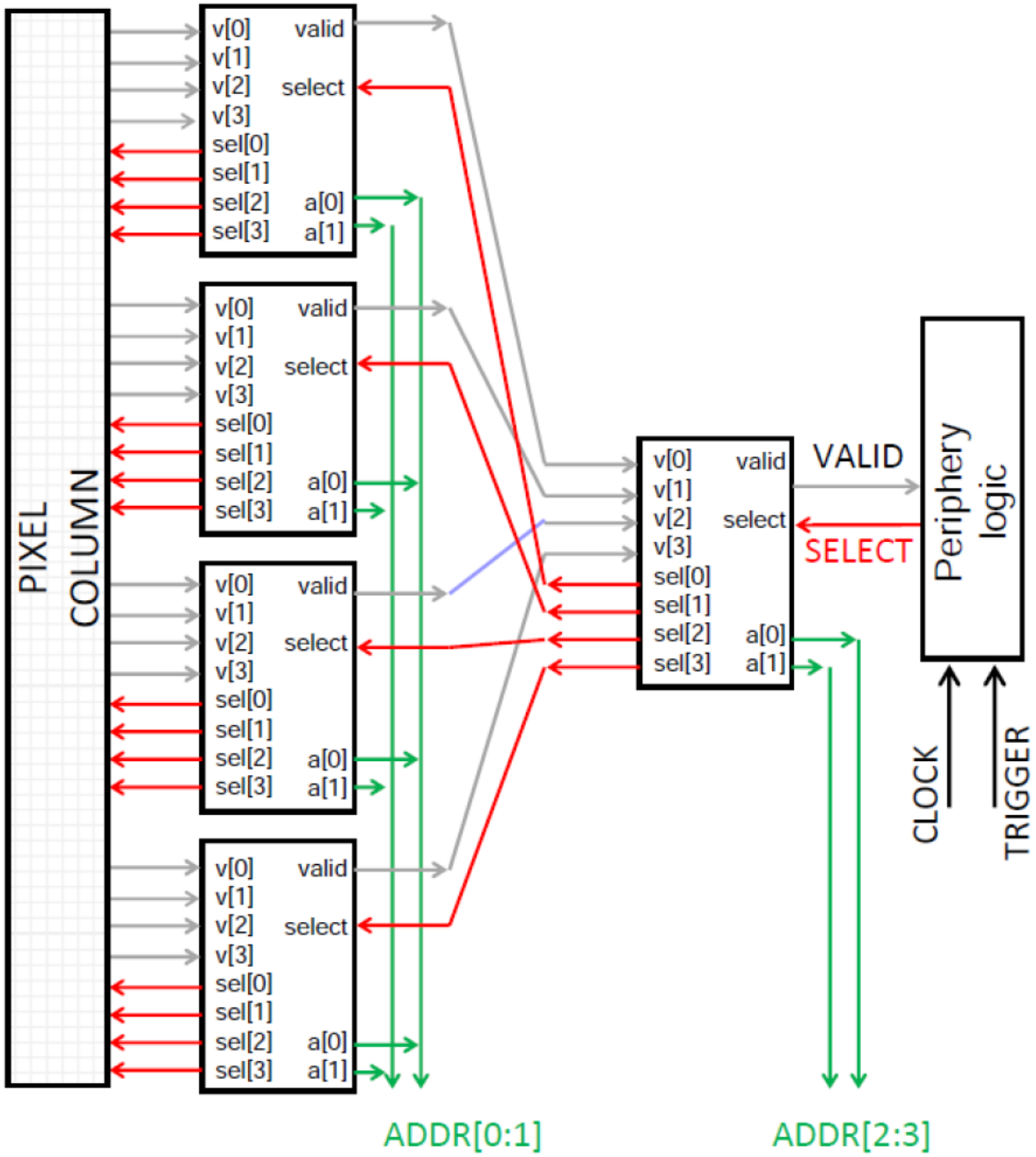
DC coupling

- Negative voltage on the anode of the collecting diode
- Transistors have negative PWELL
- Vd ≈ 2.5V

AC coupling

- Anode side grounded
- Cathode side on +HV
- Vd ≈ 15-20V

Asynchronous Read-Out Architecture : ALPIDE



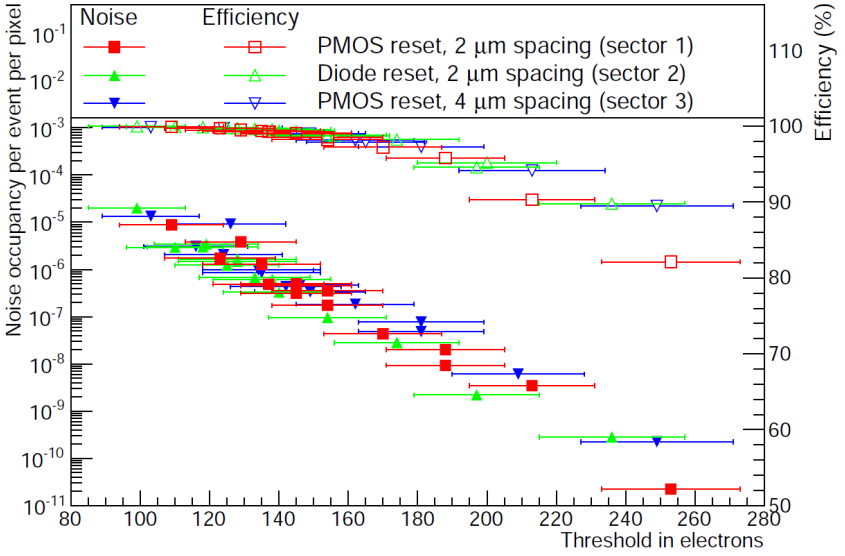
- Hierarchiral readout : 1 encoder per double column (2^{10} pixels)
- 4 inputs basic block repeated to create a larger encoder
- 1 pixel read per clock cycle
- Forward path (address encoder)
- Feed-back path (pixel reset)
- Asynchronous (combinatorial) logic
- Clock only to periphery, synchronous select only to hit pixels

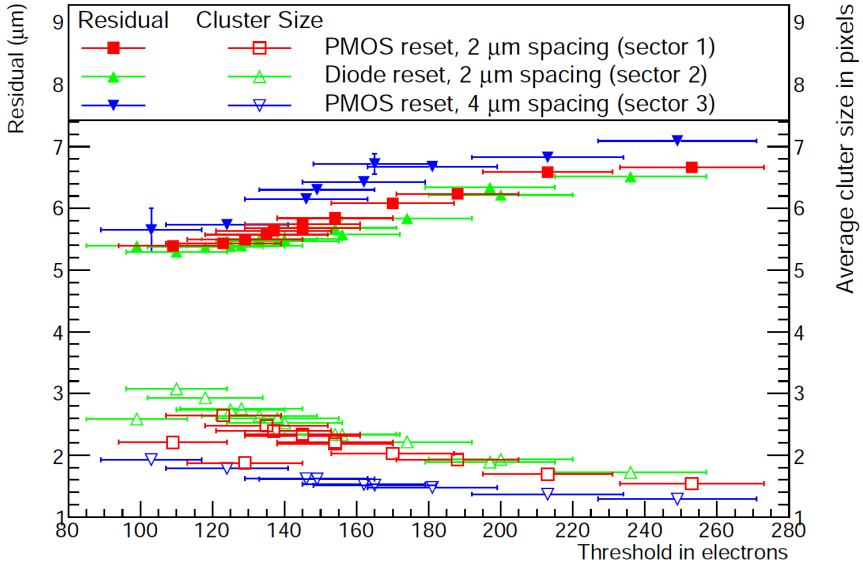
Asynchronous Read-Out Architecture : ALPIDE Beam Tests

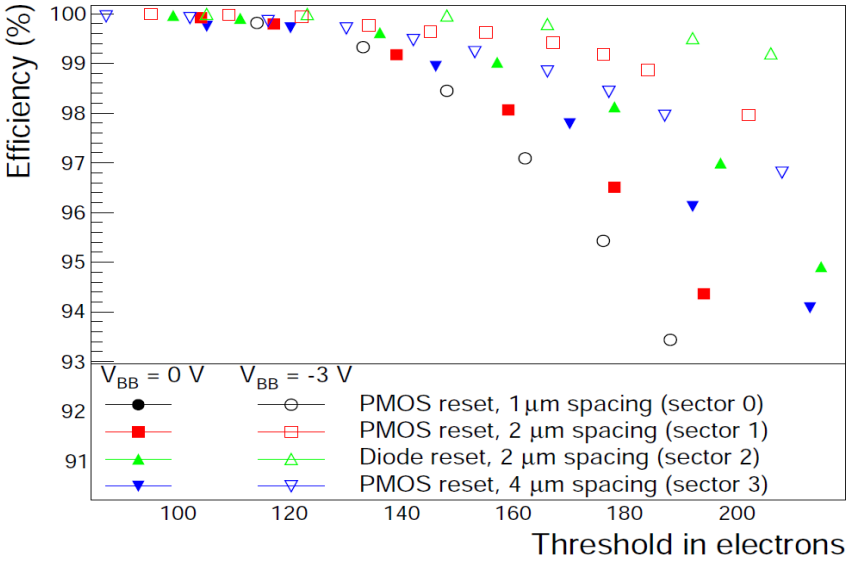
- **Beam tests at CERN-PS :**

  ↪ **Detection performance versus discri. threshold**

  - Detection efficiency and noisy pixel rate (”fakes”)
  - Sensitivity of detection efficiency to sensing node geometry and back-bias voltage (-3V)
  - Cluster mutliplicity and spatial resolution (residues)







⇒ **Satisfactory detection efficiency and spatial resolution observed**