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Overview of the RD53 Collaboration & Status Report

Hans Krüger, Bonn University

8th Terascale Detector Workshop, 2-6 March 2015, Berlin

Outline

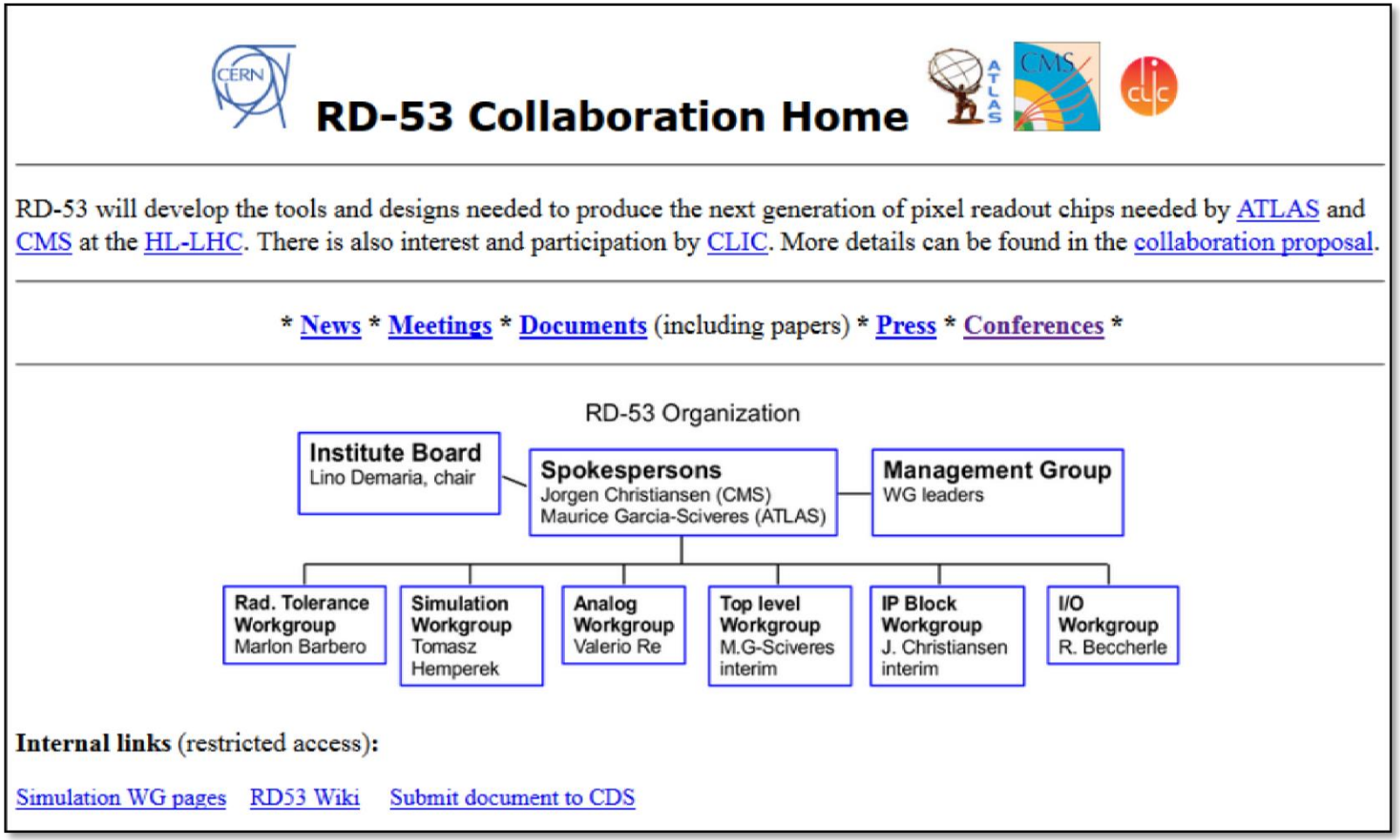
- High Luminosity LHC pixel electronics
- RD53 Organization & 65nm technology access & support
- Design strategies for the next generation 65nm pixel chips
- Bonn contributions to / experience in 65nm design

ATLAS Pixel Chip Generations

Generation	Current (FE-I3)	Phase 1 (FE-I4)	Phase 2 (preliminary assumptions)
Hit rate	100 MHz/cm^2	400 MHz/cm^2	1-2 GHz/cm^2
Trigger rate	100 kHz	100 kHz	2 MHz
Readout rate	40 Mb/s	160 Mb/s	~1-3 Gb/s
Radiation tolerance	100 Mrad	200 Mrad	1 Grad
Technology	250 nm	130 nm	65 nm
Pixel size	50×400 µm^2	50×250 µm^2	50×50 µm^2
Chip size	7.5×10.5 mm^2	20×20 mm^2	21.9×18.7 mm^2
Transistors	3.5M	87M	~500M

About RD53

- Established (April 2014) to focus the HL-LHC pixel upgrade efforts (CMS, ATLAS) and LCD vertex (CLICPix) using 65nm CMOS technology
- http://rd53.web.cern.ch



About RD53

- 21 Institutes: Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, PSI, RAL, Torino, UC Santa Cruz, LAL/OMEGA, Seville
- ~100 collaborators
- Spokes persons:
  - Maurice Garcia-Sciveres, LBNL (ATLAS),
  - Jorgen Christiansen, CERN (CMS)
- Institute Board
  - IB chair: Lino Demaria, Torino
  - Regular IB meetings
  - MOU signed
- Collaboration meetings
  - Spring 2014: April 10 & 11 at CERN
  - Fall 2014: October 16 & 17 at RAL
  - Spring 2015: April 23 & 24 at CERN

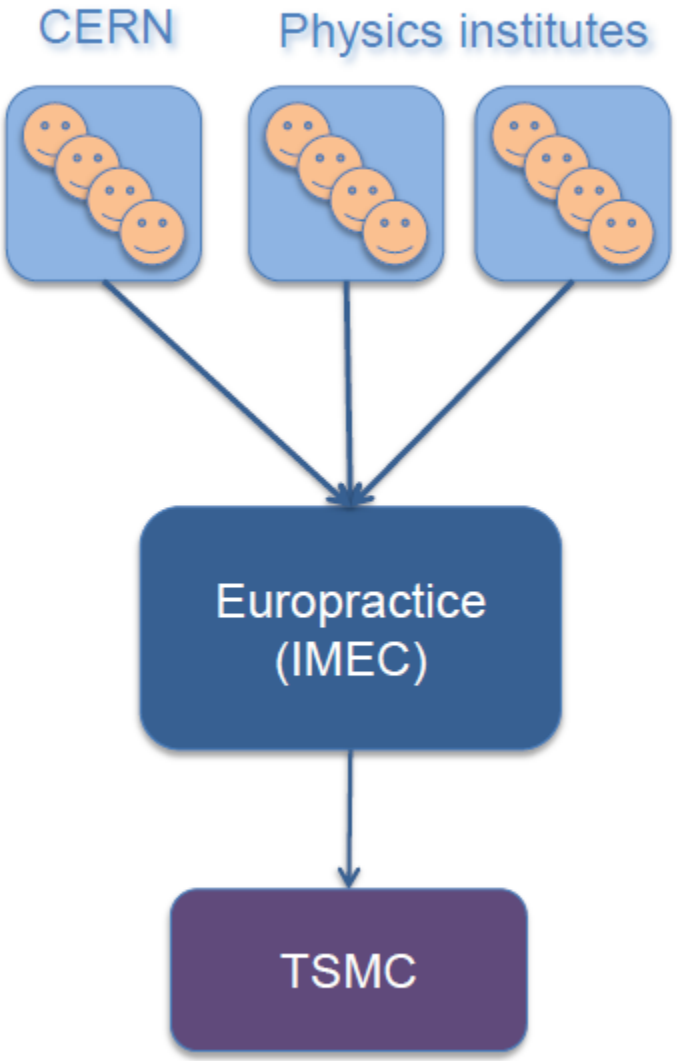
CERN Support for TSMC Technologies

- Development of a 65nm (and 130nm) Mixed Signal Design Kit
- Development of IP blocks
- Radiation tolerance characterization (up to 200MRad)
- Established a commercial contract for foundry services
- Negotiated a Non Disclosure Agreement with special provisions for HEP collaborative model

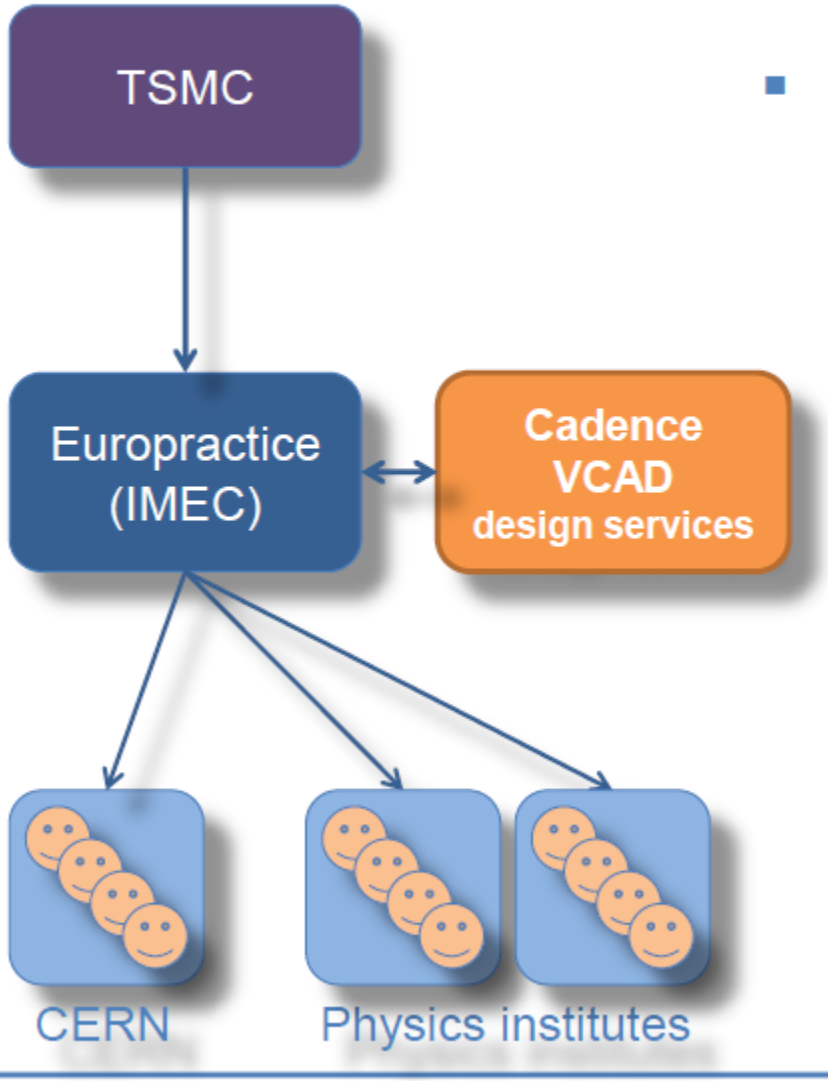
- Contacts at CERN for foundry services
  - Generic e-mail address: foundry.services@cern.ch
  - Gert Olesen Gert.Olesen@cern.ch
    - Coordinates all logistics procedures (administrative, financial, silicon handling) of the foundry services operations
  - Kostas Kloukinas Kostas.Kloukinas@cern.ch
    - Organizational matters

Foundry Services

- CERN has signed a commercial contract with IMEC for the TSMC 65nm & 130nm processes
  - Fixed prices
  - All purchase orders will pass via CERN
  - Design data will be submitted directly to IMEC
- Foundry Services schedules
  - MPWs announced schedules by IMEC and foundry
    - CyberShuttle
      - Compatible with all metal stacks
    - mini@sic
      - metal stack: 6-thin, 1-thick, 1-UTM
  - Based on demand
    - Additional runs for HEP could be organized



Support Services



- Services provided by Europractice (IMEC)
  - **Distribute** the CERN Mixed Signal Design Kit Design kit and the Workflows
  - Provide **maintenance and technical support** in collaboration with Cadence VCAD design services
  - Project specific **design services** and technical support can be made available by IMEC or VCAD at a cost.
  - CERN can not engage in a manpower demanding, long term maintenance & support program as in the past

RD53 Challenges

- Design for 1 Grad radiation tolerance
  - technology qualification
  - design guidelines
- Establish design and verification methodology adequate for >10^8 transistor mixed signal chip
- Analog design
  - Low power, low threshold operation, high in-time efficiency
- Digital design
  - Cope with $2 \cdot 10^9$ hits/sec/cm^2
  - High bandwidth readout (2-4 Gbps per chip)
- Establish and maintain a shared IP library for full-custom function blocks for ease of design re-use

➔ RD53 Working groups

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RD53 Working Groups

WG	Domain
WG1	Radiation test/qualification: M. Barbero, CPPM
	Coordinate test and qualification of 65nm for 1Grad TID and10^{16} neu/cm^2 Radiation tests and reports. Transistor simulation models after radiation degradation Expertise on radiation effects in 65nm
WG2	Top level: (M. Garcia-sciveres, LBNL)
	Design Methodology/tools for large complex pixel chip Integration of analog in large digital design Design and verification methodology for very large chips. Design methodology for low power design/synthesis. Clock distribution and optimization.
WG3	Simulation/verification framework: T. Hemperek, Bonn
	System Verilog simulation and Verification framework Optimization of global architecture/pixel regions/pixel cells
WG4	I/O : To be started
	Development of rad hard IO cells (and standard cells if required) Standardized interfaces: Control, Readout, etc.
WG5	Analog design / analog front-end: V. Re, Bergamo/Pavia
	Define detailed requirements to analog front-end and digitization Evaluate different analog design approaches for very high radiation environment. Develop analog front-ends
WG6	IP blocks: (J. Christiansen, CERN)
	Definition of required building blocks: RAM, PLL, references , ADC, DAC, power conversion, LDO, , Distribute design work among institutes Implementation, test, verification, documentation

WG1 – Radiation Hardness

- Characterization of the TID and NIEL related effects

- Irradiation campaigns with various test structures and environmental conditions
  - Dose rate and type of radiation
  - Bias conditions
  - Temperature during irradiation and annealing

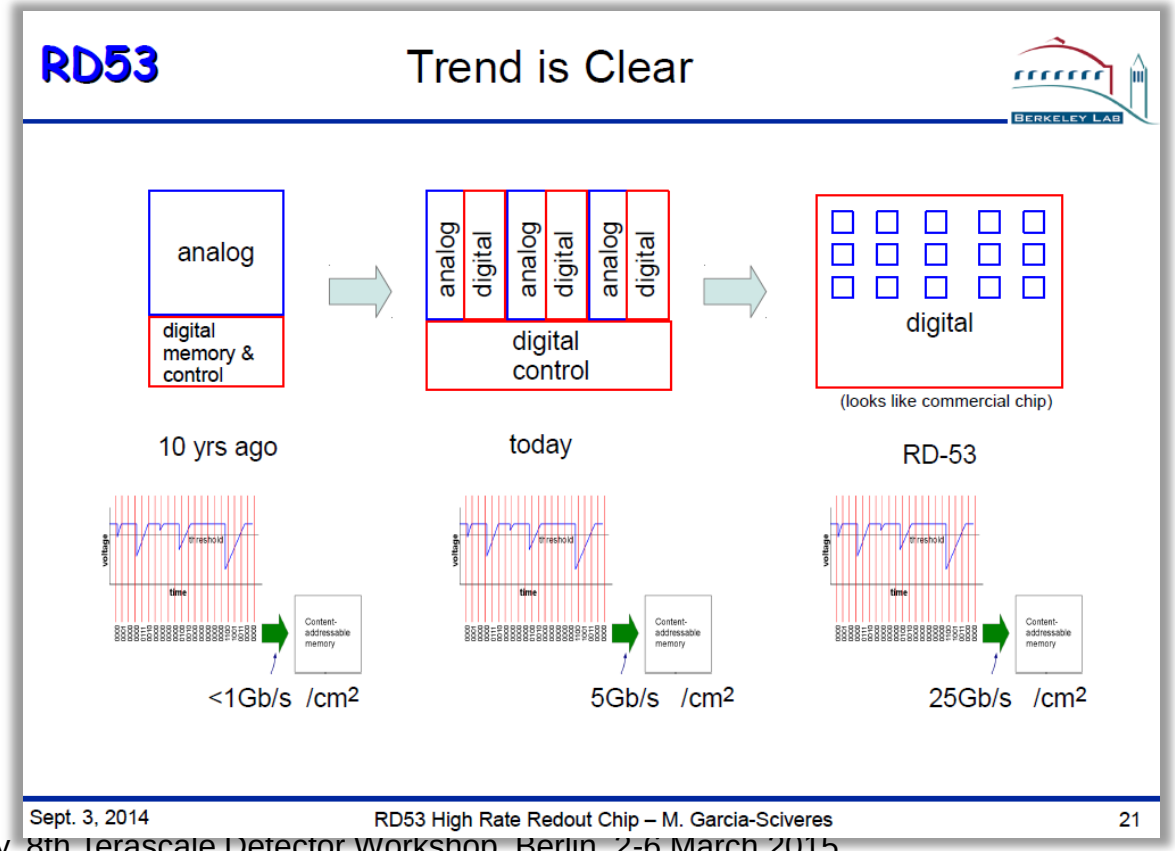
➔ Loss of transconductance after more than ~100 Mrad (threshold shift and off-leakage not so severe) in particular for narrow PMOS

- Design recommendations
  - Low temperature helps
  - Annealing is good for NMOS, but PMOS not so much (bias dependent)
  - NMOS: use large L if possible. L>120nm advised
  - PMOS: use large W to avoid loss of g_m (when large W, avoid fingered layout).

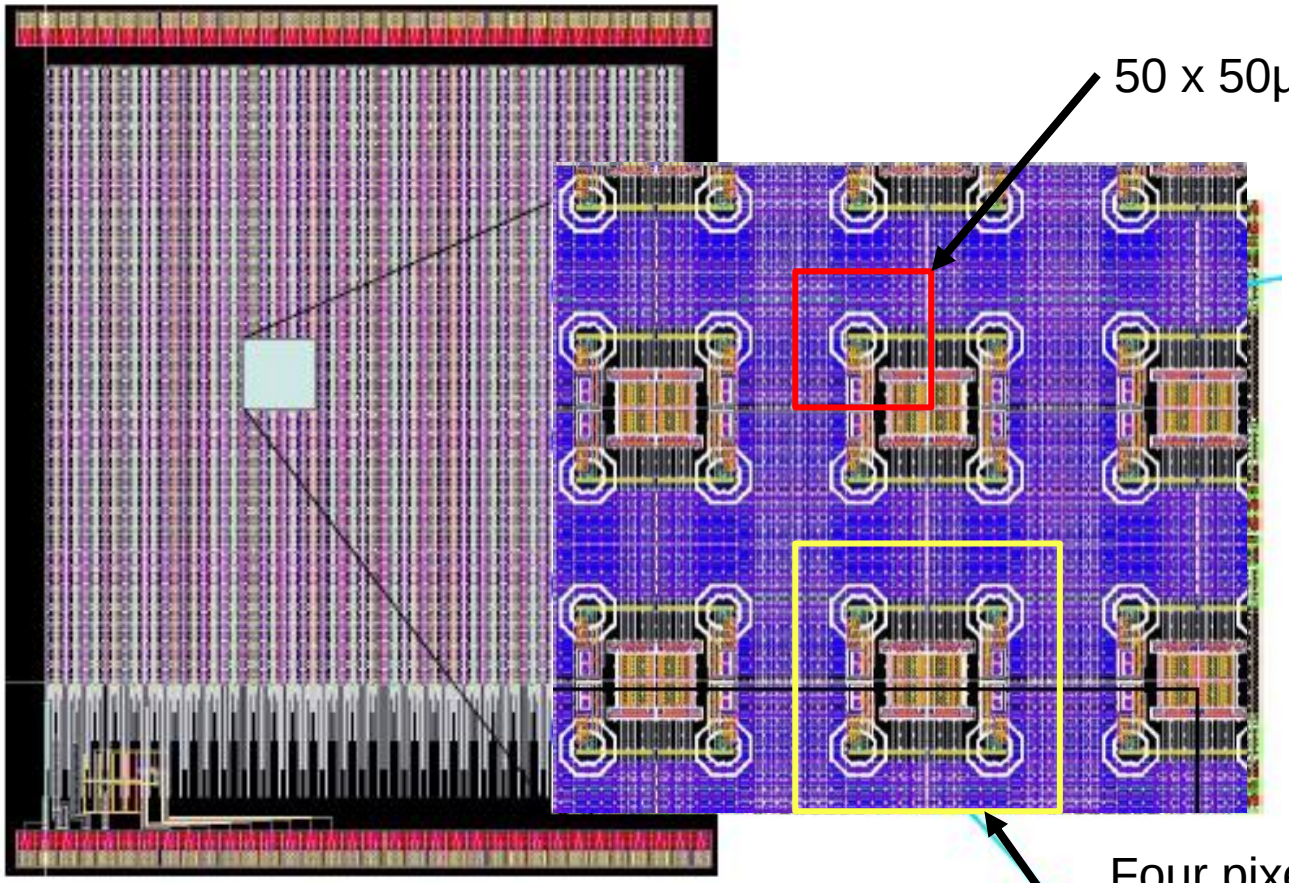
- Ongoing: Modeling of the radiation induced effects for use in circuit simulations

WG2 – Top Level Design

- Most FE-chip developments so far based on an ‘analog design flow’
  - Analog (full custom) design blocks dominate plus a few synthesized digital blocks
  - Not very efficient for complex & large chips (integration & verification)
- The complexity of next generation pixel chips require a different approach
  - Use of a ‘digital design flow’ with full custom design blocks added



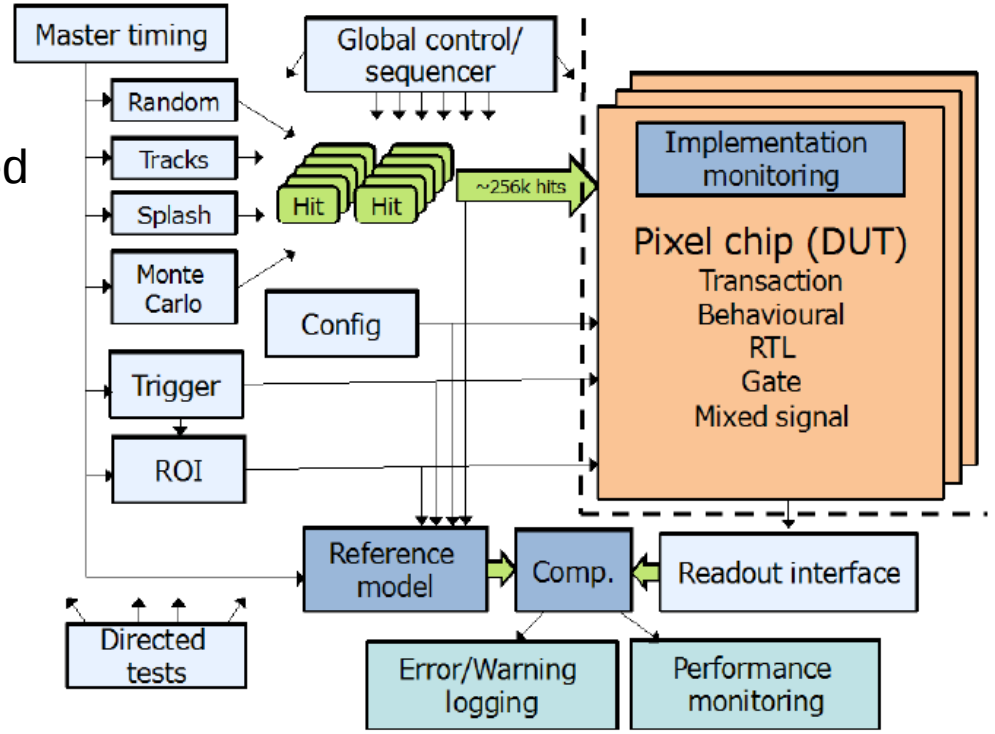
Top Level Design – Matrix Architecture



1 x 1 cm² ATLAS prototype matrix
(to be submitted May 2015)

WG3 – Simulation Test Bench

- Convener: T. Hemperek, Bonn
- Verification framework customized for complex pixel chips based on system Verilog and UVM (industry standard for ASIC design and verification)
- High abstraction level down to detailed gate/transistor level
- Benchmarked using FEI4 design
- Internal generation of appropriate hit patterns
- Integration with ROOT to import hits from detector simulations and for analyzing results.

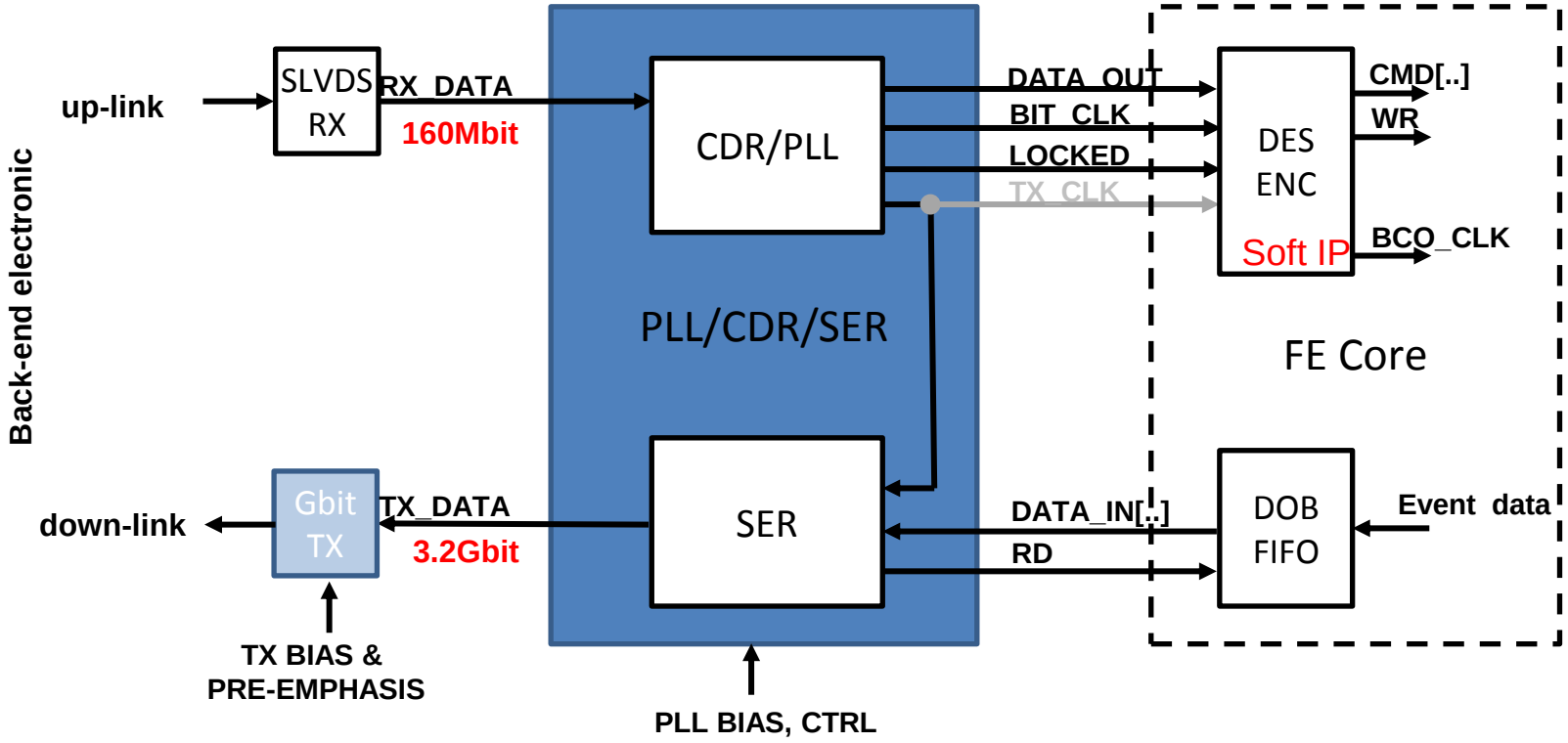


WG4 – I/O

- Definition of command input and data output protocols.
- Implementation of single serial input encoding clock and command
- High speed drivers. Need to be simulated with candidate low mass cable designs (interaction with experiments on cable R&D)
- Efforts are closely related to the design of the drivers, serializer, and clock data recovery block

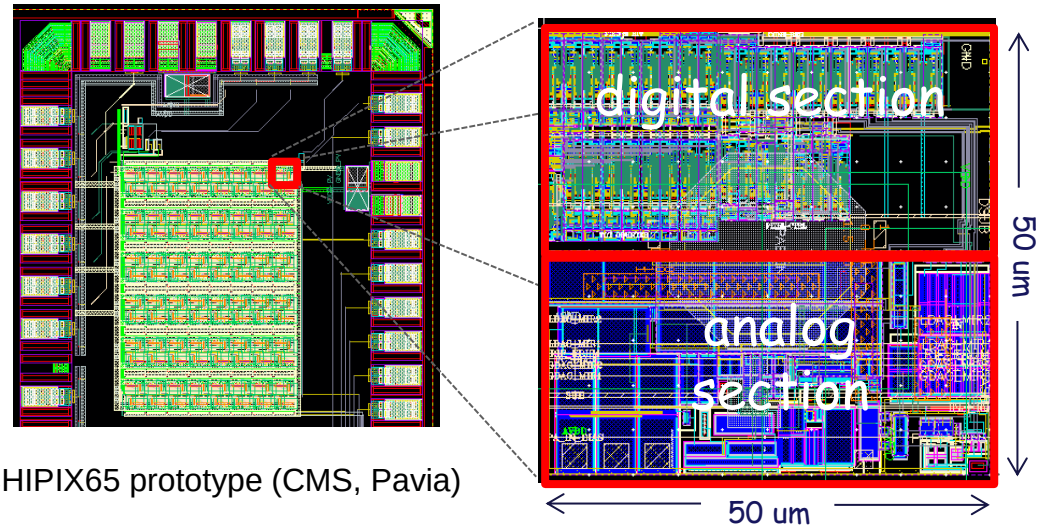
Example of IP Development for I/O

- FE interface
  - One up-link, combining CLK and CMD → needs clock/data recovery (CDR)
  - One (or more) high speed (> 2Gbps) down-links → serializer (SER) and Gbit driver (TX)
  - Bit rates and encoding schemes currently under discussion



WG5 – Analog Design

- Evaluation, design and test of appropriate low power analog pixel Front-Ends
- Develop analog front-end specifications
  - capacitance, threshold, charge resolution, noise, dead time, power...
- Sensor options
  - Planar, 3D sensors, Active CMOS
- Alternative architectures/implementations to be compared, designed and tested by different groups
  - TOT, ADC, Synchronous, Asynchronous, Threshold adjust, Auto zeroing, etc.
- Design / prototyping of FE's ongoing



CHIPIX65 prototype (CMS, Pavia)

WG6 – IP Blocks

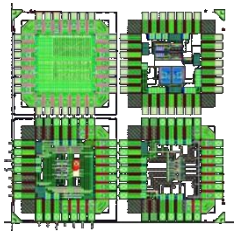
- Ambitious plan to design and maintain a broad variety of full custom blocks in a common IP/design repository
  - Definition of specifications
  - Integration into the design flow
- Time line
  - Prototyping/test of IP blocks: 2014/2015
  - IP blocks ready 2015/2016

- Bonn Contributions
  - Organization of PLL / CDR / SER development
  - Participation in the Gbit link driver design
  - Linear regulator / shunt regulator (M. Karagounis, former Bonn group member now FH Hamm-Lipstadt)
  - Various digital IP (soft cores)

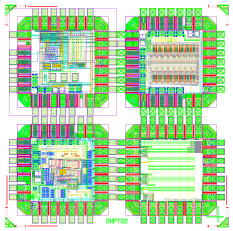
Country	DE	FR		NL	IT - INFN					US	FR	UK	US	CZ
Group	Bonn	CERN	CPPM	NIKHEF	Bari	Pav/Berg	(Milano)	Padova	Pisa	Torino	LBNL	LPNHE	RAL	Santa Cruz	(Prague)
ANALOG: Coordination with analog WG															
Temperature sensor.			O			(P)				(P)					(P)
Radiation sensor			(P)			(P)				O ?					(P)
HV leakage current sensor.			O							(P)					(P)
Band gap reference		O	O	(P)		O							(P)		
Self-biased Rail to Rail analog buffer	(P)		(P)	(P)									O		(P)
MIXED															
8 – 12 bit biasing DAC		(P)			O										(P)
10 - 12 bit slow ADC for monitoring		O	O		O										
PLL for clock multiplication	O	(P)		(P)				(P)	(P)	(P)			(P)	(P)	
High speed serializer (~Gbit/s)	O	(P)		(P)					(P)				(P)	(P)	
(Voltage controlled Oscillator)				(P)				O	(P)	(P)					
Clock recovery and jiter filter	O	(P)							(P)				(P)		
Programmable delay	O	(P)							(P)				(P)		
DIGITAL															
SRAM for pixel region	(P)	(P)					O							(P)	
SRAM/FIFO for EOC.	(P)	(P)					(P)		(P)					O	
EPROM/EFUSE	(P)	O	(P)												
DICE storage cell / config reg	(P)		O				(P)		(P)					(P)	
LP Clock driver/receiver	(P)					O							(P)		
(Dedicated rad hard digital library)	(P)	(P)	(P)						O			(P)	(P)		
(compact mini digital library for pixels)	(P)	(P)	(P)						O			(P)	(P)		
IO: Coordination with IO WG															
Basic IO cells for radiation	(P)	O													
Low speed SLVS driver (<100MHz)	(P)	(P)				O			(P)	(P)					(P)
High speed SLVS driver (~1Gbits/s)	(P)	(P)				O			(P)	(P)					(P)
SLVS receiver	(P)	(P)				O			(P)						(P)
1Gbits/s drv/rec cable equalizer															
C4 and wire bond pads	(P)	O													
(IO pad for TSV)	O		(P)									(P)		(P)	
Analog Rail to Rail output buffer	O		(P)									(P)		(P)	
Analog input pad	O											(P)			
POWER															
LDO(s)		(P)	(P)	O					(P)	(P)			(P)		
Switched capacitor DC/DC		(P)									O				(P)
Shunt regulator for serial powering				O											
Power-on reset															
Power pads with appropriate ESD	(P)	O													
SOFT IP: Coordination with IO WG															
Control and command interface		(P)			(P)				O			(P)			
Readout interface (E-link ?)		(P)			(P)				O			(P)			

Bonn 65nm CMOS Design Activities previous to RD53

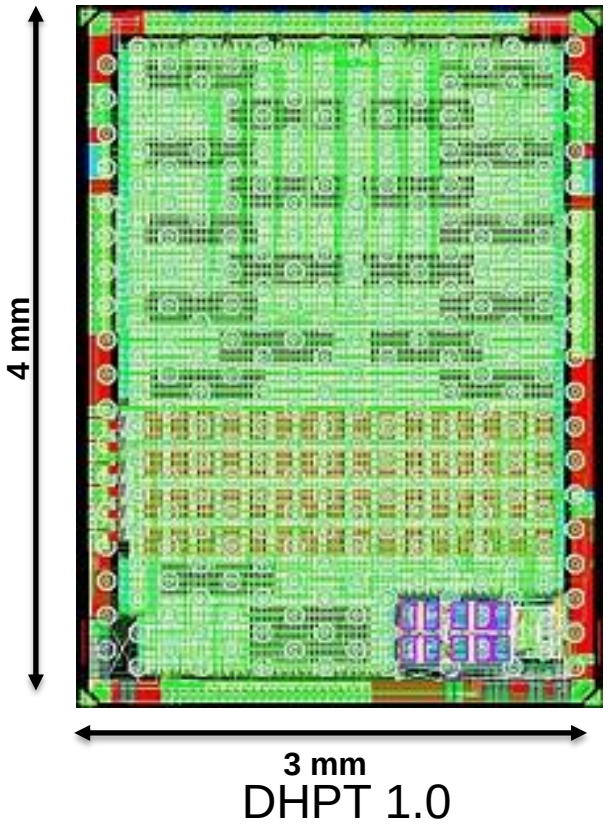
- Data handling processor (DHP) for the Belle 2 DEPFET pixel vertex detector
  - Manly digital with full-custom blocks
  - PLL (1.6 GHz)
  - High speed serial link (1.6 Gbps)
  - LVDS IO
- IP blocks for future pixel chips
  - Low power analog front-end (CSA + discr.)
  - Low power, small area ADC
  - SEU test structures
- Chip submissions
  - DHPT 0.1, four chiplets, Oct. 2011
  - DHPT 0.2, four chiplets, June 2012
  - DHPT 1.0, Oct. 2013
    - 14 mm^2 MPW
    - C4 bumps



DHPT 0.1

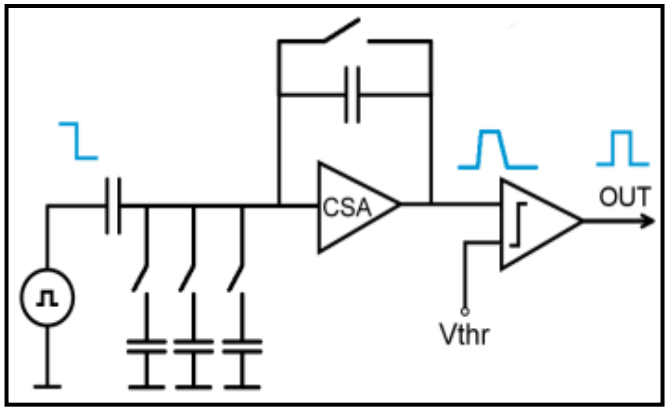


DHPT 0.2

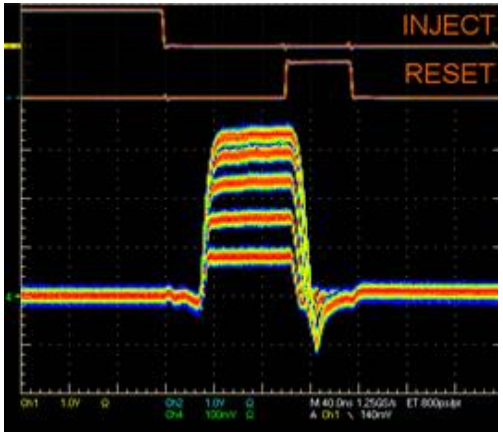


DHPT 1.0

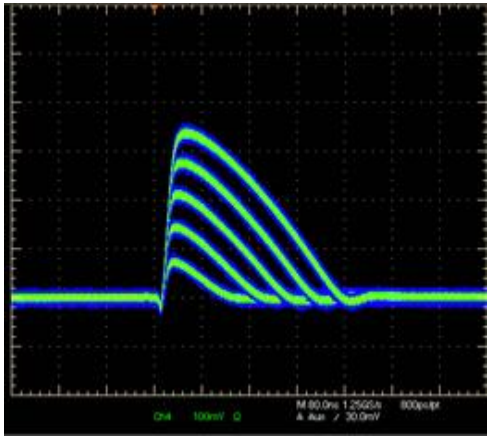
DHPT 0.2 – Pixel Analog FE Measurements



CSA with switched reset



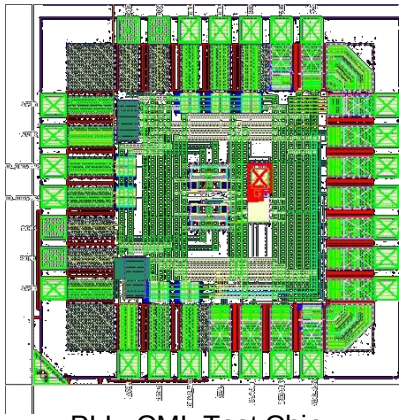
CSA with continuous reset



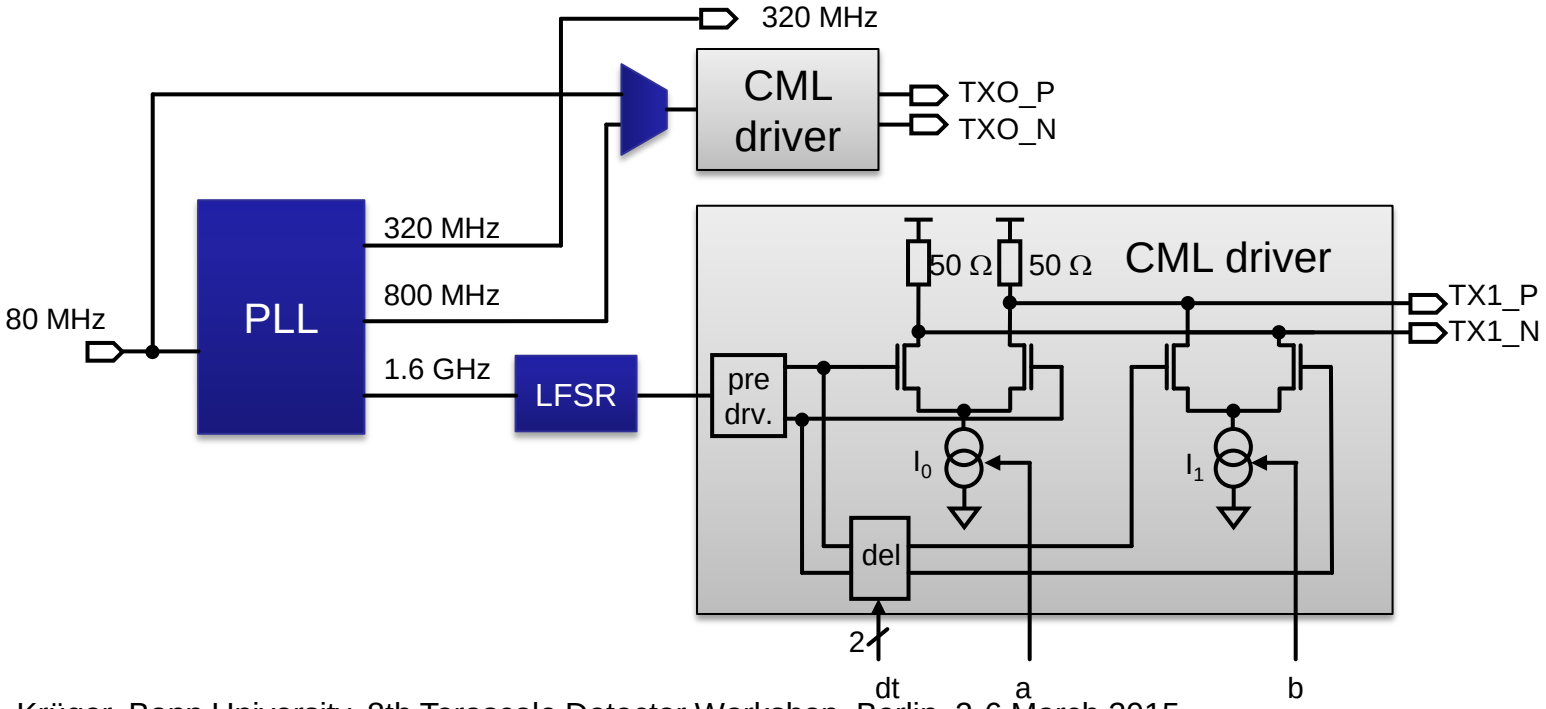
CSA	Comparator	$\langle ENC \rangle$ [e$^-$]	P [µW]
Continuous	Continuous	144	10.4
	Dynamic	183	10.6
Switched	Continuous	113	14.6
	Dynamic	157	14.8

DHPT 0.1 – PLL & High Speed Link Driver

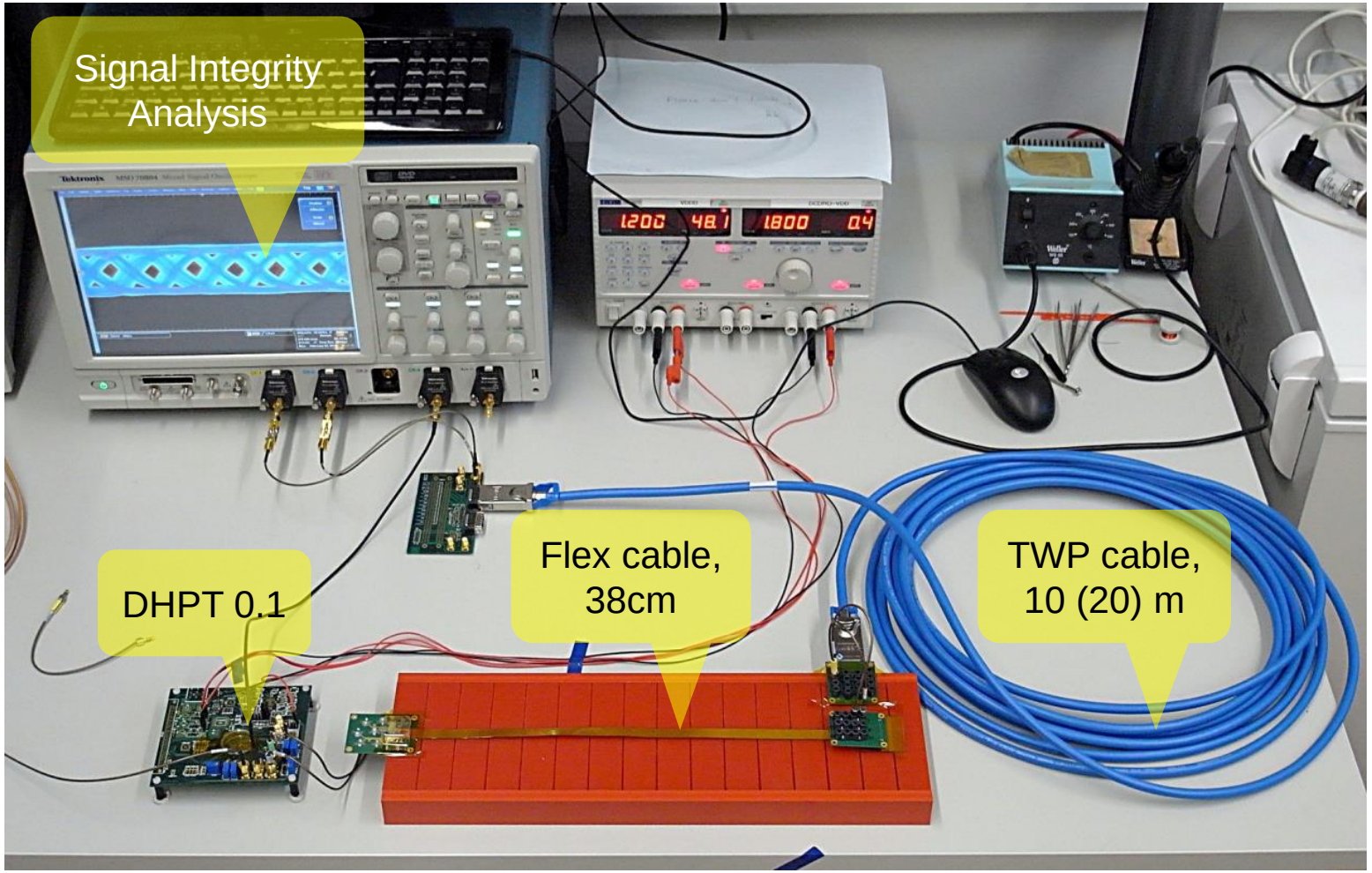
- 1.6 GHz PLL, 80 MHz input clock
- Pseudo random bit sequence generator (8 bit LFSR) for bit error rate tests
- Current mode logic (CML) driver
- Programmable pre-emphasis (first order FIR filter)
  - Needed to compensate the high frequency attenuation of the data cable



PLL_CML Test Chip,
T. Kishishita

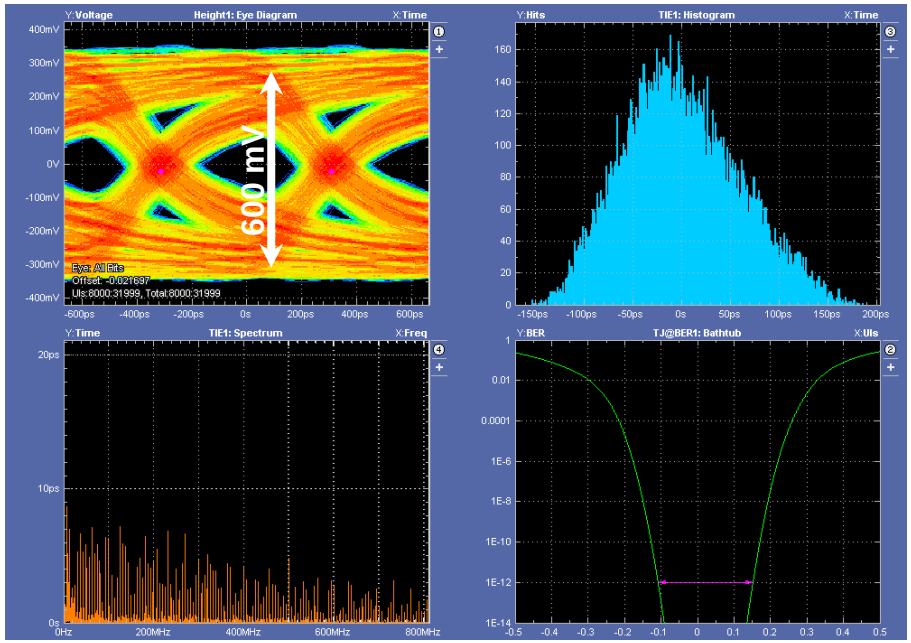


Gbit Link Test Setup

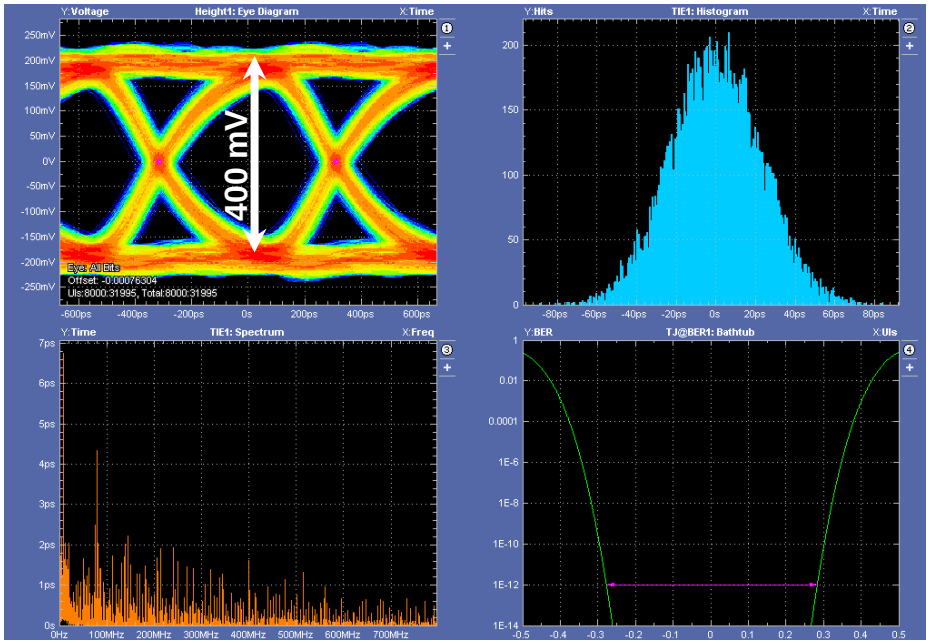


DHPT 0.1 – Signal Integrity Analysis

- 1.6 Gbps, 8bit LFSR sequence
- 10m Infiniband cable (LEONI, AWG 26)



Preemphasis off



Preemphasis on (600ps, max. I_{boost})

Conclusion & Outlook

- The development effort needed for **ATLAS/CMS HL-LHC pixel chips** is based on the RD53 collaboration, established to focus on 65nm CMOS technology

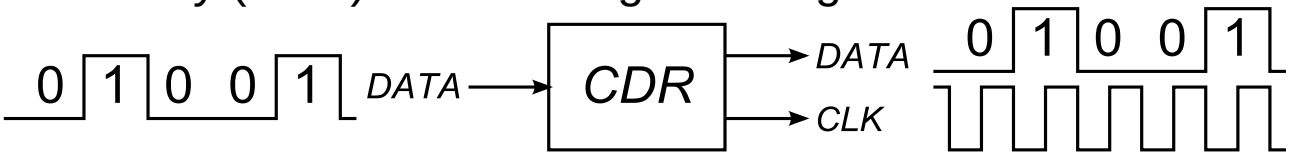
- Challenging goals (technical, and collaborative)

- Design effort in full swing
  - Various MPW chips for IP prototyping (in preparation / done)
  - Small analog-only matrices have been submitted end of last year
  - First medium size (1 x 1 cm^2) full matrix submission planned for May 2015

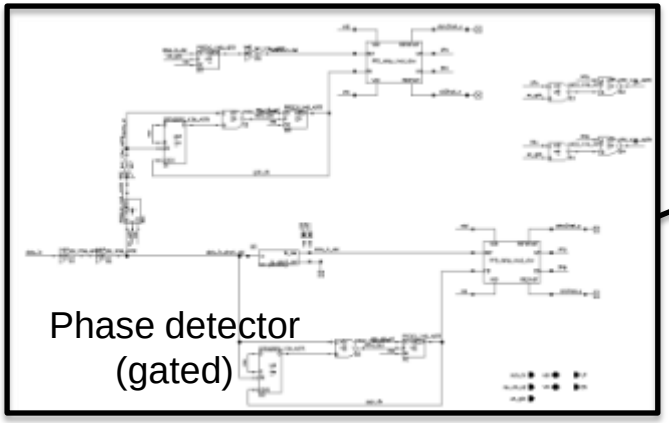
- General timeline
  - Radiation hardness conclusions – early 2015
  - Analog, I/O and IP prototype tests chips – now to end of 2015 (multiple submissions)
  - Full or half-size prototype(s) – 2016 (wafer run order in CERN frame contract process)
  - Test, design iteration and refinements – 2017
  - Hand over to ATLAS and CMS for final chip designs – 2018

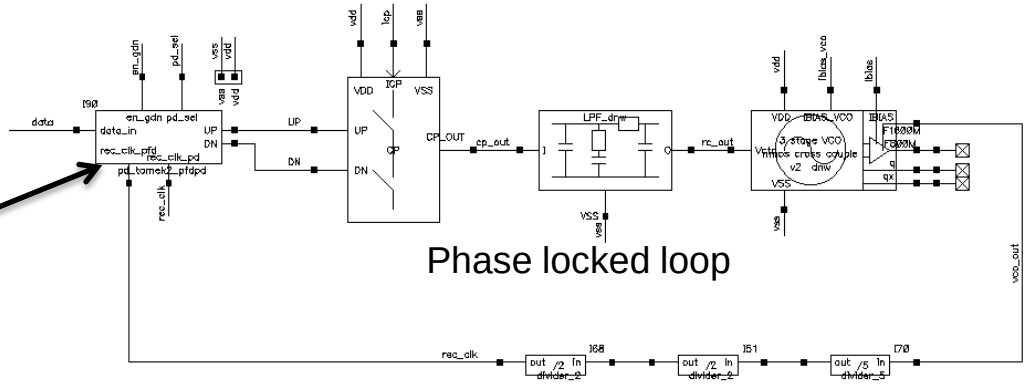
IP Example – Clock Data Recovery

- Clock Data Recovery (CDR) – recovering clock signal from randomized data



- Implementation: Phase-locked-loop with special phase detector (gated)





Piotr Rymaszewski

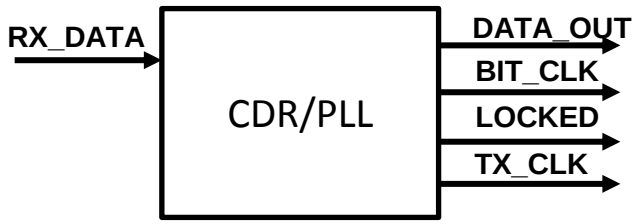
- Prototype RD53 CDR/SER submission foreseen for May 2015

IP Block: PLL/CDR

Parameter	Value
Size	?
Supply voltage	1.08-1.32V
Power	?
Temperature range	-20C +50C
Input Data/Clock Frequency	200 MHz – 400 MHz
VCO Frequency	1.6 GHz (or 3.2 GHz, tbd.)
Max variation (1Grad, 10^{16} n/cm^2)	??? (define max. SEU cross section)?
Max jitter	tbd.
Metal layers used	3? (tbd.)
Capacitor (& other special options)	tbd.
Active element used	tbd.
Status (19.1.2015)	Schematic ready
Designer (Email)	Piotr Rymaszewski rymaszewski@physik.uni-bonn.de

I/O signals	Function
RX_DATA (input)	Serial input data
DATA_OUT (output)	Resynchronized input data
BIT_CLK (output)	Recovered input clock
TX_CLK (output)	High speed clock for SER
LOCKED (output)	PLL status

Block Diagram

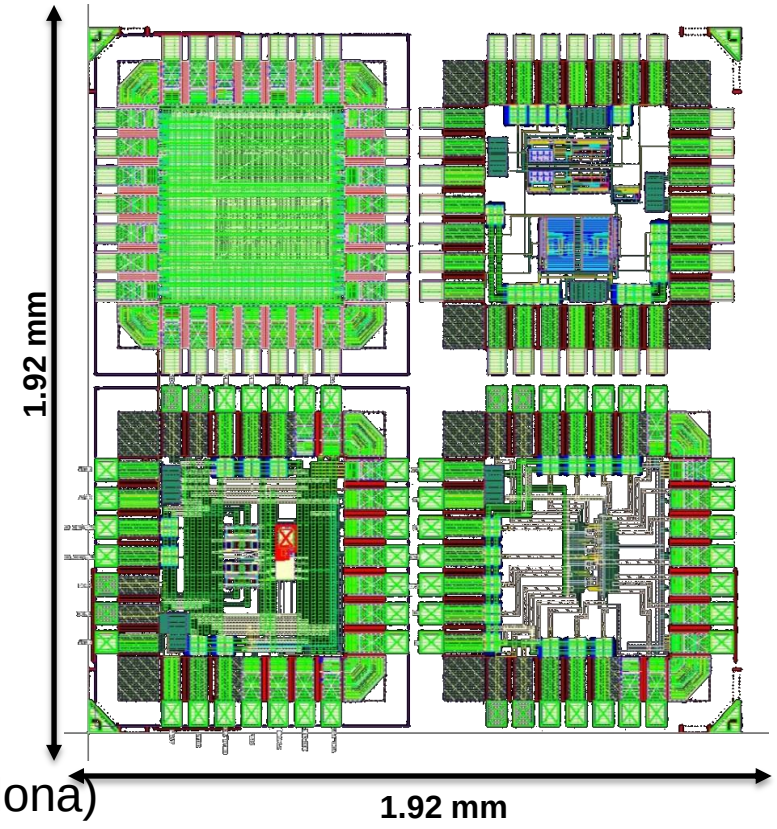


Schedule

Status	Date
Initial spec	Q2 2014
Schematic	Q3 2014
Layout	Q4 2014/Q1 2015
Final spec	Q1 2015
Prototype 1 submission	Q1 2015
Prototype characterized	Q3 2015
Prototype 2 submission	Q4 2015
Prototype 2 characterized	Q1 2016
Full IP available	Q1 2016

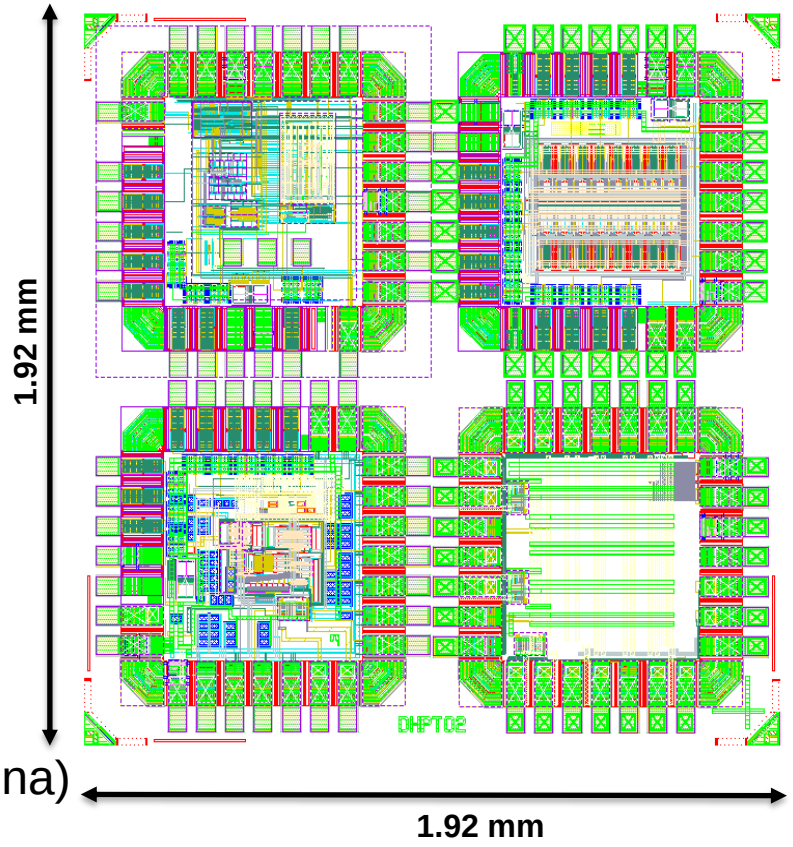
DHPT 0.1

- High Speed Link
  - 1.6 GHz PLL
  - Differential 1.6 Gbit CML driver with programmable pre-emphasis
  - Low jitter (~ 80ps)
- Analog Front-end (4 types)
  - 2 charge sensitive amplifiers
  - 2 comparators (static & dynamic)
  - ~ 36×25 µm²
- Memory Test
  - Different memory types, compiled SRAM & custom register file
  - JTAG interface
- Analog Periphery Blocks (University of Barcelona)
  - 8 bit current steering DAC
  - Temperature independent current reference



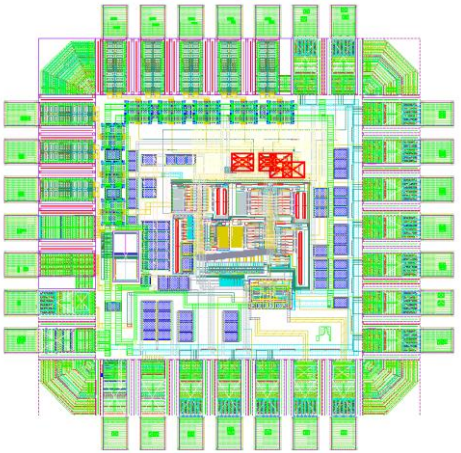
DHPT 0.2

- Pixel Array
  - Array of 32 pixels
  - Four flavors (as in DHPT 0.1)
  - Small size (~25×60 µm²)
- ADC (8 bit, 10MS/s)
  - Low area (30×70 µm²)
  - Low power (40 µW @ 10 MS/s)
  - Asynchronous
  - Good linearity (INL, DNL < 0.4 LSB)
- LVDS TX/RX
  - Rail-to-Rail 1.8/2.5V LVDS Receiver
  - 1.8/2.5V LVDS Transmitter
- Temperature Sensor (University of Barcelona)

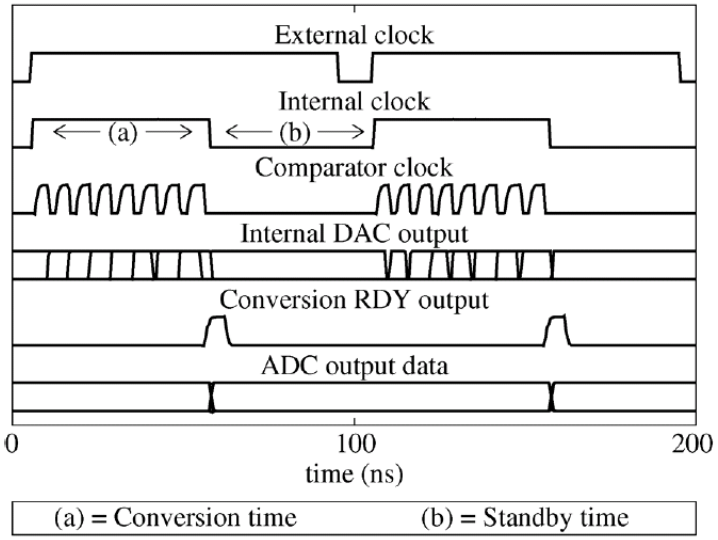


DHPT 0.1 – Low Power ADC

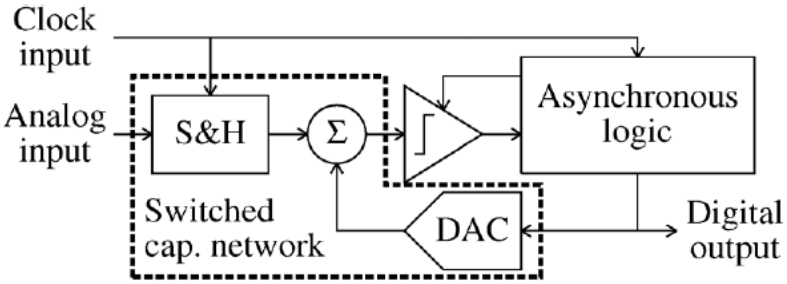
- 8bit ADC
  - 10 Msps
  - Charge redistribution
- Asynchronous operation → low power
  - No clock distribution needed
  - Sample signal triggers digitization sequence
- Serial LVDS data out



T. Hemperek, T. Kisisita



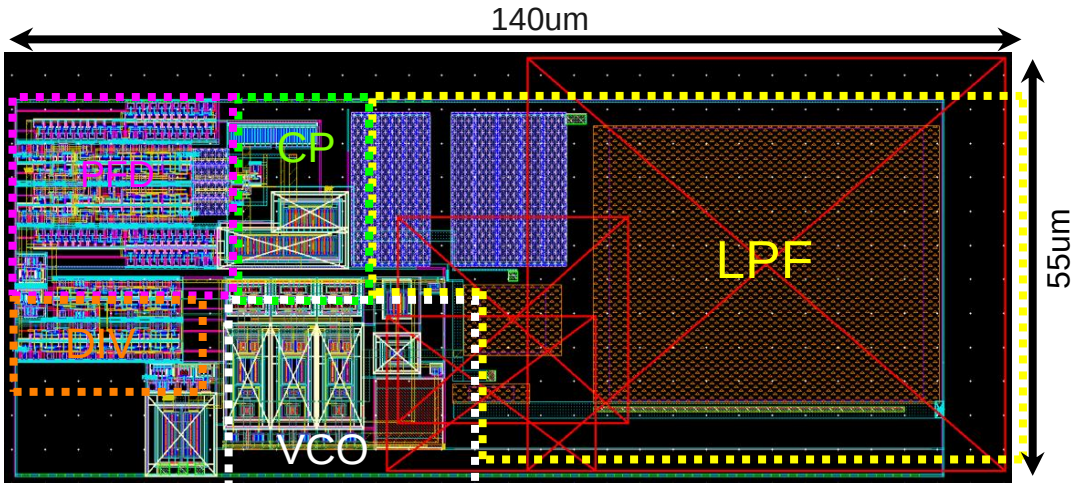
Asynchronous ADC timing



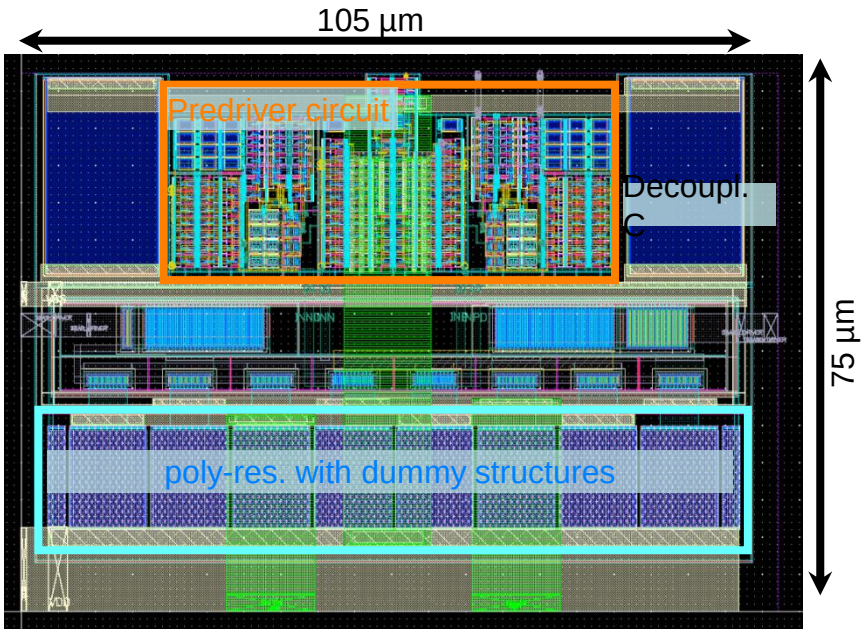
Function Diagram

Layouts

PLL

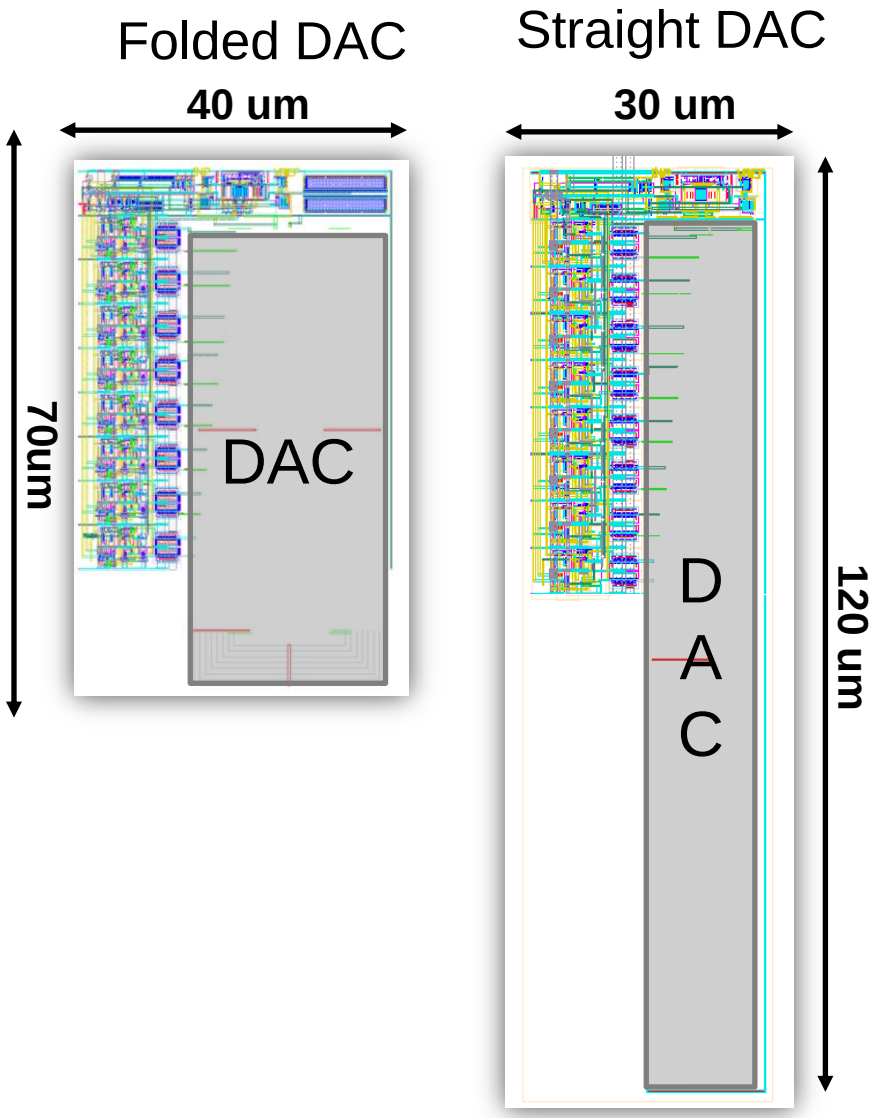


CML driver



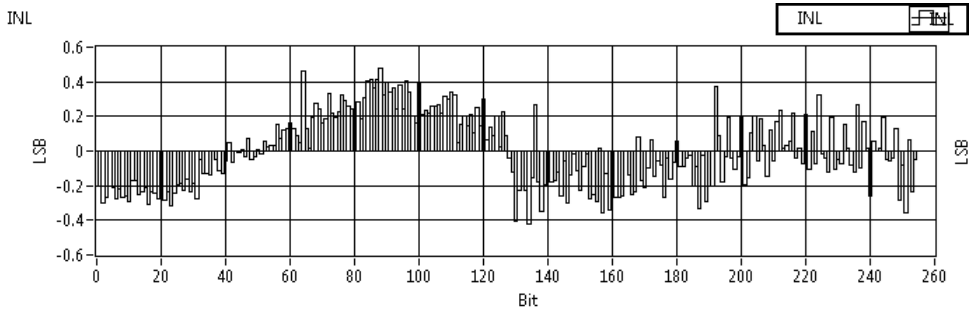
DHPT 0.1 – ADC Layout

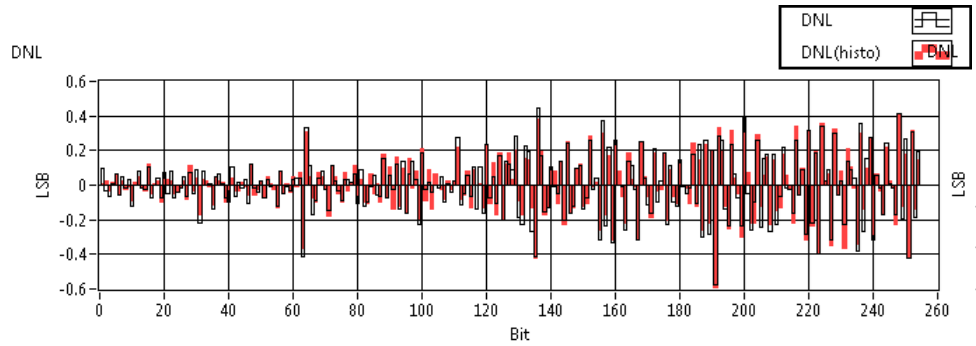
- ADC area dominated by DAC
- Switched capacitor DAC layout critical for DNL performance
- 8 bit ➔ 7 bit: half size



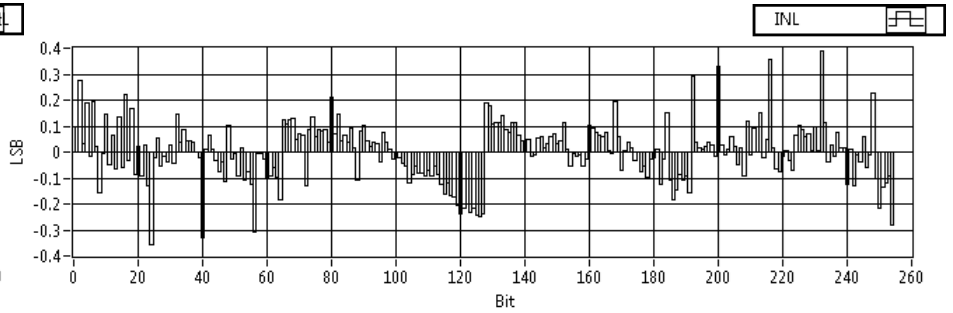
Asynchronous ADC Measurements

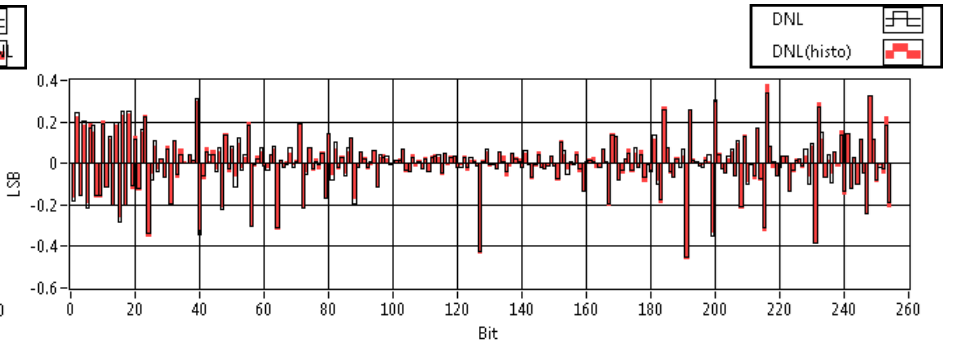
Single Ended Mode





Differential Mode





- Measured at 10 MHz sample rate
- Power consumption: ~40uW
- Works up to 12.5 Msps

General purpose IP Blocks in 65nm

- Distributed by CERN
  - SRAM compiler (*access fee apply*)
  - I/O pad library
  - Monitoring ADC
  - Bandgaps
  - Rad-hard to 200Mrad according to specifications
  - Deliverables
    - Schematic (OA)
    - Layout (OA)
    - Abstract (OA)
    - .lib (Liberty) capacitance limits and timing if applicable
    - Verilog / Verilog-AMS models
    - Datasheet

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