HV-MAPS-Track Triggers

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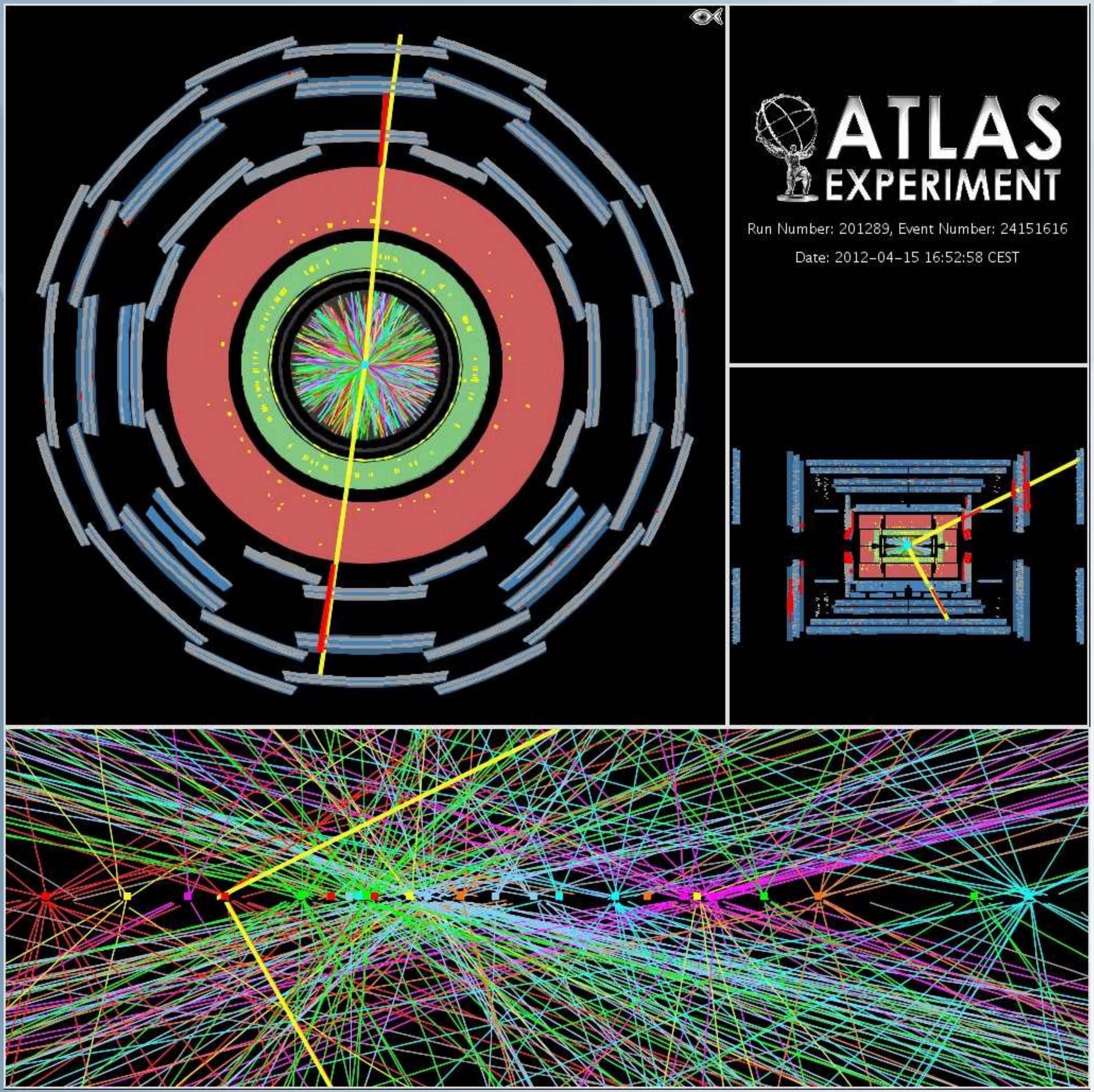
8. Terascale Detector Workshop

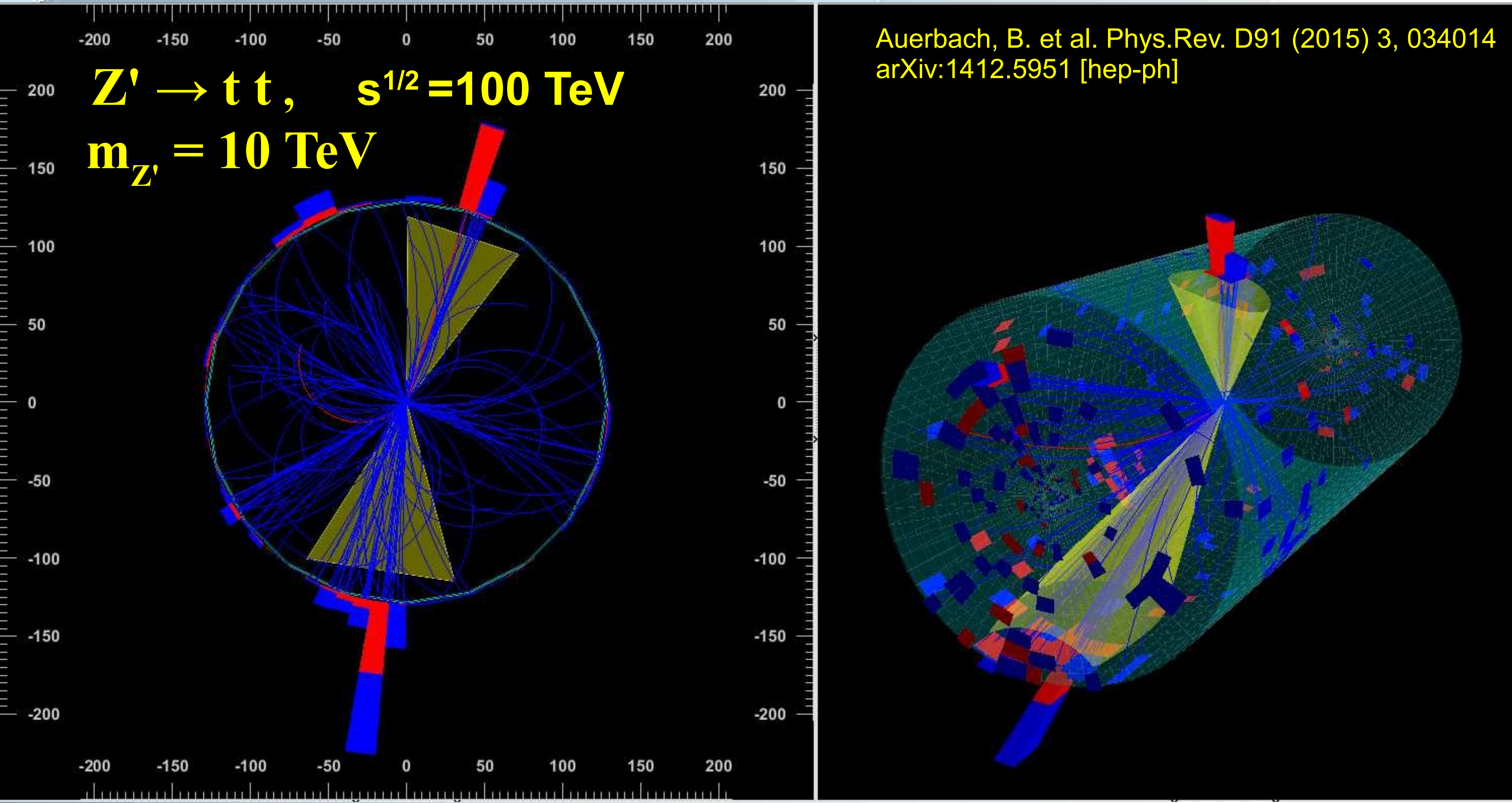
Berlin 2.-6.3.2015

Track Trigger Motivation for LHC



- **Improve lepton/hadron separation**
  (in combination with calori-meters and muon detectors)
- **Pileup suppression e.g. 2-lepton signature**
  (requires vertex reconstruction)

Track Trigger for Future Colliders



- **Tracks (trigger) can resolve highly collimated jets**

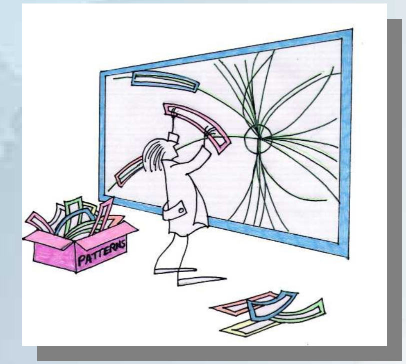
Track Trigger Concepts @ ATLAS+CMS

- **ATLAS FTK (Fast TracKer)** — **Run2+3**

- **ATLAS L1TT: Region of Interest**
- **ATLAS L1TT: Self Seeded**
- **CMS L1 Track Trigger (Self Seeded)**

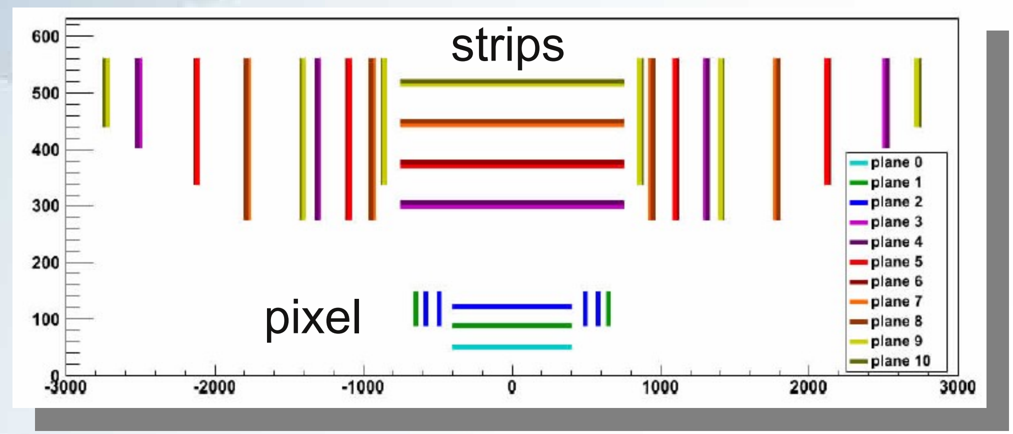
} **HL-LHC**

ATLAS Fast Tracker (FTK) Run2+3



ATLAS FTK (Fast Tracker)

- fast HW track processor for **Level2**
- **full event**
- **pixel+strip sensors**
- O(10000) associated memory chips (**AMchip**) for fast linking
- linearised track fits in **DSPs**
- latency **~50 µs @ 100 kHz**



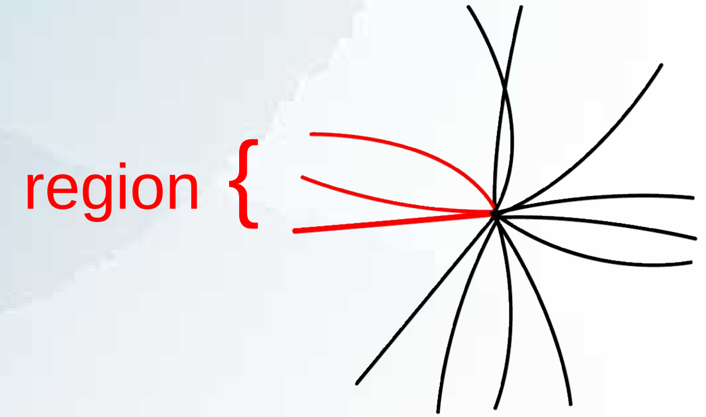
Main Disadvantages

- based on **previous trigger** Level1 trigger decision
- concept as such too **slow** for L1 trigger applications
- **not** designed for **HL-LHC**

ATLAS L1TT Region of Interest

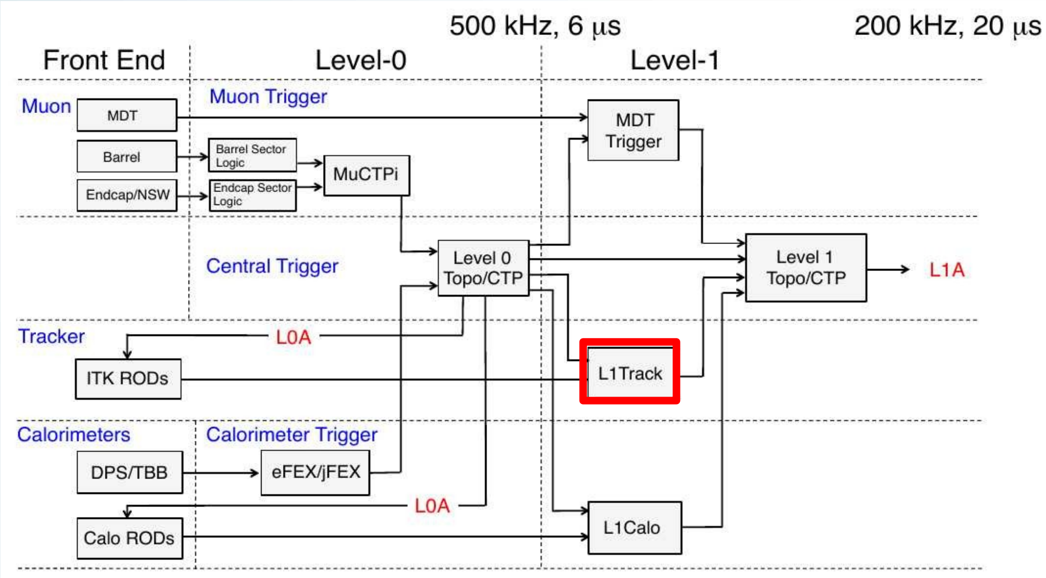
ATLAS Level 1 Track Trigger (L1TT) baseline design

- fast HW track processor for **Level1**
- **only region of interest**
- **pixel+strip sensors**
- highly parallel track linking (AMchip2020)
- latency **~10 µs @ 500-1000 MHz**
- need **extra L0 trigger** (Calo+Muon) to reduce event rate



Main Disadvantages

- **huge pattern banks** required!
- need **extra L0 trigger** (calo+muon) to reduce event rate
- only **partial track reconstruction** of the event

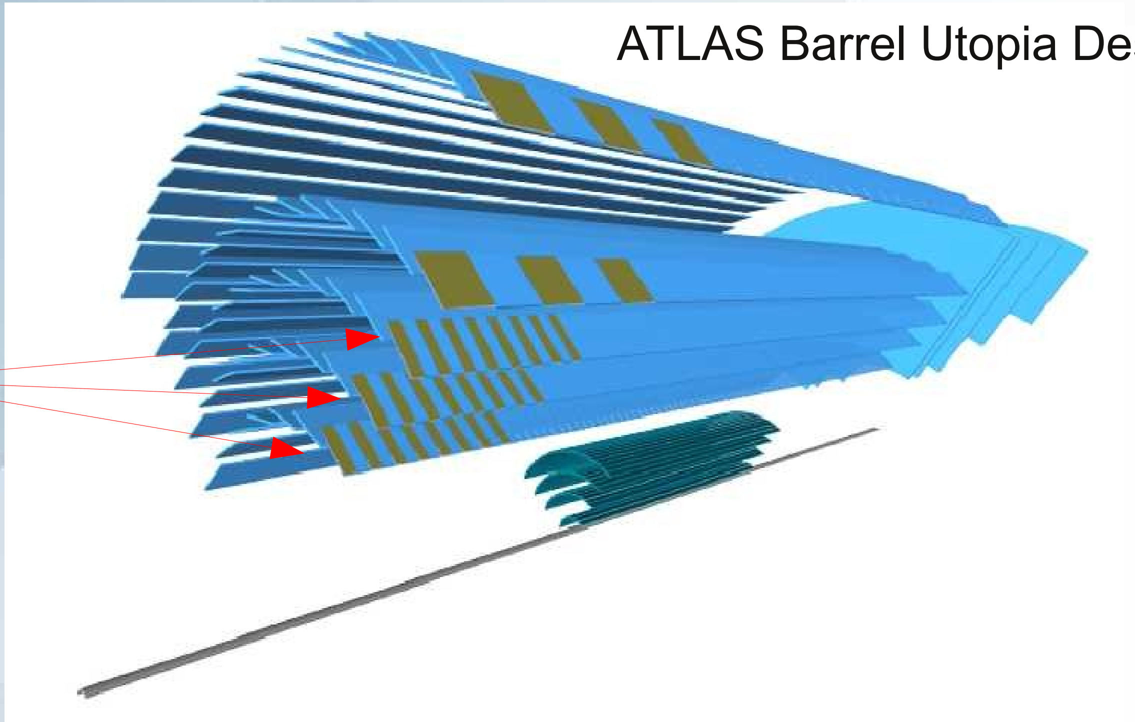


Track Trigger Bandwidth Problem

High-Luminosity-LHC: L ~ <10^{35} $cm^{-2}s^{-1}$

just 3 layers of short strips
(25 million channels)

→ 900 Tbit/s



ATLAS + CMS

Impossible to get all hit data out (for every bunch crossing) with nowadays readout technologies!

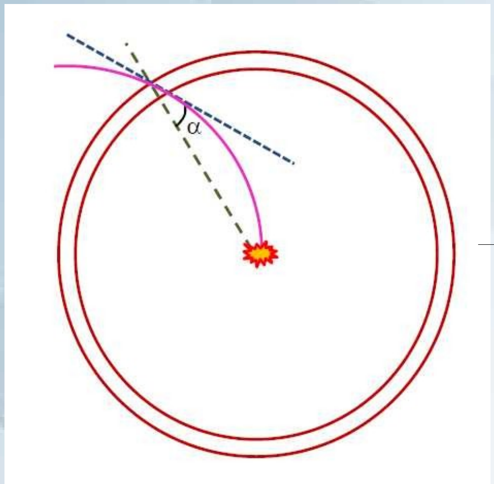
solution → filter hits

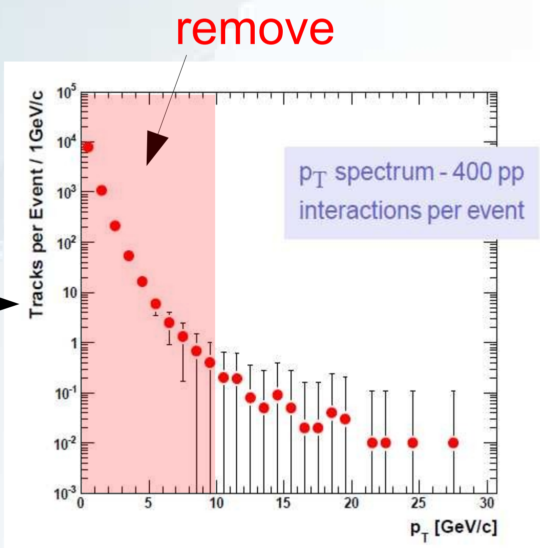
Frontend Hit Filtering

On-detector rate reduction by hit filtering:

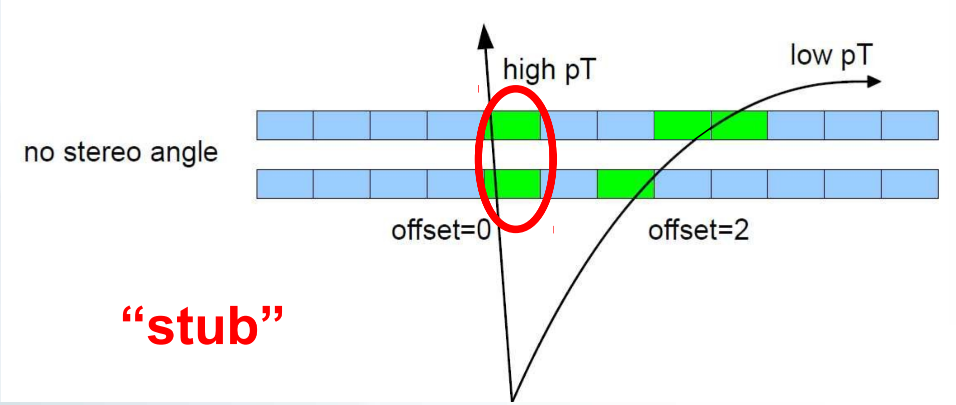
Vector Tracking!

exploiting beamline constraint





stacked layers (doublets):

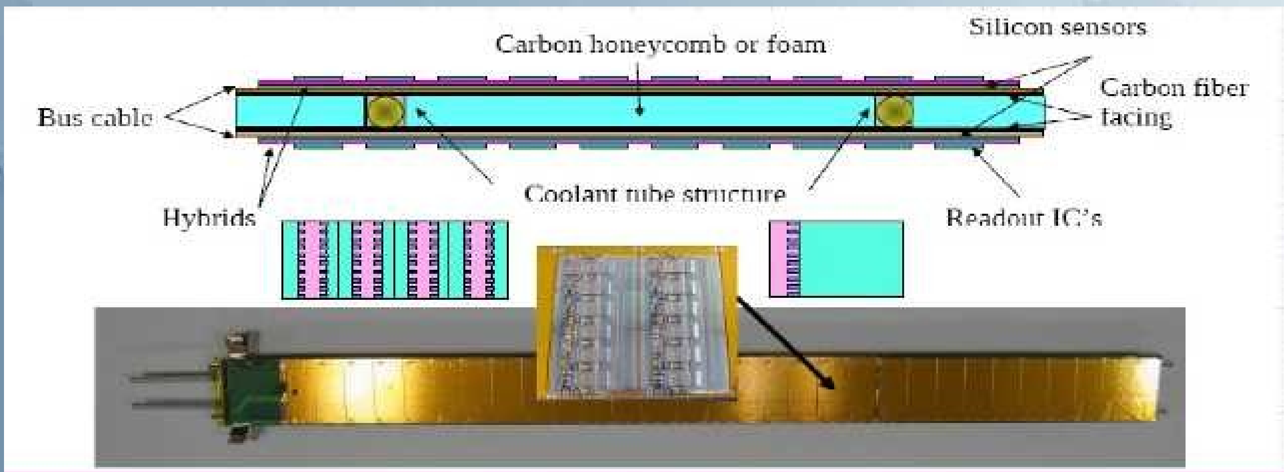


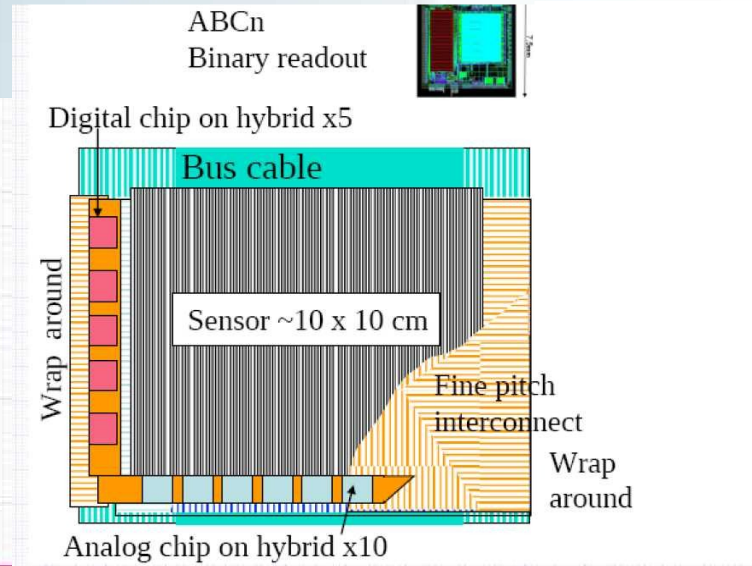
can also exploit cluster size

Local Coincidence (Stub Reco)

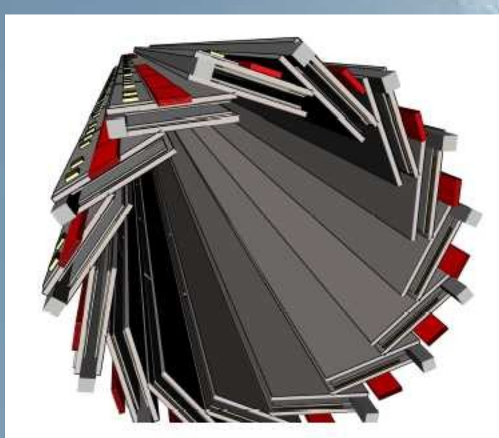
ATLAS

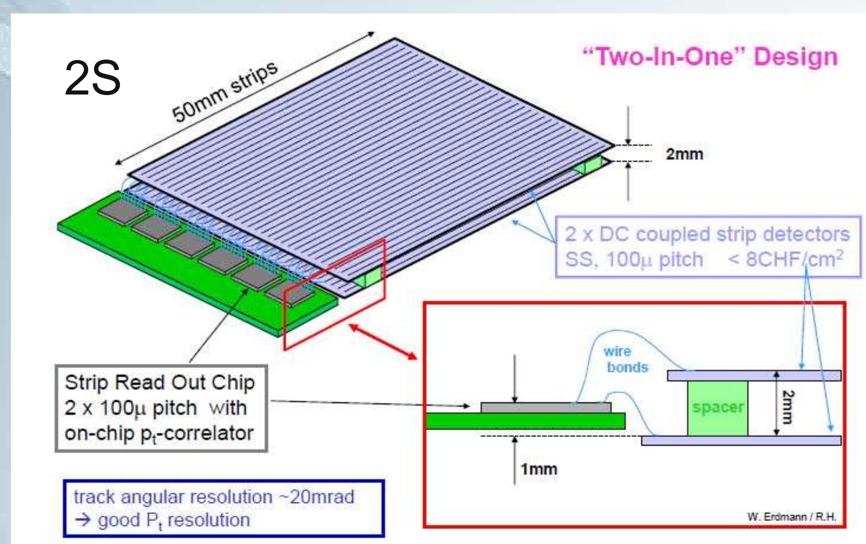
→ remove stereo angle in double strips
(not baseline design)

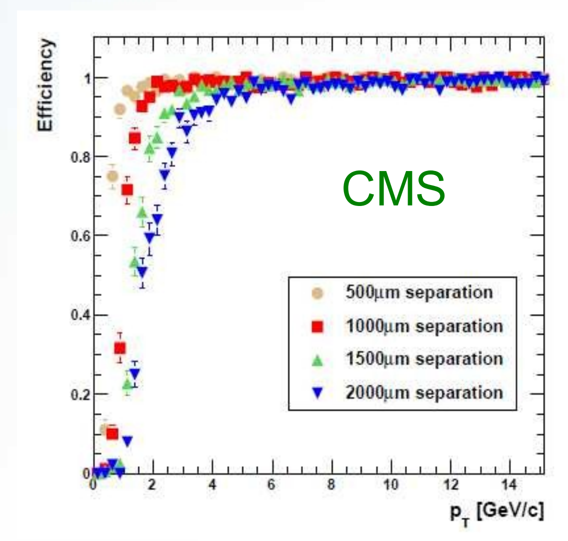




CMS



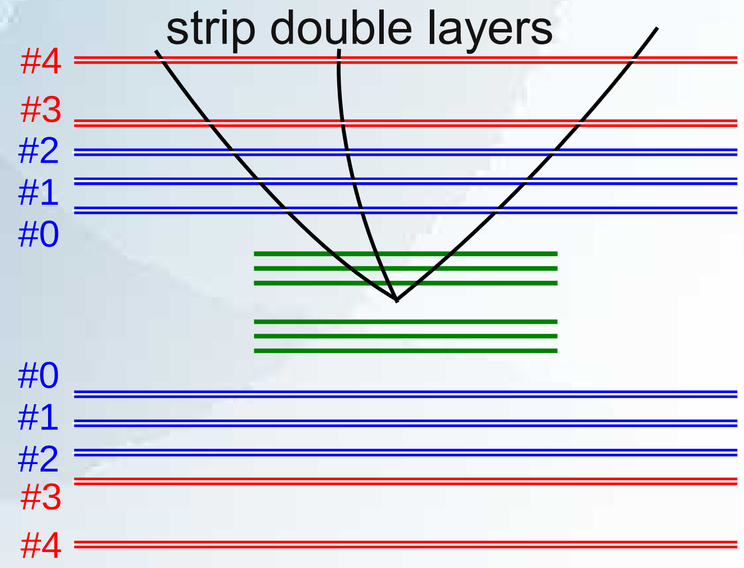




Challenges of Self-Seeded Concepts

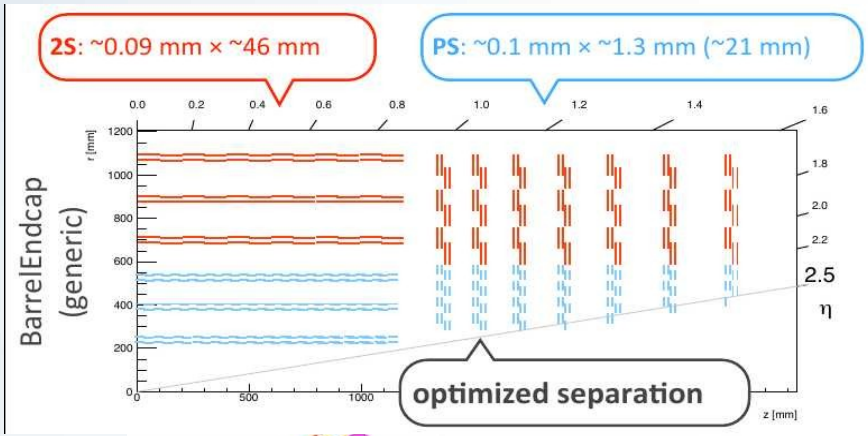
ATLAS L1TT Self-Seeded

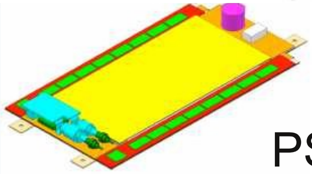
- cluster + coincidence filtering
- all 5 strip layers w/o stereo required for robust trigger
- track p_T>10-20 GeV



CMS L1 Track Trigger (Self-Seeded)

- design with strip-strip (2S) and pixel-strip (PS) modules
- optical link on every single module
- high bandwidth!



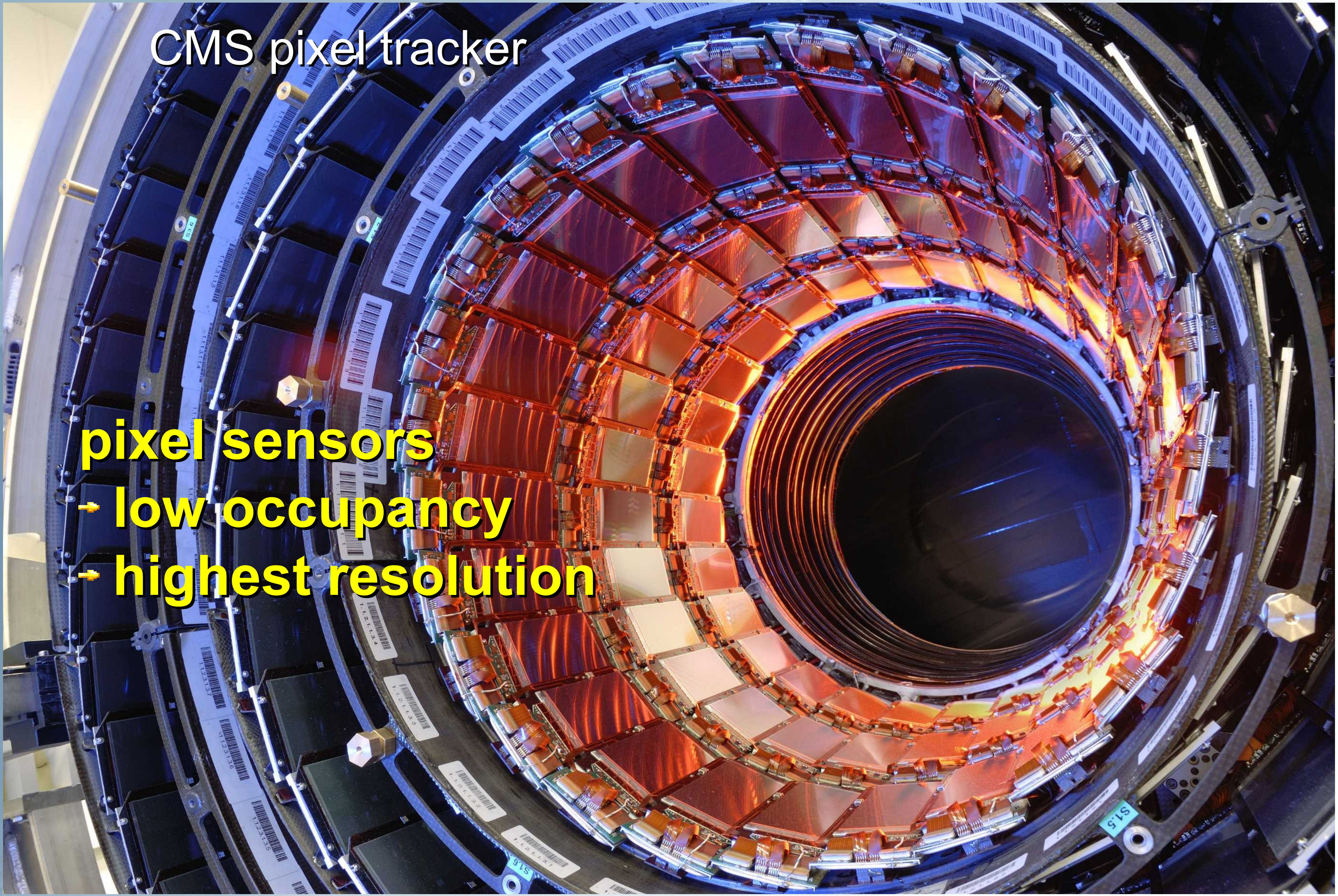


PS module

General concerns (ATLAS+CMS)

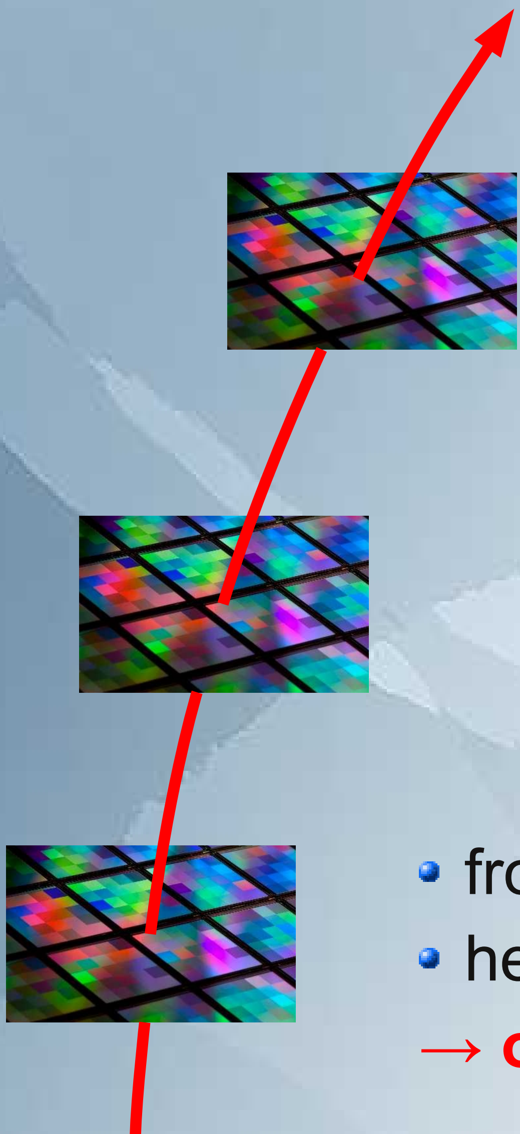
- **losses between modules**
- **loss due to (cluster) filtering**
- **bandwidth and power**
- **no z-vertex pointing (ATLAS strips)**

“Ideal” Tracking Detector Concept

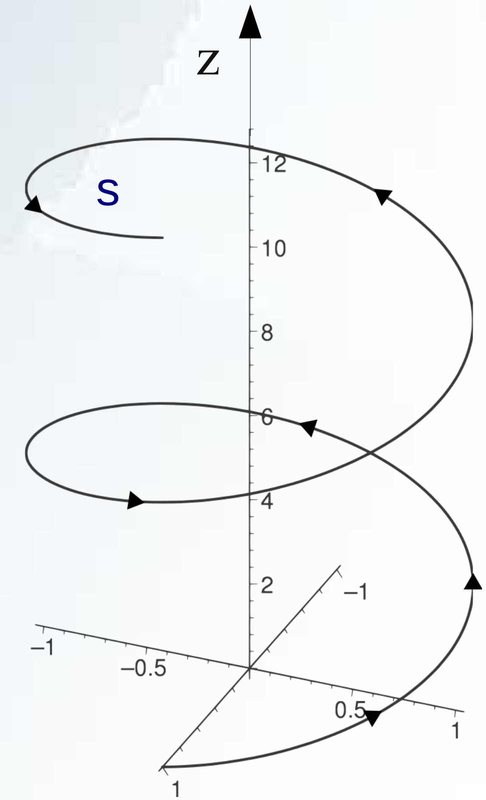


Track Parameters from Space Points

basic assumption: solenoidal magnetic field



3D tracking:
- **simple**
- **robust**

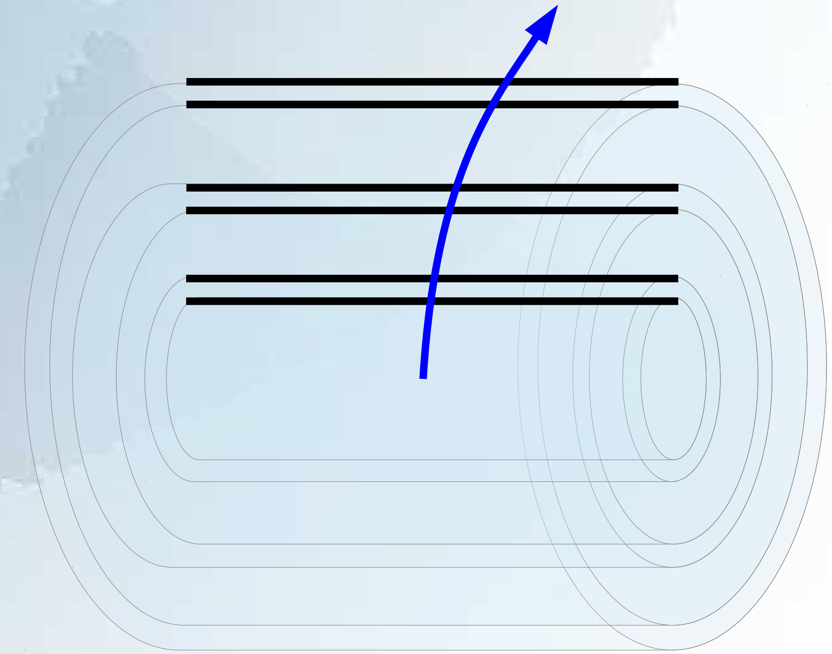


- from three planes → **9 parameters**
- helix and crossings described by **8 parameters**

→ **over-constrained fit**

Optimal Design for 3D Tracking

A: equidistant pixel layers

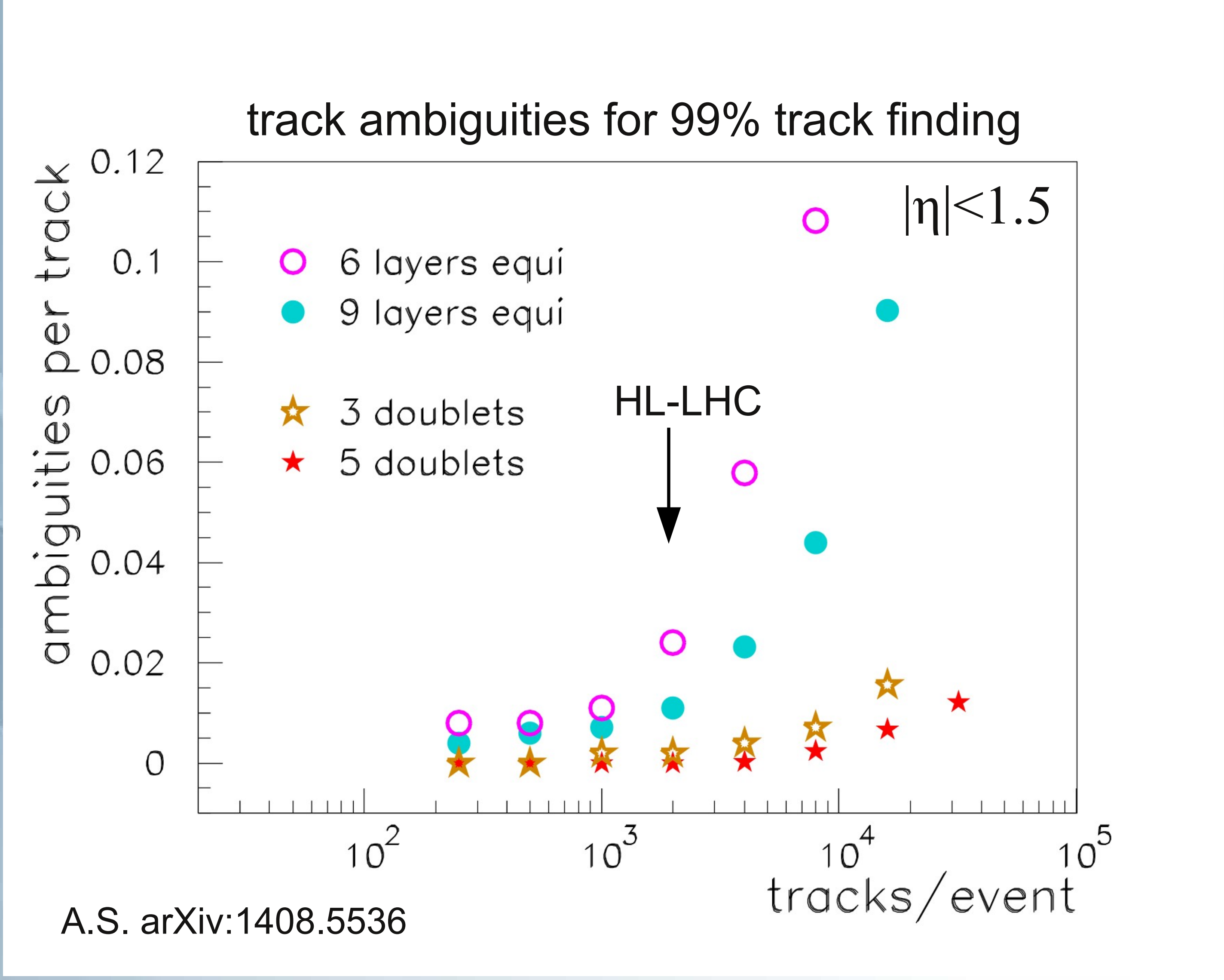


B: doublet pixel layers

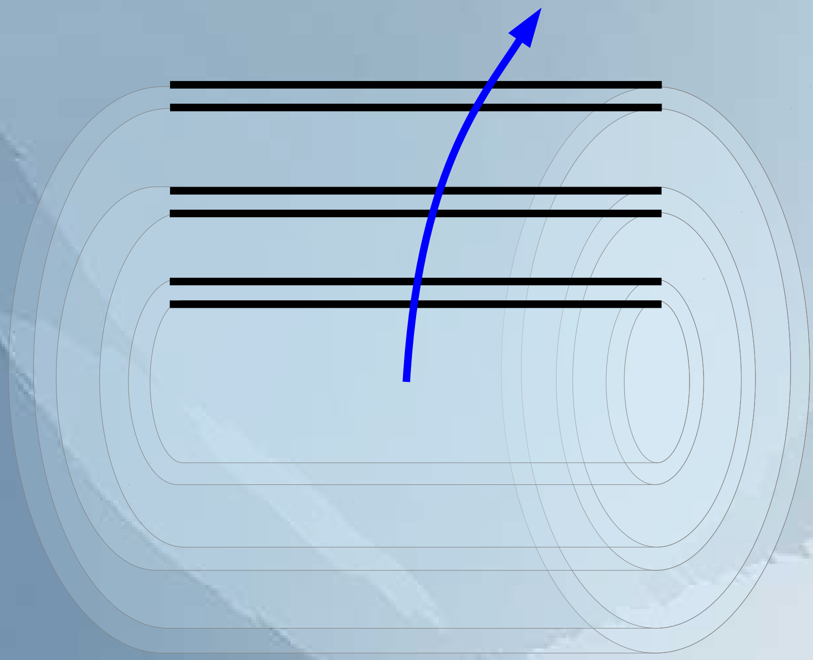
Track reconstruction @ HL-LHC:

which design has fewer track ambiguities?

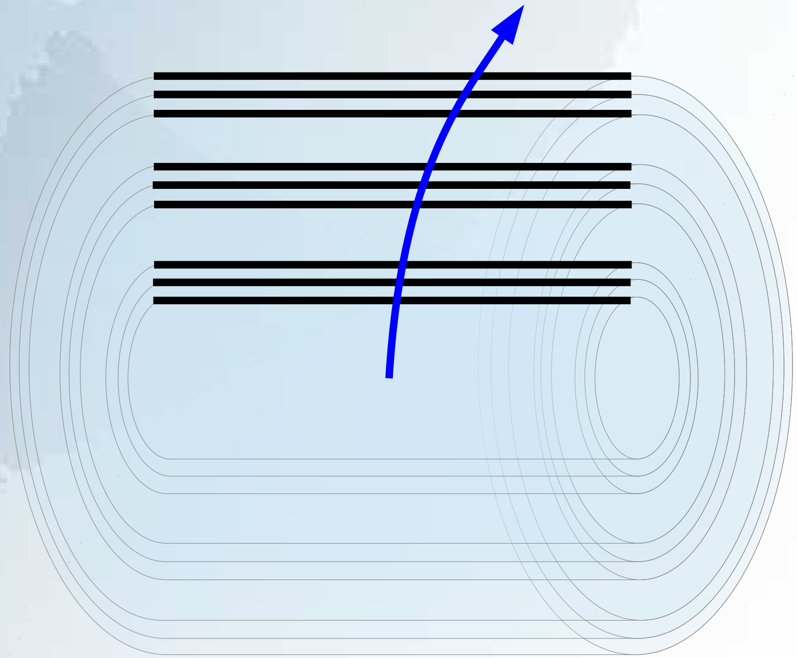
Track Ambiguities for Pixel Tracker



Optimal Design for 3D Tracking



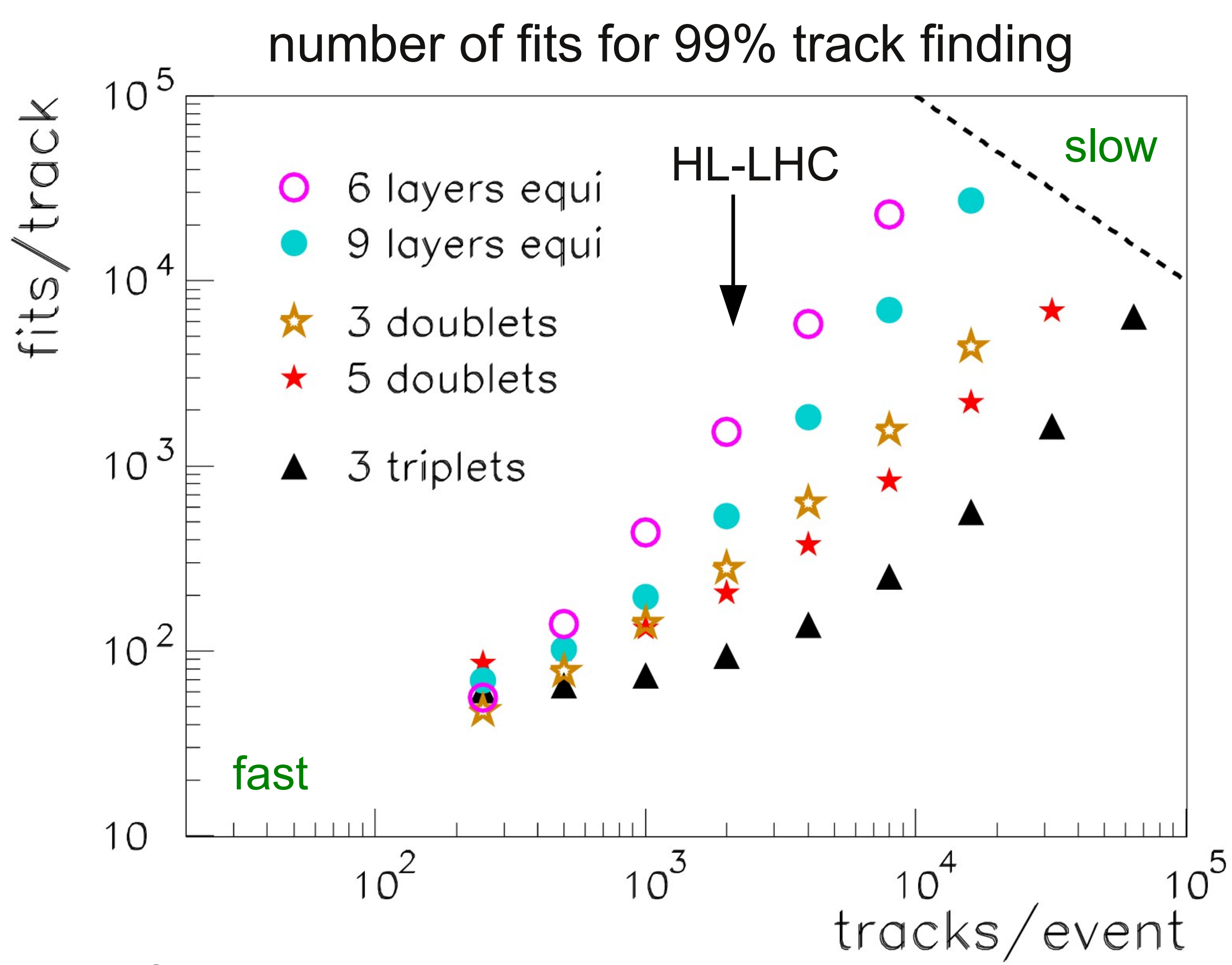
A: doublet layers



B: triplet layers

faster reconstruction?

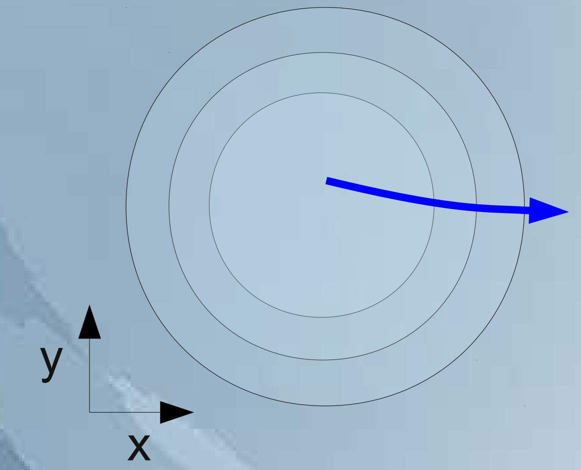
Pixel Tracker Reconstruction Speed

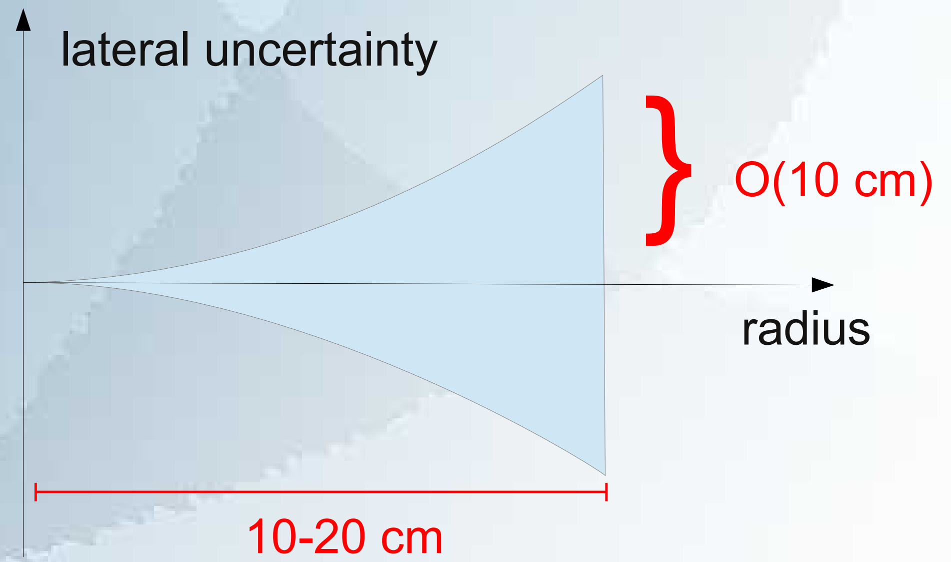


A.S. arXiv:1408.5536

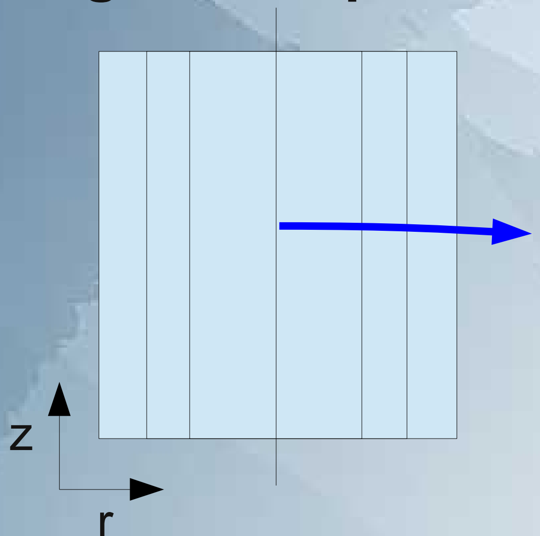
Track Extrapolation Uncertainty

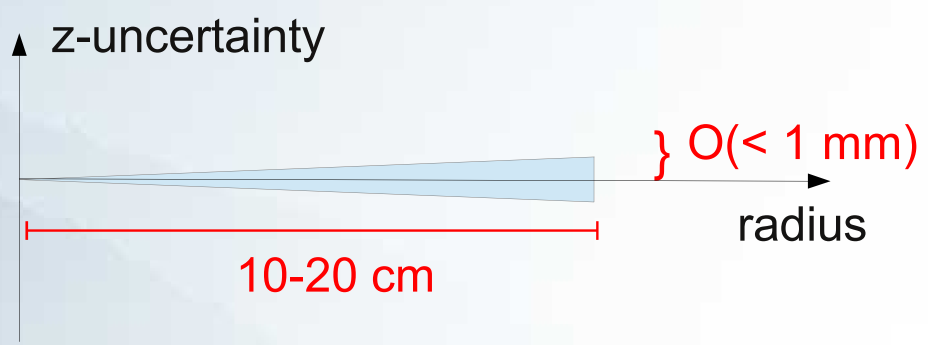
Transverse plane:





Longitudinal plane:





z-extrapolation is much more precise!

→ use pixel not strips for fast linking

First Summary

Would like to have a Pixel Track Trigger for several reasons:

- full 3D-tracking with only 3 layers possible
- high intrinsic redundancy and robustness
- track linking is fast and simple → trigger
- pixels allow to reconstruct event vertex with sub-mm precision

Pixel only Track Trigger?

Semiconductor Pixel Detectors

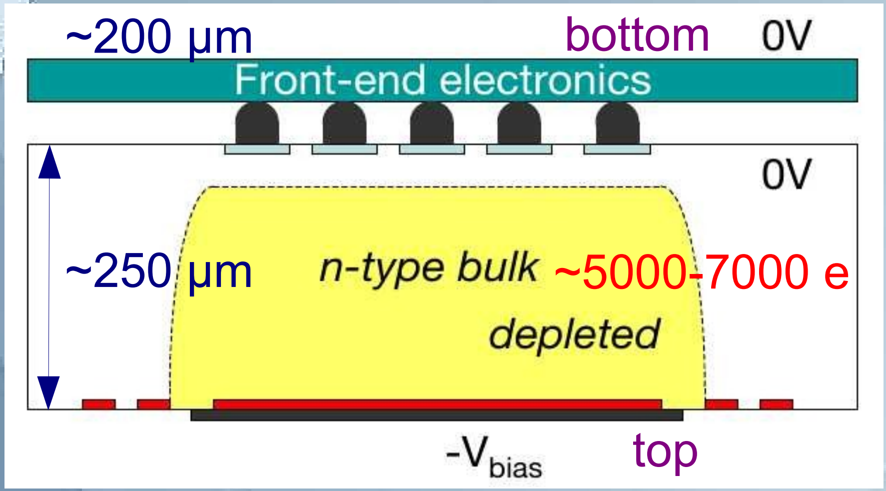
Advantages

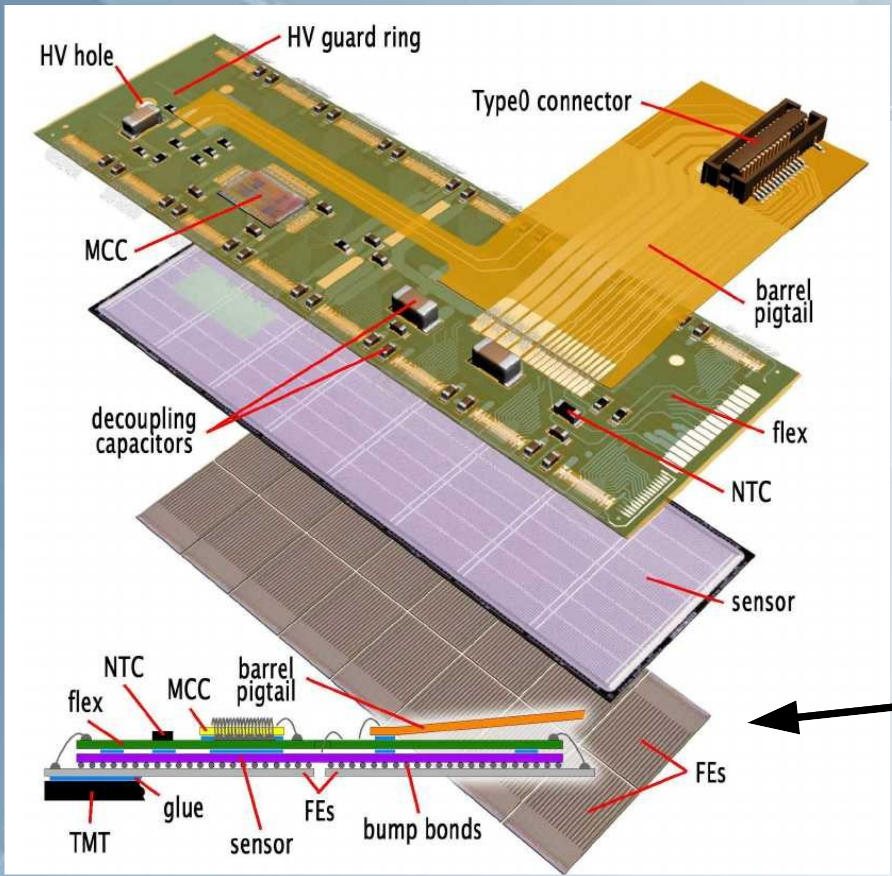
- fast signals → good for triggering
- small deadtime → good for triggering
- low occupancy (rate) → good for triggering
- high resolution (precision) → good for triggering
- 3D tracking (fast reconstruction) → good for triggering
- no ambiguities (less complexity) → good for triggering

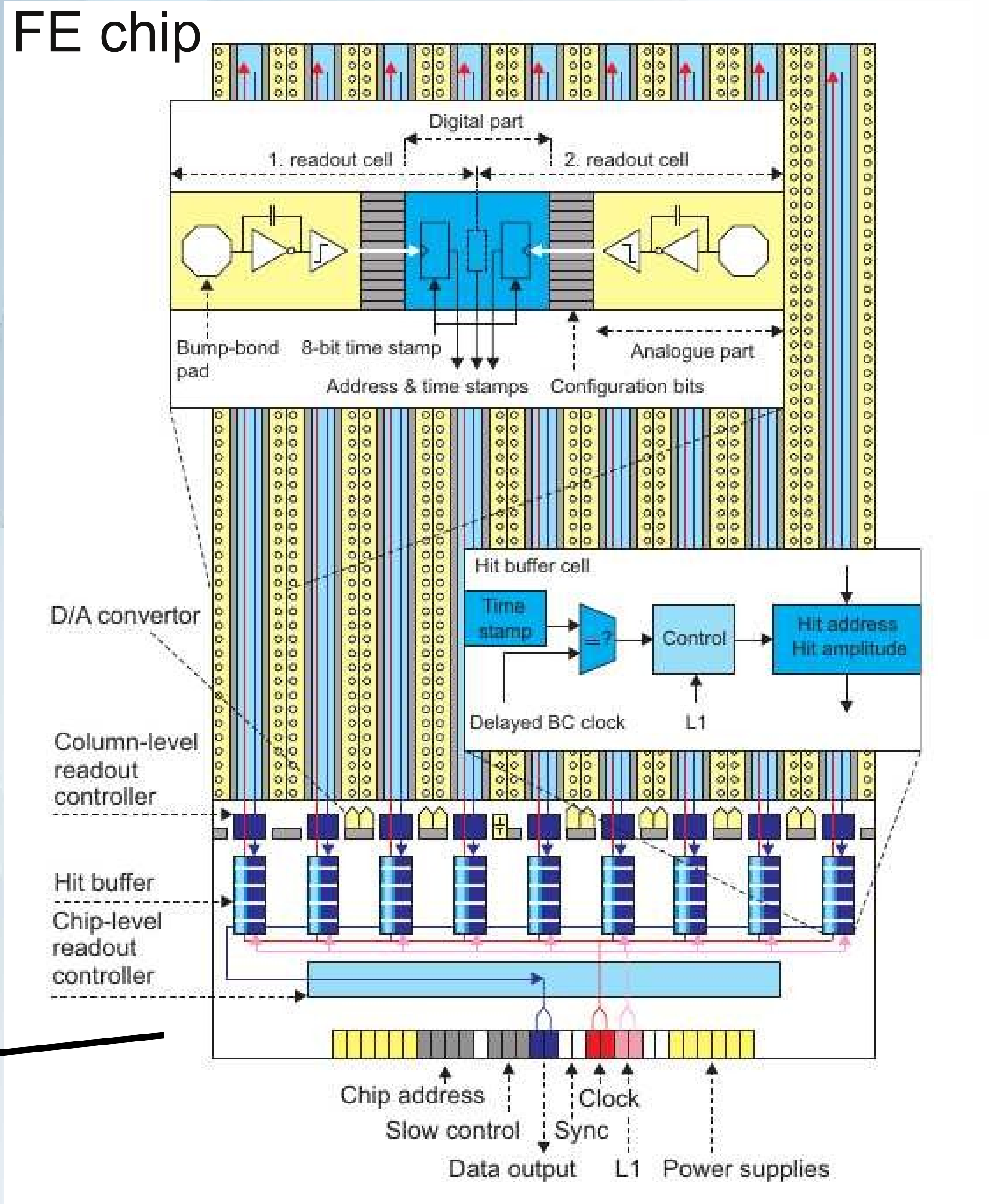
Backdraws

- power consumption → challenge for system design
- many channels → challenge for readout
- high entropy (information) → challenge for trigger processing
- small structures → scalability

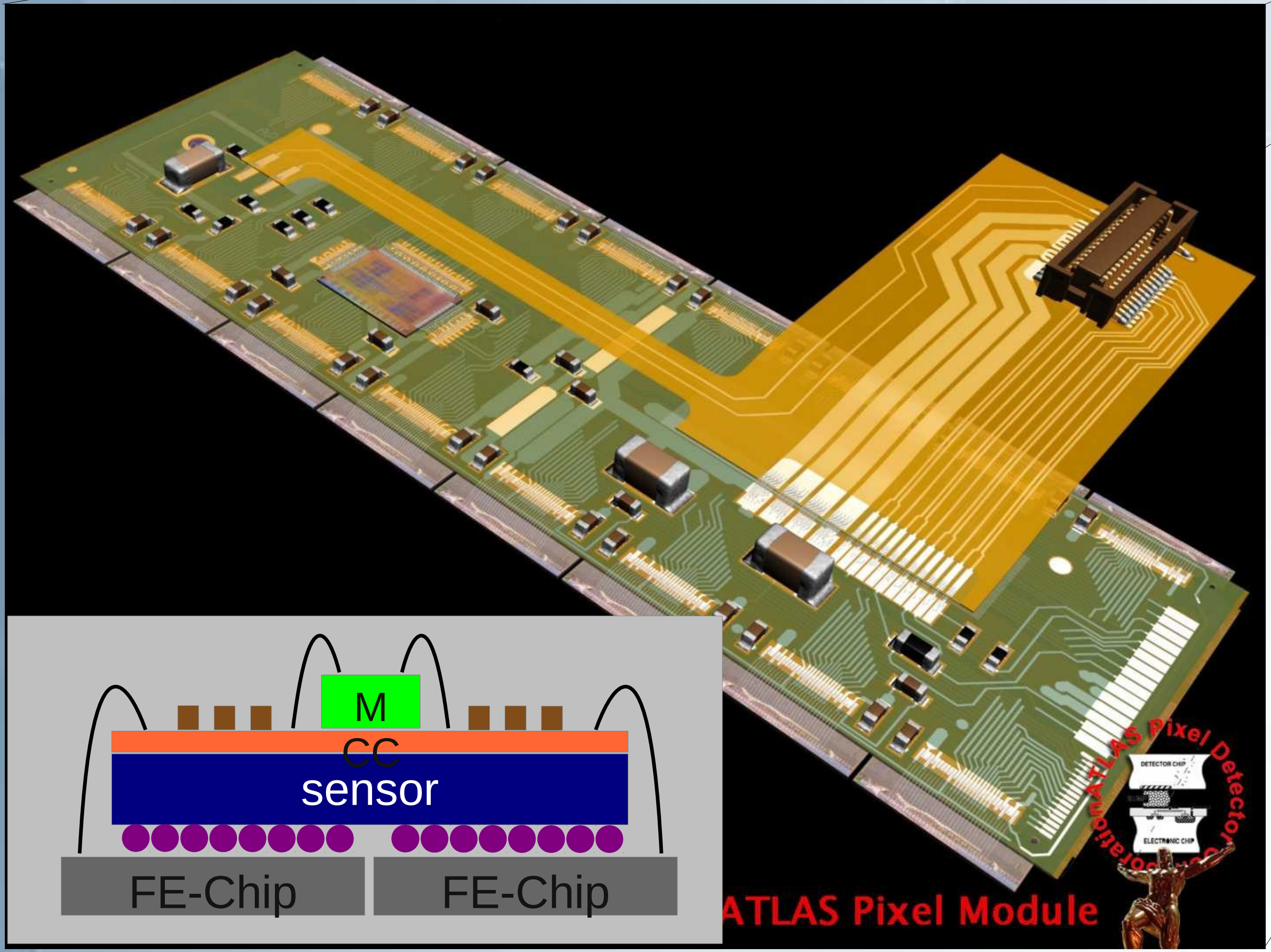
ATLAS Hybrid Pixel Module

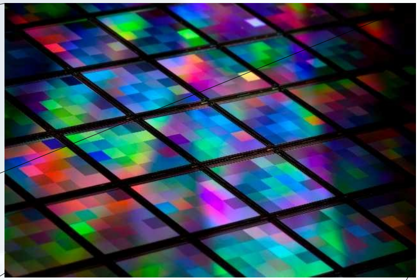






Detector System on Chip?





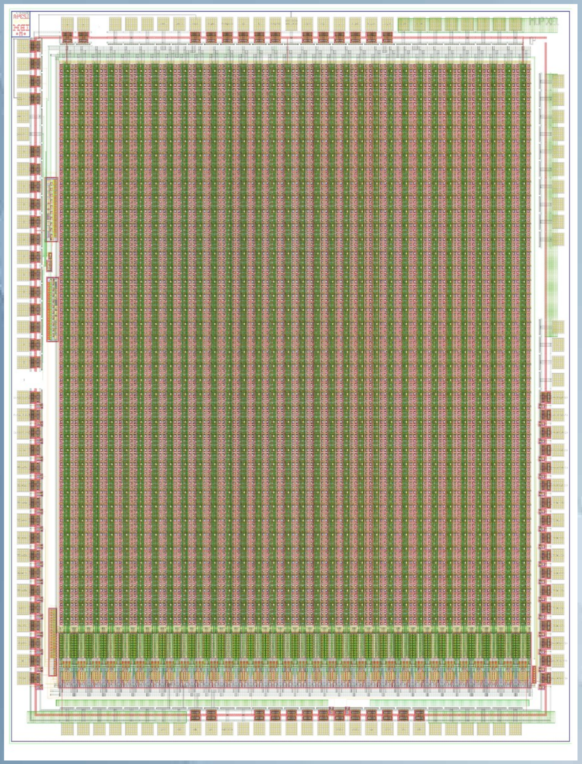
highly integrated chip

~ 10^8-10^9 pixels/m^2

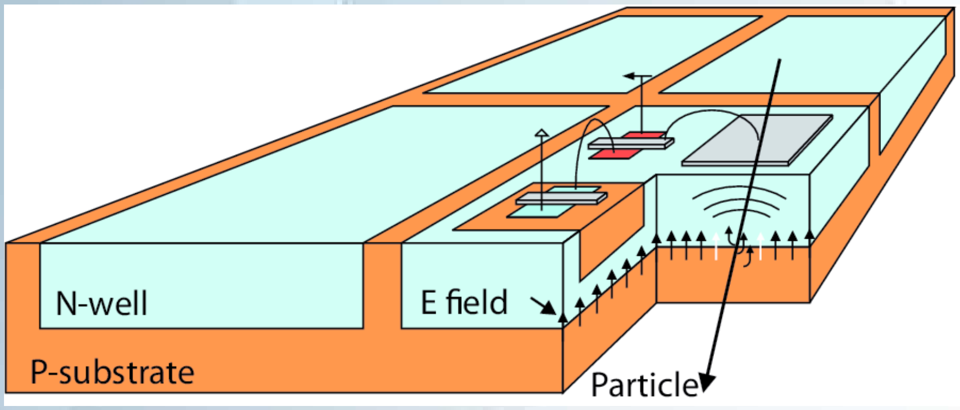
HV-MAPS Technology

Ivan Perić, NIMA 582 (2007) 876

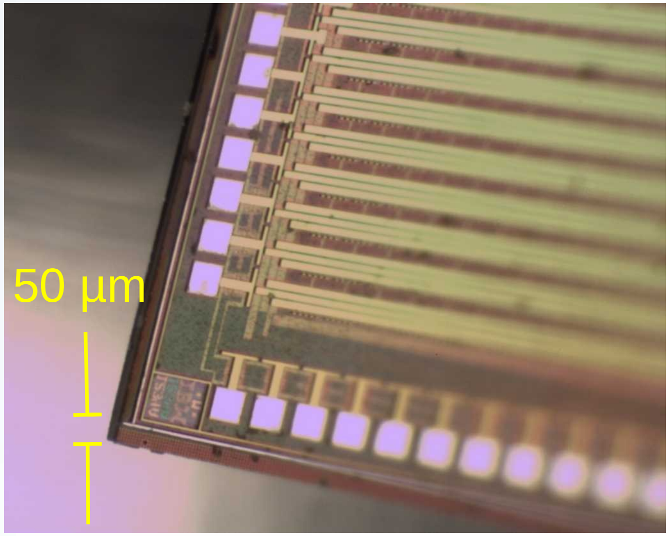
MuPix prototype



System on a chip: sensor + readout



- no composite - no interconnects
- simplified design (ASIC)
- sparsified readout (zero suppressed)
- fast signals
- low noise
- thin sensor!
- LVDS link



MAPS = Monolithic Active Pixel Sensor

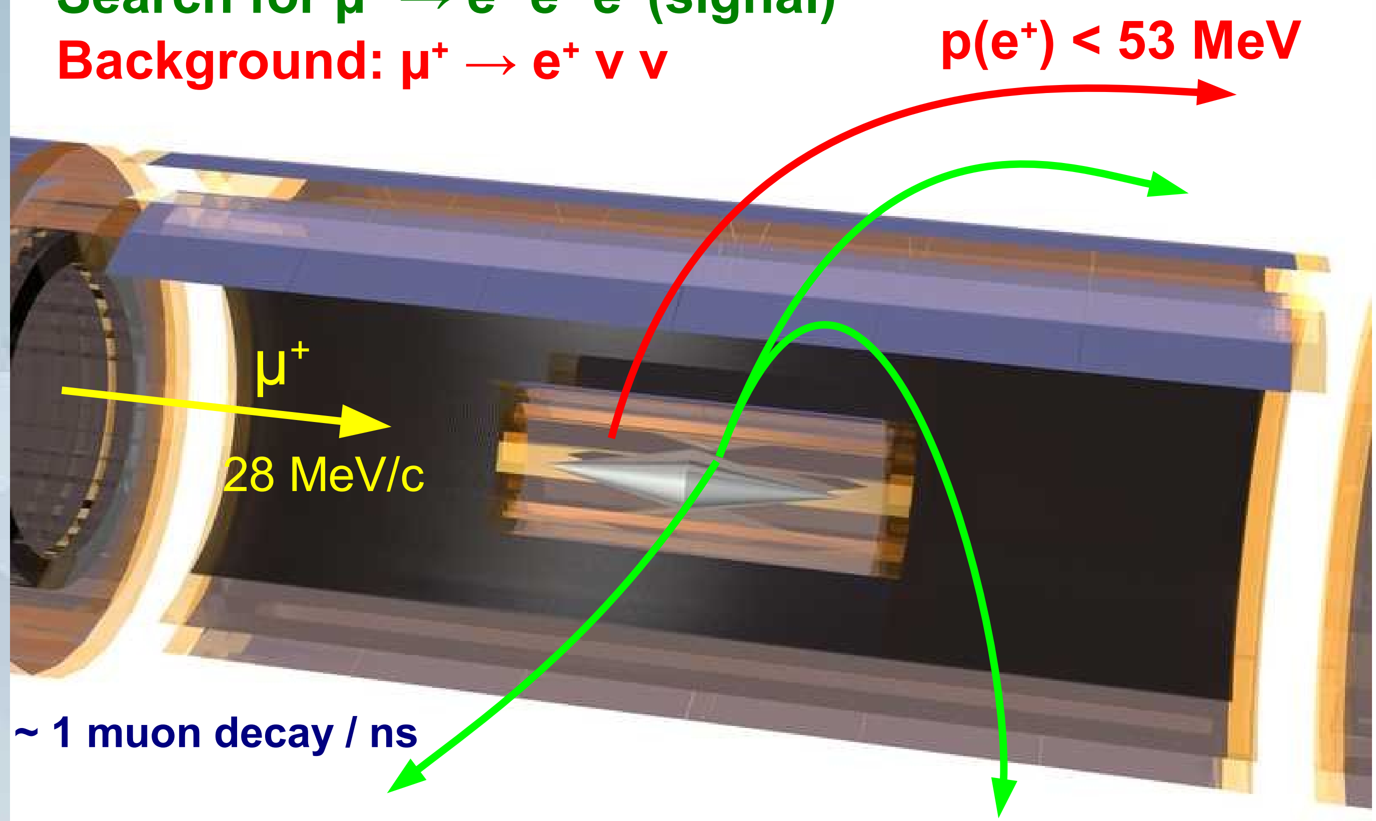
Mu3e Experiment at PSI

- beam with 10^9 muons/s
- muon stopping target
- 4-layer HV-MAPS tracker with 50μm thin sensors
- time-of-flight system
- magnet B = 1 T
- online filter farm

Aim: $BR(\mu^+ \rightarrow e^+ e^+ e^-) \sim 10^{-16}$

Search for $\mu^+ \rightarrow e^+ e^+ e^-$ (signal)

Background: $\mu^+ \rightarrow e^+ \nu \nu$



Fast and very thin detector required → MuPix sensor

Status:

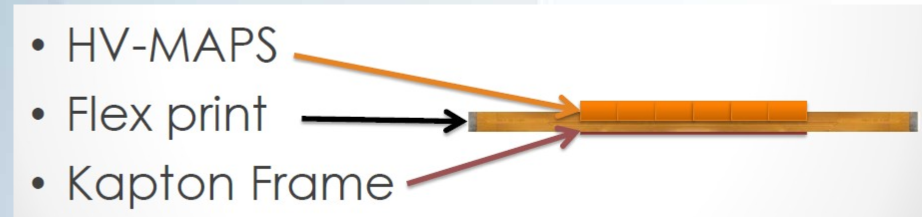
- R&D finalisation 2015
- construction in 2015-17
- commissioning in 2017

Mu3e-Tracker Construction

<u>Ultra-thin detector mock-up:</u>

- sandwich of 25 µm Kapton®
- 50 µm glass (instead of Si)

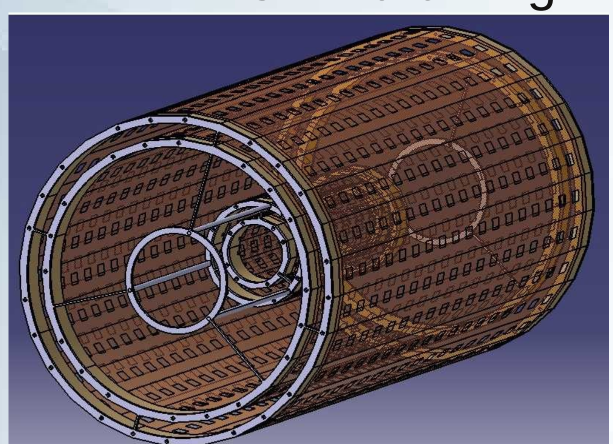
sandwich design:



He-gas cooling (<400mW/cm^2)

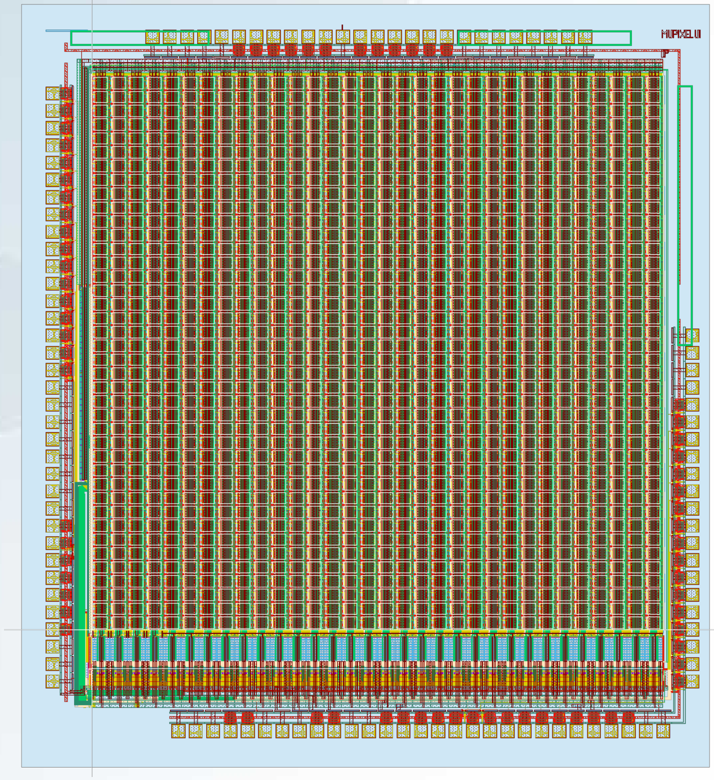
→ X/X_0 ~ 0.1% per layer

CAD drawing



50 µm silicon wafer

Mupix 7 Prototype Chip



Mupix7 parameters:

- ~ 3 x 3 mm^2
- ~1200 pixels
- pixel size ~ 80 x 100 μm^2 (huge!)

Mupix7 features:

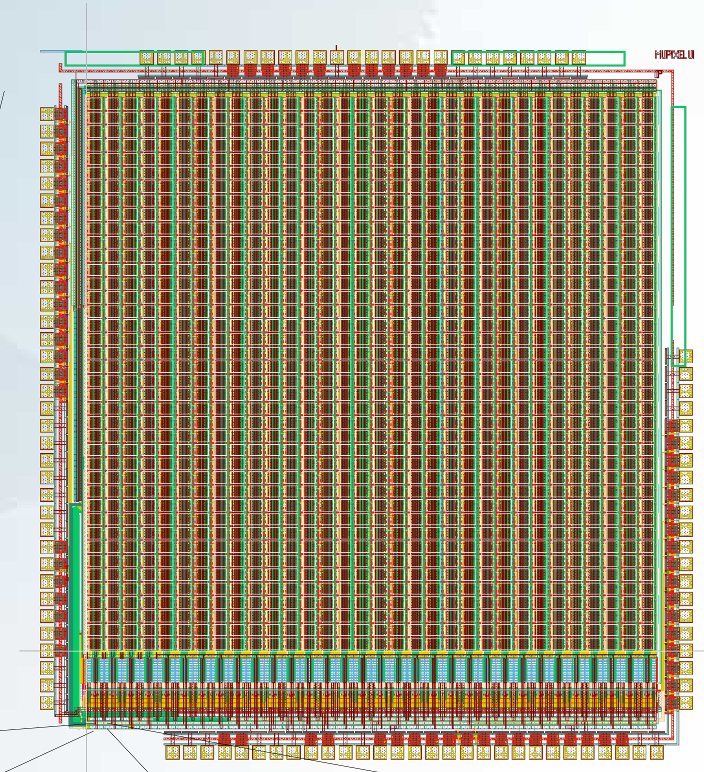
- tune DACs for every pixel
- double stage amplifier (every pixel)
- zero suppression + digital readout
- timestamp generation up to O(100) MHz → O(10) ns
- 1.2 GHz PLL
- integrated 1.2 (2.4) Gbit/s link
- about 40 pads (wire bonding)

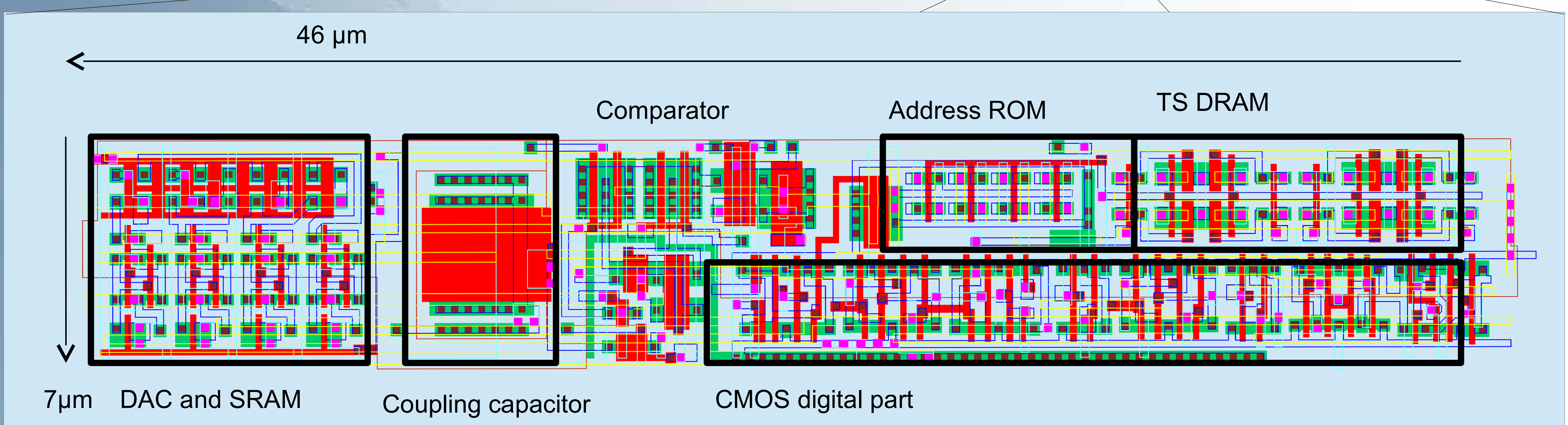
being currently tested!

Mupix Readout Design

Mupix7 prototype:

- ~ 3 x 3 mm²
- ~1200 pixels
- pixel size ~ 80 x 100 µm²

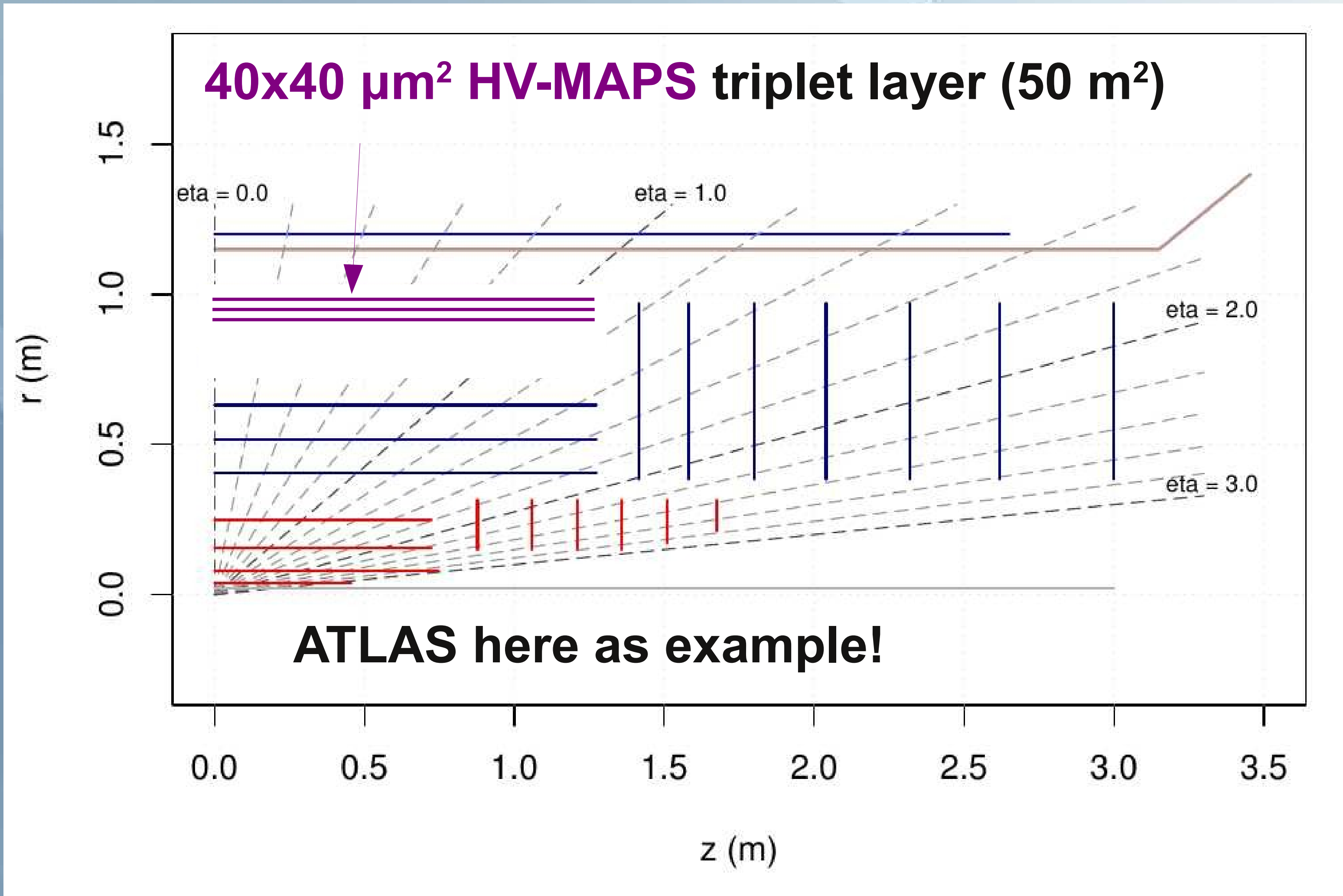




What now follows sounds crazy

but it is not!

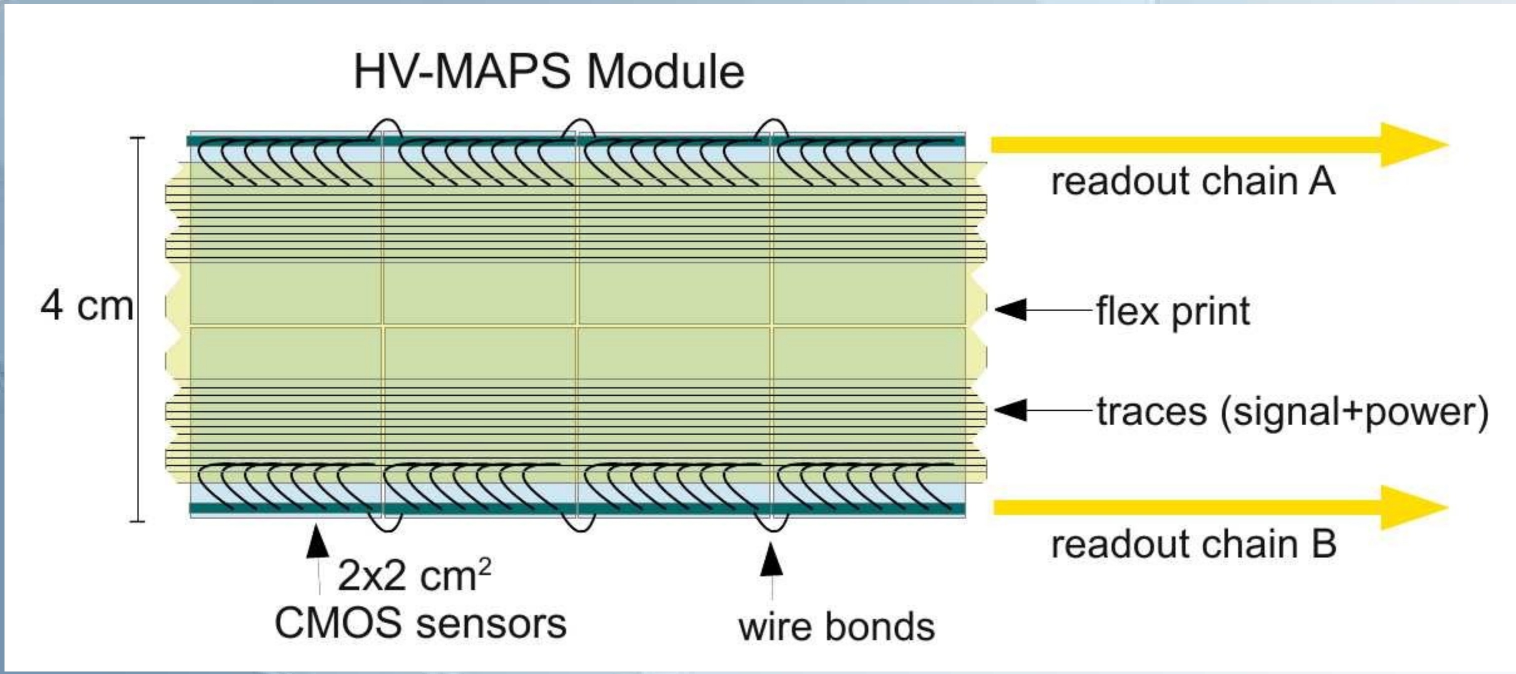
HV-MAPS Triplet Trigger Example

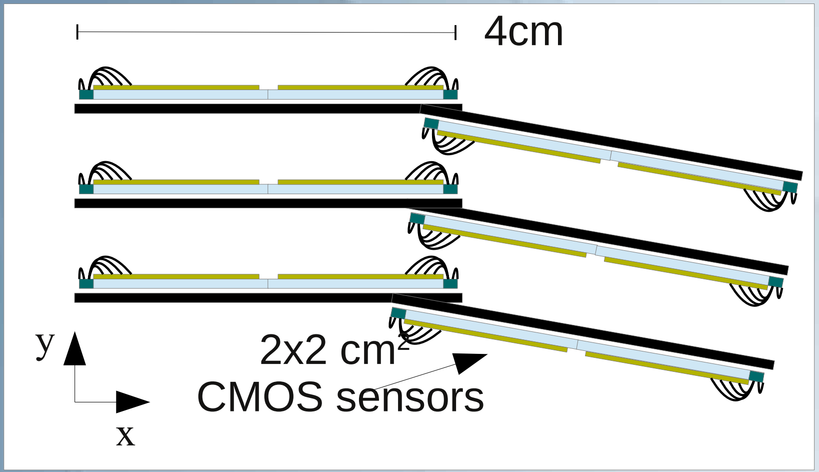


~ 6·10^{6} wire bonds to HV-MAPS (c.t. ~ 8·10^{6} wire bonds to 10 cm strips)

(BTW: 40 x 40 hybrid pixel would require 3·10^{10} bump bonds)

HV-MAPS Triplet Modules for LHC





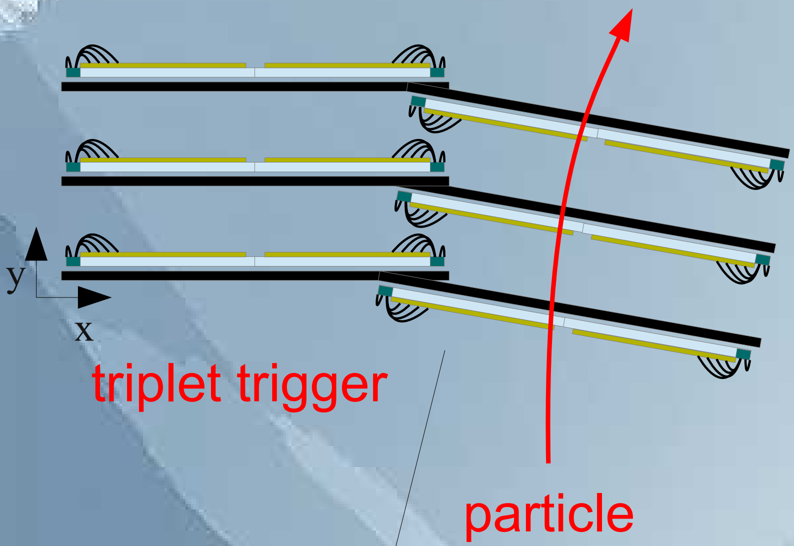
Basic design considerations

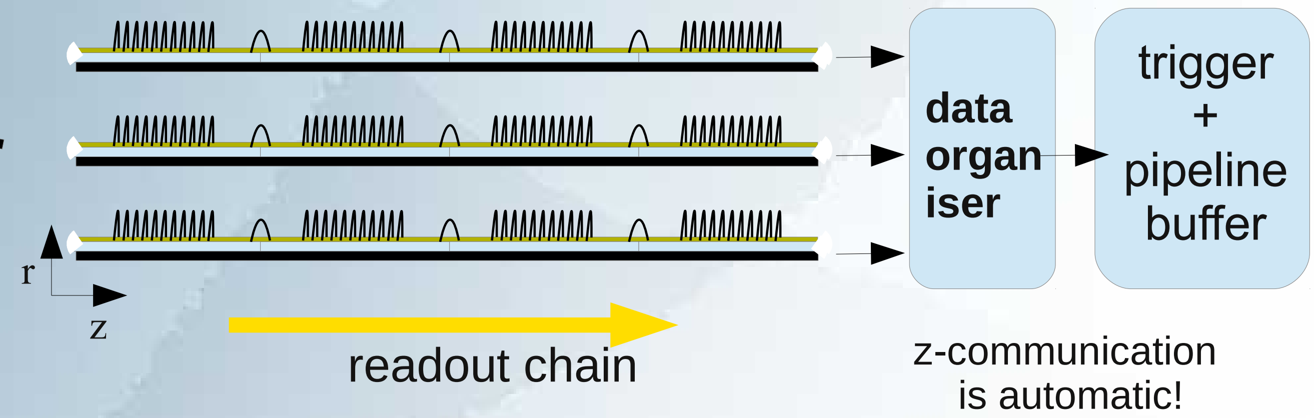
- modules from **2 x 2 cm²** reticles
- glued on kapton flexprints (LVDS RO)
- pixel size **40x40 μm²**
- power goal **100 mW/cm²**
- X/X_0 ~0.1% per layer w/o support+cooling
- module size e.g. **100-150 x 4 cm²**

HV-MAPS Trigger Triplets

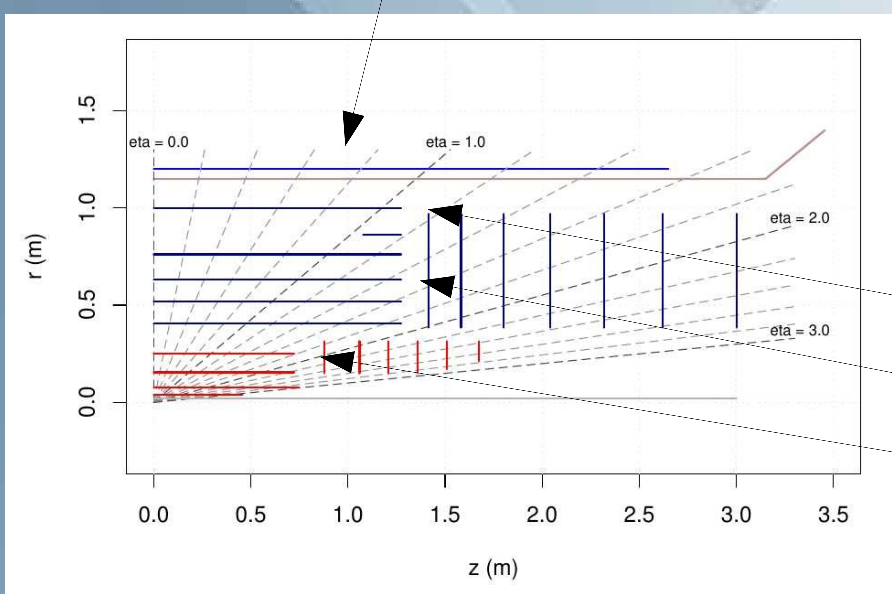
→ standalone tracking + first level trigger

arXiv:1408.5536





~ 1% momentum resolution @ 1 GeV

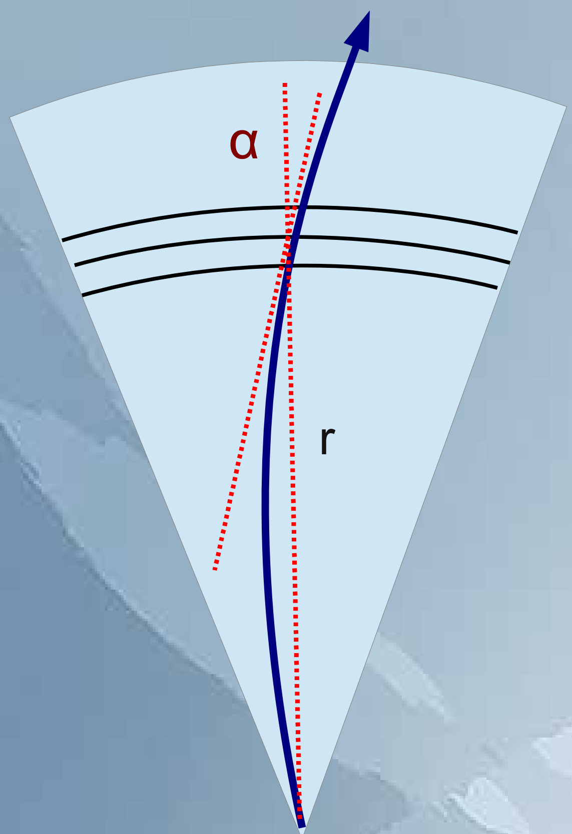


Rate Estimates for HL-LHC $|\eta|<1.5$

triplet radius	#ladders	data rate/ module (Gbit/s)	#hits per half-ladder	proces-sors
100 cm	164	24	$0.24 \cdot 10^9$/s	330
60 cm	100	40	$0.4 \cdot 10^9$/s	200
20 cm	36	120	$1.2 \cdot 10^9$/s	70

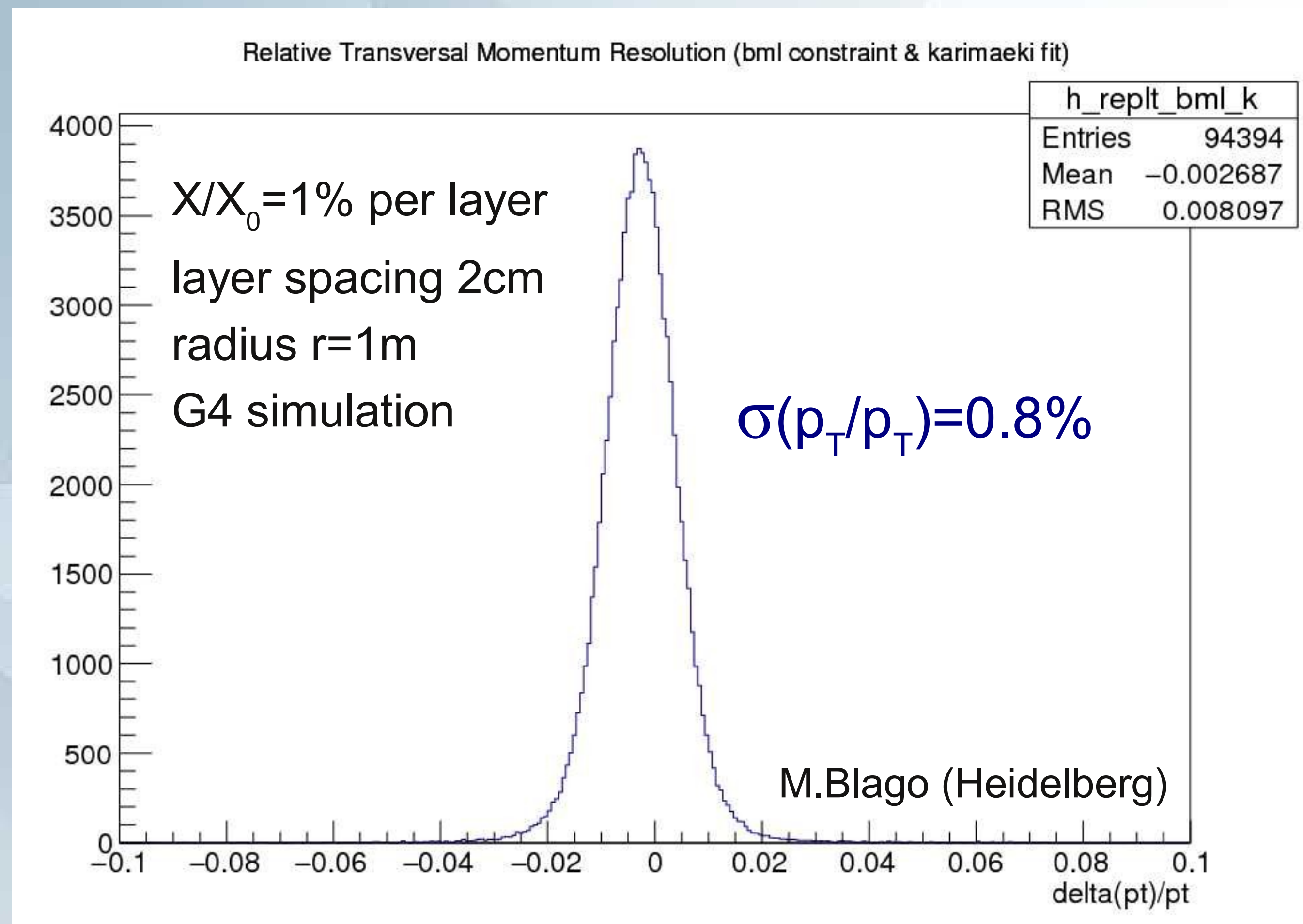
→ z-vertex reconstruction on mm-scale!

First Simulation Results



$$p_T \propto \frac{r}{2\sin(\alpha/2)}$$

p_T resolution for 1 GeV muons



precise (trigger) tracking with just 3 pixel layers!

Plans for Future HV-MAPS Research

HV-MAPS

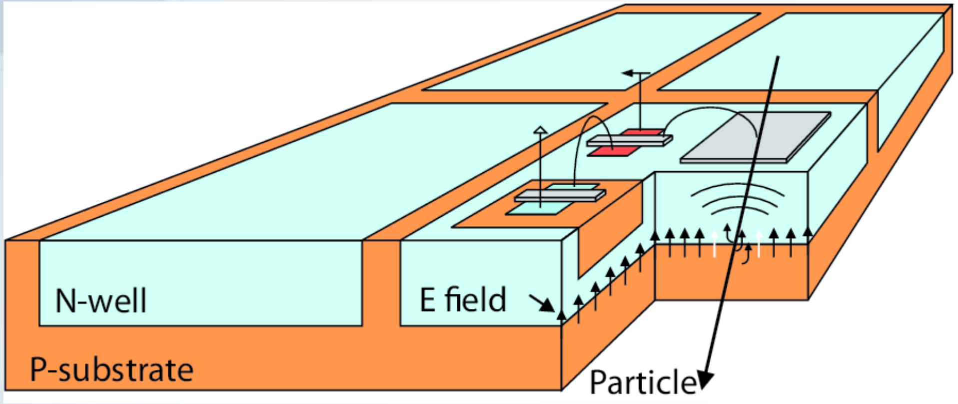
- small pixel sizes over larges scales feasible
- highly integrated design (much less complex than strip hybrids)
- low power but power is an issue
- very low material budget (X= 0.1% X_0 for Mu3e)
- low noise and fast readout → trigger
- relatively radiation hard but more tests are required
- standard commercial process + relatively cheap technology
- new technology and not much experience

Planning to build HV-MAPS hardware demonstrator for LHC Heidelberg + Karlsruhe (KIT).

New collaborators highly welcome!

Summary

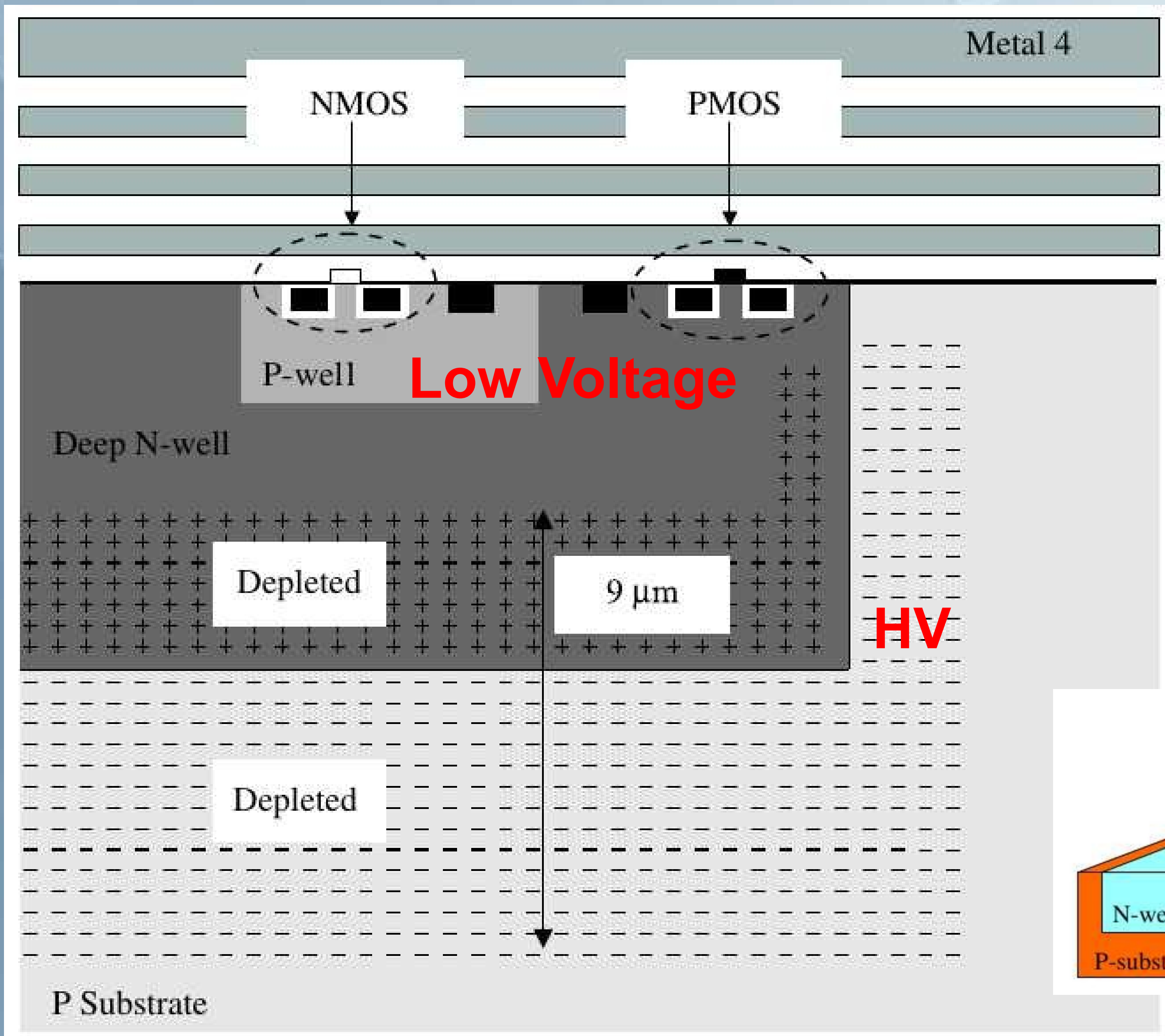
- **HV-MAPS Track Trigger seems technically possible!**
- **Pixel Trigger in Endcaps?**
- **Pixel only Detector?**



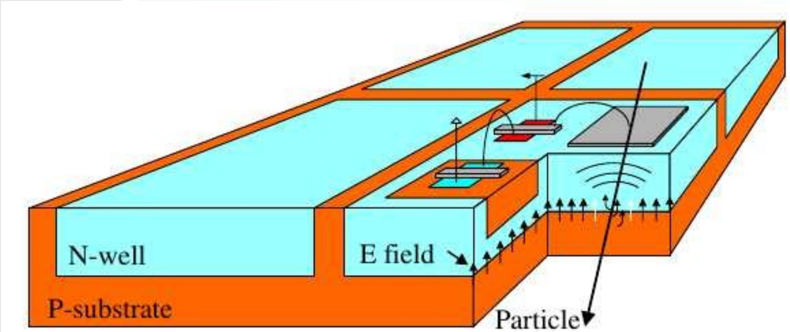
BACKUP

High Voltage MAPS

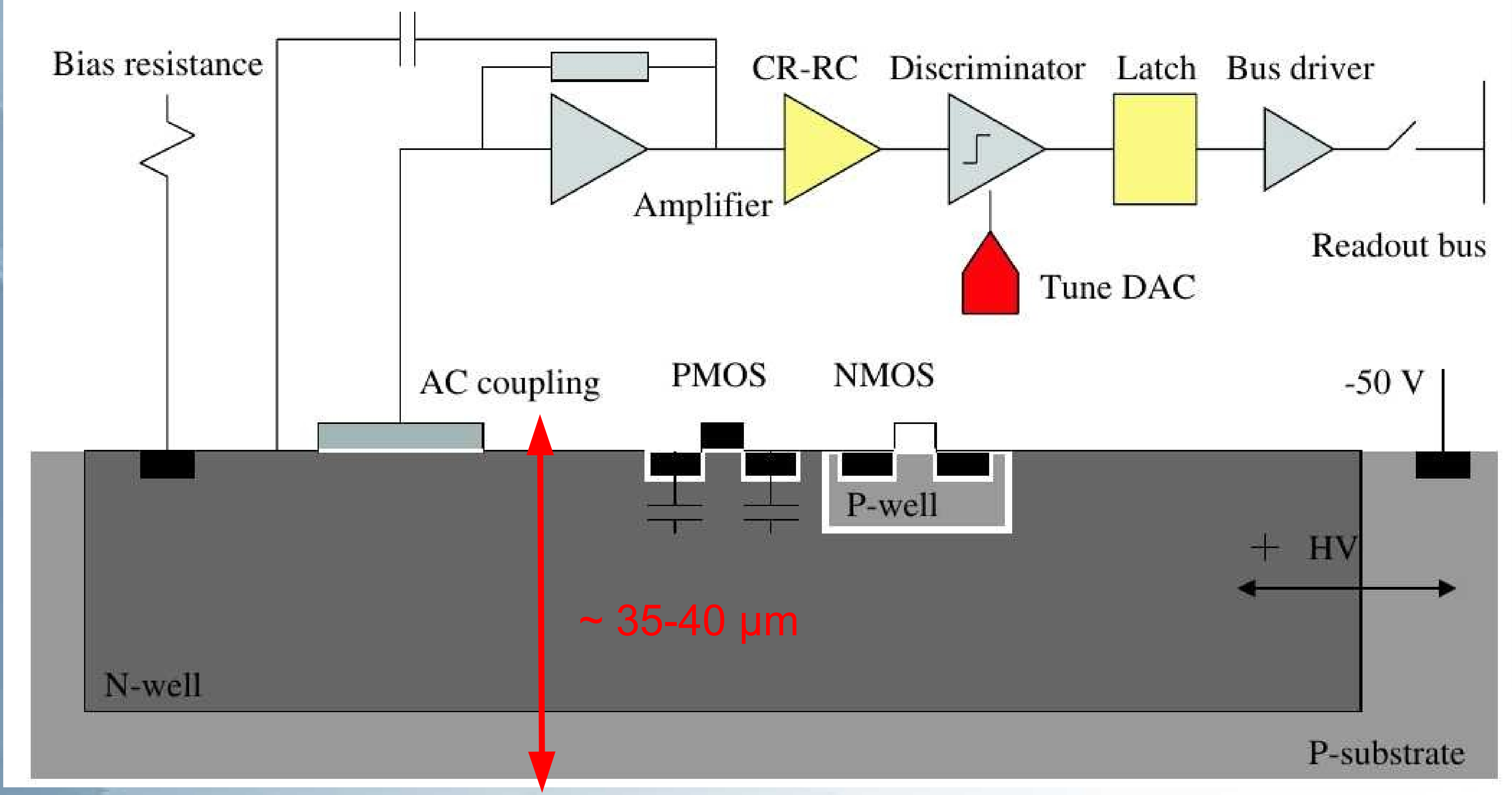
Ivan Perić, NIMA 582 (2007) 876



- Floating structure
- MOSFETS in well
- 100% fill factor
- high depletion at 50 V



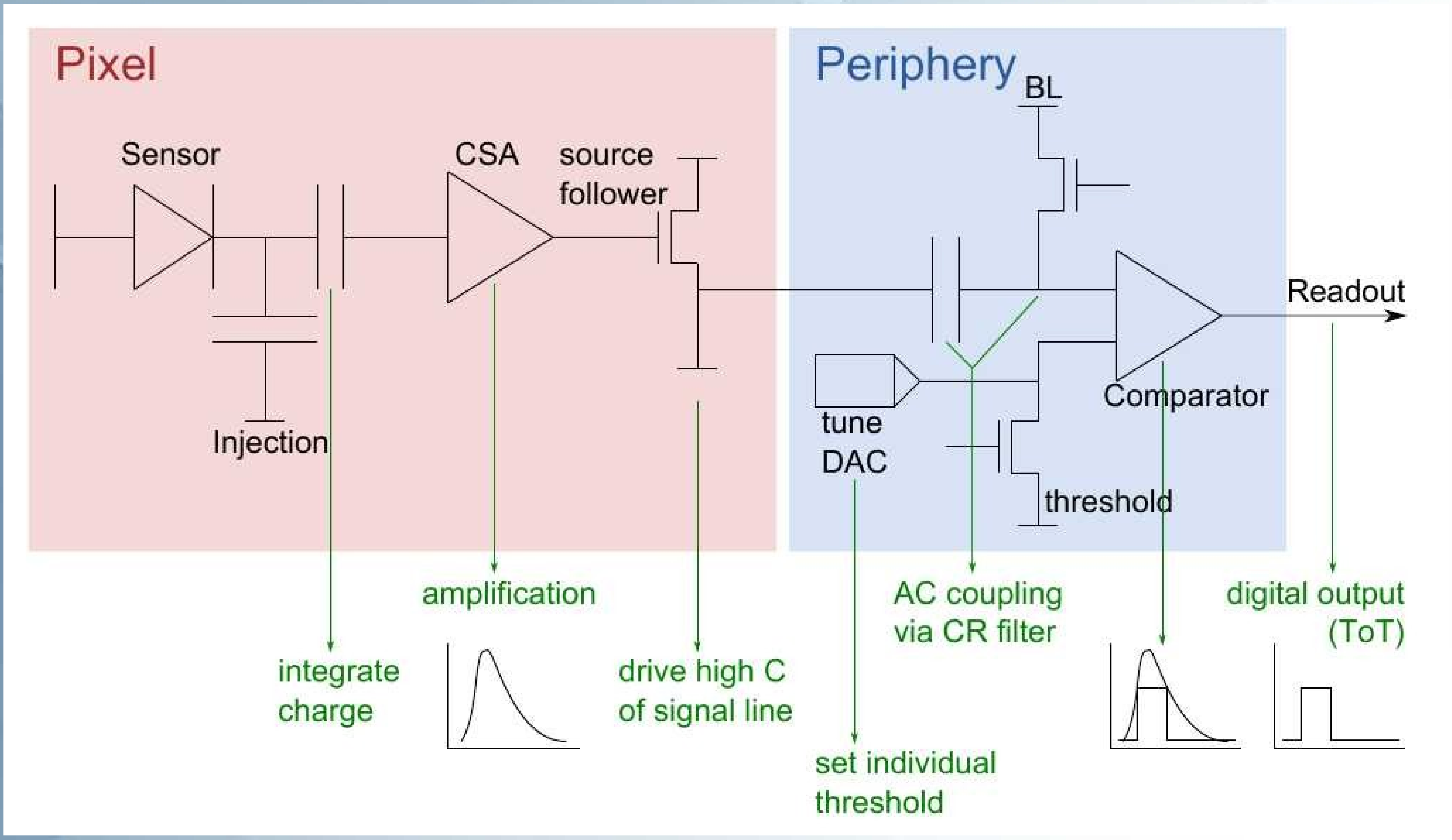
HV-MAPS Pixel Design



Fast circuit and thin sensor!

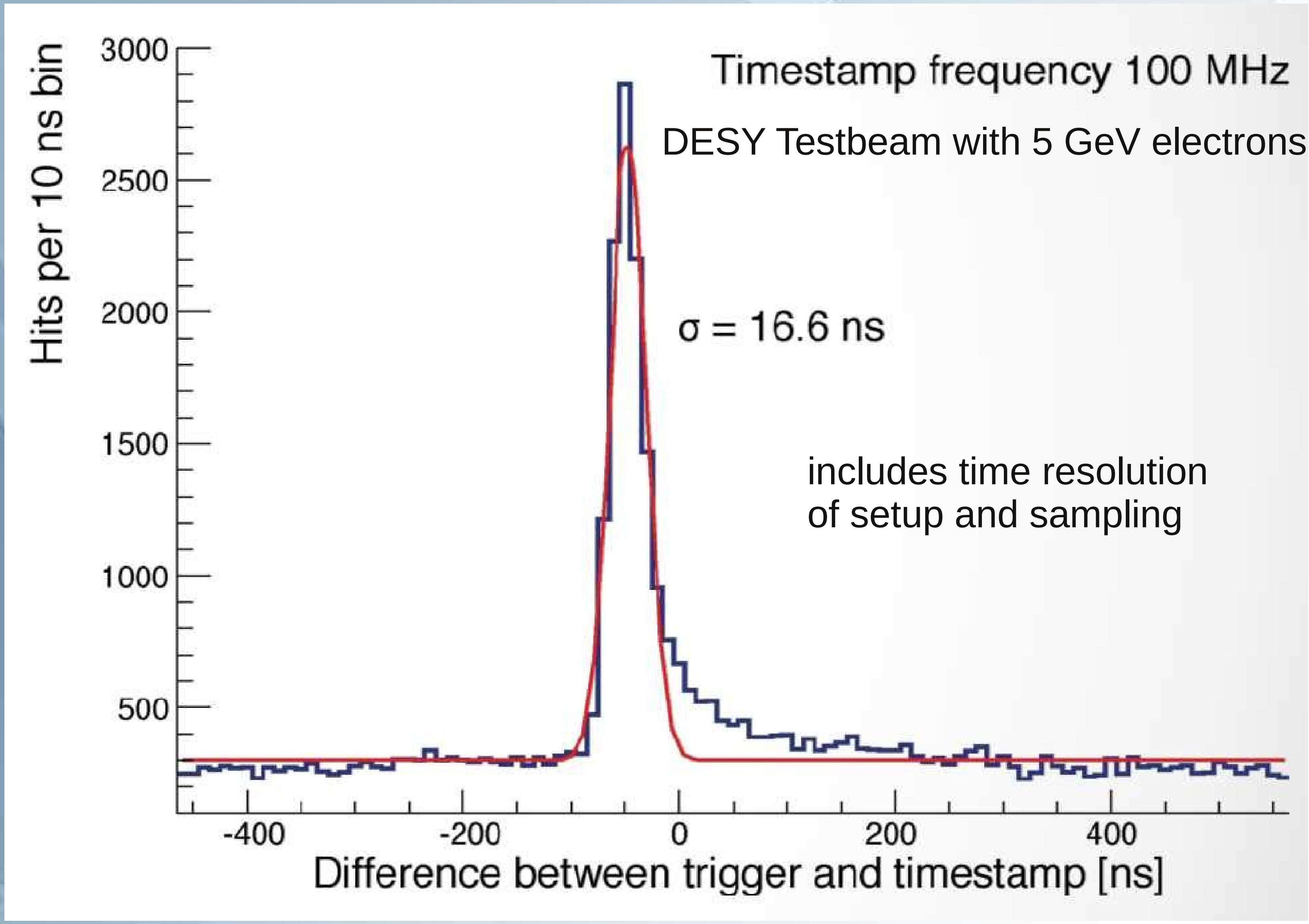
DAC = digital to analog converter → adjustment of threshold

Mupix Chip

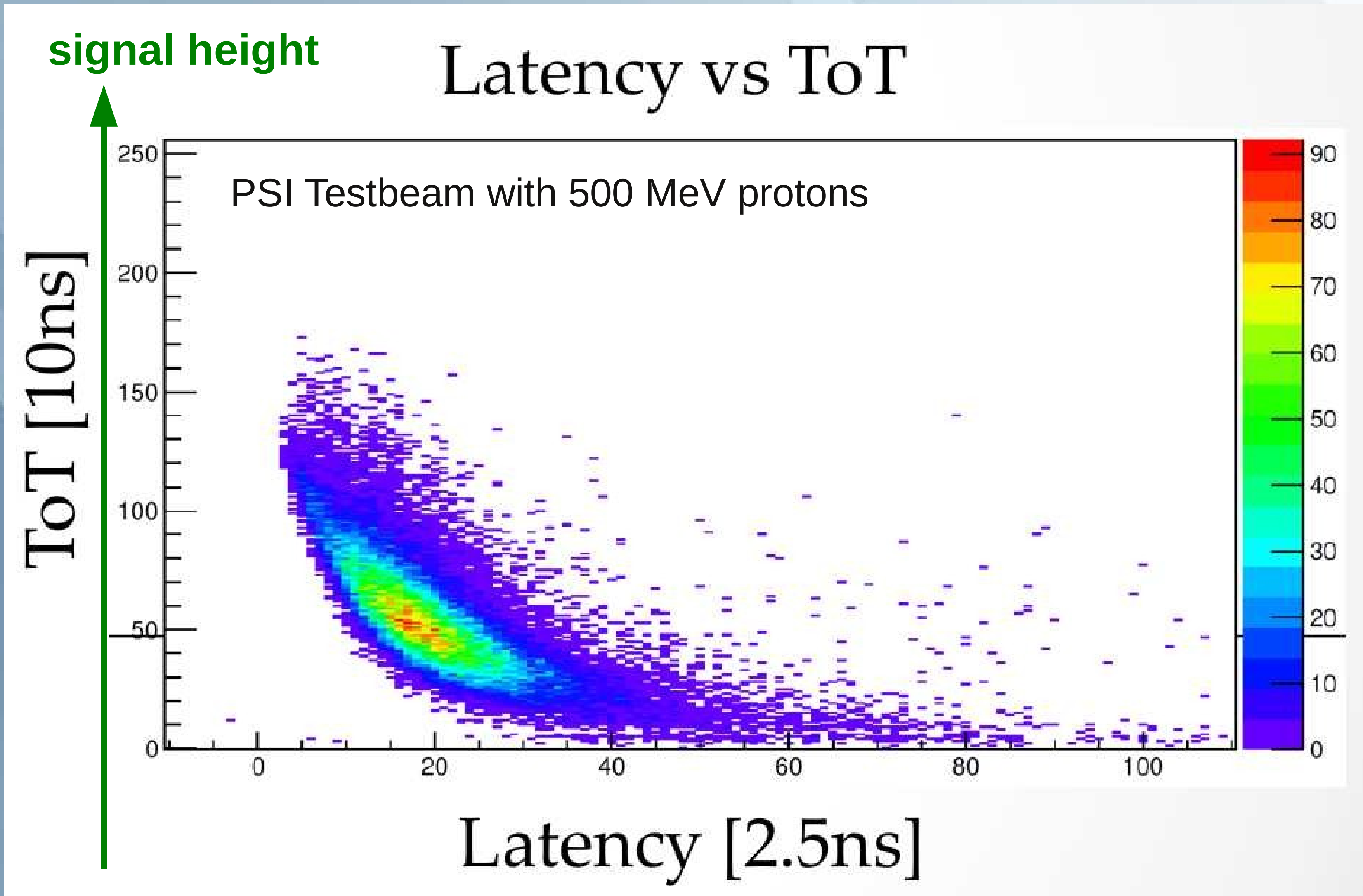


Pixel
Periphery
BL
Sensor
CSA
source follower
Readout
Injection
tune DAC
Comparator
threshold
amplification
AC coupling via CR filter
digital output (ToT)
integrate charge
drive high C of signal line
set individual threshold

MuPix Time Resolution

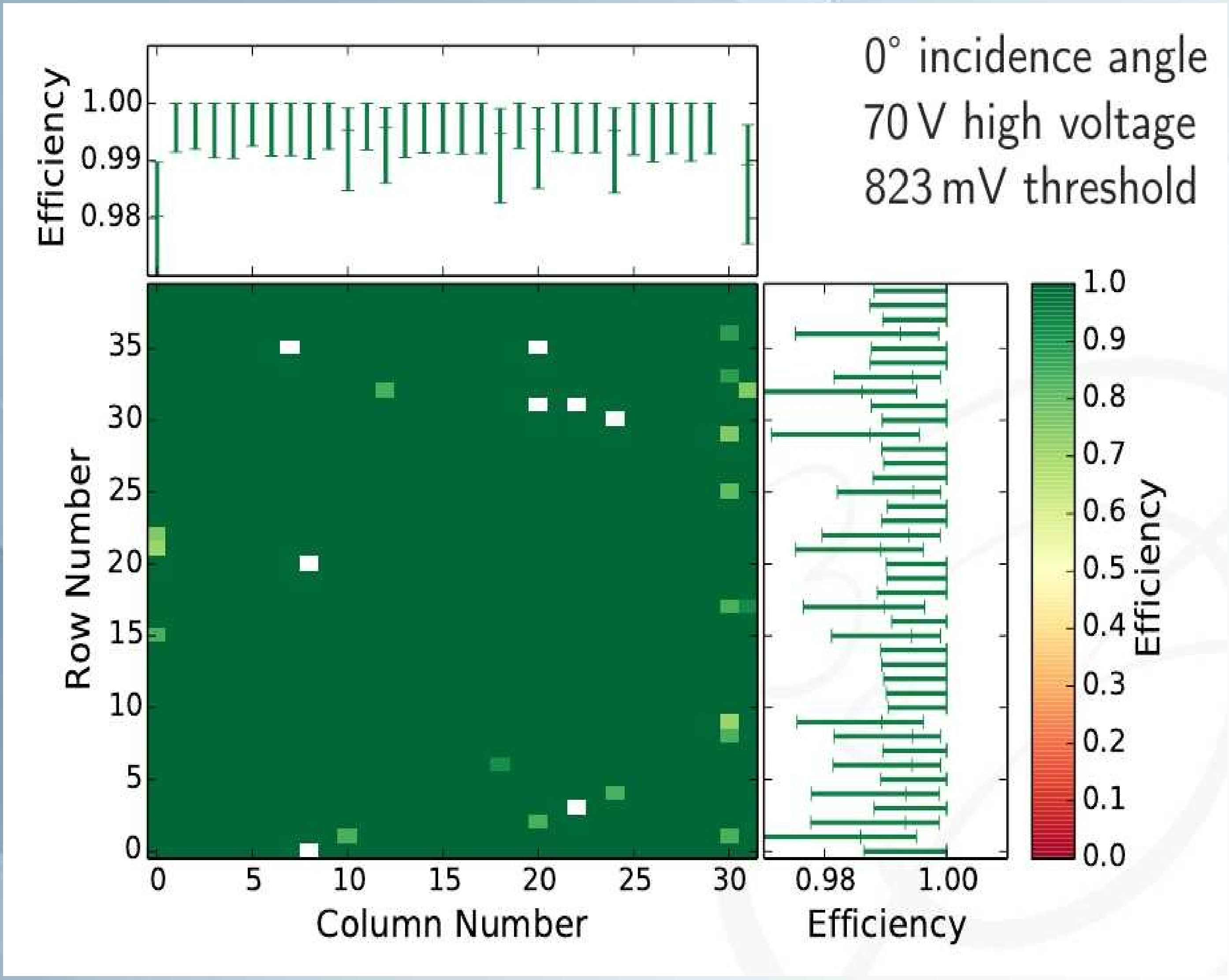


MuPix Time Resolution



→ **timewalk correction possible**

MuPix Pixel Efficiency



Efficiency > 99.5%

Simulation Results

- muons with p=1 GeV/c
- X/X_0=1% per layer
- G4 simulation
- layer spacing 2cm
- radius ~1m
- pixel size 80 x 80 mu^2