Helmholtz-Alliance

8th Detector Workshop of the Terascale Alliance 2015
Berlin, 06.03.2015

CMOS Pixels Overview
(for LHC – pp – Experiments)

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SI LAB
Silizium Labor Bonn

Outline

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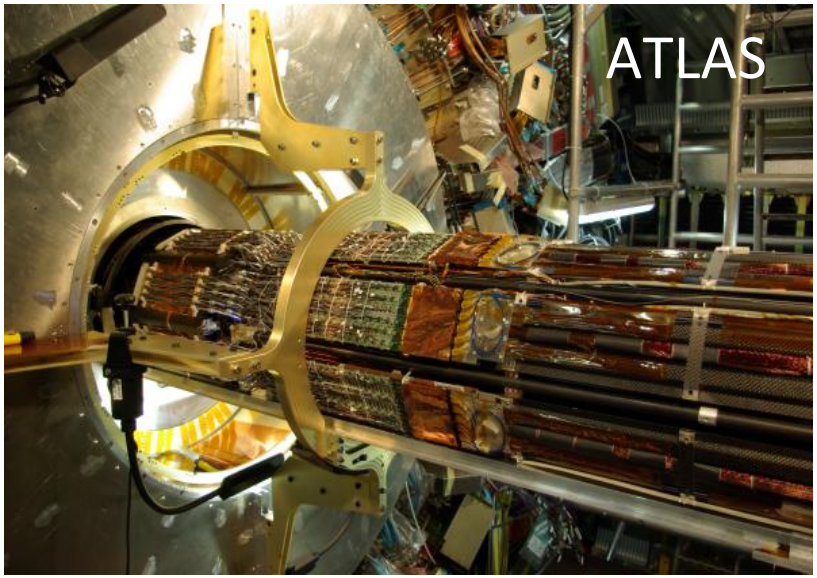
Demands on Pixels at the HL-LHC

MAPS

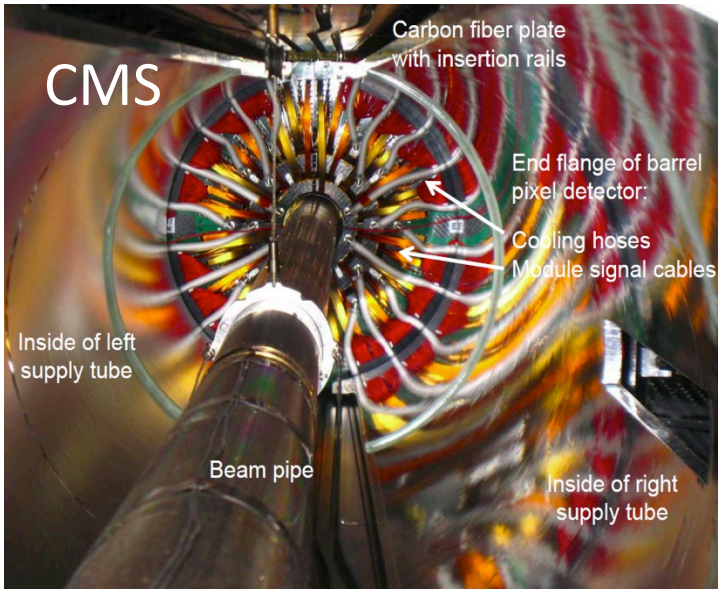
CMOS Pixels

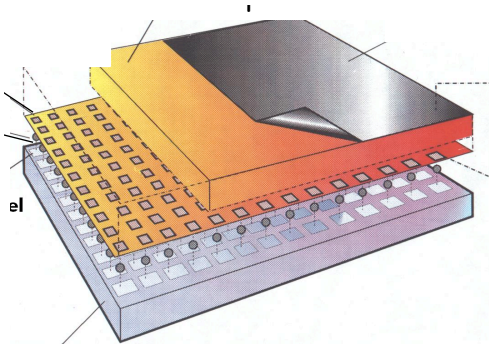
Some prototype results

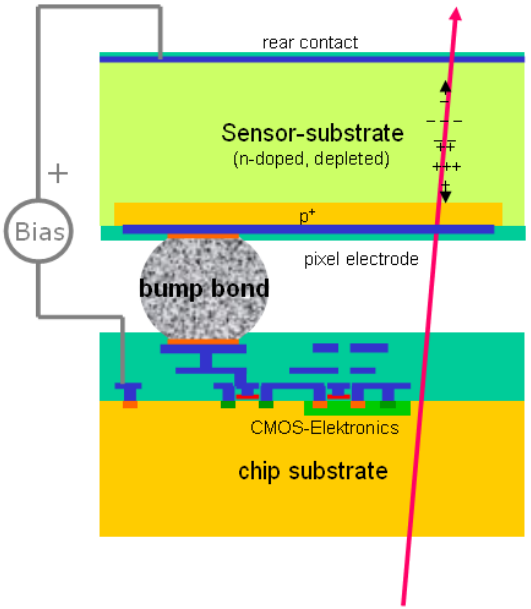
Today's running LHC detectors



all based on
"Hybrid Pixels"







- amplification by a dedicated R/O chip
- 1-1 cell correspondence

1st Upgrade …

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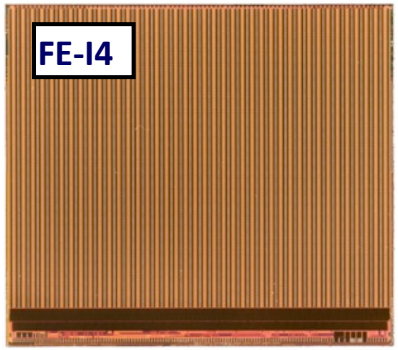
IBL = ATLAS' insertable B-Layer

- move closer to IP (5.5 cm -> 3.5 cm)
- higher rate
- higher radiation levels (~$1/r^2$)

FE-I4: larger chip
smaller feature size
higher rate capability

~0.6 × 1.1 cm²

~2 × 2 cm²



250 nm technology

pixel size 400 × 50 µm²

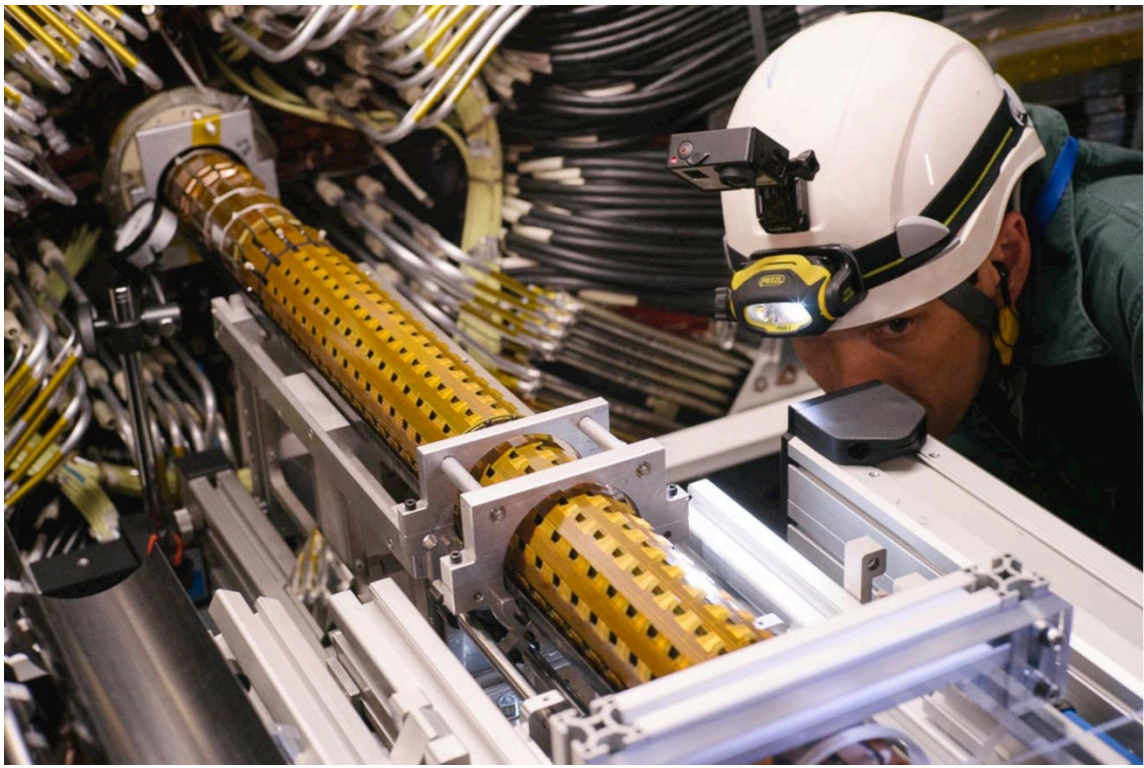
3.5 M transistors

130 nm technology

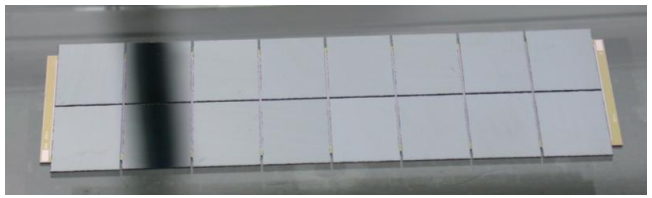
pixel size 250 × 50 µm²

70 M transistors

installed in ATLAS: May 2014

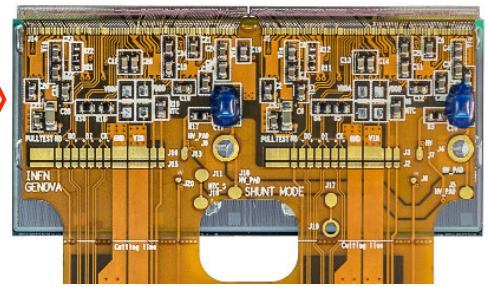


~2 × 5 cm²



ATLAS Pixel 16-chip module

~2 × 4 cm²



IBL: 2-chip module

The typical LHC case (... here ATLAS)

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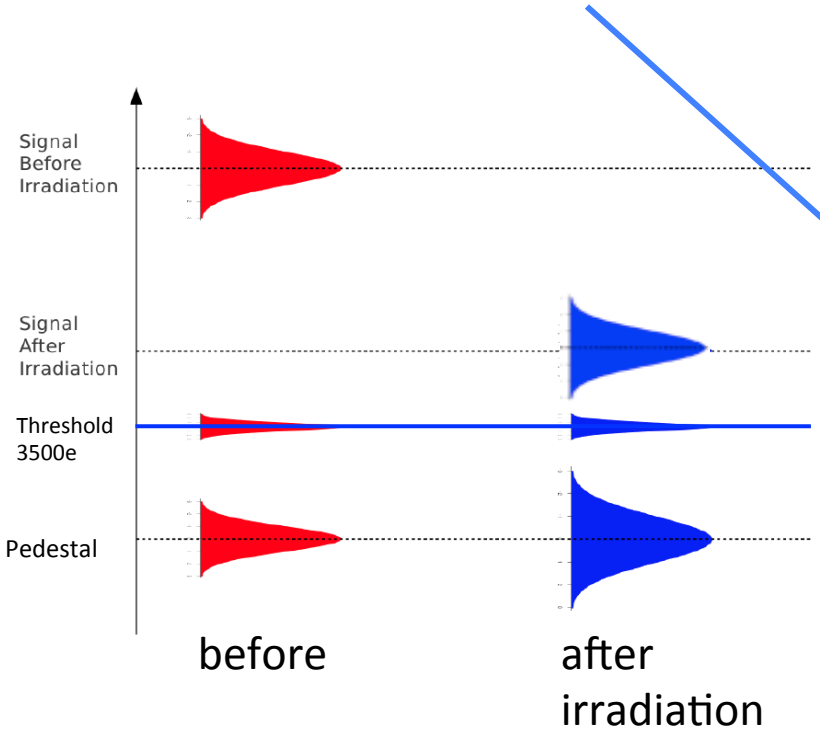
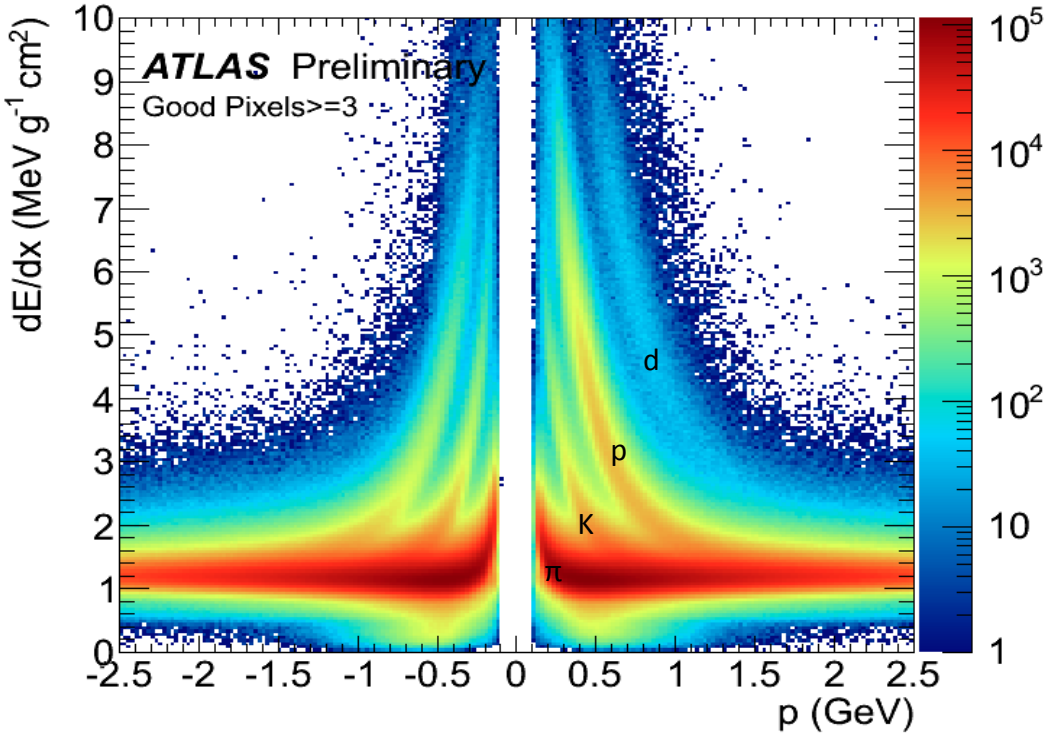
Signal of a min. ionizing particle ≙ 19500 e^- => <10000 e^- after irrad.

- Discriminator thresholds = 3500 e, ~40 e spread, ~170 e noise
- 99.8% data taking efficiency
- 95.9% of detector is operational
- ca. 10 µm x 100 µm resolution (track angle dependent)
- 12% dE/dx resolution





C. Gemme et al., ATLAS-CONF-2011-016

Hybrid Pixels @ LHC: PROs and CONs

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- complex signal processing already in pixel cells possible
  - zero suppression
  - temporary storage of hits during L1 latency
- radiation hardness to >10^{15} n_{eq}/cm^2
- high rate capability (~MHz/mm^2)
- spatial resolution ~ 10 – 15 µm

PRO

… but also

- relatively large material budget: **~3% X_0** per layer (1% X_0 @ ALICE)
  - sensor + chip + flex kapton + passive components
  - support, cooling (-10°C operation), services
- complex and laborious module production
  - bump-bonding / flip-chip
  - many production steps
  - expensive

CON

CMOS Pixels

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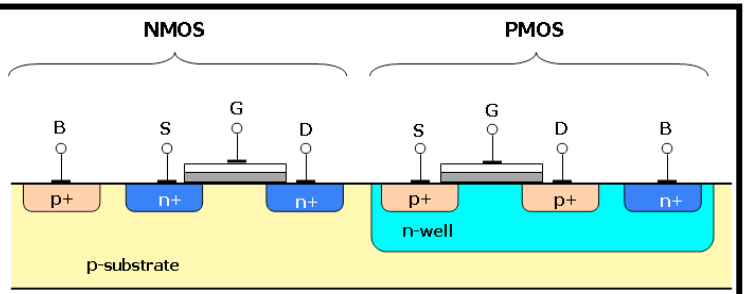
- Use commercial CMOS technology
  - mature (world market)
  - cheap in comparison
- Monolithic (i.e. one sensor/chip entity)
  - avoids hybridization
  - wafer scale processes
  - large modules possible (employ stitching over reticules)
- Small pixels
  - o (25 x 25 µm^2)



BUT

- Industry does not care about particle detection
  - they use cheap low resistive substrate Si (not depletable) … Q-coll by diffusion (slow)
  - some (CMOS camera) technology have relatively thick epitaxial layer (~15 µm)

  ⇒ try to exploit special technology features to make detectors
  multiple wells, some (thin) depletion layer, backside contacts => optimize Q-coll.

Rate and radiation challenges at the innermost pixel layers

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Hybrid Pixels

	BX time	Particle Rate	NIEL Fluence	Ion. Dose
	ns	kHz/mm^2	n_{eq}/cm^2 per lifetime*	Mrad per lifetime*
LHC (10^{34} cm^{-2}s^{-1})	25	1000	2×10^{15}	79
HL-LHC (10^{35} cm^{-2}s^{-1})	25	10000	2×10^{16}	> 500
LHC Heavy Ions (6×10^{27} cm^{-2} s^{-1})	20.000	10	$>10^{13}$	0.7
RHIC (8×10^{27} cm^{-2}s^{-1})	110	3.8	few 10^{12}	0.2
SuperKEKB (10^{35} cm^{-2}s^{-1})	2	400	~3 x 10^{12}	10
ILC (10^{34} cm^{-2}s^{-1})	350	250	10^{12}	0.4

Monolithic Pixels

lower rates
lower radiation
smaller pixels
less material
better resolution

DEPFET: Belle II
MAPS: STAR@RHIC
and future
ALICE ITS

assumed lifetimes:
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years

Rate and radiation challenges at outer/interm. pixel layers

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focus in this talk (CMOS pixels for LHC-pp)

	BX time	Particle Rate	NIEL Fluence	Ion. Dose
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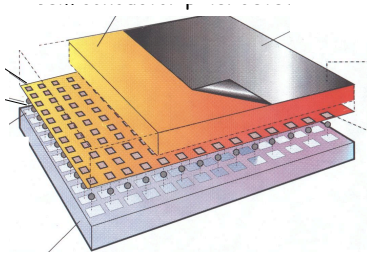
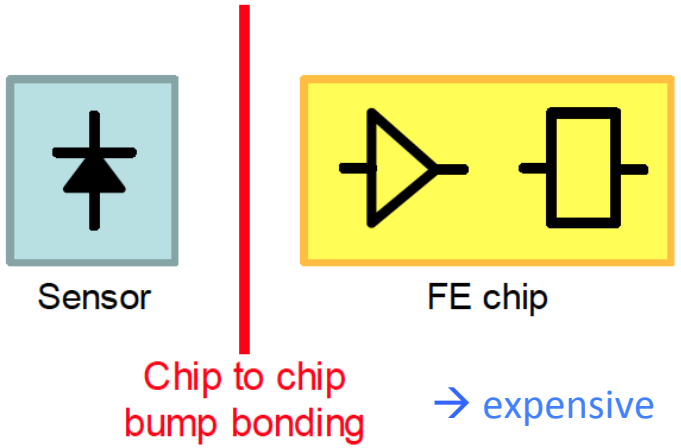
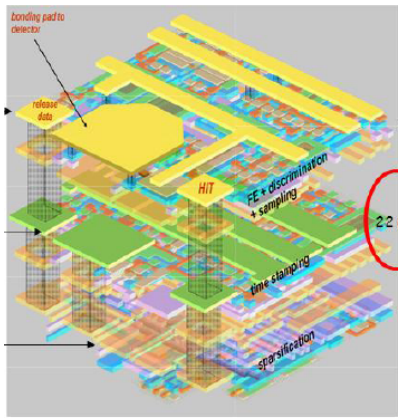
A classification ... from HYBRID to new challenges

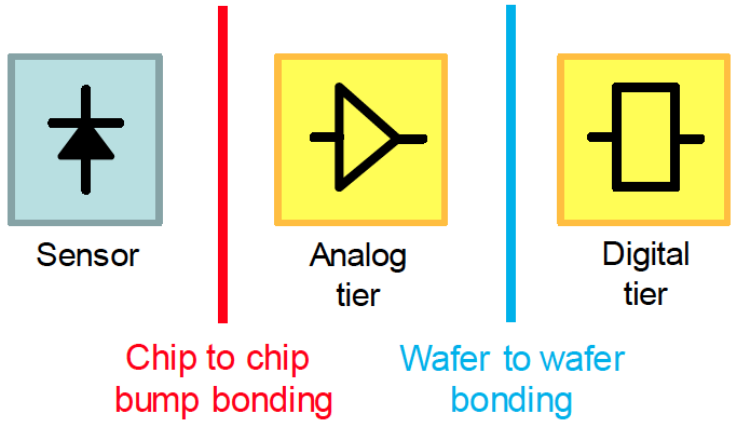


- standard HYBRID pixels
  - various sensors: planar-Si, 3D-Si, diamond
  - mixed signal R/O chip (FE-I3, FE-I4, ROC ...)



- 3D integration of CMOS Tiers
  - separate analog / digital / opto
  - FE-TC4 (Tezzaron/Chartered)





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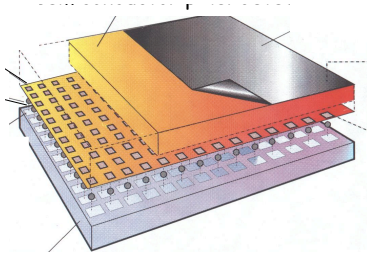

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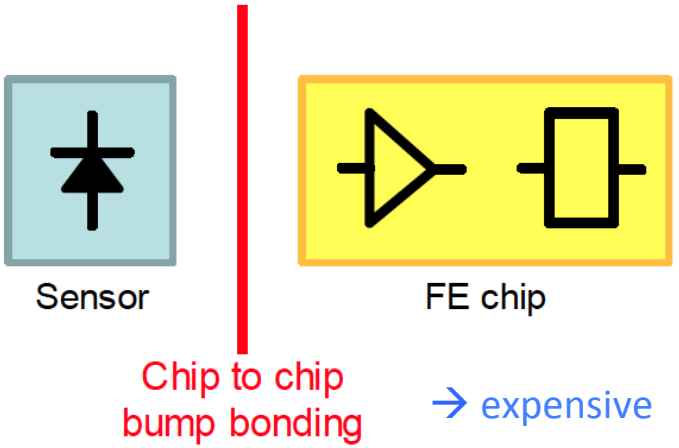
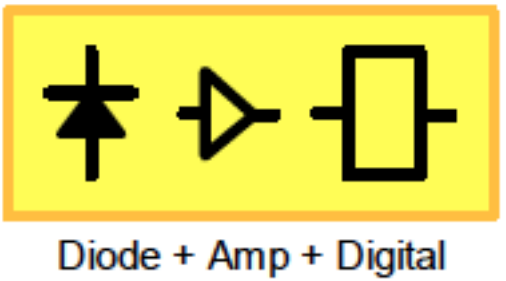


- Monolithic Active Pixel Sensors
  - MAPS using CMOS with Q-collection in epi-layer (usually by diffusion → recent advances)
  - depleted DMAPS using HR substrate or HV process to create depletion region: $d \sim \sqrt{\rho \cdot V}$
  - CMOS on SOI



A classification ... from HYBRID to new challenges

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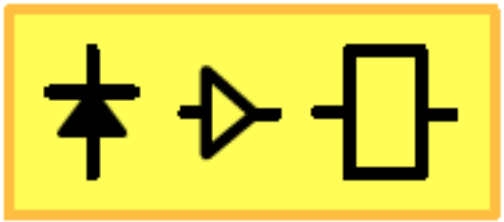
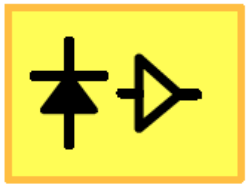
- (D)MAPS



Diode + Amp + Digital

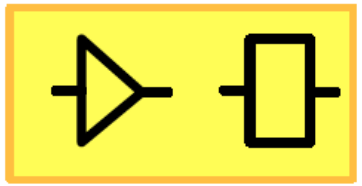
~100 trans./pixel



Diode + preamp

Wafer to wafer bonding

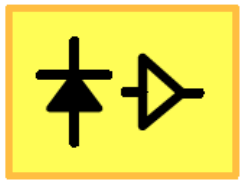
~100M trans.



FE chip

or chip to wafer

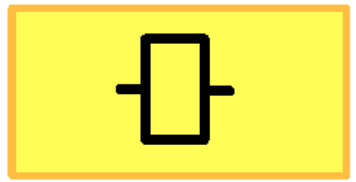
~100 trans./pixel



Diode + full analog processing

Wafer to wafer bonding

~100M trans.



Digital only FE chip

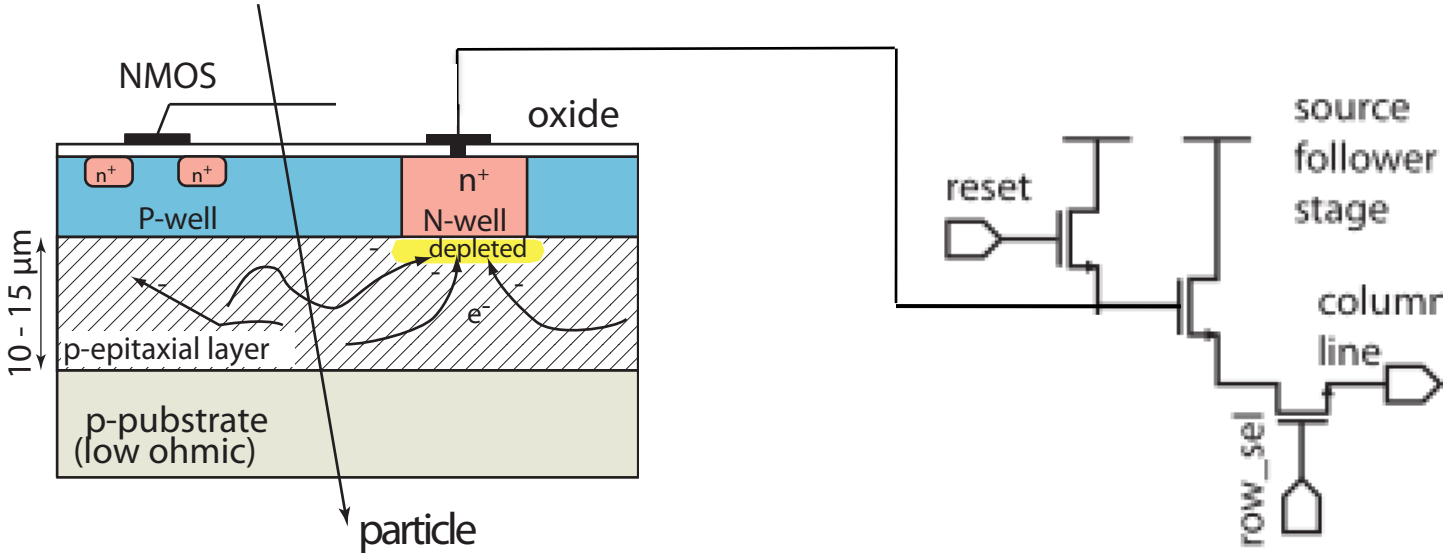
or chip to wafer

- HYBRID pixels using "active" sensors
  - 8" HV or HR sensor w/ few transistors
  - (voltage) signal coupled to R/O-chip

- CMOS ACTIVE Sensors + digital R/O chip
  - HR or HV CMOS sensor with CSA+disc
  - dedicated digital R/O chip

Early MAPS developments (Monolithic Active Pixel Sensor)

CMOS Sensors (MAPS)
CMOS pixels with epitaxial layer as sensor



3Transistor R/O

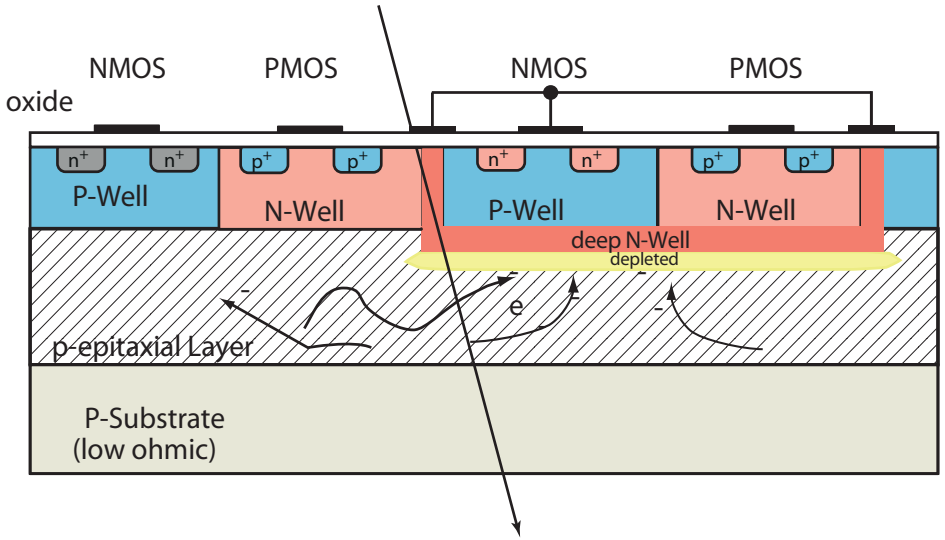
rolling shutter mode addressing

B. Dierickx, D. Meynants, G. Scheffer, SPIE 3410:68-76 (1998)
R. Turchetta, …, M. Winter et al, NIM A458 (2001) 677-689

\+ ‘standard CMOS’ process
− limited to NMOS usage, however
\+ low power
− small and incomplete signal collection
− slow charge collection (diffusion) and R/O
− radiation soft

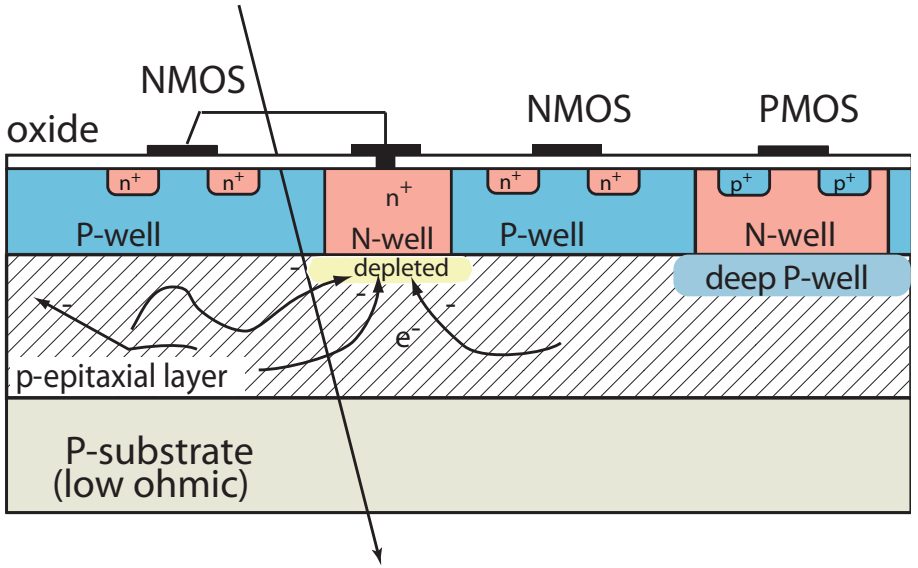
developed for more than 10 years
⇒ goals:
better/faster Q-collection
radiation tolerance
⇒ TID o(~Mrad), NIEL o(10^{13} /cm^2)
⇒ **not suited for LHC - pp**

Improvements



- a **large deep n-well** for charge collection containing NMOS and PMOS transistors

L. Ratti, V. Re, G. Rizzo et al., e.g
eConf C0604032 (2006), S. 0008



- using **„triple/quadruple“ well processes** to shield the PMOS transistor wells

J.P. Crooks, …, R. Turchetta et al. IEEE TNS 2007
& Sensors (2008), ISSN 1424-8820

MAPS Pixel Detector Projects

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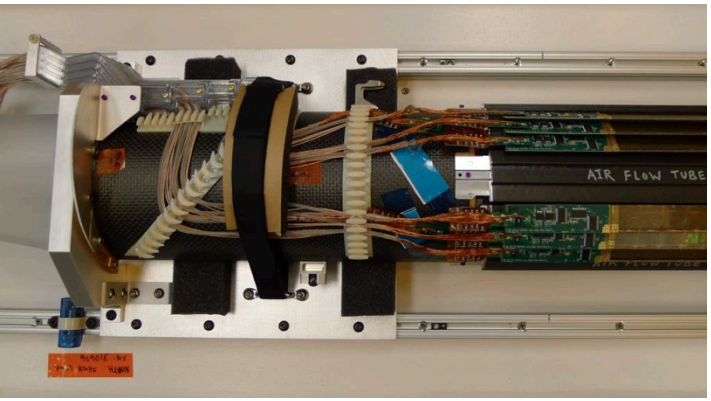
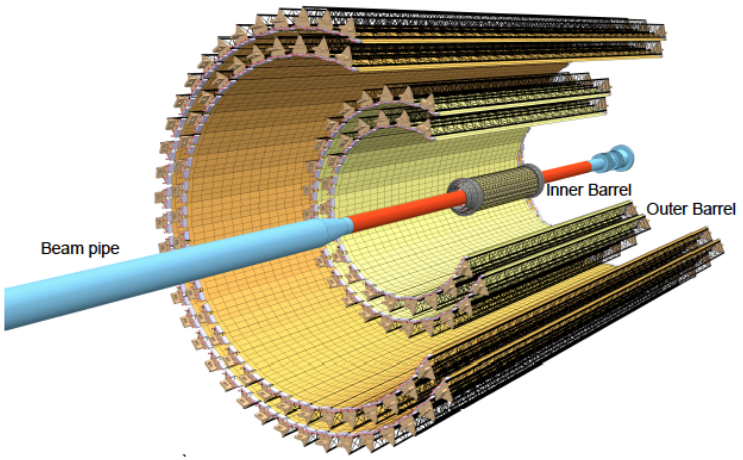
STAR / RHIC



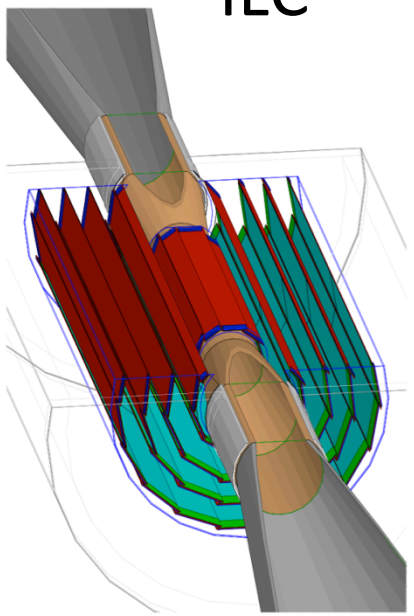
in operation since 2014

ALICE – Phase I Upgrade



under development
target: 2018

ILC



current baseline

see talk by Marc Winter

Interest in CMOS Pixels for LHC-pp => (D)MAPS

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- driven by the need/hope for
  - low cost large area detectors … more pixel layers in trackers …. commercial
  - less material … ? … not clear
  - less power … ? … not clear

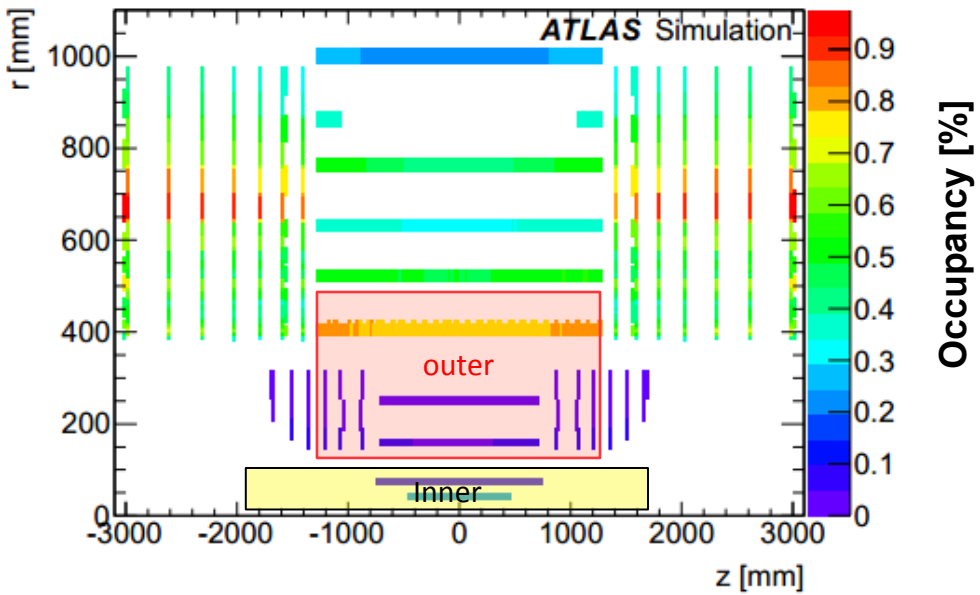
- facing the challenges of HL-LHC

	inner layers (<6 cm)	outer layers (>25 cm)
• high rates	10 MHz/mm^2	1 MHz/mm^2
• radiation	> 1 Grad TID	50 Mrad
	2 x 10^{16} n_{eq}/cm^2	10^{15} n_{eq}/cm^2

note: at > 10^{15} n_{eq}/cm^2 trapping becomes the dominant radiation effect

- **goal:** some (40 – 80 µm) depletion depth for …
  - fast charge collection (< 25ns "in-time" efficient)
  - a reasonably large signal ~4000 e-
  - not too large a travel distance to avoid trapping (rad hardness)

High Luminosity LHC Environment - Requirements



Detector:	Silicon area [m^2]	Channels [10^6]
Pixel barrel	5.1	445
Pixel end-cap	3.1	193
Pixel total	**8.2**	**638**
Strip barrel	122	47
Strip end-cap	71	27
Strip total	**193**	**74**

ATLAS Phase II Letter of Intent

Inner layer

1. **Low power**
2. **Low material**
3. Occupancy
4. Resolution

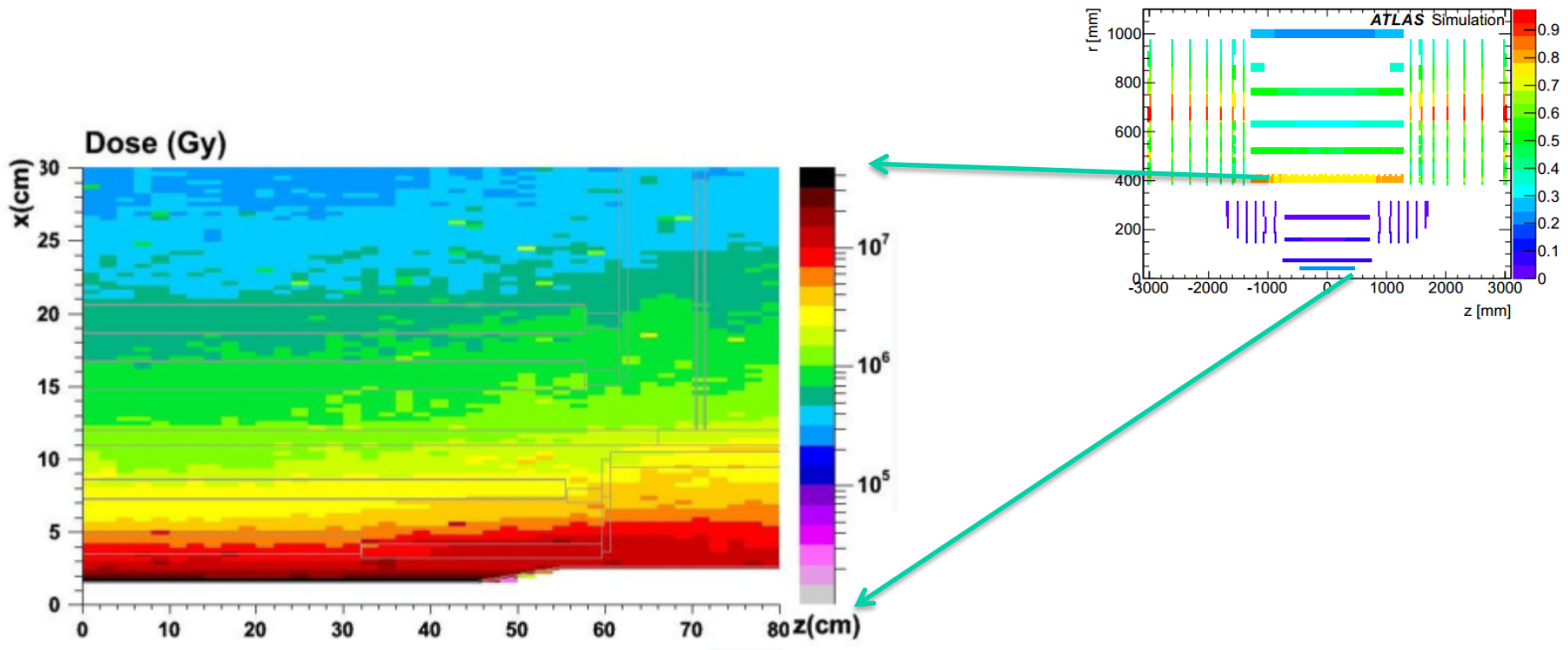
hybrid pixels (65nm? + sensor?)

Outer layer

1. **Low cost**
2. **Low power**
3. Low material
4. Resolution

low cost hybrid pixels or monolithic?

High Luminosity LHC Environment - Requirements

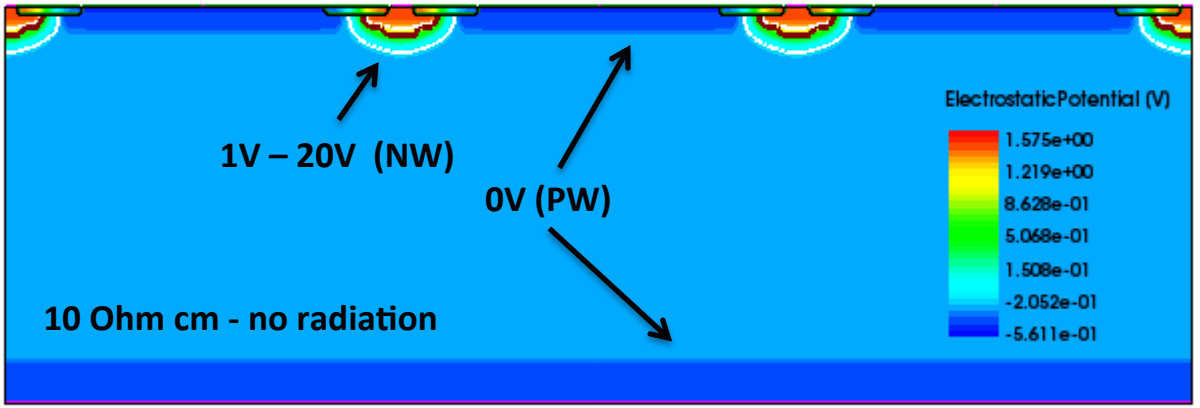


Radiation levels:

- at 5 cm : ~1500 Mrad (2×10^{16} n_{eq}/cm^2)
- at 25cm : ~100 Mrad (10^{15} n_{eq}/cm^2)

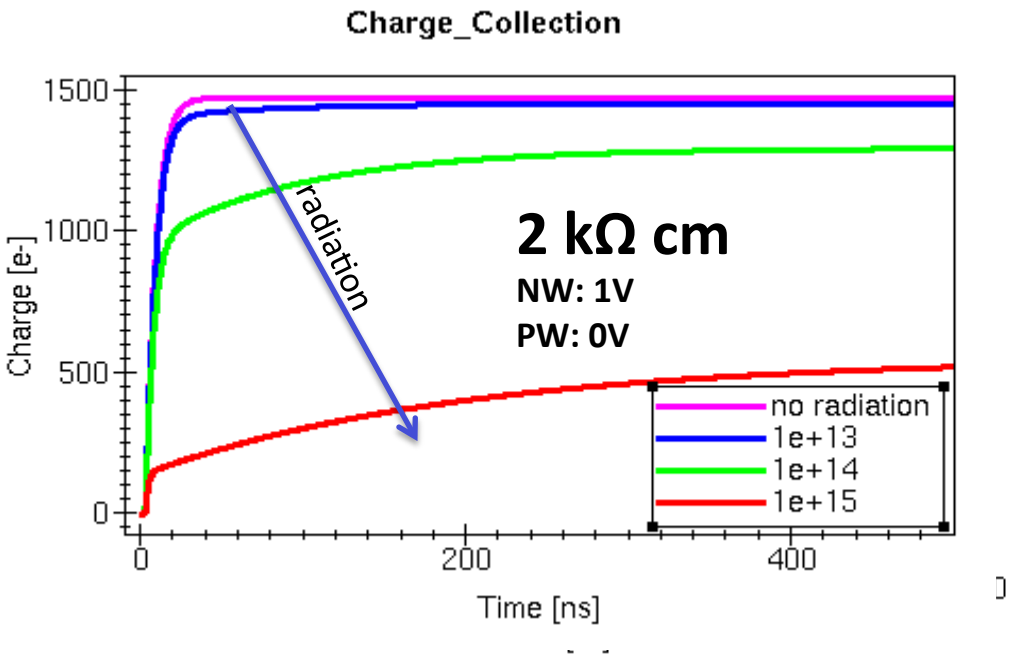
** estimates for 10years of operation*

TCAD simulations: resistivity – voltage – fill factor

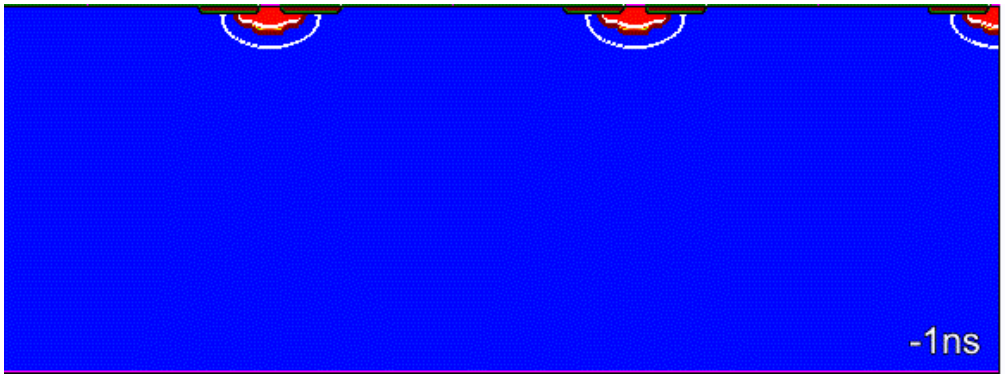


Substrate:10 Ωcm – 2kΩ cm
Nwell: 1V – 20 V
Pwell: 0V

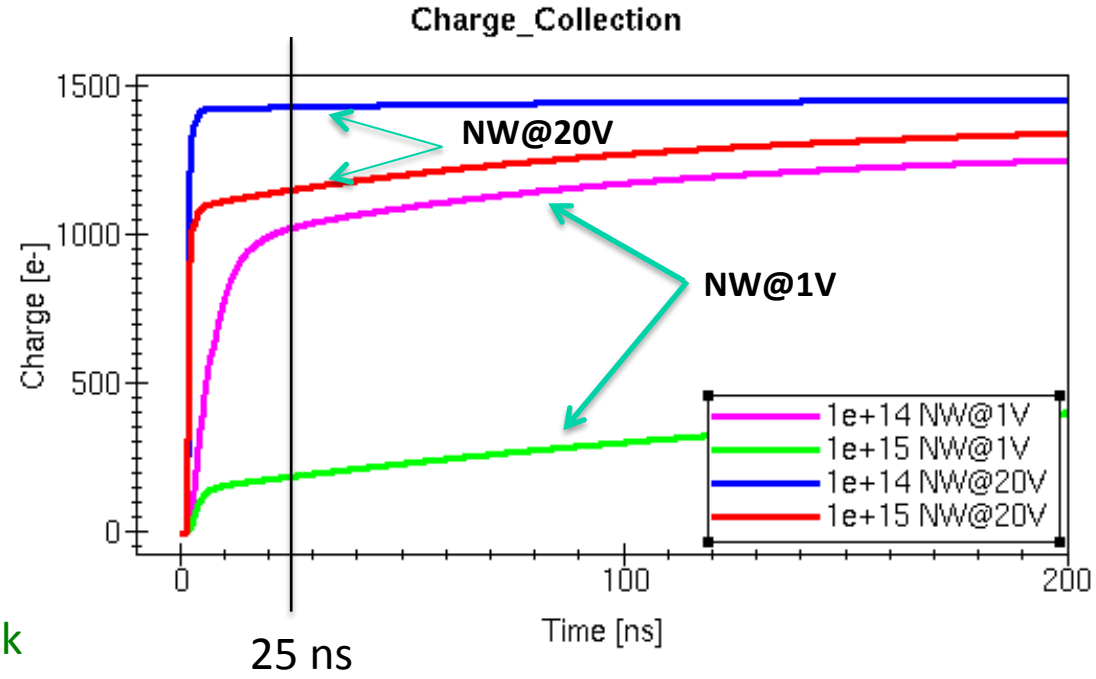
from Tomasz Hemperek



Electron Concentration



2 kΩcm **PLUS** potential difference

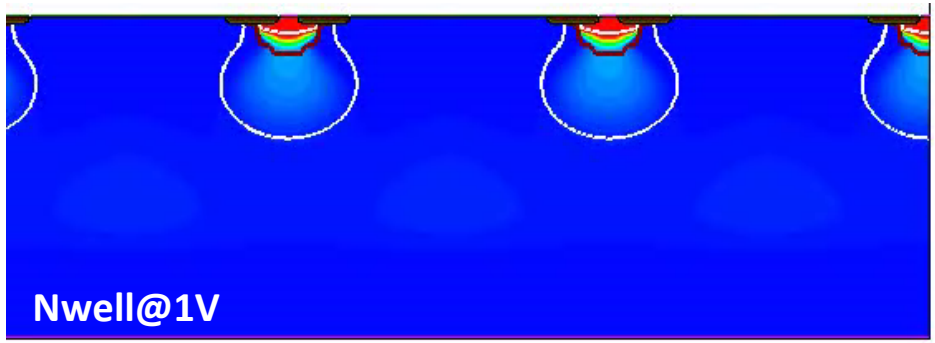


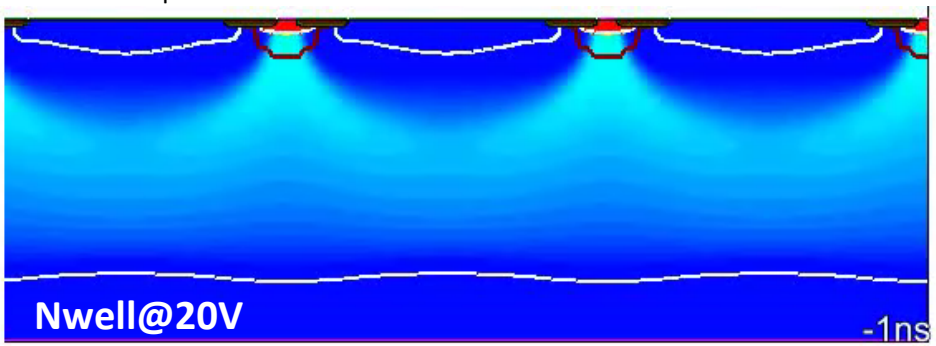
from Tomasz Hemperek

25 ns

Electron Concentration (10^{15} n_{eq}/cm^2)

Substrate:2kΩ cm





Fill Factor influence: here at 10^{15} n_{eq}/cm^2

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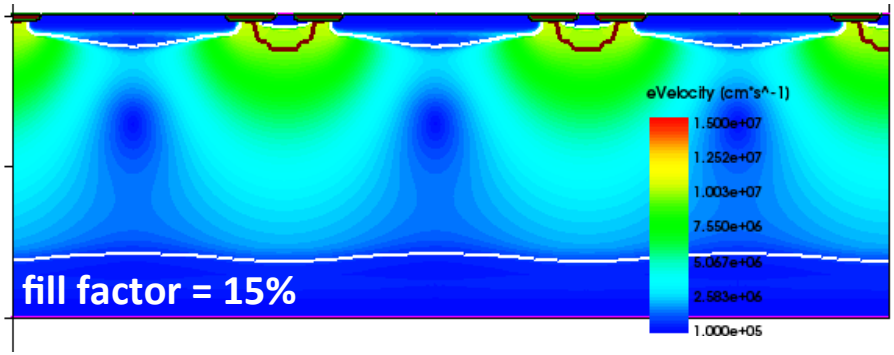
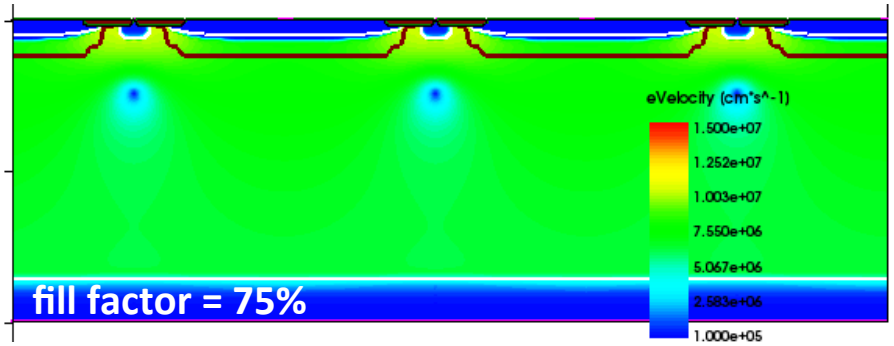
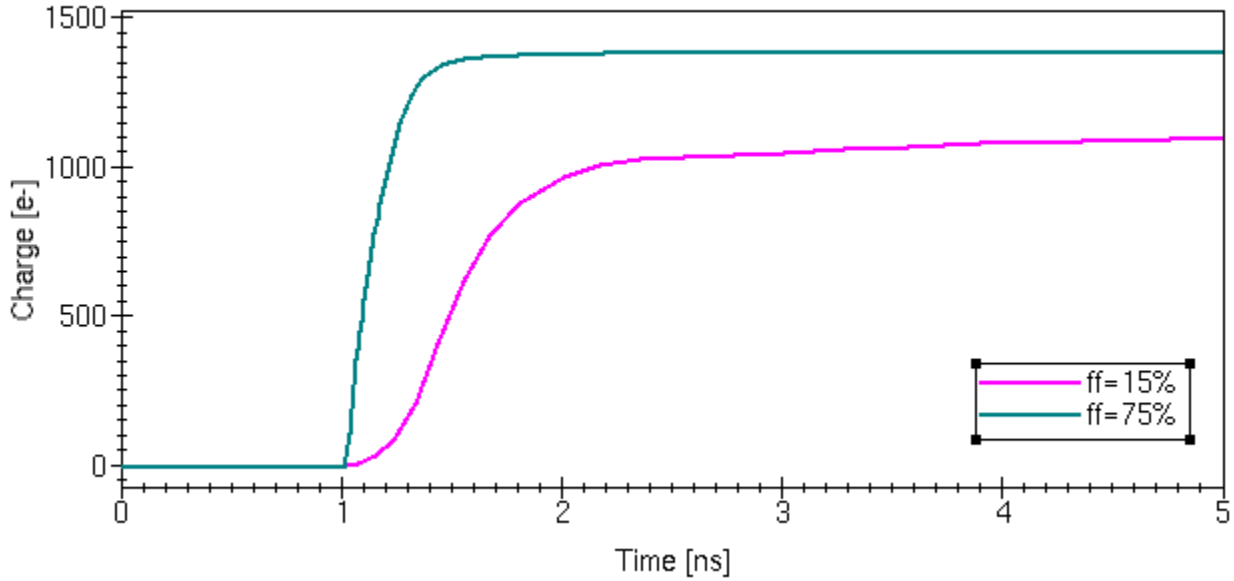
Electron Velocity





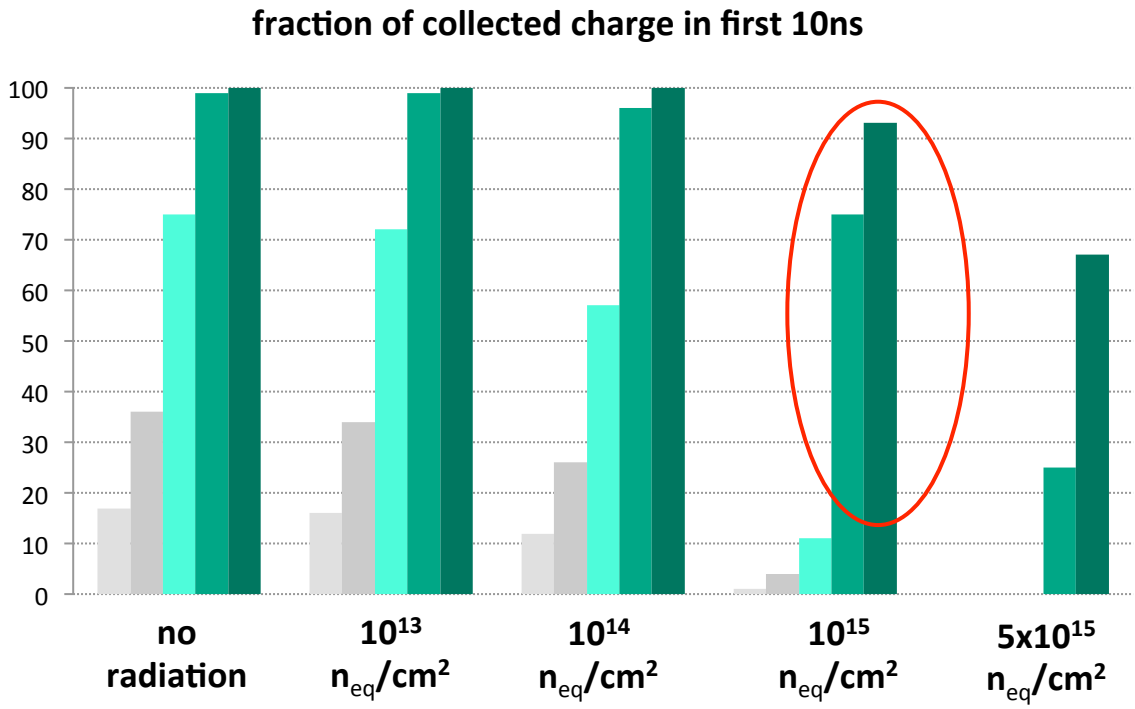
Charge_Collection



NW: 20V
PW: 0V
Substrate:2kΩ cm
Dose: 10^{15} n_{eq}/cm^2

from Tomasz Hemperek

Summary: Resistivity, Voltage, Fill-Factor



	substrate resistivity [Ωcm]	Bias [V]	Fill Factor [%]
	10	1	15
	10	20	15
	2k	1	15
	2k	20	15
	2k	20	75

from Tomasz Hemperek

Enabling technologies

universitätbonn

"High" Voltage add-ons

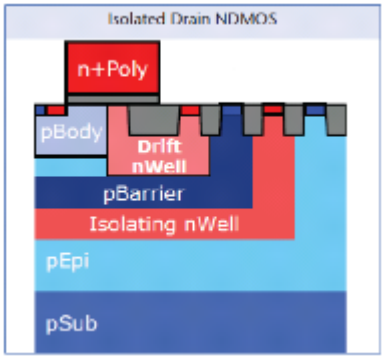
Special processing add-ons (from automotive and power management applications) **increase the voltage handling capability** and create a depletion layer in a well's pn-junction of o(10-15 µm).

"High" Resistive Wafers

8" hi/mid **resistivity** silicon wafers accepted/qualified by the foundry. Create depletion layer due the high resistivity.

Technology features (130-180 nm)

Radiation hard processes with **multiple nested wells**. Foundry must accept some process/DRC changes in order to optimize the design for HEP.



from: www.xfab.com

Backside Processing

Wafer thinning from backside and backside implant to fabricate a **backside contact** after CMOS processing.

Technical support

Current approaches (a classification)

universitätbonn

HV - CMOS

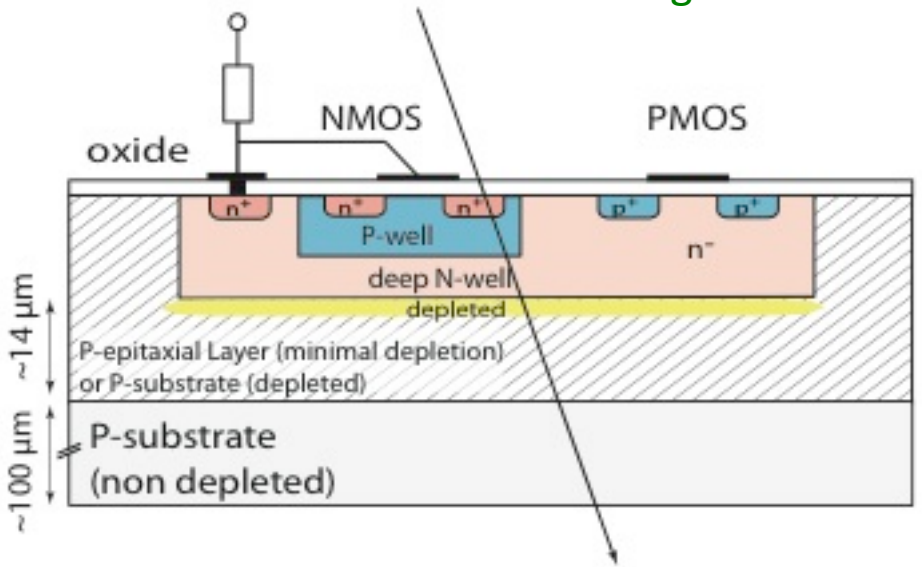
$$d \sim \sqrt{\rho \cdot V}$$

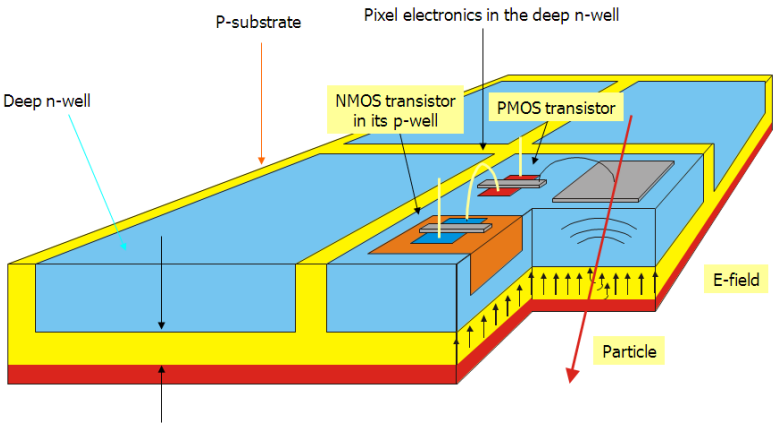
I. Peric et al.

Nucl.Instrum.Meth. A582 (2007) 876-885

Nucl.Instrum.Meth. A765 (2014) 172-176

e.g. AMS technology





- AMS 350 nm and 180 nm HV process (p-bulk) ... 60-100 V
- deep n-well to put nMOS (in extra p-well) and pMOS (limitation)
- ~10 - 15 µm depletion depth → 1-2 ke signal
- various pixel sizes (~20 x 20 to 50 x 125 µm^2)
- so far: replaces „sensor“ (amplified signal) in a „hybrid pixel“ bonding (bump, **glue**, other...) to FE-chip => **CCPD**

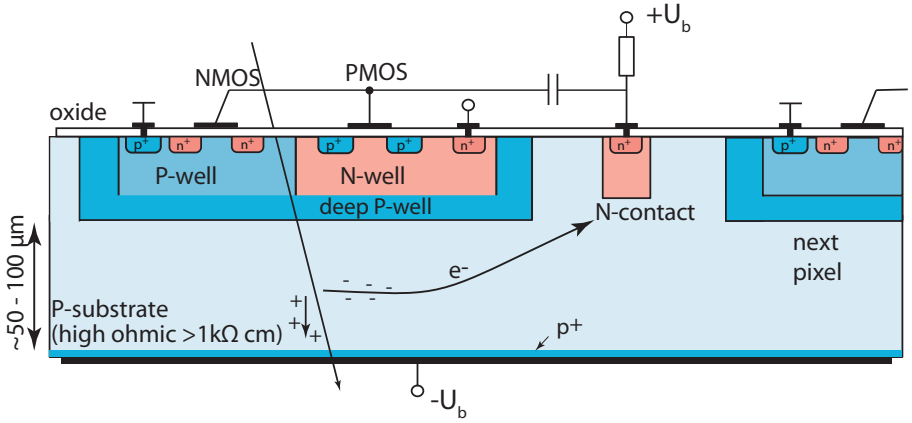
see also talk by Andre Schöning

Current approaches (a classification)

HR - CMOS

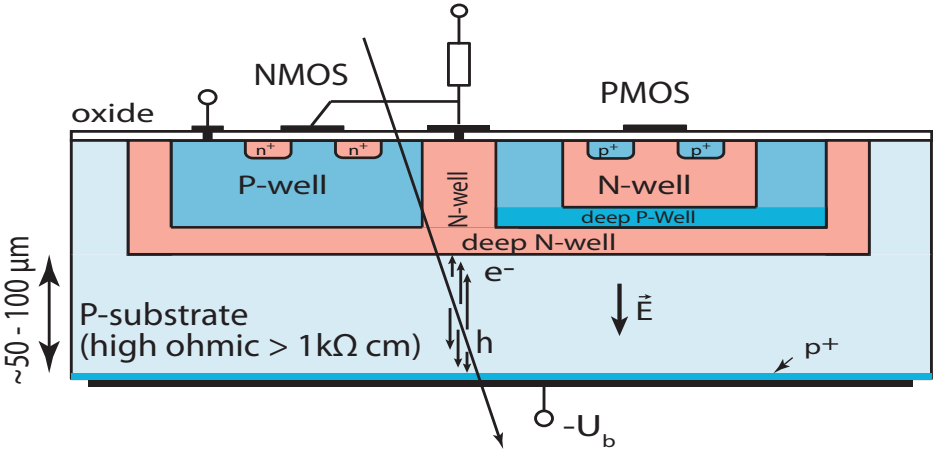
$$d \sim \sqrt{\rho \cdot V}$$

Havranek, Hemperek, Krüger et al.
JINST 10 (2015) 02, P02013



- (D)MAPS like configuration but w/ depleted bulk
- small collection node
- long drift path

=> **smaller C, more trapping**



- deep n and deep p wells
- large collection node
- short drift path

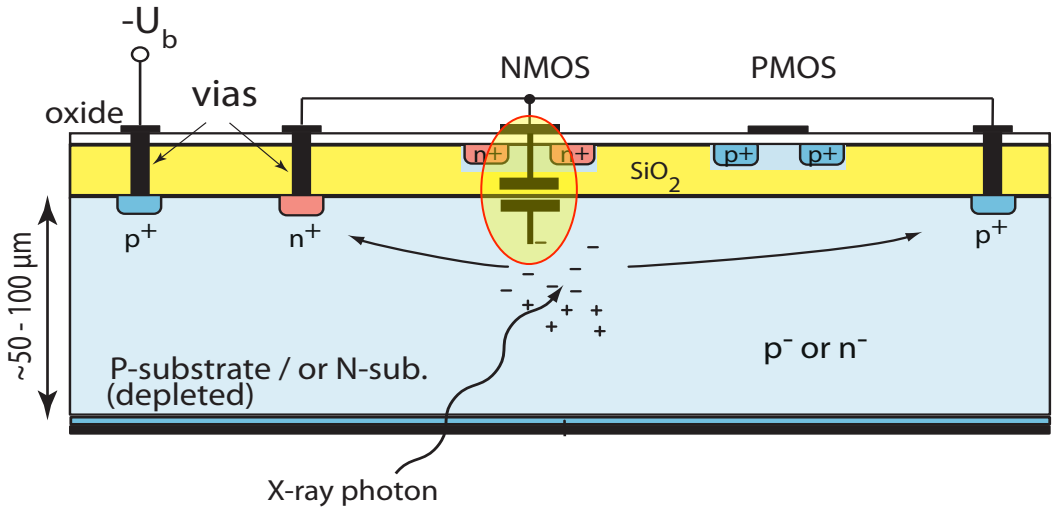
=> **larger C, less trapping**

Current approaches (a classification)

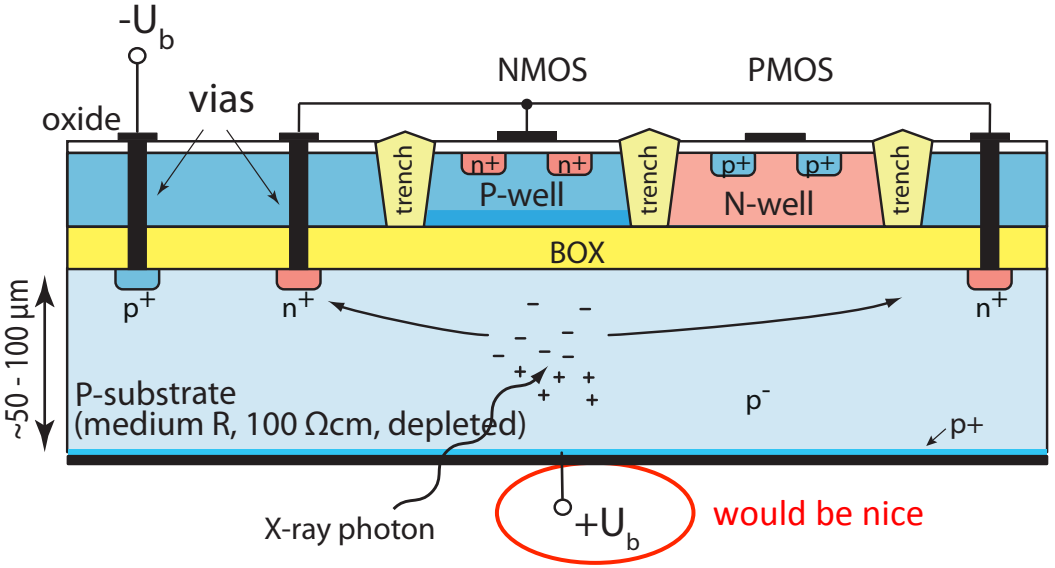
universitätbonn

CMOS on SOI

$$d \sim \sqrt{\rho \cdot V}$$

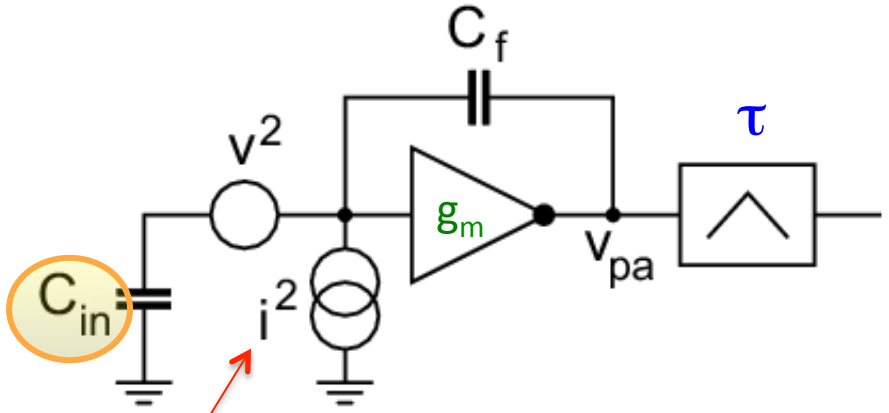


- **FD-SOI**
- OKI/LAPIS/KEK
  Y. Arai et al.
- issues
  - back gate effect
  - radiation issues due to BOX
- cures invented in recent years
- but not suited for LHC - pp



- **HV-SOI (thick film)**
- Hemperek, Kishishita, Krüger, NW
  doi:10.1016/j.nima.2015.02.052
- a promising alternative
- doped, non-depleted P- and N-wells prevent back gate effect and increase the radiation tolerance

Noise in a pixel detector



speed

rad. damage

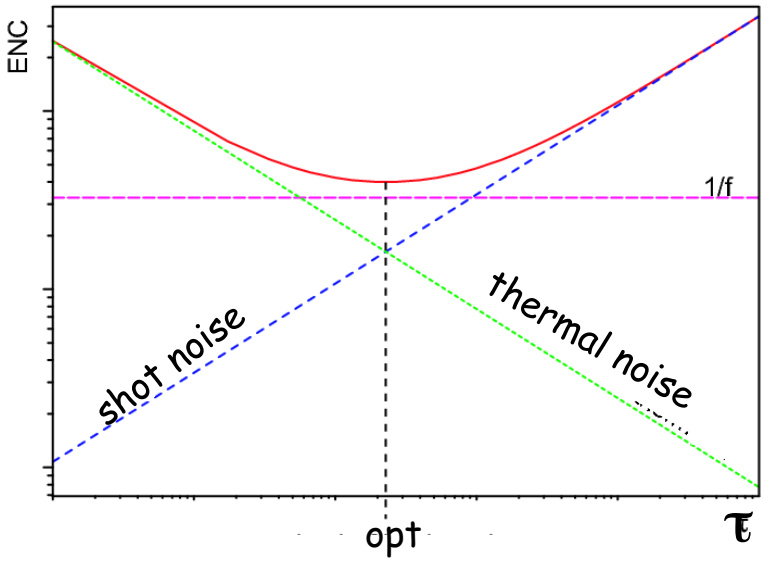
$$\left(\frac{\mathrm{ENC}}{\mathrm{e}^-}\right)^2 = 115 \cdot \frac{\tau}{10\,\mathrm{ns}} \cdot \frac{I_{\mathrm{leak}}}{1\,\mathrm{nA}}$$ - shot

$$+ 388 \cdot \frac{10\,\mathrm{ns}}{\tau} \cdot \frac{\mathrm{mS}}{g_m} \cdot \left(\frac{C_{\mathrm{in}}}{100\,\mathrm{fF}}\right)^2$$ - thermal

power

$$+ 74 \cdot \left(\frac{C_{\mathrm{in}}}{100\,\mathrm{fF}}\right)^2 \cdot$$ - 1/f

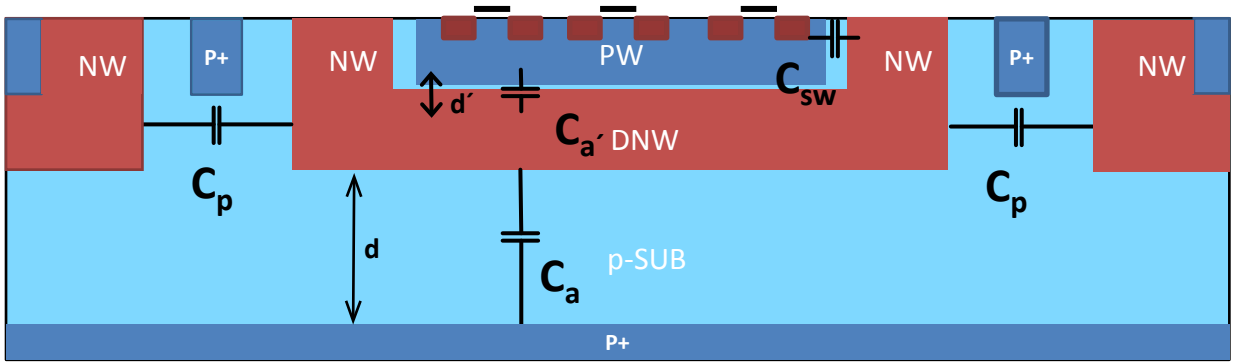
~80-200 fF for pixels



fast and low noise => needs g_m -> i.e. power

The input capacitance to the CSA is crucial ...

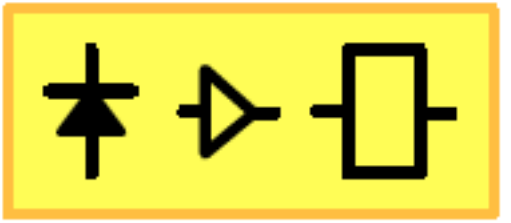
- noise (ENC ~ C_{in}) increases with the input capacitance
- speed also depends on C_{in} => the smaller the better
- for active CMOS pixels there are additional capacitance contributions
  (see H. Krüger, http://indico.cern.ch/event/328762/contribution/4/material/slides/0.pdf)
  - C between deep N-well and P-well is dominant
  - C_{in} does not scale (down) with area



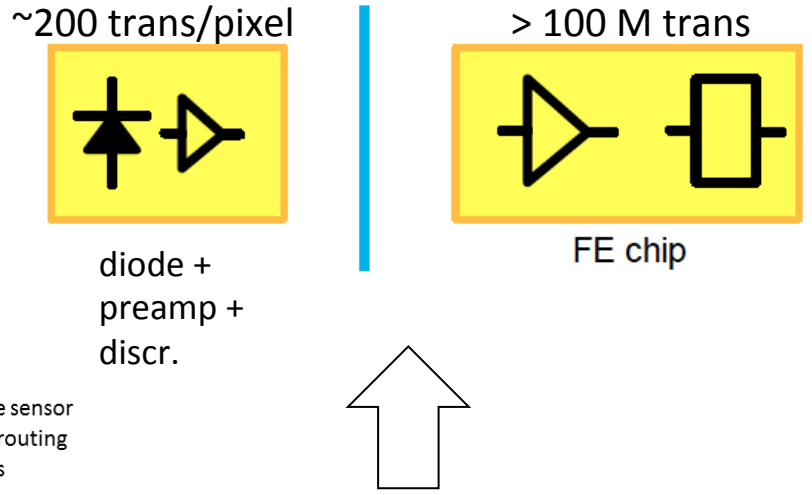
- hybrid planar pixels (e.g. ATLAS IBL, 50×250×200 µm^3): **C_{in} = 109 fF** (Havranek et al, NIMA 714 (2013) 83-89
- CMOS pixel extrapolation: **C_{in} ≈ 200 fF**

One can think of different realisations for the ITK

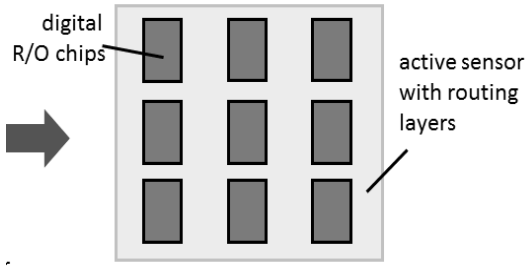
- fully monolithic providing the complete R/O architecture on-chip (FE-I3 or FE-I4 like)



- smart CMOS pixel sensor + FE-chip



- Sparsified CMOS exploiting in-Si routing options and possibly large bump pitches, eg C4 bumps, for low cost



current focus of CMOS demonstrator WG using well understood FE-I4 as R/O chip

demands/requirements are quite different for inner pixel layers (r=3-6 cm, small area) and outer pixel layers (r > 25 cm, large area)

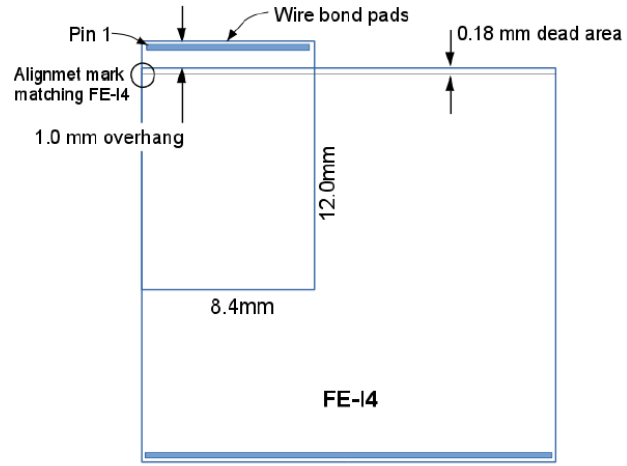


Fig. 1: Alignment of demonstrator to FE-I4 chip

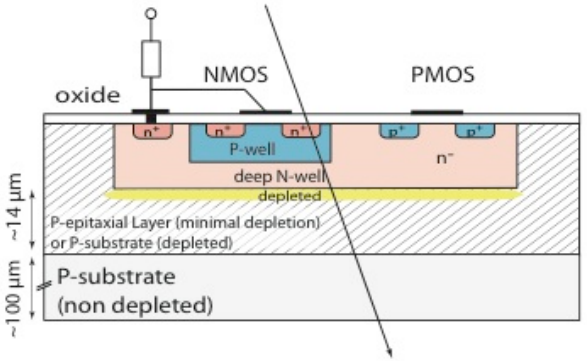
- **goal:** develop a **cm² sized CMOS pixel module**
  - at first: bondable to a FE-I4 R/O chip (option

- **specs**
  - radiation tolerant to **50 Mrad (TID), 10^{15} /cm² (NIEL)**
  - **> 95% in-time** (<25 ns) efficiency after irradiation
  - < 20 µA power per pixel
  - **bondable** via bumps or glue to FE-I4

  - an area read out **through the pixel chip** (bonded to FE-I4)
  - an area read out **standalone** -> to characterize CMOS part
  - a **passive** area -> to compare to standard hybrid pixels

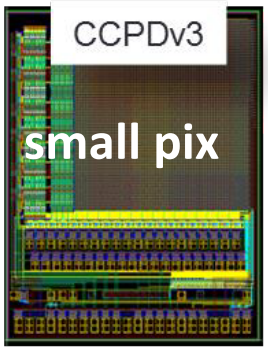
Some selected pre-demonstrator prototype results

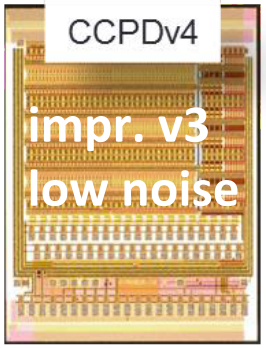
HV-CMOS (H18 180 nm)



Karlsruhe (design&test)
Geneva, CCPM, CERN,
Bonn (char&tests)

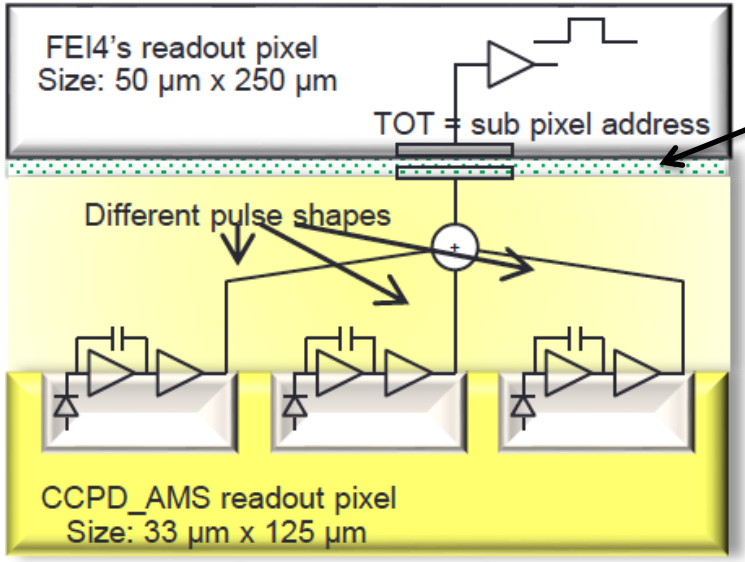
4 versions since 2011





specs

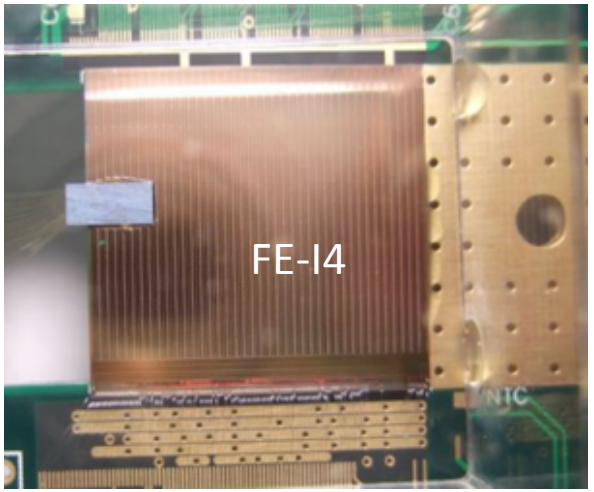
- ρ = 10 Ωcm
- bias 60 – 100 V
- depletion depth ~10 µm
- Q (theoretical) ~1000 e- by drift
- R/O via ATLAS pixel chip capacitively coupled
- design ported also to **GF & LF** (CPPM/KIT)



glue

sub-pixel decoding
through pulse shape
(TOT => sub-address)

50 × 250 µm² => 33 × 125 µm²
effectively

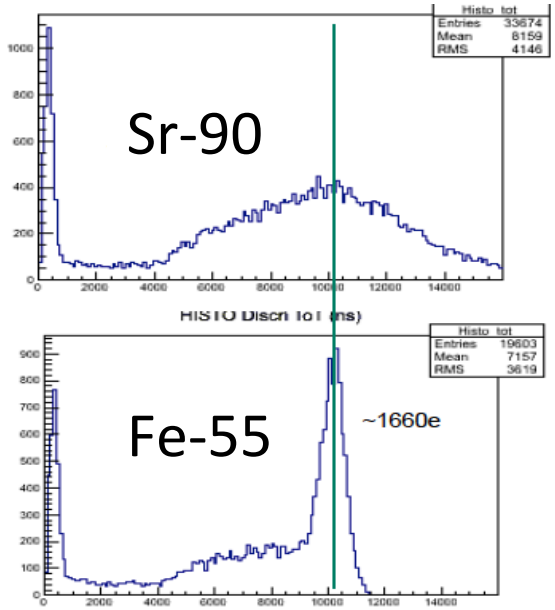


I. Peric et al., NIM A765 (2014) 172-176

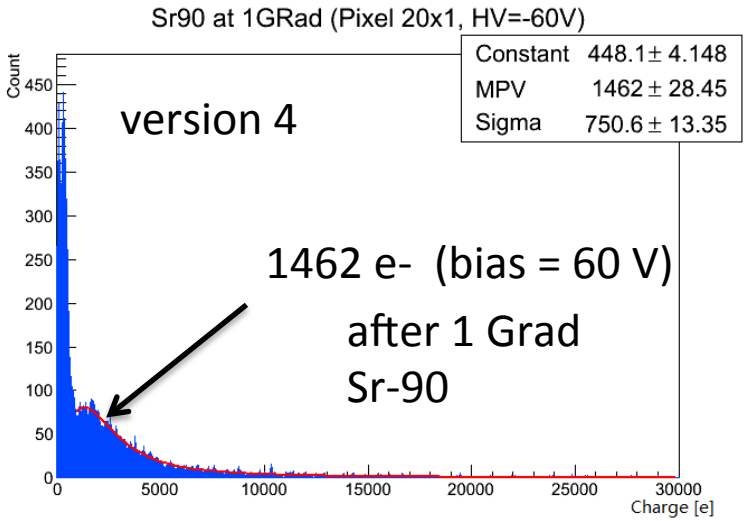
AMS 180 nm

some encouraging results

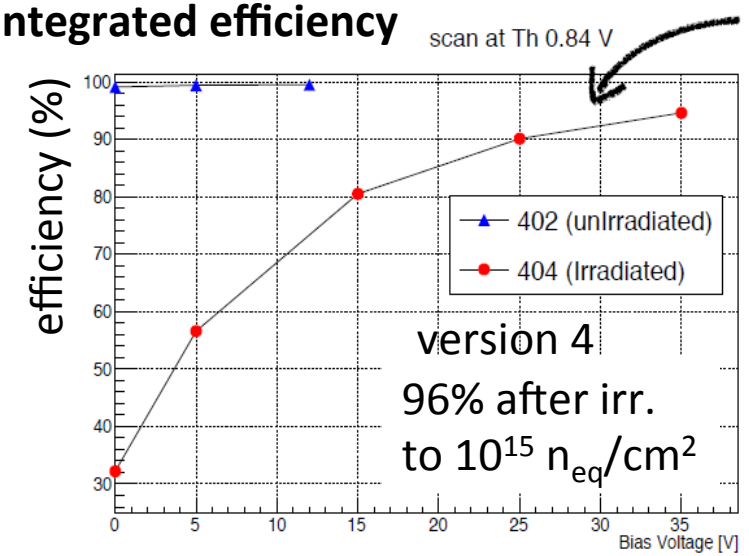
- **capacitive coupling** seems to work in principle whether it is competitive in terms of reliability and price is unclear
- chips stand TIDs up to **1 Grad**
- proton irradiation 10^{15} n_{eq}/cm^2 performed
- efficiency (time integrated): 99% -> **96%**
- **in-time efficiency** not yet met (τ_{rise}~100 ns)
- signal ~ 1500 e ; SNR ~ 25
- characterizations w/o FE-I4 ongoing



version 2
before
irradiation



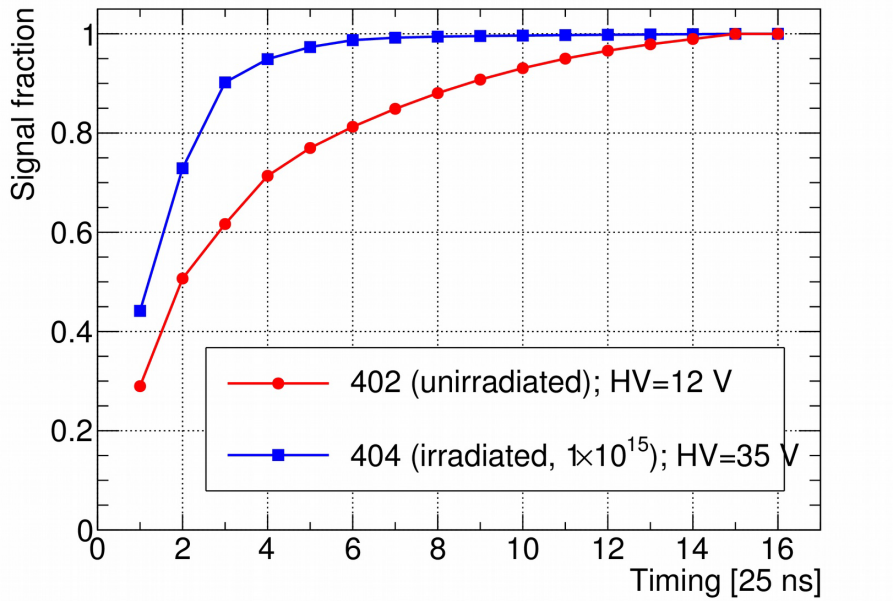
time integrated efficiency

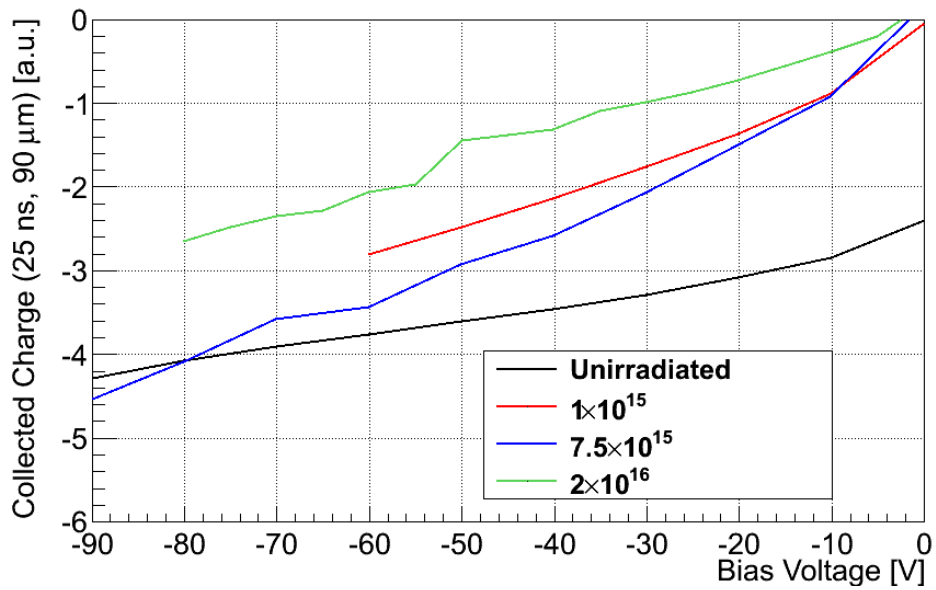


AMS 180 nm version4

The only CMOS sensor which has seen >> 10^{15} neutrons / cm^2 (up to 2 x 10^{16} n/cm^2, i.e. HL-LHC)

Geneva characterizations



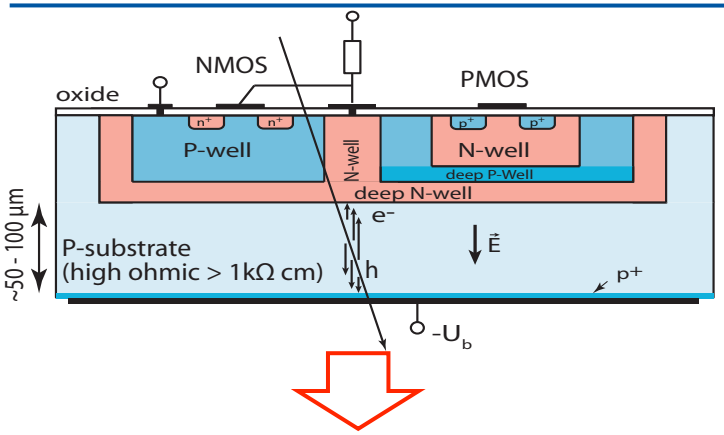


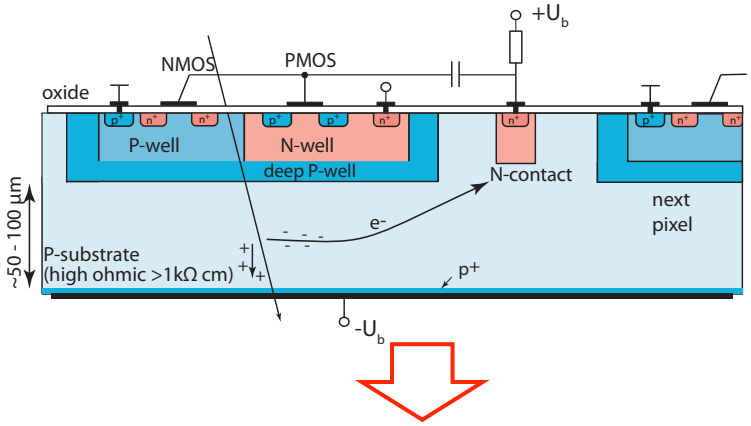
timing issue

more in dedicated HV-CMOS talk by Andre Schöning

Intime signal fraction <u>increases</u> with irradiation, probably due to acceptor removal and larger fraction of charge collected by drift **also depletion depth** increases to ~20 µm @ -80V

HR-CMOS:

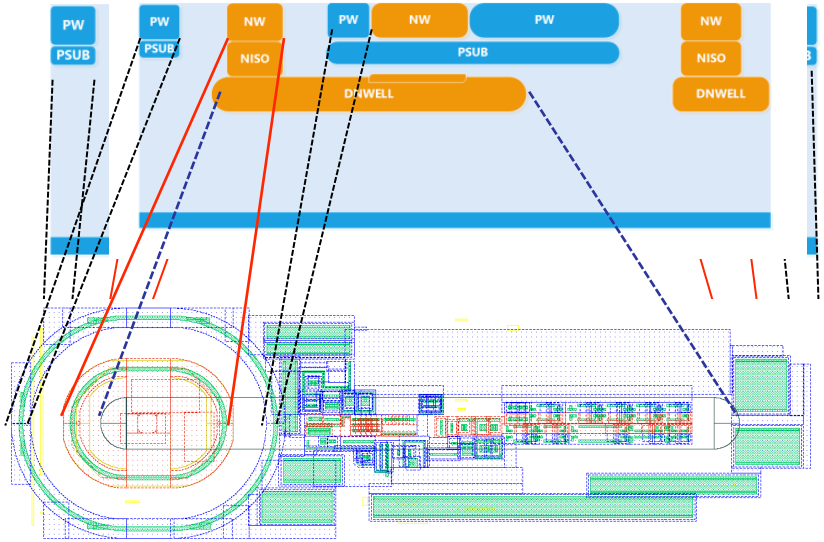




Electronics inside collection well

- Large fill factor for high CCE and rad-hardness
- Full CMOS, isolation via deep p-well (PSUB)
- HR substrate **(2 kΩ cm)**, p bulk
- 150 nm process

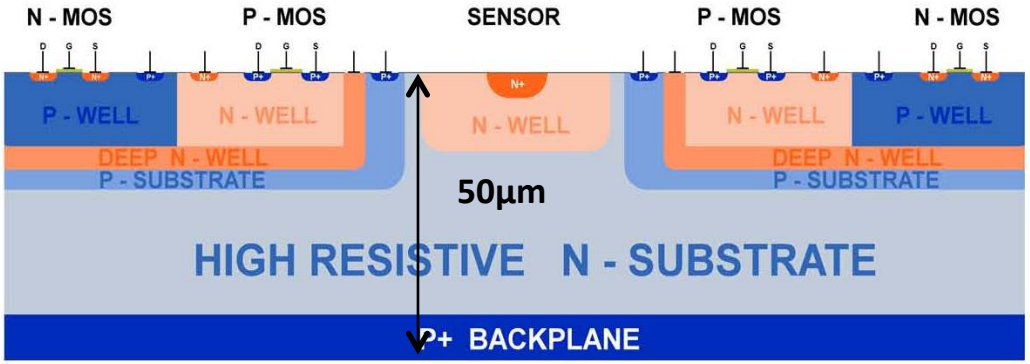
Bonn, CPPM, Karlsruhe



Electronics outside collection well

- Small fill factor, no competing wells
- Full CMOS, isolation via deep n- and p-well
- HR substrate **>2kΩ cm**, n bulk
- **Backside** thinning **and implant**: default option
- 150 nm

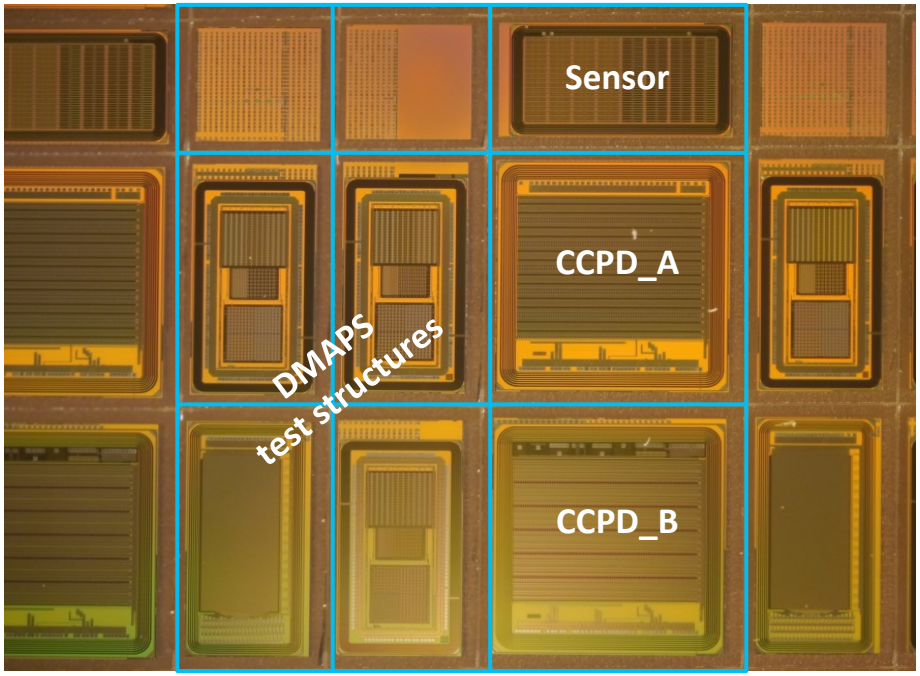
Bonn, Prague
(design+tests)

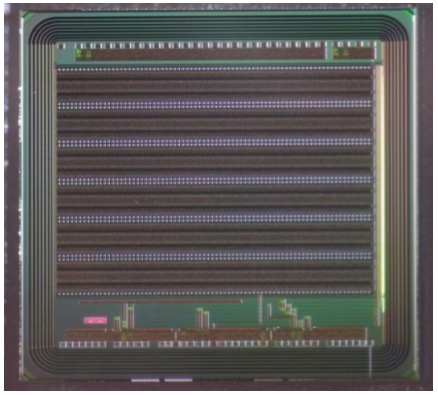


Prototypes: CCPD_LF (also: LF_CMOS sensor)

- **First wafer** received 2 weeks ago from cutting. Full thickness, no backside processing
  - 5 wafers at the foundry for backside processing (i.e. thinning and backside implant)

- Wafer: CZ 8”, p-type, min. **2kOhm cm**
- **Technology parameters:**
  - 150nm CMOS node
  - only regular transistors used
  - 4 metal layers used (6 available)
  - deep n-well and deep p-well
- **Many testing capabilities**
  - readout w/ **and** w/o FE-I4 chip
  - every pixel hit information can be read independently via shift register
  - every preamplifier output and comparator output can be monitored
  - HitOr
- **Testing just started**



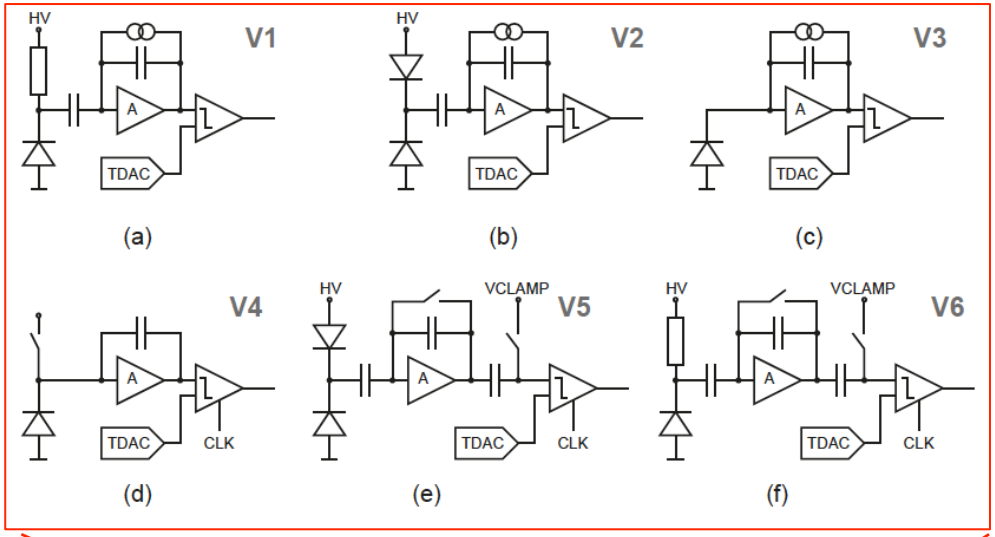


Design: Bonn, CPPM, Karlsruhe

Prototypes: test chips EPCB01 and EPCB02

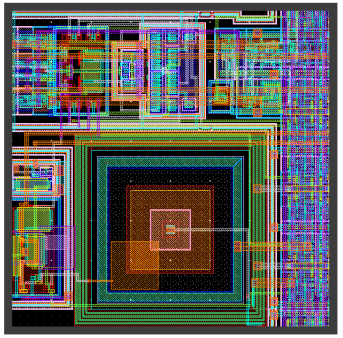
universitätbonn

- 150nm CMOS, 6 metal layers
- deep p-well, isolated full CMOS
- substrate: **n-type bulk** (> 2 kΩ cm)
- bias voltage up to 20V
- **50µm thin + p-implant (backside)**
- 6 pixel matrices
- pixel size: 40 × 40µm²
- **~50 µm depletion depth**

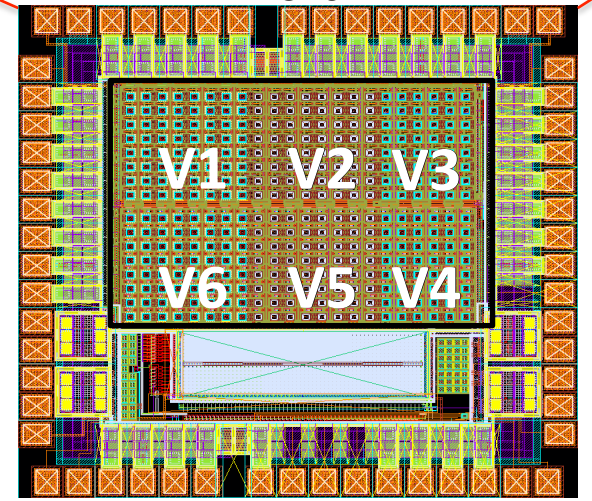


main goal: characterization of designs & technology

Matrix version	Biasing & coupling	Analog FE
V1	Resistor + AC	Continuous
V2	Diode + AC	Continuous
V3	Direct + DC	Continuous
V4	Direct + DC	Switched
V5	Diode + AC	Switched
V6	Resistor + AC	Switched



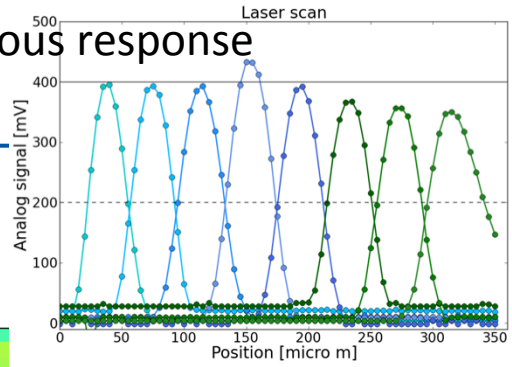
EPCB01



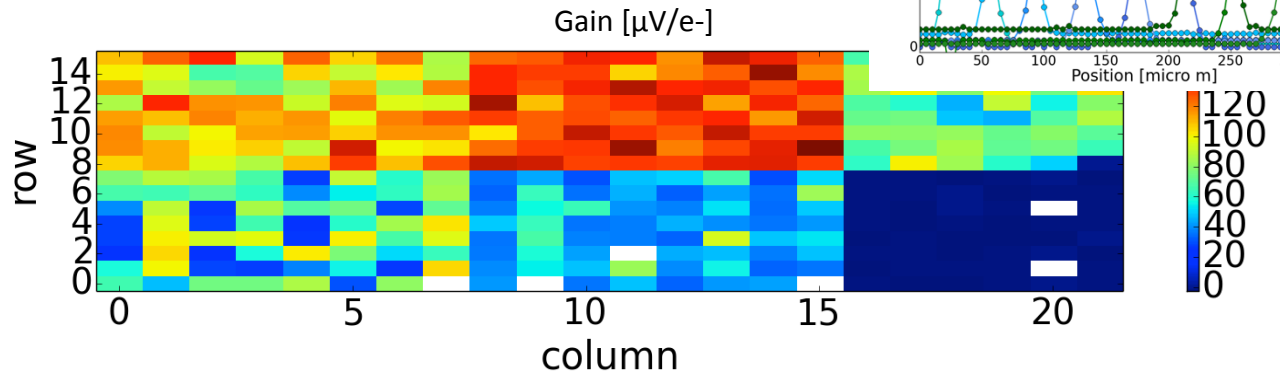
Design & testing: Bonn, Prague

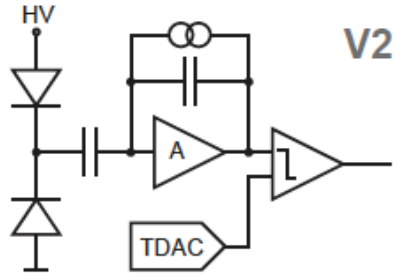
EPBC01 & EPBC02 (improved version)

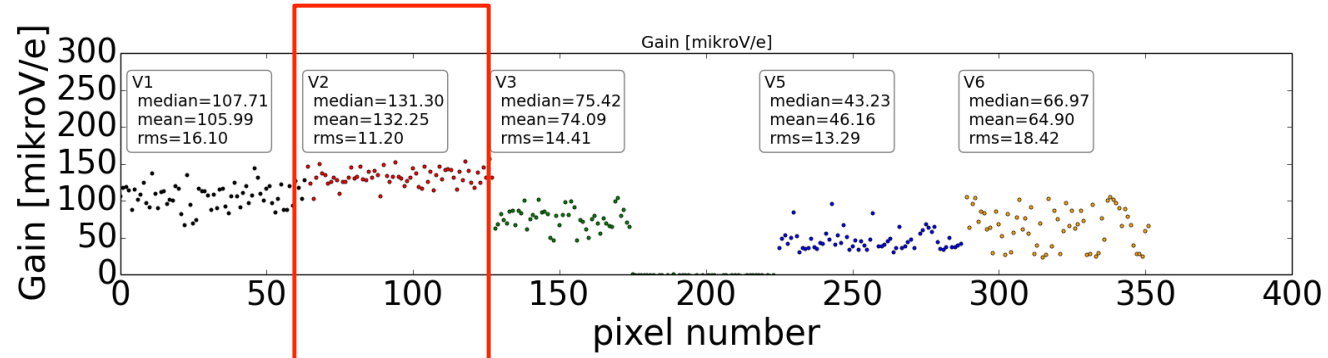
homogeneous response to laser

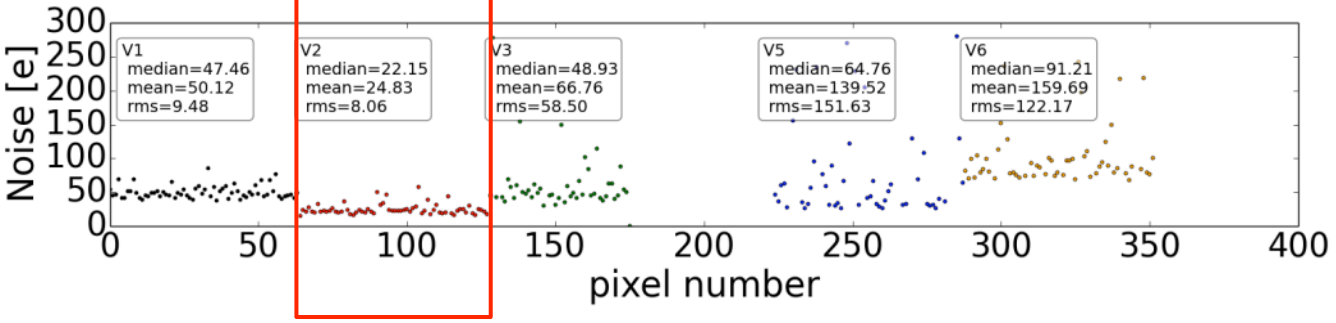


- Best values for **V2:**
  - Noise = 25e-
  - Gain = 135 µV/e- spread = 11µV/e-
- Threshold dispersion
  - 80e- after tuning (V2 @1000e-)
- some charge loss in EPBC01, no loss in EPCB02
- irradiations ongoing

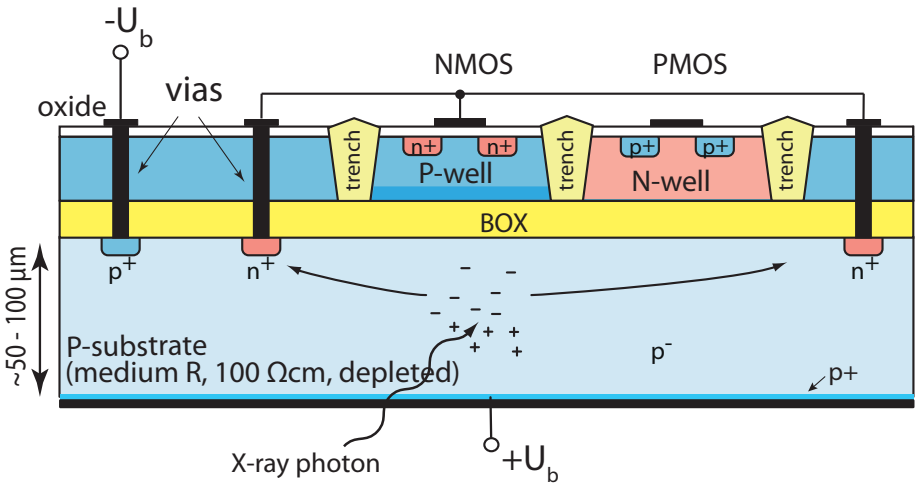








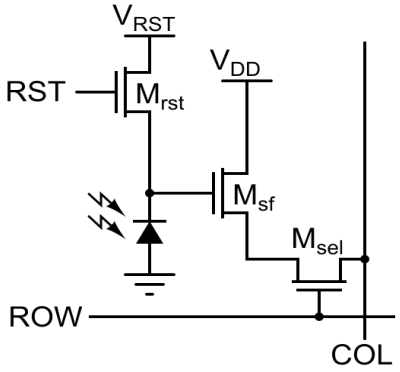
HV-SOI: test chips XTB01 and XTB02

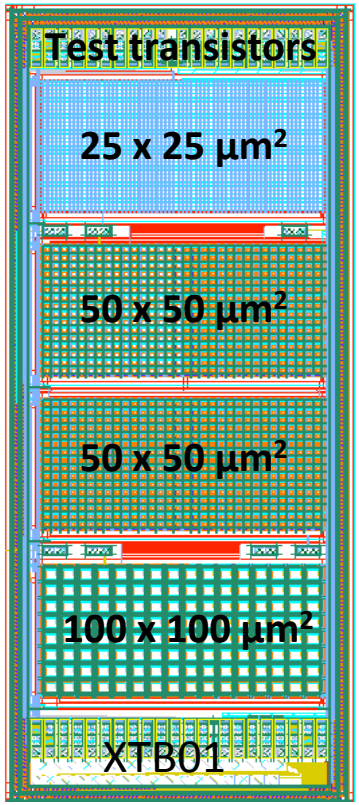


180 nm: Electronics outside collection well

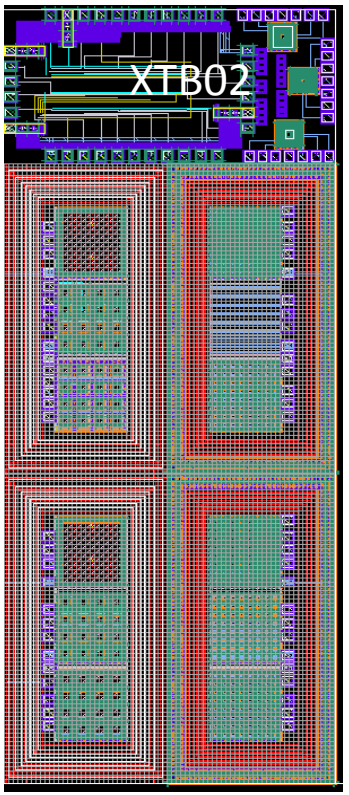
- Small charge collection well
- Full CMOS, no backgate effect
  due to isolation via deep p-well (non-depleted)
  between CMOS layer and BOX
- HV technology + MR substrate (100 Ωcm), p bulk

- 3 T readout





Design: Bonn
Testing: Bonn, CERN



dedicated structures to test the technology further (leakage, break down voltage, etc.)

XTB01 test chip: first irradiation tests

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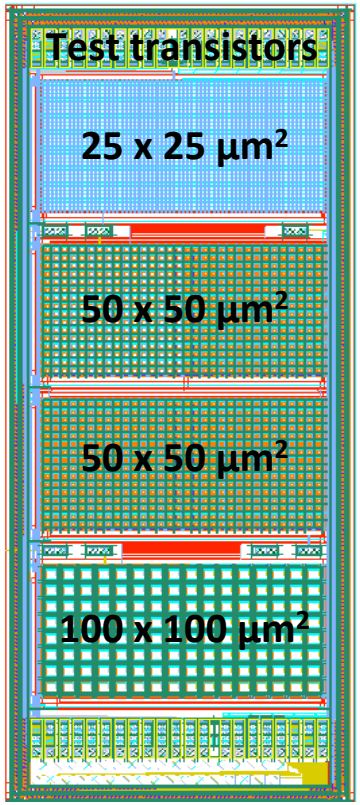
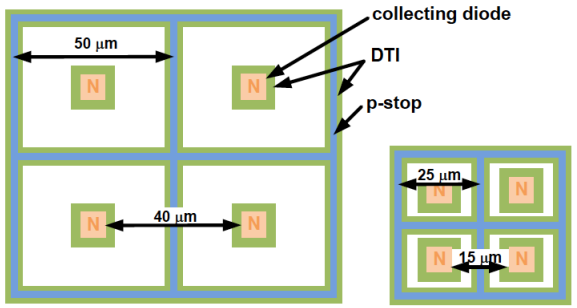


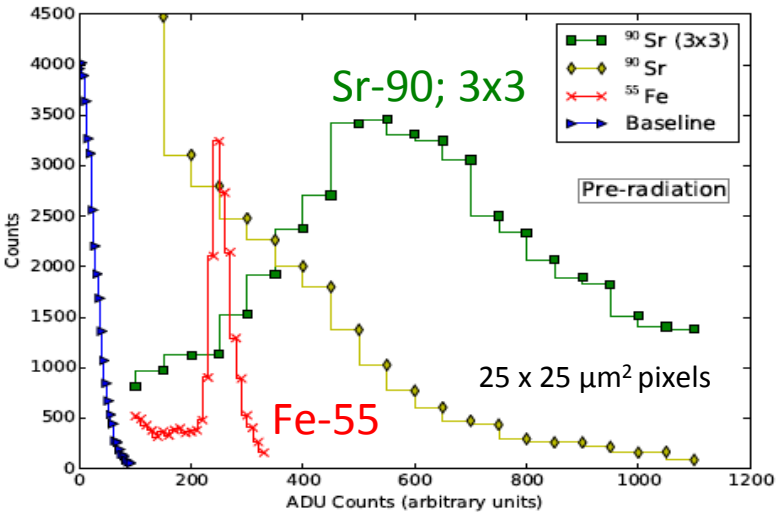
Design: Bonn
Testing: Bonn, CERN



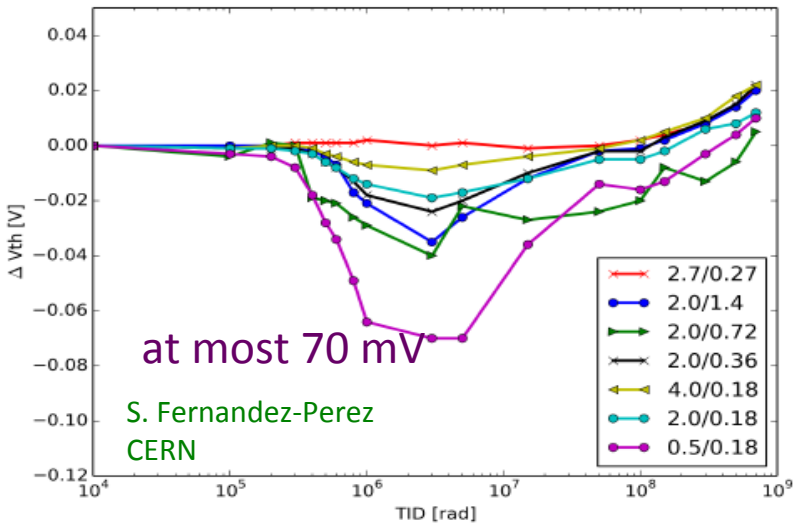
NIEL

TID

before irradiation

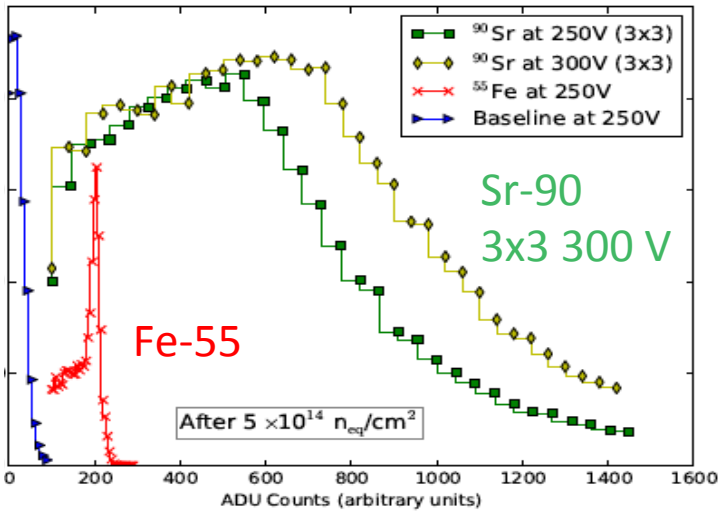


NMOS threshold shift after **700 Mrad**



S. Fernandez-Perez
CERN

after irradiation: **5 x 10¹⁴** n_{eq}/cm^2



Hemperek, Kishishita, Krüger, NW
arxiv 1412.3973, accepted NIM A

XBT01 in test beam - 50x50µm² pixel

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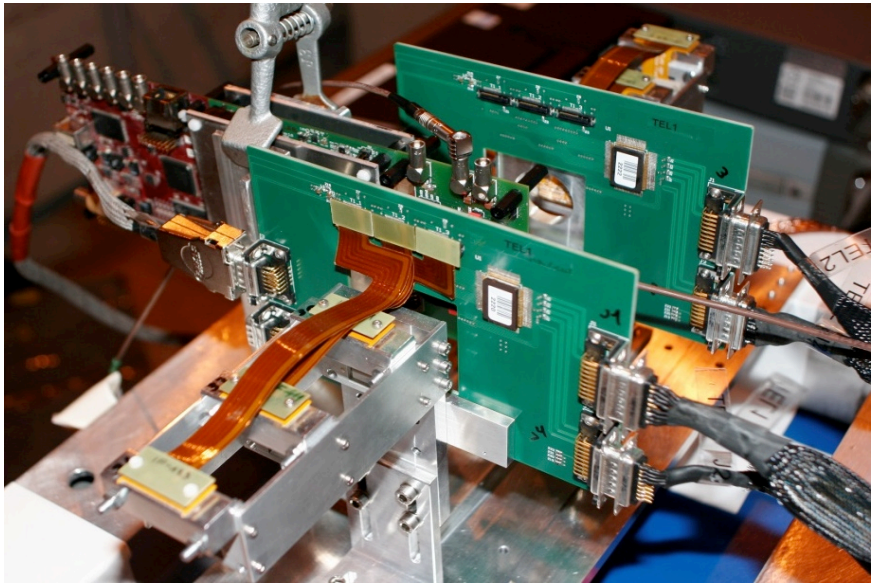

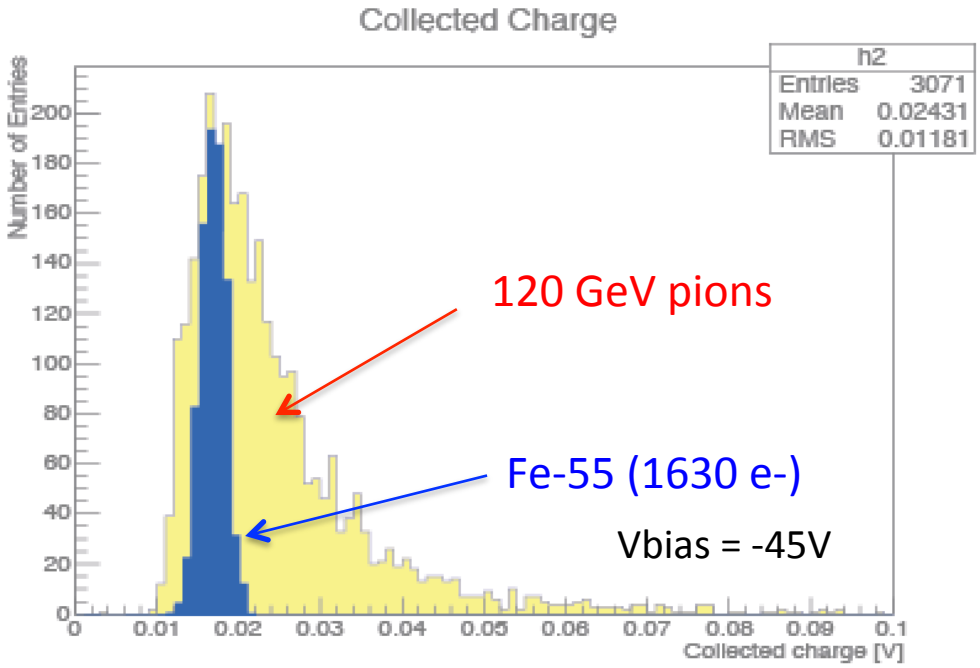

Depletion depth ≈ 31µm

Calculated depletion depth = 36µm (@100 Ωcm, -45V)

Conclusions

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- There is a large momentum in R&D for CMOS active pixels as an attractive direction for LHC experiments, even for LHC-pp.
- … and if not for HL-LHC (too late?) … then for sure for other applications (e.g. photon science).
- R&D profits from modern micro electronics technologies and its rapid progress.