Development of hybrid pixel modules for HL-LHC

Δp.Δg≥źt



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Introduction

- Thinning technologies for pixel sensors
- Comparison of Charge Collection results at different thicknesses after irradiation
- Effect of thickness on tracking at high eta
- Performance of active / slim edge 3D and planar sensors
- Module design for hybrid pixel modules at HL-LHC

Thin pixel sensors for HL-LHC

*Thin active thickness very attractive:



- After irradiation charge collection length reduced, so thickness no advantage
- Higher electric field, faster collection times
- lacksim Lower operation bias voltages ightarrow lower power
- Lower occupancy at high eta
- Possibility to reduce material (multiple scattering)

Reduce dead regions at edge of sensors

Allows the innermost layers to remain closer to the IP by avoiding the need for tiling → several methods investigated



Thin planar pixels on SOI material + active edges



- First production: n-in-p pixels on FZ and MCZ SOI material
- 🗖 100 μm and 200 μm thickness

□ Flip-chipping performed at VTT after removal of support wafer (etching down to SiO₂ interface, acting as a natural etching stop)







Thin Silicon Substrates



- Use wafer stacks with a low resistivity substrate than can be used as a contact on the backside
 - Epi material with MCz substrate
 - Si-Si direct bonding: for our applications high resistivity FZ to low resistivity MCz

CMS HPK Campaign

- Deep Diffused Silicon, effective thin active layer created on thicker substrate
- Smoother Neff transition than in composite substrates



Alternative thinning method without support wafers (I)



- relatively simple technology without using support / handling wafers
 - □ anisotropic wet etching (KOH) on <100> wafers
 - Experience with this technology at CIS for MEMS/ pressure sensors production



- First R&D production on 4" p-type FZ wafers; process contributed by CIS; target thickness 100 and 150 μm
 - **Δ** Starting thickness 525 μm
 - Front-side processing up to nitride deposition

- Back-side p+ implantation, top-side p-spray → common annealing step
- Metallization on the front and back side
- UBM (electroless Nickel at CiS or standard one at IZM)
- dicing



Alternative thinning method without support wafers (II)



Two sets of dicing lines:

- $\hfill\square$ On the 420 μm wide frame between the structures
- Dicing along the sensor perimeter on the thinned substrate
- Guard ring structure within the thinned area

Design in collaboration between MPP and CIS

- First etching trials on test wafers :
- 325 minutes etching time

Maximum thickness variation inside the quad sensors ~ 10 μm



Comparison between 100 and 200 µm thick sensors

FE-I4, 100 μ m thick, 5x10¹⁵ n_{eq} /cm²



FE-I4, 200 μm thick, 5x10¹⁵ n_{e0}/cm²



VTT FE-I3 100 μ m, Φ =5x10¹⁵ n_{e0}/cm²

(99.0±0.3)% global hit efficiency at Vbias= $300 V (125 \mu m edge)$

VTT FE-I₄ 100 μm, Φ=5x10¹⁵ neq/cm²

(97.0±0.3)% global hit efficiency at Vbias ≥ 350 V

VTT FE-I₄ 200 μm, Φ=6x10¹⁵ neg/cm²

 (96.9 ± 0.3) % global hit efficiency at Vbias= 500 V

Charge collection for pixels of different thickness (I)

At higher fluences the effect of charge trapping tends to equalize the charge collection efficiency for all thicknesses



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Charge collection for pixels of different thickness (II)

- Epitaxial strip silicon sensors of n and p-type baby sensors from HPK campaign
- **1** 100 μ m active thickness + 200 μ m thickness for 1.3 x 10¹⁶ neq cm⁻²
- \square MCZ with 200 µm physical thickness, only @ 1.3 x 10¹⁶ neq cm⁻²
 - \rightarrow 100 µm \rightarrow faster signal recovery
 - ightarrow 200 μ m ightarrow higher breakdown voltage
 - ightarrow Similar signal height for both thicknesses at highest bias





Effect of thickness on tracking at high eta

¶∆p.∆g≥<mark>źź</mark>

Tracking with 50x50 μ m² pitch pixels: Cluster Multiplicity



Planar Sensor (100 μ m thick), eta=2.5



Module Tuning:

- Threshold 1 ke (planar, 3D), 1.5 ke (3D)
- Charge calibration 6 ToT at 4 ke
- Measured cluster width in Y (along 50 µm pitch direction) 2-3 units less than pure geometrical expectations
- Difference is due to ~ 1 degree misalignment and threshold effects in the entrance and exit pixels

3D Sensor (230 µm thick), eta=2.5





Slim / active edges

Hit efficiency for active edge planar pixel modules

- **Γ** FE-I3: 50 μm active edge with floating GR
- □ 4 GeV electrons, EUDET telescope
- 99 % hit efficiency on the last pixel column
- (87.4 ±0.7) % hit efficiency between pixel implant and sensor edge (50 μm)
- $\boldsymbol{\rightarrow}$ Completely efficient up to last 20 μm from the edge







Slim edge pixel modules after irradiation

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- irradiated at Φ=5x10¹⁵ n_{eq}/cm²
- threshold: 1500 e-
- (69±3=2)% hit efficiency between the last pixel implant and the BR (DESY, 4 GeV electrons)
- ightarrow 100 μ m effective inactive edge









 $\Delta p \cdot \Delta q \ge \frac{1}{2}$

Active / slim edge 3D sensors

- Studies to achieve very slim edges with 3D sensors for ATLAS Forward Physics Experiment (AFP)
- Edge termination: CNM: 3D guard ring of n⁺ columns + p⁺ ohmic-column fence
- □ FBK: p⁺ ohmic-column fence
- Left/right edge: already 200 μm slim edge for IBL
- Bottom (should be slim for AFP): 1.5 mm bias tab in IBL production (not needed!)



E. Cavallaro, Status of the 3D silicon detectors for the ATLAS AFP, Trento Workshop 2015

Test beam results of active / slim edge 3D sensors

E. Cavallaro, Status of the 3D silicon detectors for the ATLAS AFP, Trento Workshop 2015



- DESY testbeam (4-5 GeV e-) with EUDET-type telescope
- Efficiency stable up to last pixel (smeared by telescope resolution)
- For FBK even ~75 um beyond pixel edge → Efficient edge due to absence of guard ring
- For both CNM and FBK <150 µm insensitive edge! → Slimmest edge apart from fully active edge technology

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Slim edge in the ATLAS IBL n-in-n sensors





 $\mathbb{Z}_{p\cdot\Delta_g}$

Multi chip module assemblies for HL-LHC



Outer pixel layers will be instrumented with multi chip modules: quad sensors cover 4 FE-I4 chips, using long and ganged pixels between FE-I4 to increase active area



Quad modules are being developed by German, Japan, UK ATLAS groups

Liverpool Quad PCB





Thinning the read-out chip

- Good yield for full thickness modules with solder bump bonding and different vendors
- Modules with chips thickness ≤ 150 µm shows disconnected areas at the edges → Bowing due to CTE mismatch between metal stack and silicon substrate



- ATLAS: Investigate remove or reduce bowing with stress compensation layer on back of chip
- Effort underway at a number of vendors (HPK, LETI)
- Measurement of bow and material properties suggest using: 0.5µm SiN/Ti/4µm Al-Si SCL

Large area pixel modules for HL-.-LHC pixel upgrades, C.Buttar, Pixel 2014



- IZM developed a glass carrier substrate, glued with polyimide glue, that can be dissolved by laser exposure
- Used for the ATLAS IBL with chip 150 μm thick, now under study for quad modules and chips 100 μm thick

Spark protection

- Consequence of p-type choice: HV is close to ASIC and sparking can occur
- As voltages of up to 1000V may be required, protection is necessary





Development of HPK/KEK pixel sensors, Y. Unno. Pixel 2014

→ no HV breakdown up to 1000 V

Very good radiation hardness shown with sensors of the CMS HPK campaign



- 3 μm thick BCB coating (ATLAS) with lithography on sensor surface to open the bump contact \rightarrow also tested up to 1000V
- The vertical walls of the sensors are still unprotected \rightarrow BCB coating also on the cantilever side of the chip could help

Alternative interconnection methods

- A cheaper alternative sensor post-processing under development at CIS is electroless Nickel UBM (w/ or w/o mask), in combination with IZM solder bumps
 - \rightarrow also in this case UBM pad= 20 μ m
 - At ADVACAM thin film UBM pads on sensor side compatible with SnPb solder bumps processed in house or Cu pillars in collaboration with CEA-LETI







Summary

- Different technologies are being investigated for the production of thin hybrid pixel modules for the ATLAS/CMS trackers at HL-LHC
 - Charge collection measurements and beam tests prove the possibility of operating thinner detectors at reduced bias voltages with respect to thicker devices
 - Islim/ active edges can be employed to avoid module superimposition in the inner layers → compromise between reduction of inactive area and achievable V_{break}
 - Many engineering solutions explored for the production of full hybrid pixel modules for HL-LHC. Prototyping effort needed to address:
 - Spark protection
 - Flip-chipping of thin read-out chips
 - Low cost bump-bonding

Additional material

 $\mathbb{A}_{p} \mathbb{A}_{g} \ge \frac{1}{2}$

Phase II Pixel System Layout and Requirements



2 Outer Barrel Layers / Disks

- Planar n-in-p sensors baseline option
- Sensor thickness 150 μm
- □ 2x2 (Quad) chip modules

2 Inner Barrel Layers

- Sensors: different materials and technologies possible
- Radiation hardness up to 2x10¹⁶ n_{eq}/cm²
- **□** Thickness: 150 µm or lower
- Pixel pitch of 25x100 µm² or 50x50 µm² → FE-chip in 65 nm CMOS technology

Second production of active edge pixels at ADVACAM



Active edge process for all the structures

Wafer layout of the new production at ADVACAM (spin-off VTT)

- In collaboration with Glasgow, Göttingen, LAL, CLIC CERN-LCD,
- Geneva University for medical applications

50, 100, 150 μm sensor thickness: 5 FZ p-type wafers for each thickness

- FE-I4 quad sensor
- FE-I4 single chip sensors different geometries
- Omegapix sensors
- TIMEPIX sensors for CLIC R&D
- CLICpix sensors for CLIC R&D
- Pixel and strip structures for medical applications

FE-I₄ Single Chip Modules



FE-I4 with 50 µm edge, one GR, no punch-through structure



FE-I4 with 100 µm edge, Bias Ring + Guard Ring, std punch-through structure



FE-I4 with 100 µm edge, Bias Ring, new external punch-through structure



FE-I4 with 100 µm edge, Bias Ring, std punch-through structure









 $\Delta p \Delta q \ge \frac{1}{2}$



50 μm active sensor thickness 380 μm thick handle wafer



- Production of the sensor wafers completed
- Next steps:
 - Electroless UBM
 - Removal of the handle wafer
 - Flip-chipping of the first FE-I4 and TIMEPix modules



Comparison between 100 and 200 μm thick sensors

FE-I4, 100 μm thick, 5x1015 n_{eq}/cm^2



 $\Phi = 0, \text{ thr.: } 1600 \text{ e}$ $\Phi = 2, \text{ thr.: } 1000 \text{ e}$ $\Phi = 6, \text{ thr.: } 1000 \text{ e}$ $\Phi = 6, \text{ thr.: } 1000 \text{ e}$ $\Phi = 6, \text{ thr.: } 1000 \text{ e}$ $\Phi = 10^{15}/\text{cm}^2$ $\Phi = 0, \text{ thr.: } 1000 \text{ e}$ $\Phi = 10^{15}/\text{cm}^2$ $\Phi = 0, \text{ thr.: } 1000 \text{ e}$ $\Phi = 0, \text{ thr.: } 1000 \text{ thr.$

FE-I4, 200 μm thick, 5x10¹⁵ n_{e0}/cm²

VTT FE-l3 100 μm, Φ=5x10¹⁵ n_{eq}/cm²

(99.0±0.3)% global hit efficiency at Vbias= 300 V (125 μm edge)

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Hit efficiency for slim edge pixel modules









Γ FE-I3: 125 μm edge with BR

- not irradiated
- V_{bias}= 20V
- threshold: 1500 e-
- (69±3)% hit efficiency between the last pixel implant and the BR (CERN SpS, 120 GeV pions)



50 µm

VTT active edge sensors

□ Irradiation of active edge FE-I₃ module with reactor neutrons in Ljubljana at Φ =2x10¹⁵ n_{eq}/cm²

🗖 100 µm thickness

Charge collection measurements after irradiation with a ⁹⁰Sr source and the USBPix system

CC comparison between central and edge columns

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Comparison of FE-I₃ and FE-I₄ performance



Development of hybrid pixel modules for HL-LHC

100 µm thickness: FE-I3 modules show a hit efficiency higher than FE-I4 modules at equal fluence and voltage

FE-I₃ module

 $V_{bias}=350 V$

Comparison of FE-I₃ and FE-I₄ performance



Active edges with planar n-in-p sensors - 100 μm thick





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Charge collection efficiency after irradiation

FE-I3 100 µm thick sensor with 125 µm slim edge, threshold 1500 e- → 87% CCE at 300 V for both all and edge pixels after irradiation at KIT (1x10¹⁵ n_{eq}/cm²)



p-type MCZ FE-I4, 100 μm thick sensor, with 125 μm slim edge, threshold 1100 e → compatible charge collection properties between edge and internal pixels



Charge collection efficiency after irradiation

FE-I3 100 µm thick sensor with 125 µm slim edge, threshold 1500 e- → 87% CCE at 300 V for both all and edge pixels after irradiation at KIT (1x10¹⁵ n_{eq}/cm²) and in Ljubljana (5x10¹⁵ n_{eq}/cm²)



p-type MCZ FE-I4, 100 μm thick sensor, with 125 μm slim edge, threshold 1100 e → compatible charge collection properties between edge and internal pixels



Charge collection for pixels of different thickness

 \odot pixel modules for HL-LH Development of hybrid



Charge collection for pixels of different thickness





Tracking with 50 μm pitch pixels at high eta

- lacksquare Aim: study the performance of 50x50 μ m² pitch at high η
- □ Solution: use FE-I₄ modules at high ϕ (80° \rightarrow η =2.5) almost parallel to the beam but rotated by 90° with respect to their normal pixel orientation in the detector
- Samples: 100 μm thick planar sensor (VTT) + 230 μm thick 3D sensor (CNM), back to back in the beam
- ITK/ RD50 test-beam at CERN SPS, October 2014





- **3D** sensor results by I.Lopez
- E. Cavallaro, S. Grinstein, J. Lange

Tracking with 50 μm pitch pixels at high eta (II)



- □ No tracking information from EUDET telescope used (problems encountered in reconstruction)
- □ Very long cluster expected along z for high $\phi = 80^{\circ}$ (η =2.5), use them as "tracks"
 - ~100 % cluster efficiency, more interesting to look at cluster splitting
 - Per pixel hit efficiency determined looking at the pixel w or w/o hits inside the cluster, excluding entrance and exit pixels.



Tracking with 50 μm pitch pixels: Charge Collection

