Karlsruhe Institute of Technology

# ► HV-CMOS

**28.10.2014**

Robert Eber



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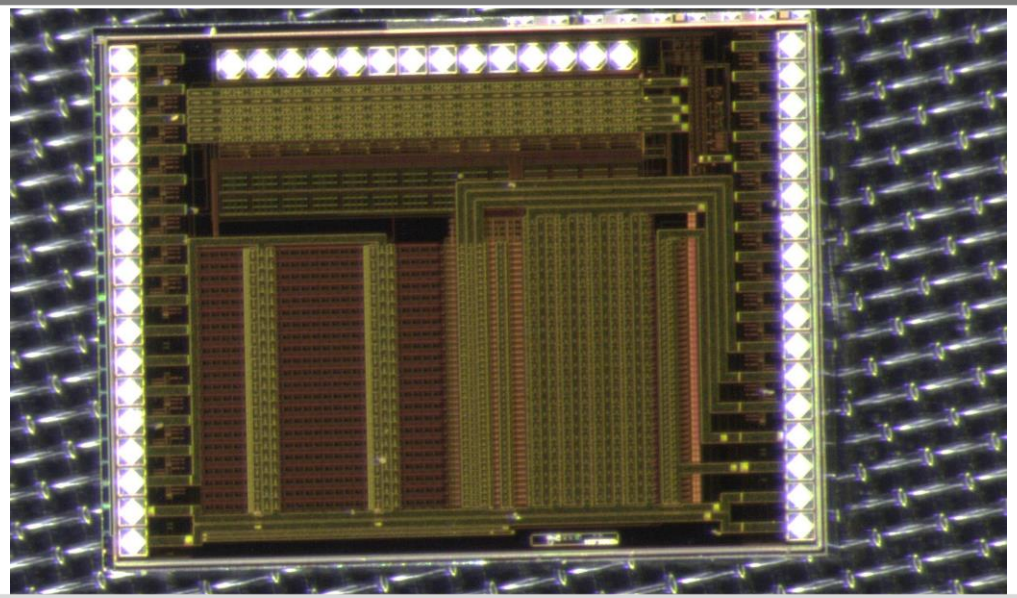
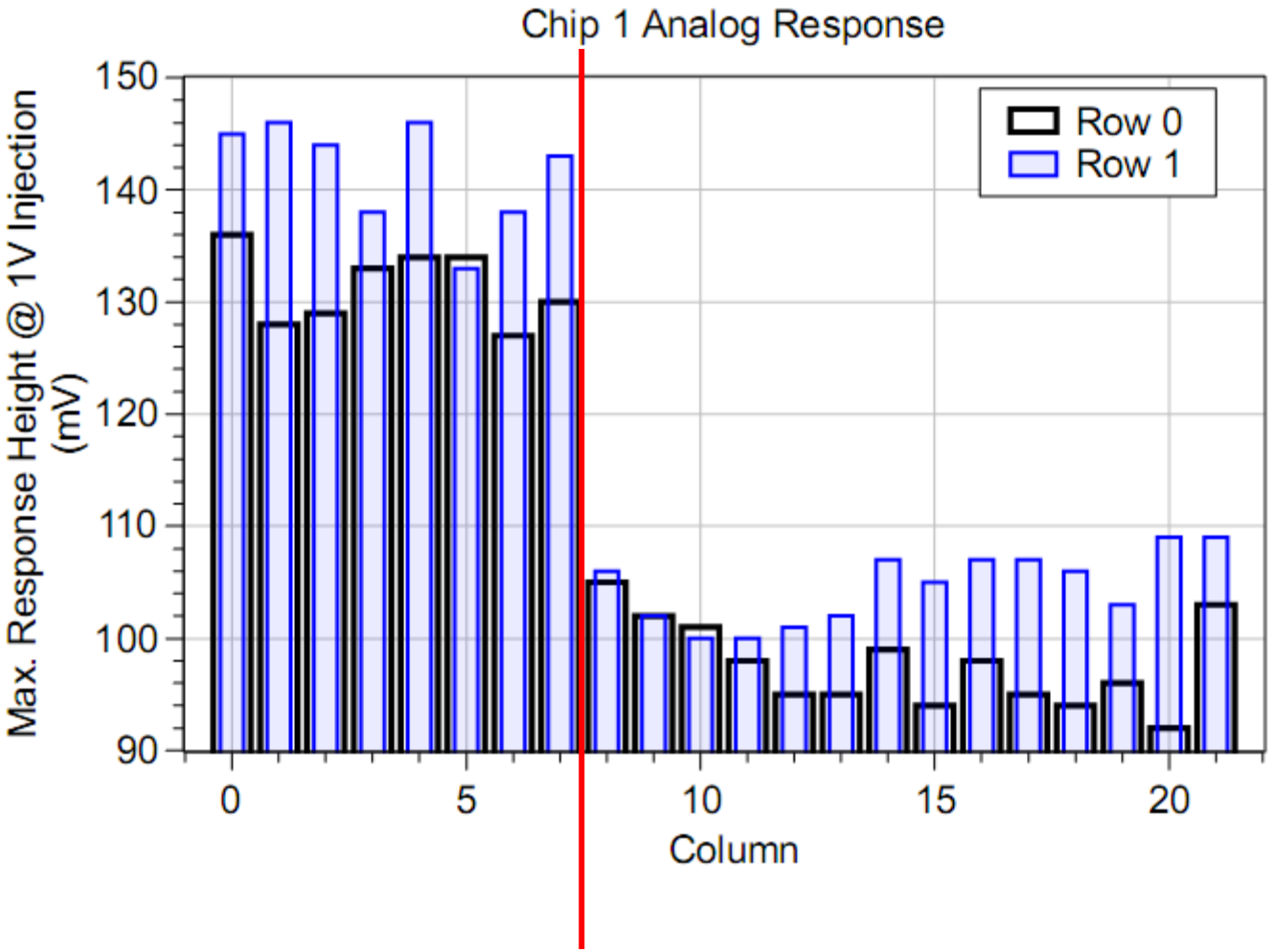


# Analog Response to 1V Injection




- First 8 Pixel use the linear feedback transistor (according to Ivan)
  → higher gain
- Others use the enclosed (circular) transistors
- Compare test structures:
  - NMOSlin
  - NMOScirc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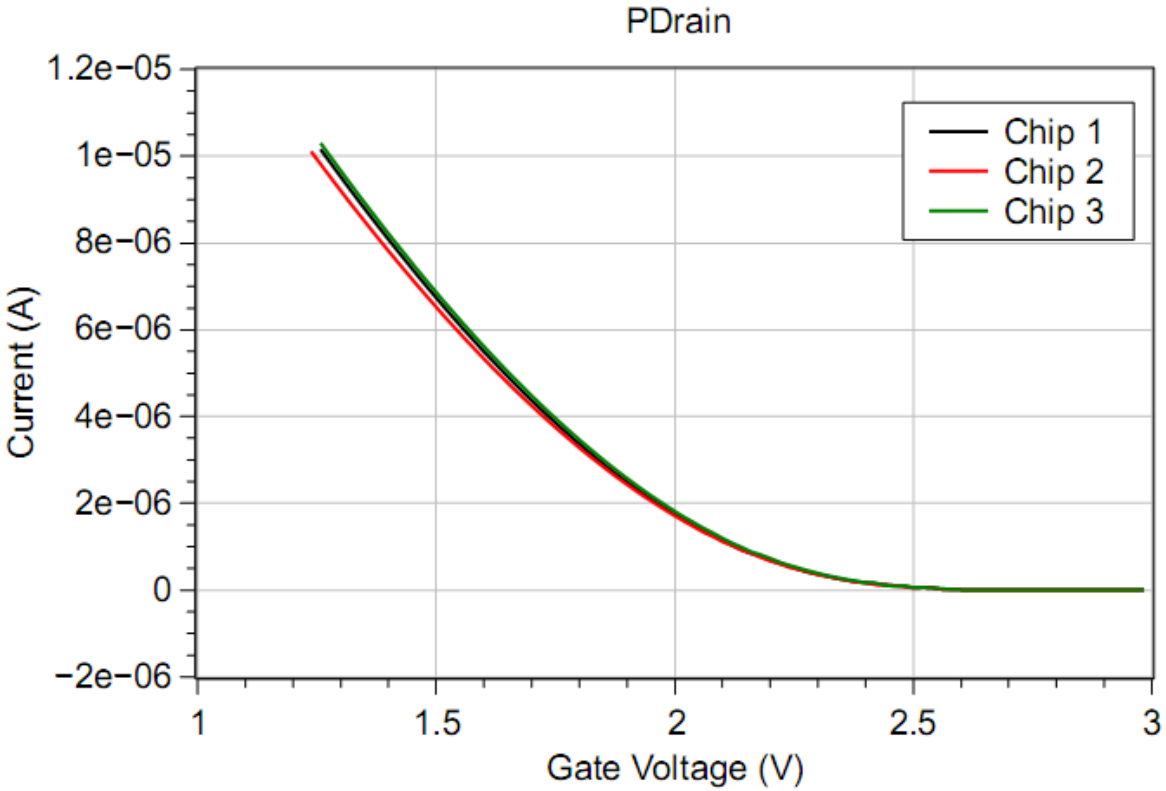
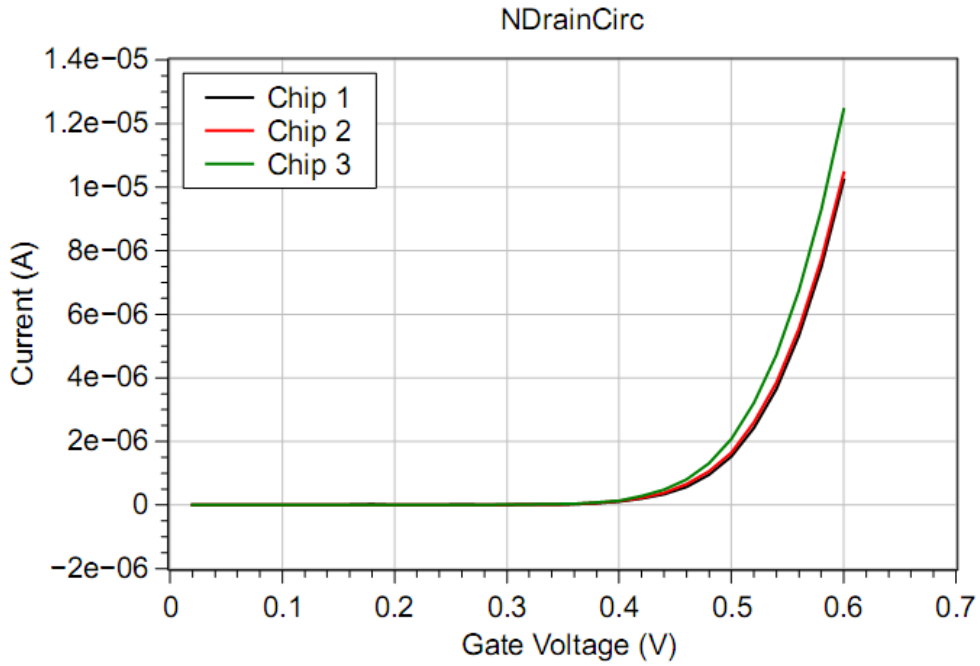
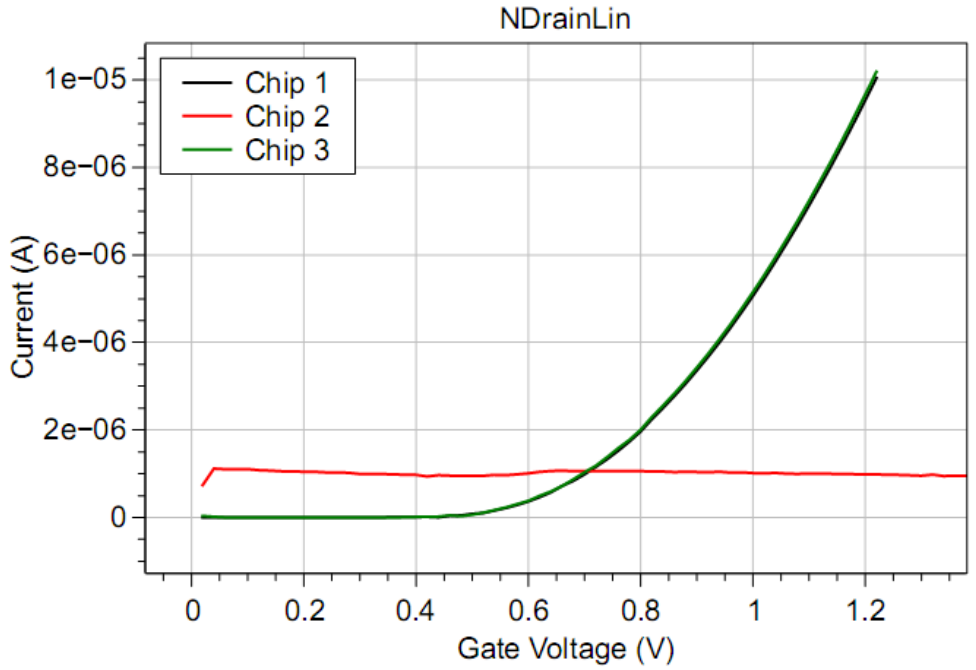
# Test structures: NMOS, PMOS



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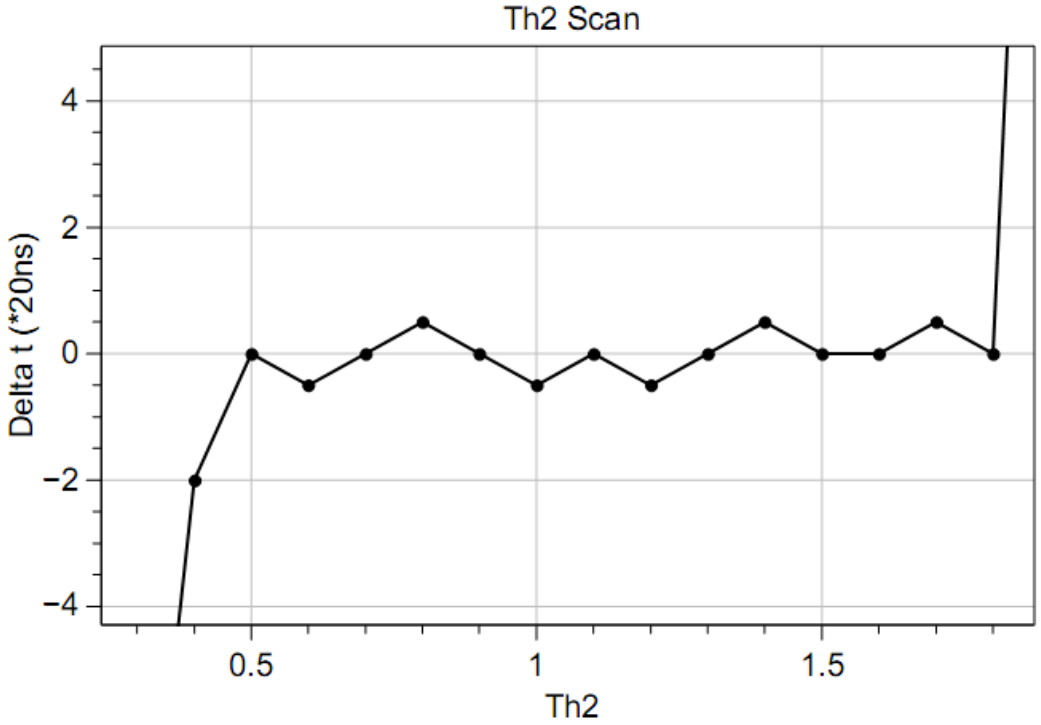
# Timewalk compensated comparator

- Compensate timewalk due to different amplitude
- Implemented time counter into FPGA
  - 50MHz, time resolution ~10ns
  - Count difference between injection and out




Difference between 0.5V and 1V injection

Chip Settings

| | |
|---|---|
| VN CNor | 20 |
| VN TW | 5 |
| ThRes | 10 |
| TWdown | 25 |
| BLRes | 10 |
| VNBiasR | 0 |
| VN FB | 5 |
| VPLdAmp | 10 |
| Tune1 | 0 |
| VNFS | 10 |
| Tune2 | 0 |
| TuneNor | 10 |
| VNAmp | 60 |
| VPAB | 35 |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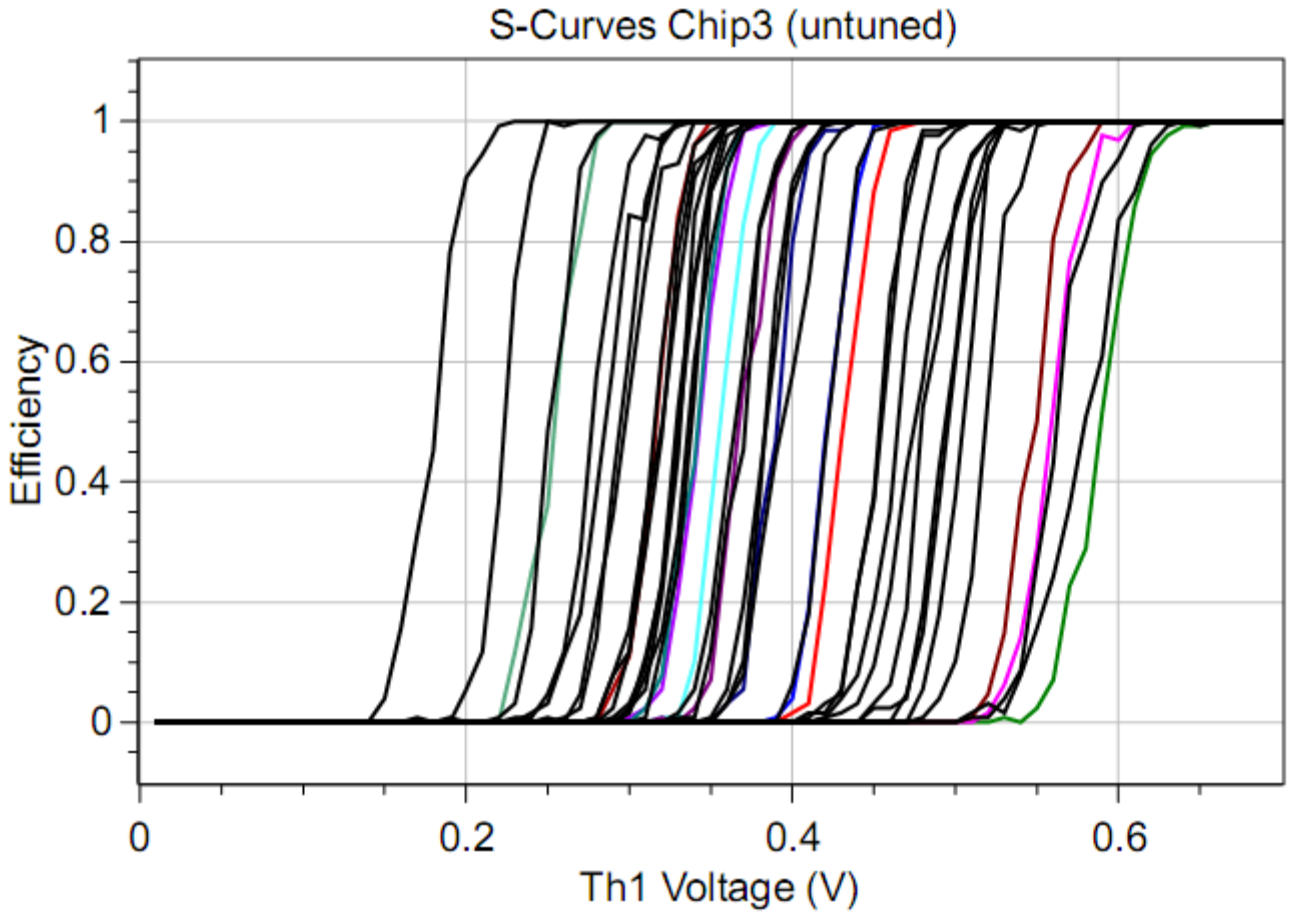
# Before irradiation




- Th1: 2.00V
- BL Voltage: ~1.98V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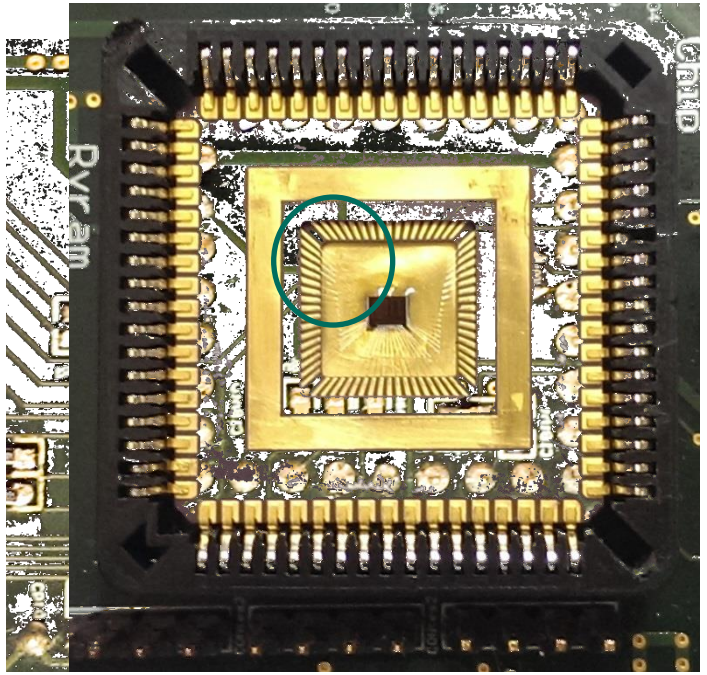
# X-Ray Irradiation

- X-Ray Setup @ KIT
  - 60kV X-Ray source, 20kGy/h (depending on spot size)
  - Calibrated to SiO2 dose
- Irradiated 1 Chip over last weekend
  - Bias applied
  - Chip fully powered
  - Hits found in hitbus during irradiation
- Small X-Ray spot
  - Missed the chip slightly – most probably not 600kGy (but rather 200kGy?)

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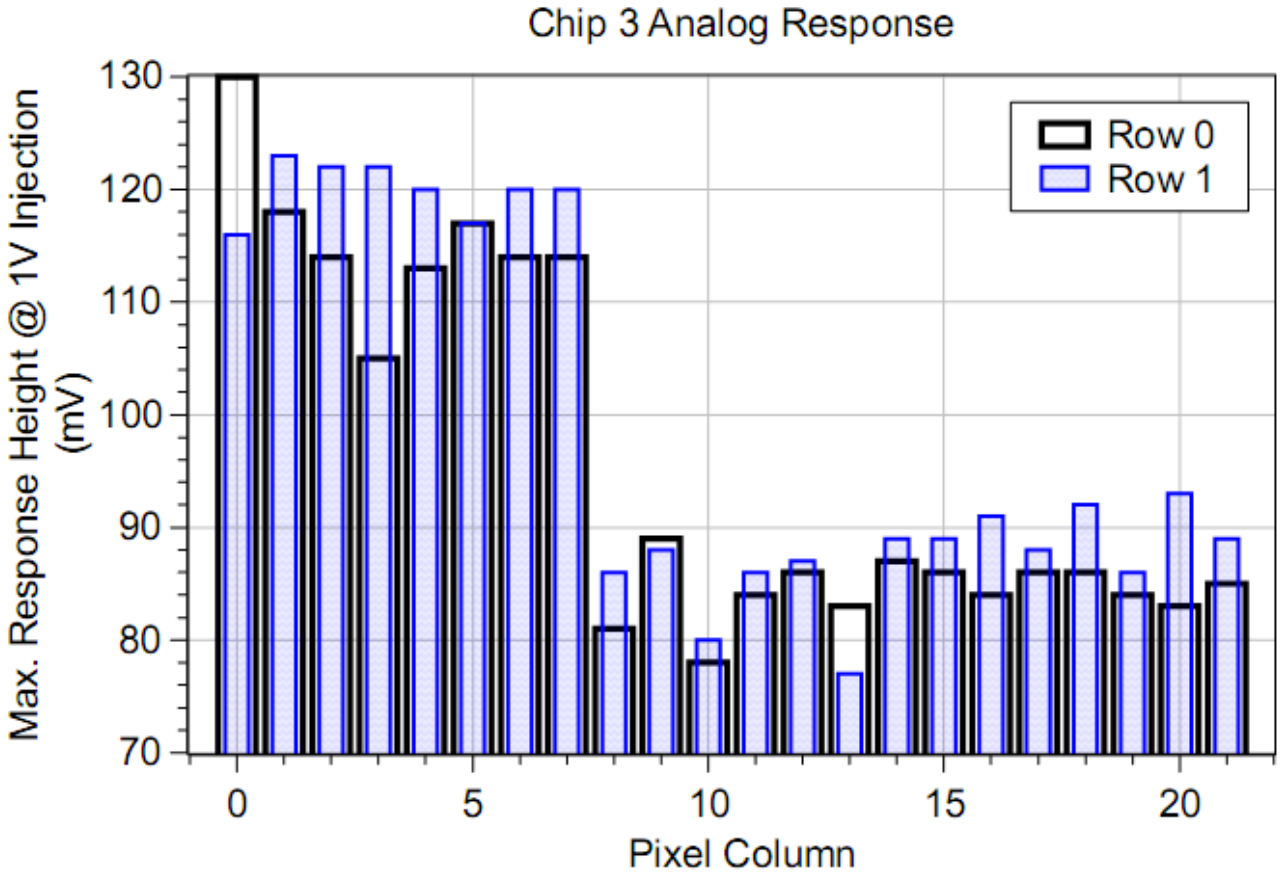
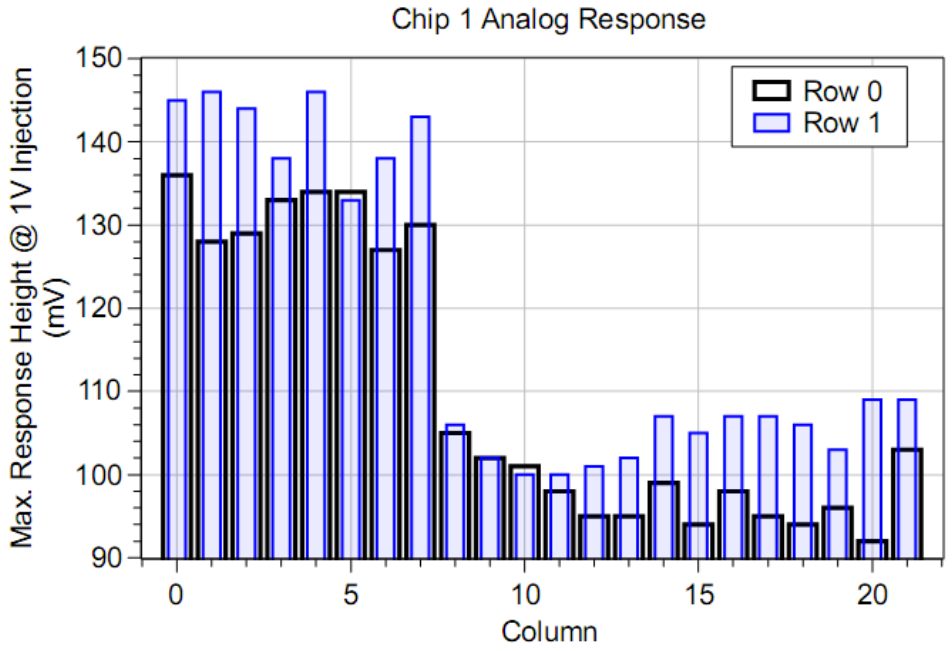
# After Irradiation




- Analog response about > 10mV smaller



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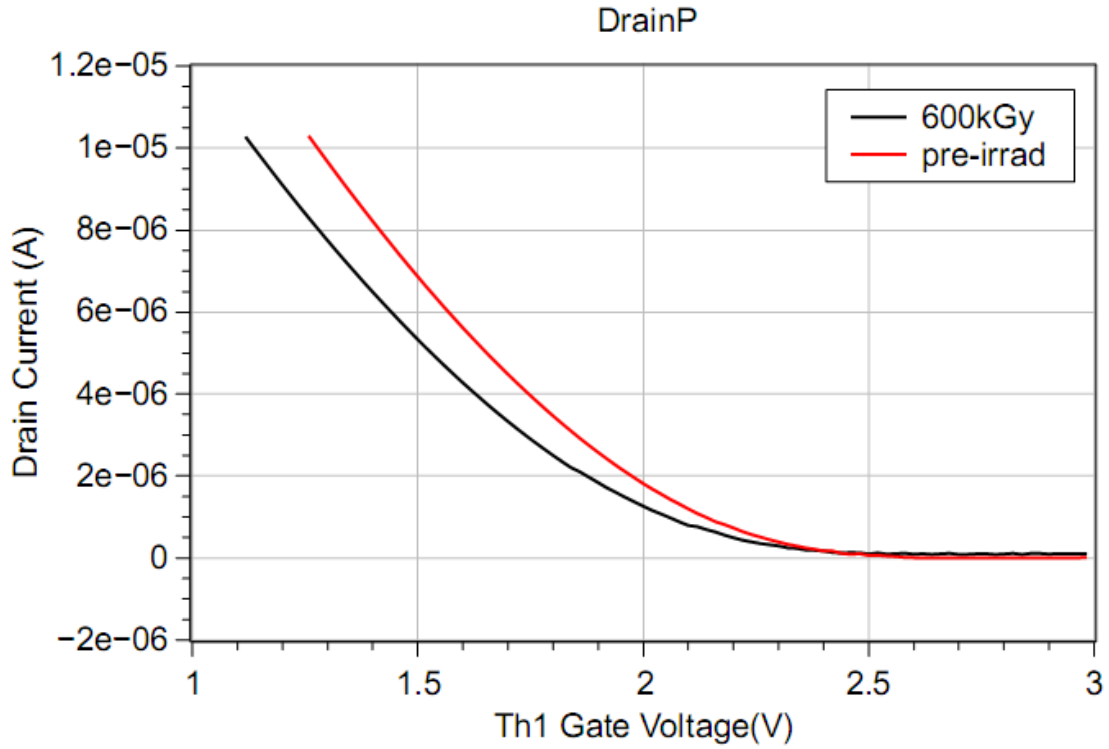
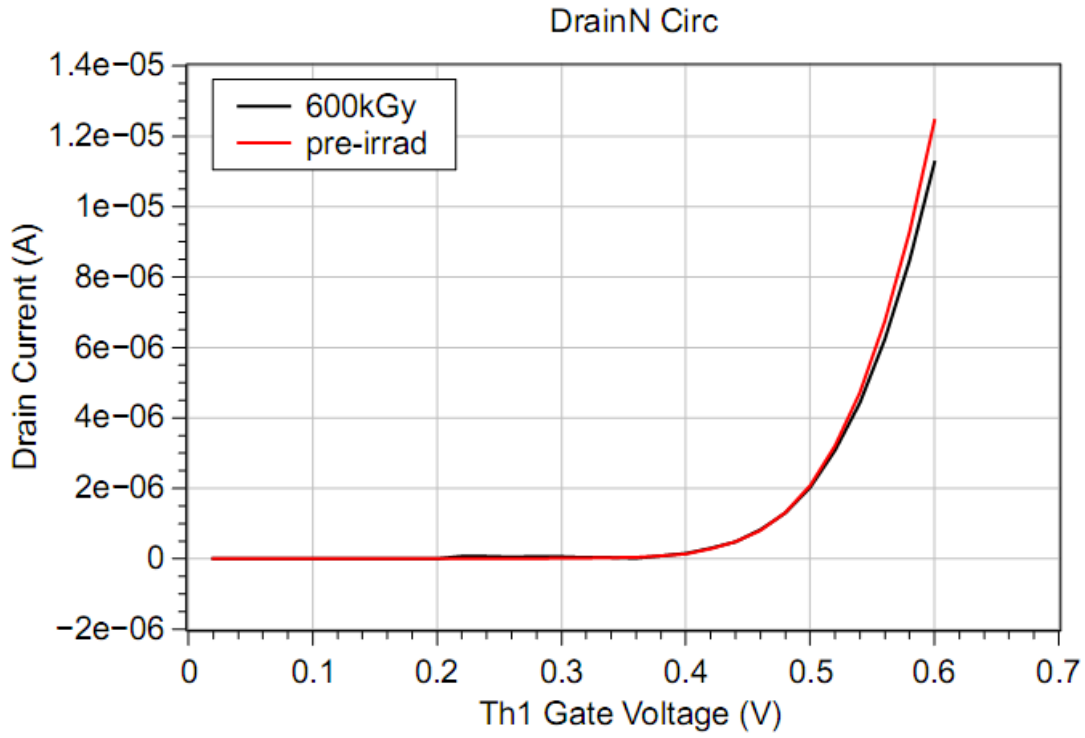
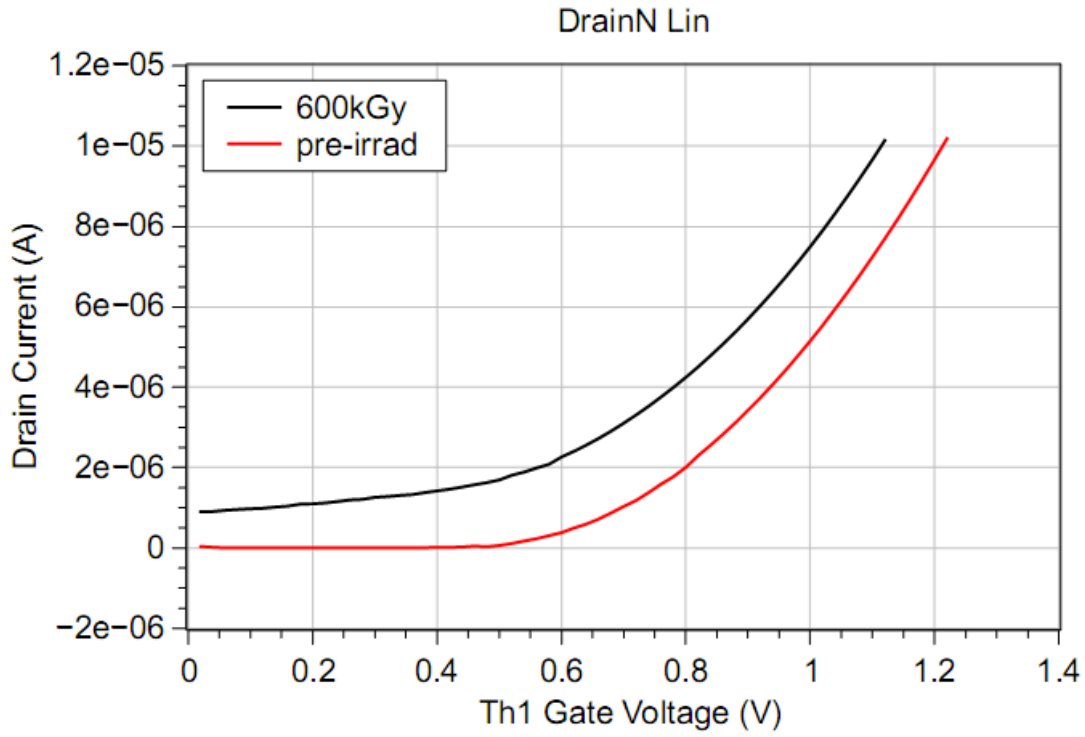
# Test Structure after Irradiatic

- Applied 3.3V to Gate (Th1) during irrad.
- Large change for NMOSlin



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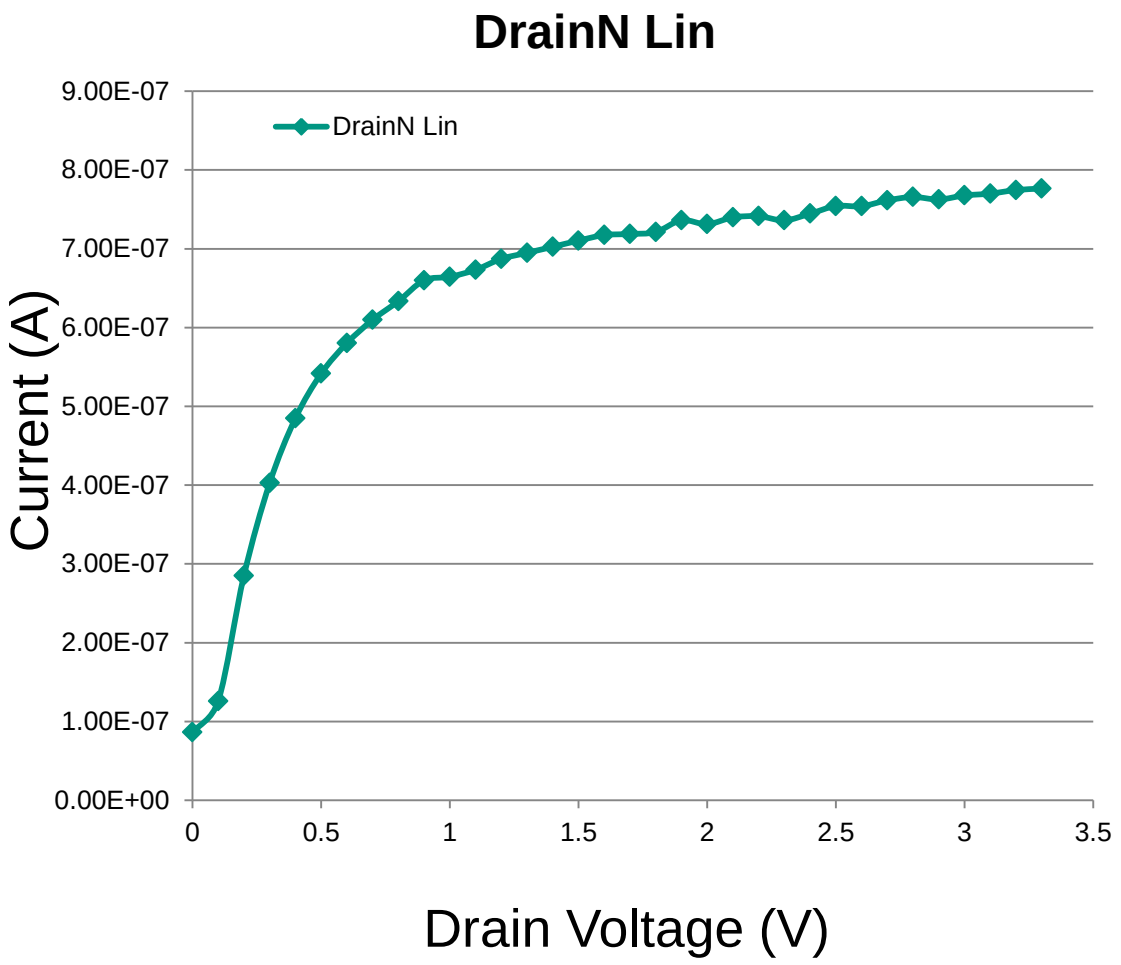
# Linear NMOS after irradiation




- Current of linear MOS
  - Gate (Th1) = 0V
  - Varying Drain Voltage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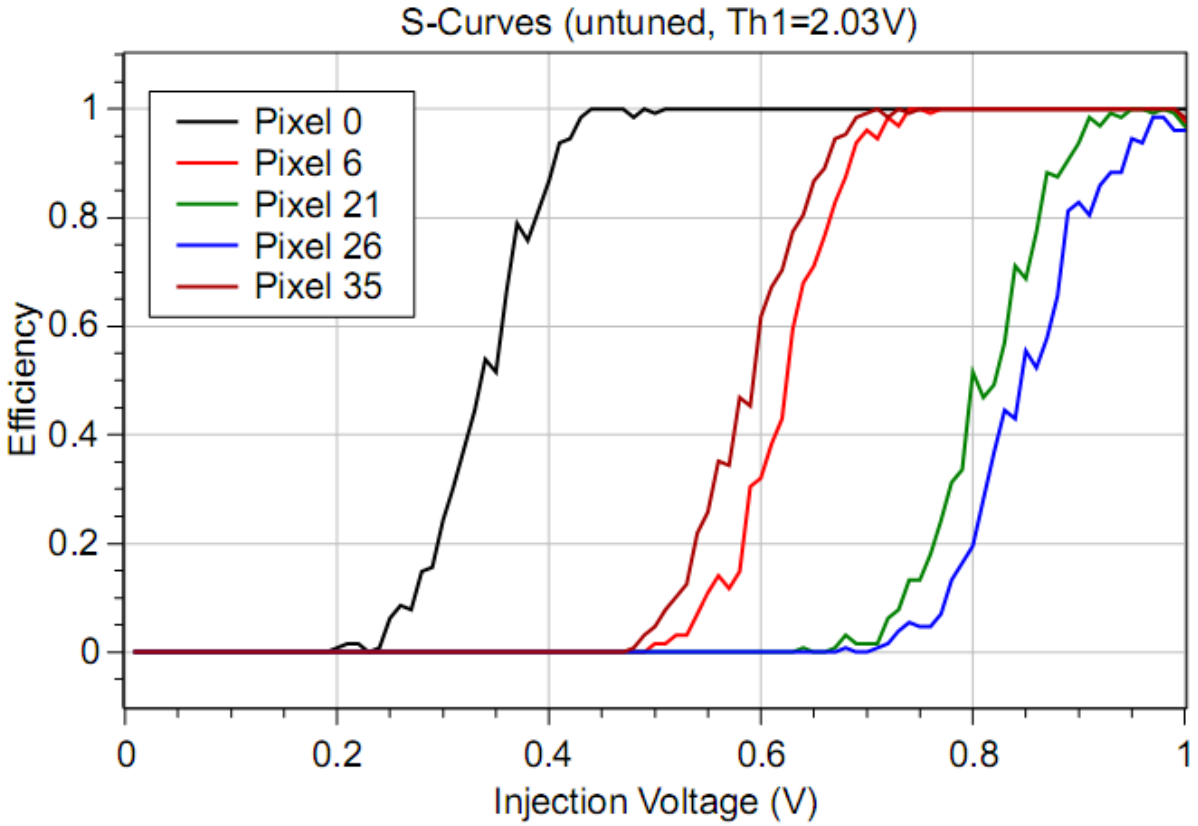
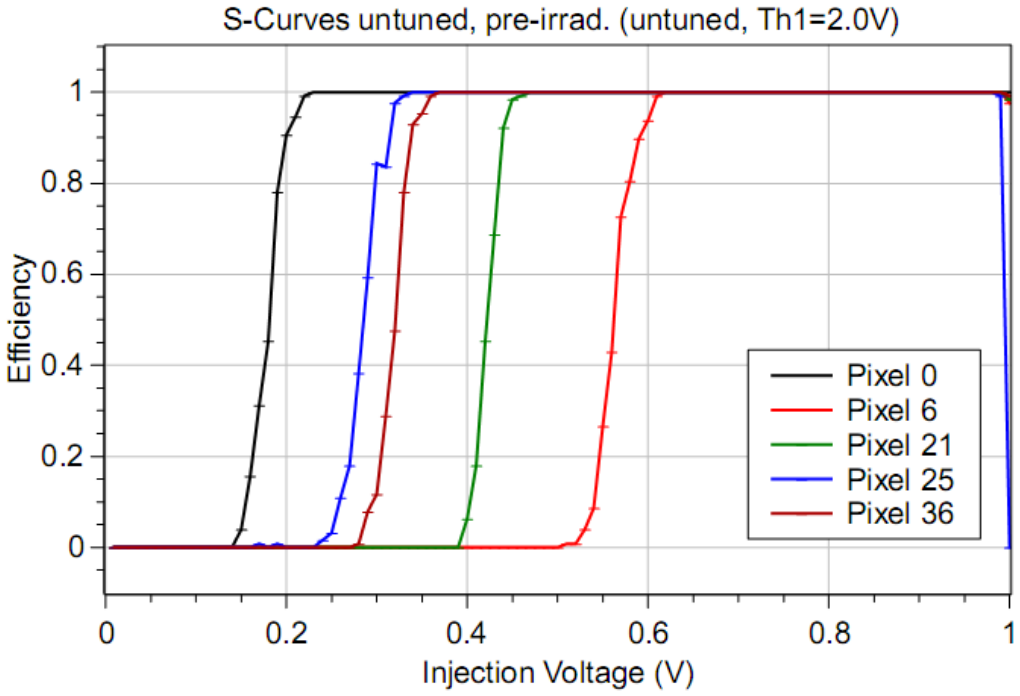
# S-Curves




- Th1: 2.03V
  - Going noisy if lower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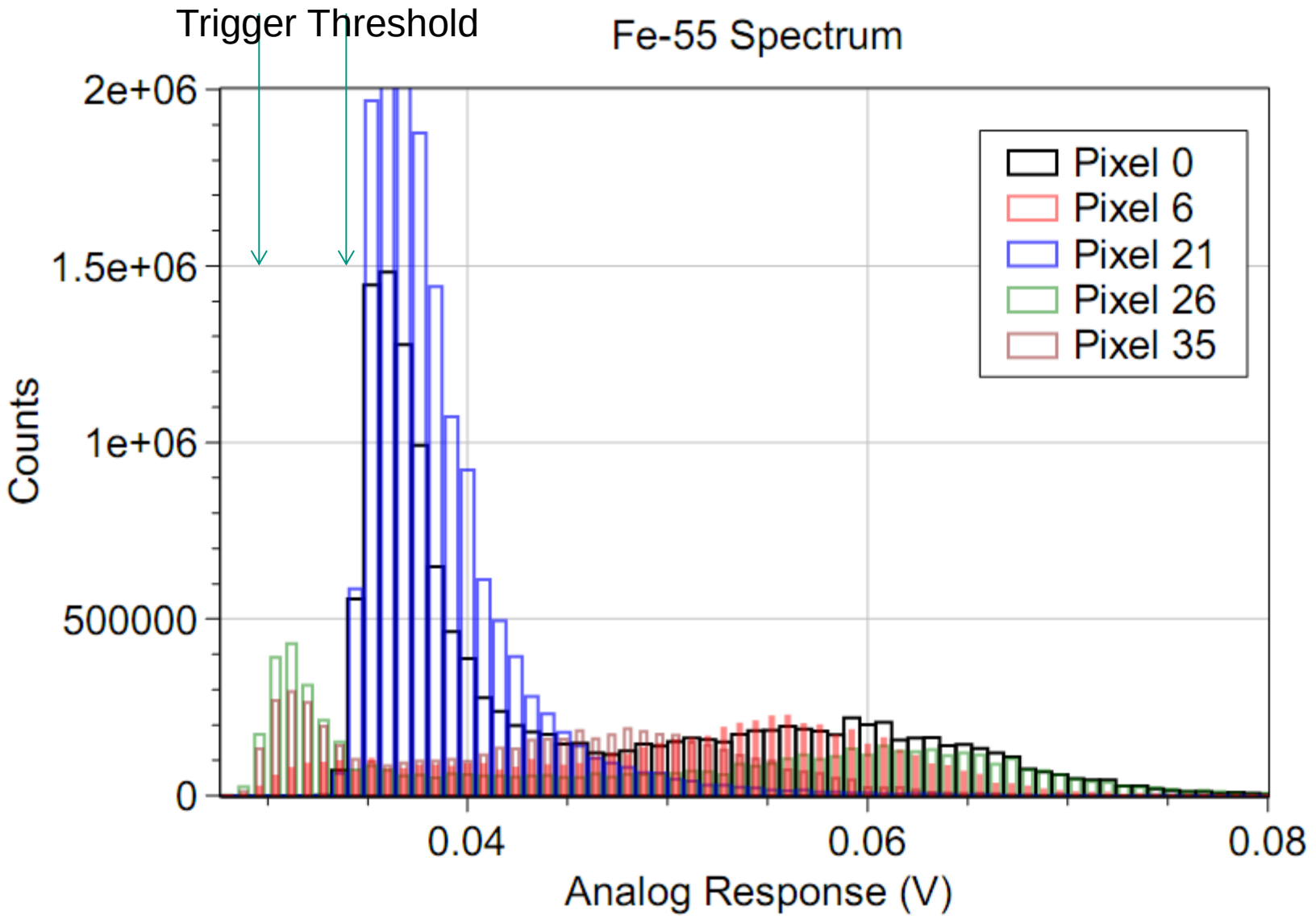
# Fe-55 Source Measurements

- Analog out
- Trigger threshold 30mV, 35mV
- Significant more noise belowe threshold
- Non-irrad. Threshold: 20mV





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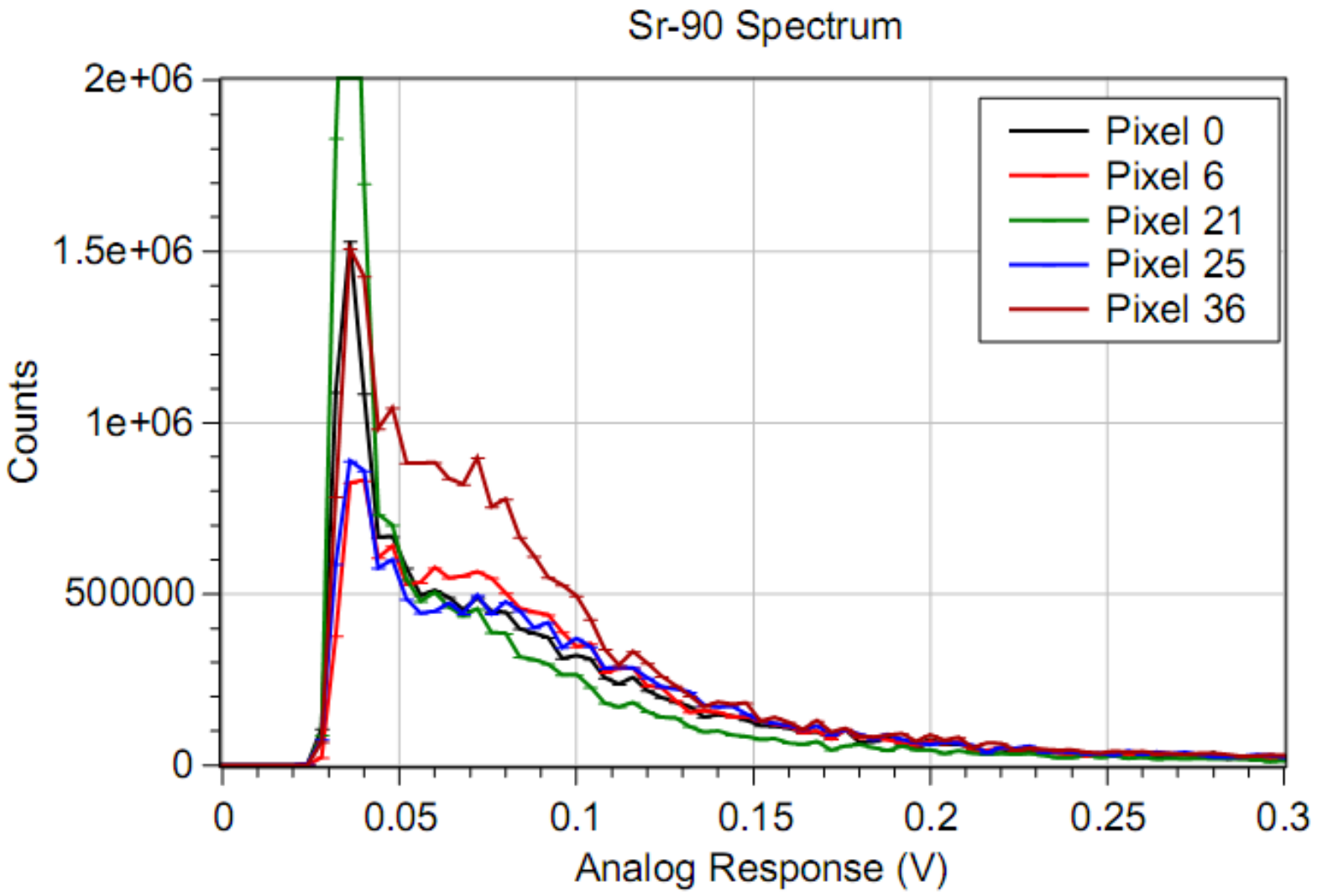
# Sr-90 Source Measurements



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# Plans

- Stepwise X-Ray irradiation
- Integration of digital readout


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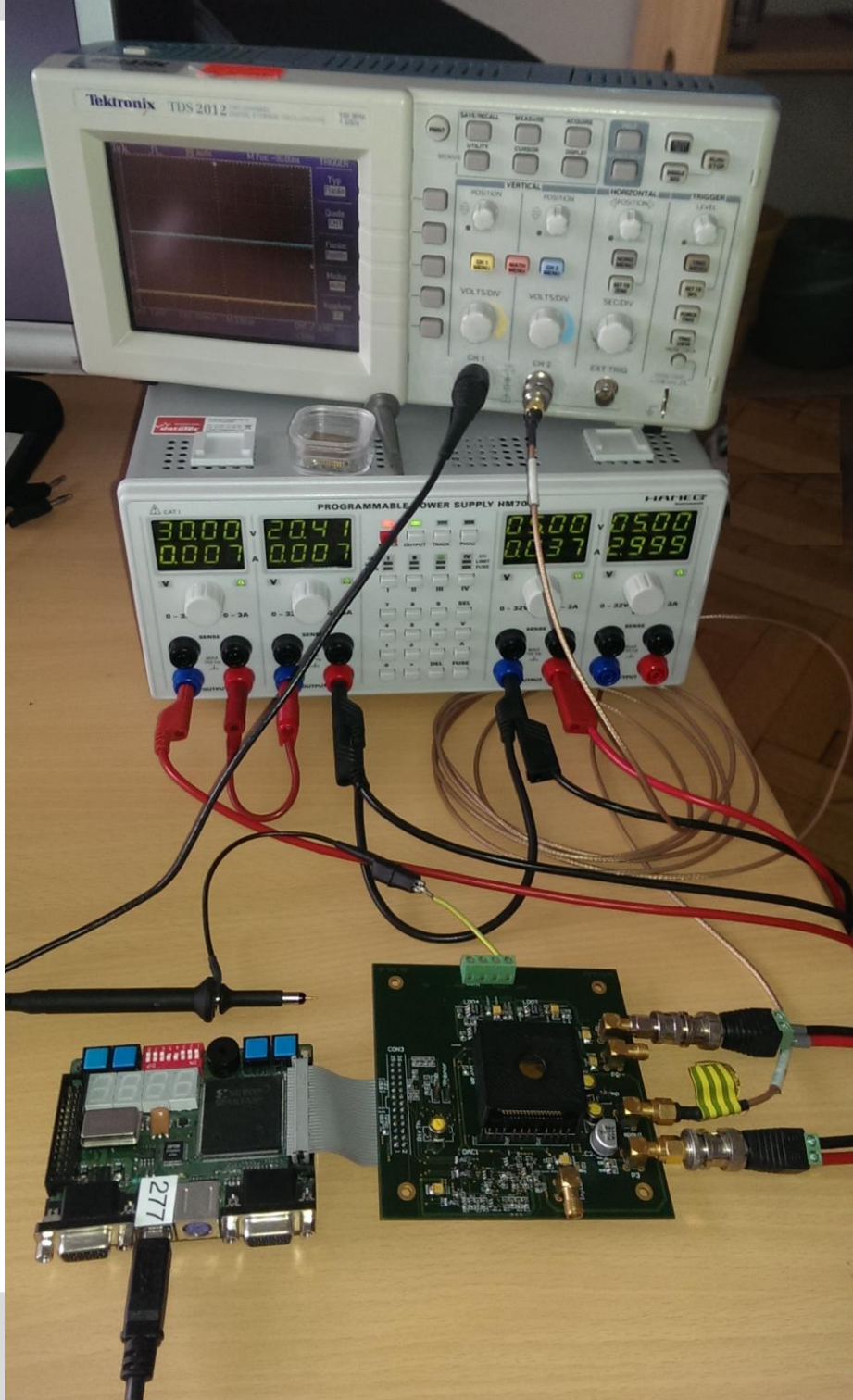
# BACKUP

# Overview of Components

- Uxibo (FPGA board, Spartan-II)
  - Readout framework provided by Ivan Peric
  - Simple wiring done for H35
- HV-Board
  - Complete assembly at KIT
- HVStripV1 Chip (HV-CMOS chip to be tested)
  - Some difficulties with bonding
  - 2 Chips available atm
- Voltage source (5V supply)
- HV source (~ – 60V bias voltage)
- Oscilloscope (TEK, up to 1GHz, 5GS/s available)
- Sr-90, Fe-55 sources available



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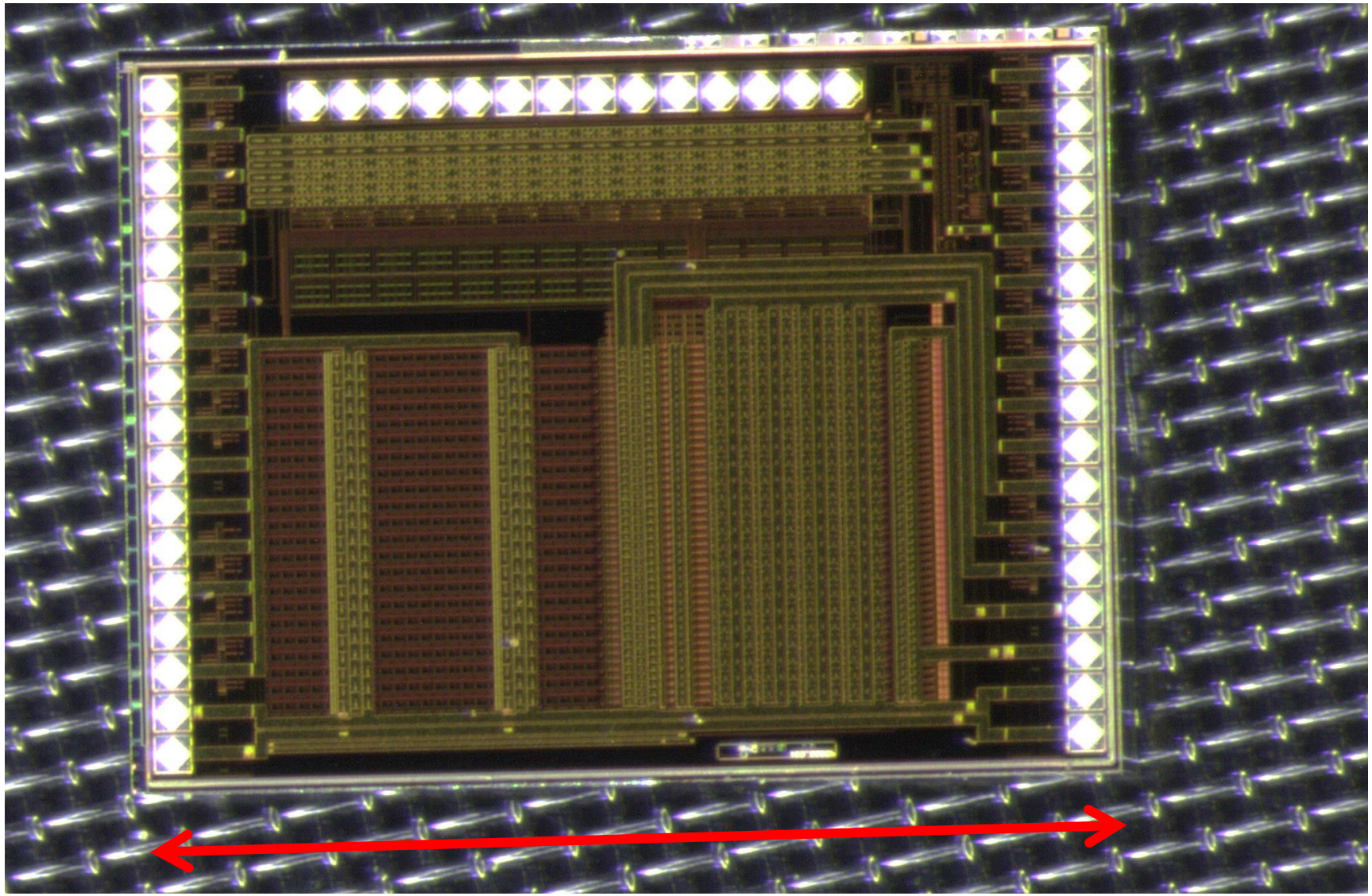
# H35 Chip under the microscope



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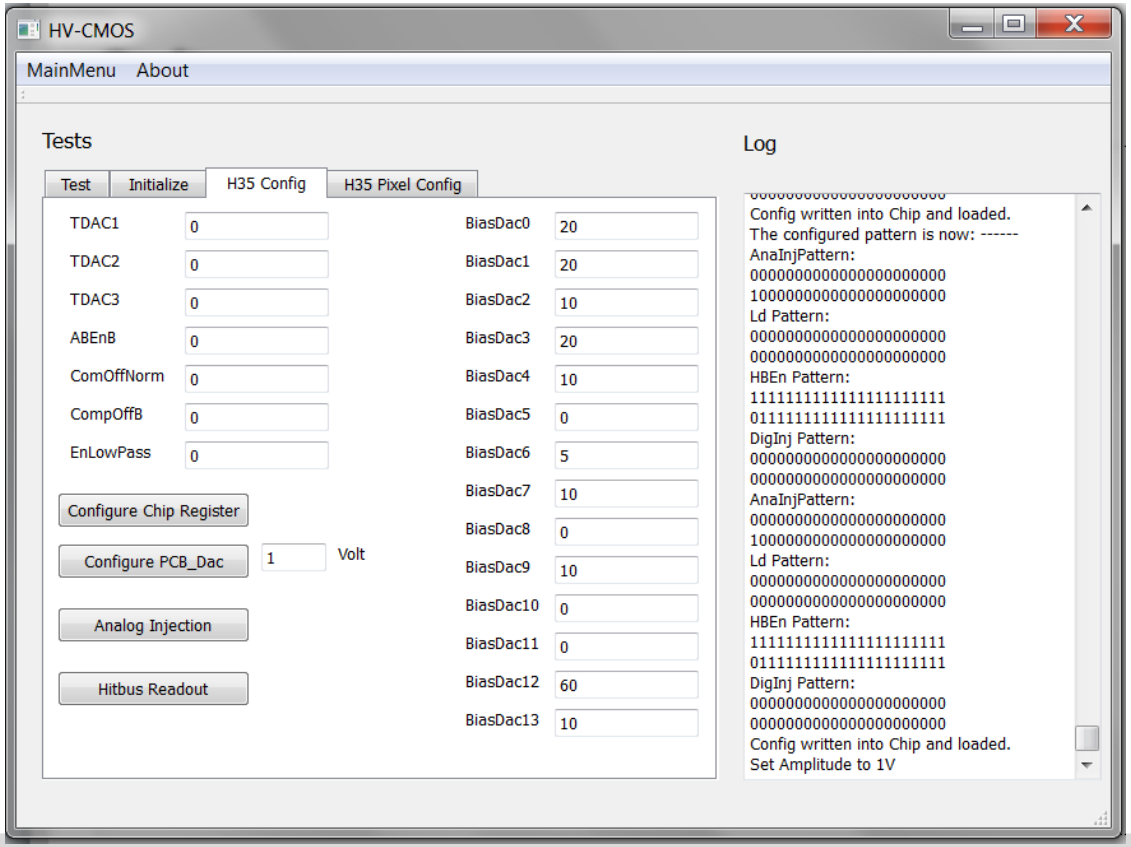
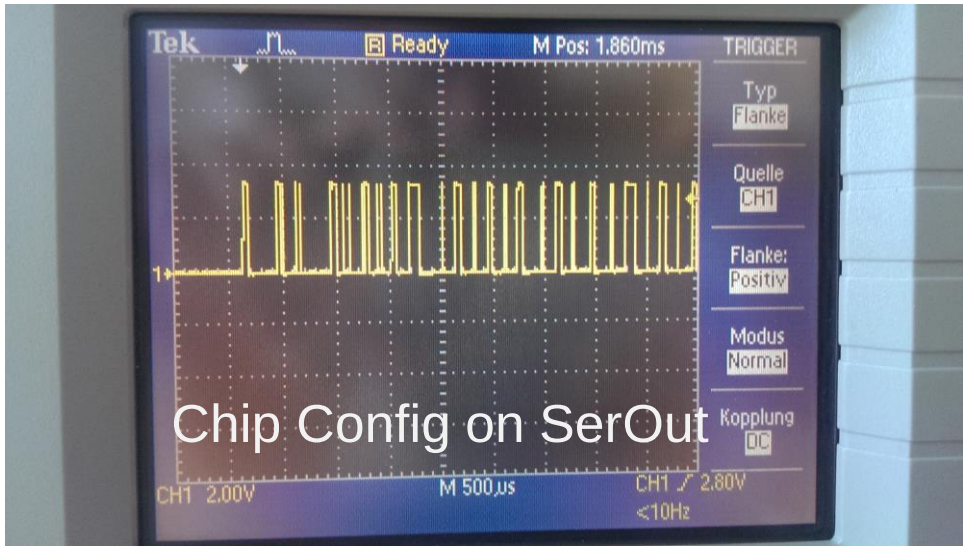
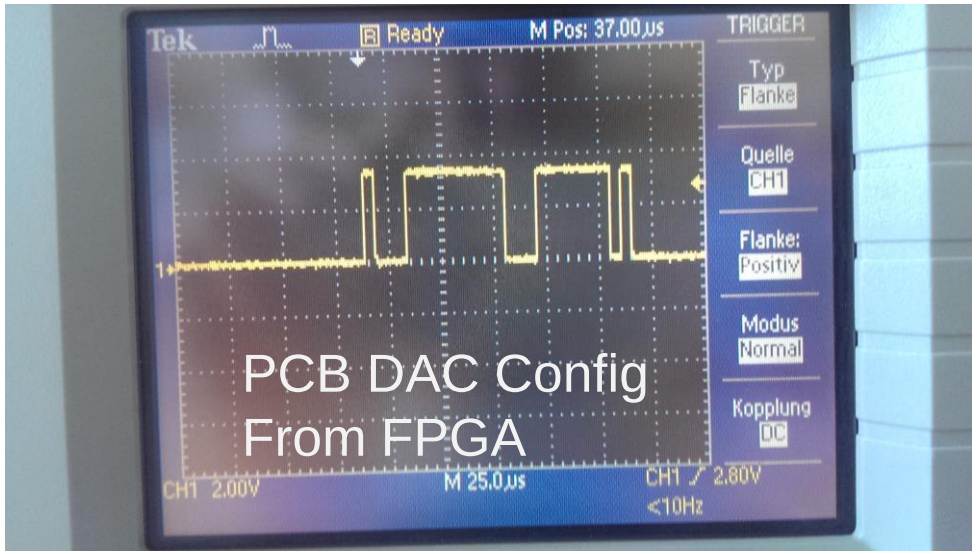
# Software

- Configuration to Chip working
  - Output visible on SerOut
- DACs on PCB configurable





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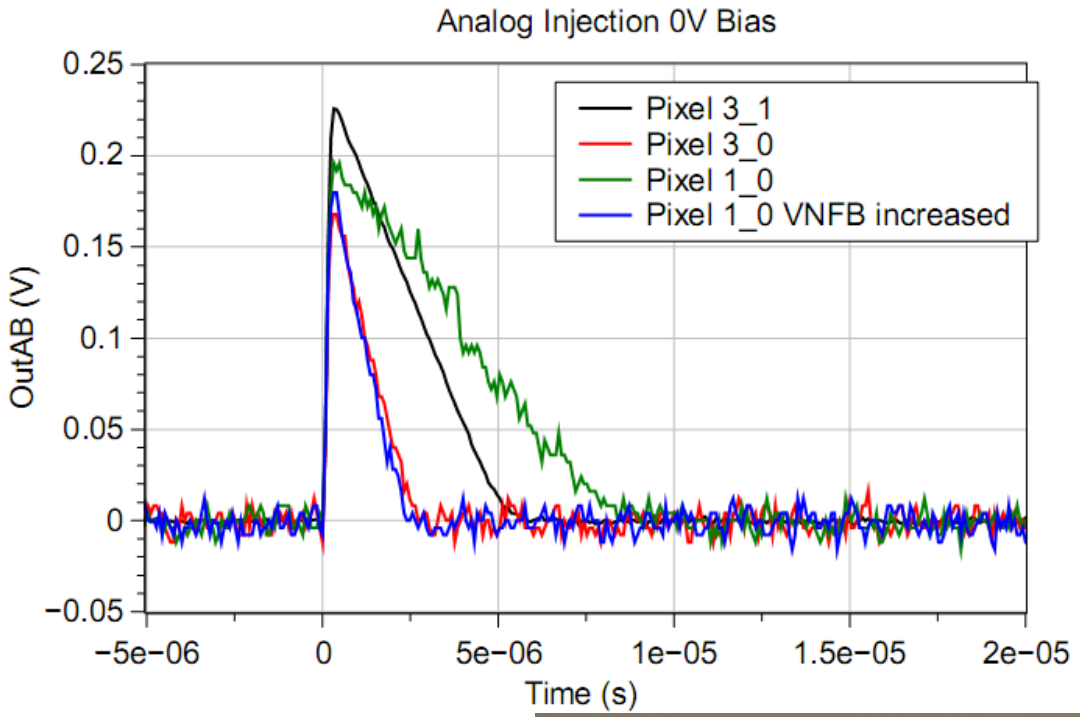
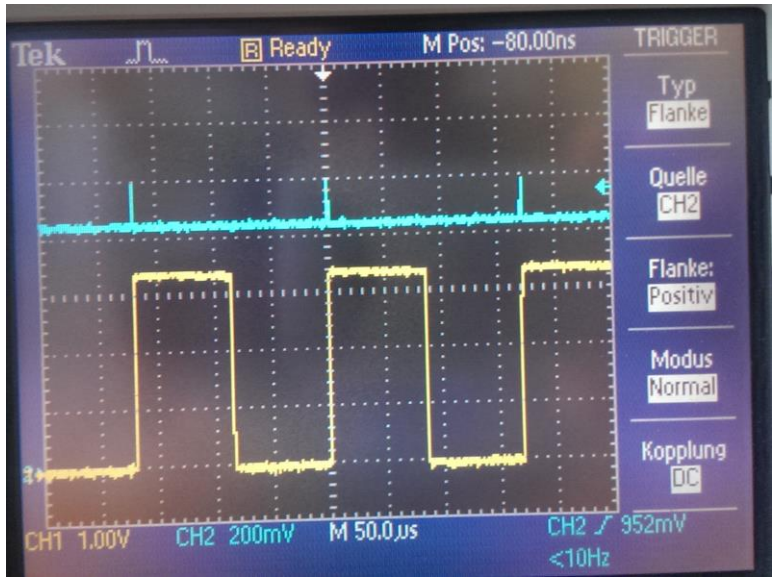
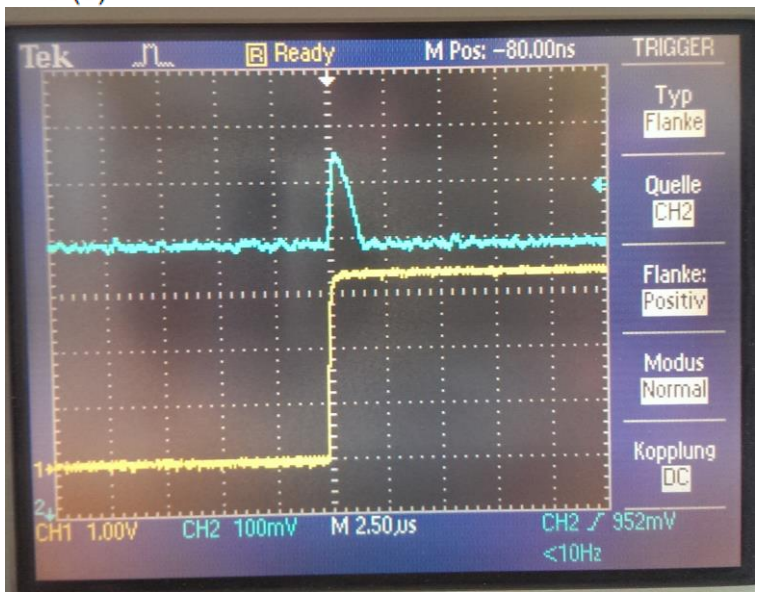
# Measurements

- Analog Injection into Pixels
  - Output on OutAB




Pattern



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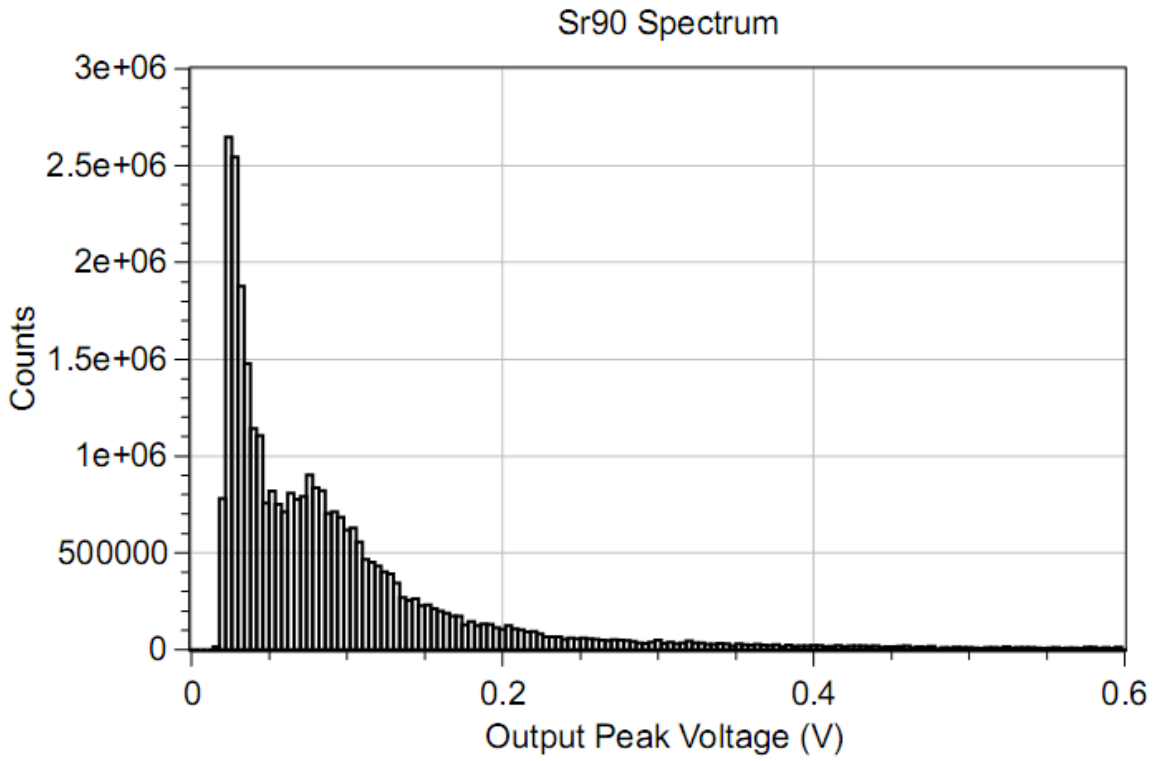
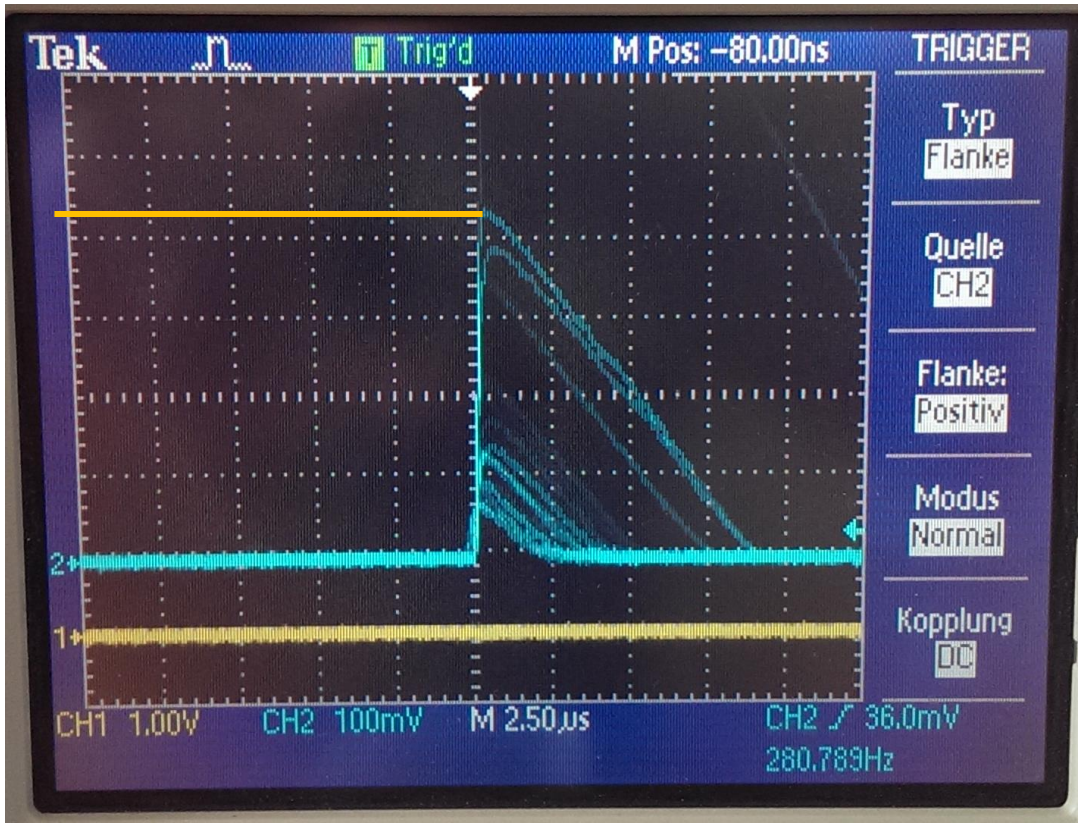
# Measurements

- Test with SR-90 source (MBq)



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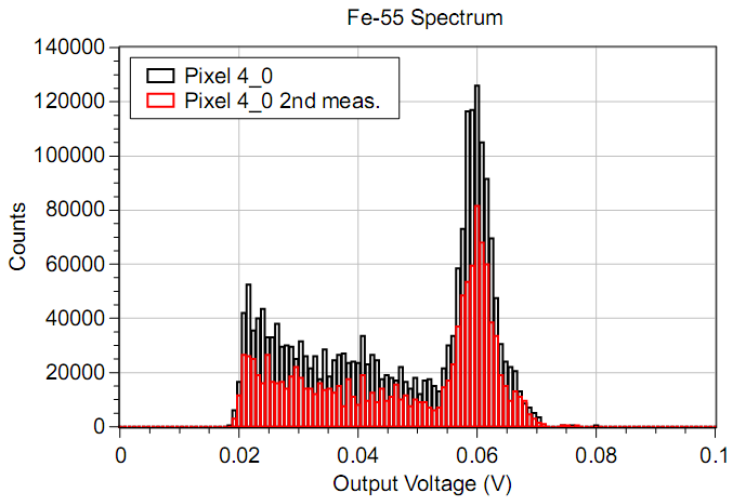
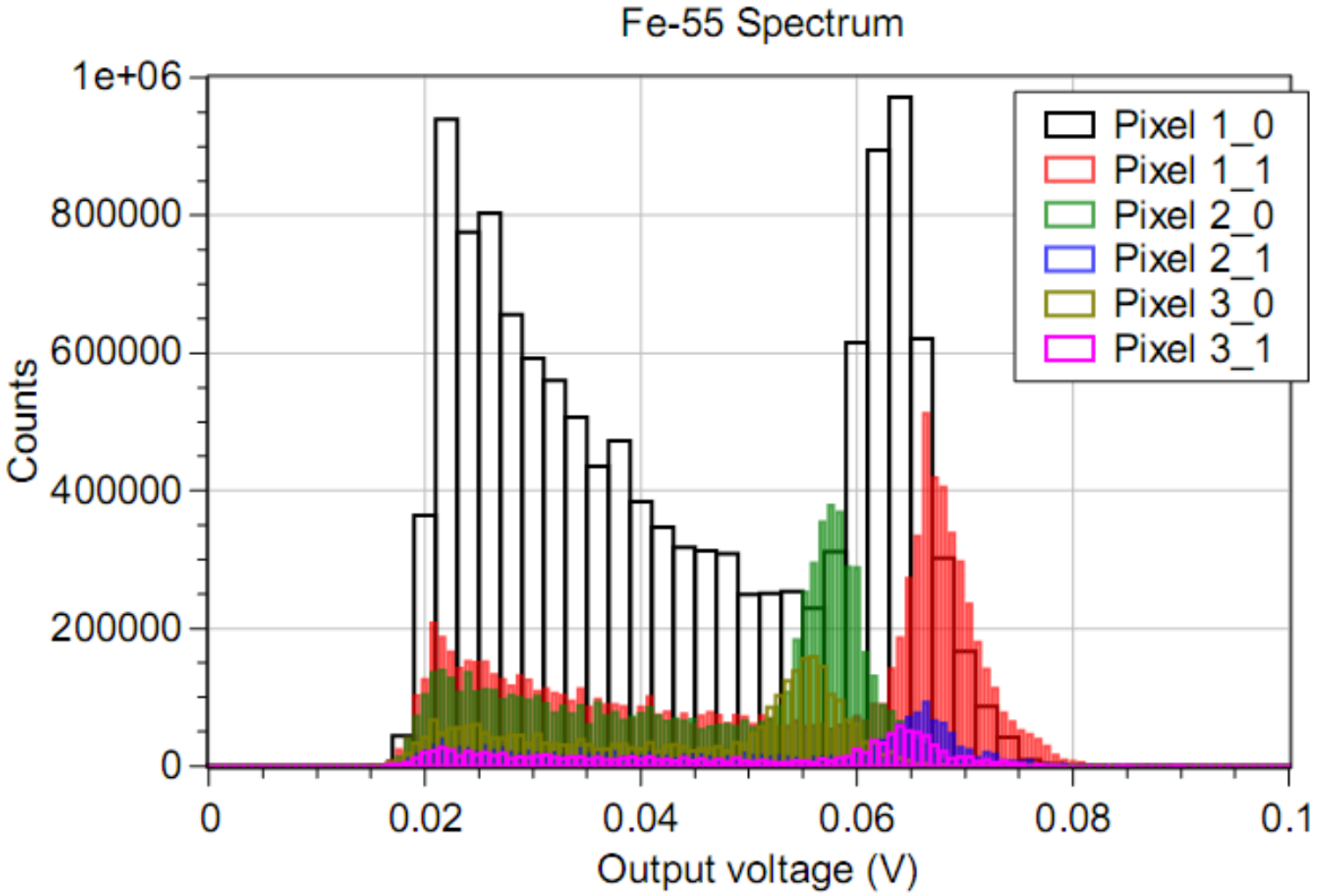
# Measurements

- Calibration with Fe-55 source
- Bias: - 60V
- Activity: ~8MBq





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# Plans

- Irradiation with X-Rays
  - X-Rays @ KIT: 60keV, 30mA, 10kGy/h
    - 60h for 600kGy (60MRad)

- Irradiation with 23MeV cyclotron protons
  - 1e15$n_{eq}$/$cm^2$ reasonable. Preferences?
  - Also a lot of ionizing dose (~1.5MGy)

- Digital readout of the chip
  - Few more steps in FPGA wiring and software configuration