JÜLICH
FORSCHUNGSZENTRUM

Report from the „Common Fund“: RTMs for the HGF-AMC (for PANDA)

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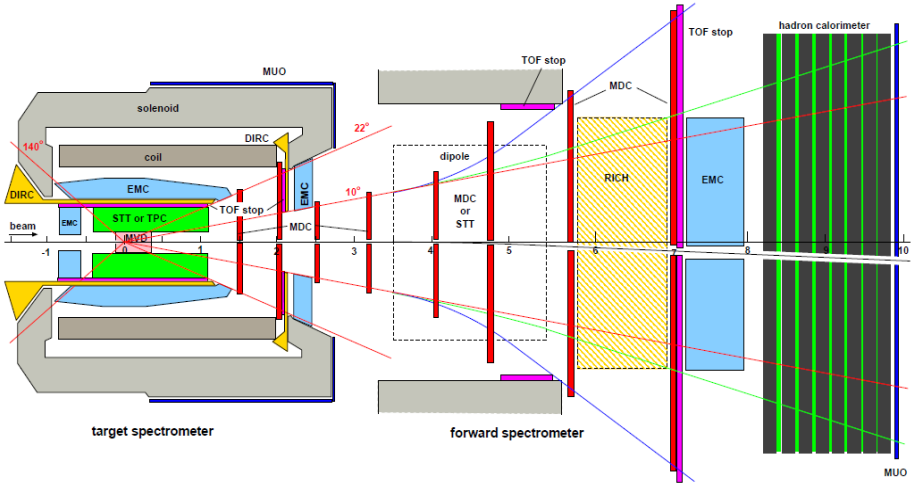
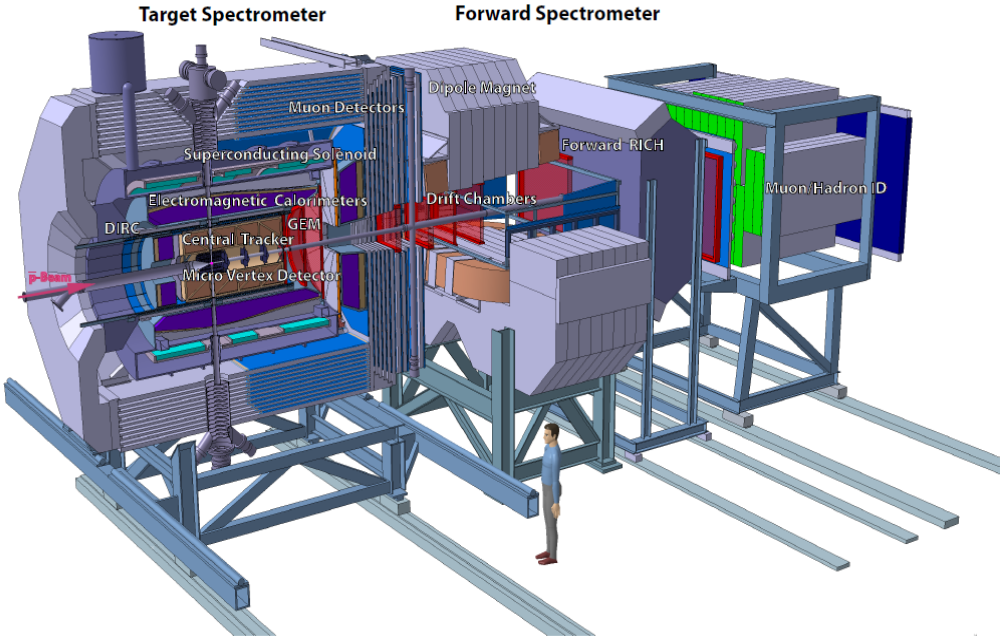
PANDA (AntiProton Annihilations at Darmstadt)

- Detector system (with palled target) planned at HESR (High Energy Storage Ring) of future FAIR (Facility for Antiproton and Ion Research) complex in Darmstadt
- Multipurpose fixed target experiment

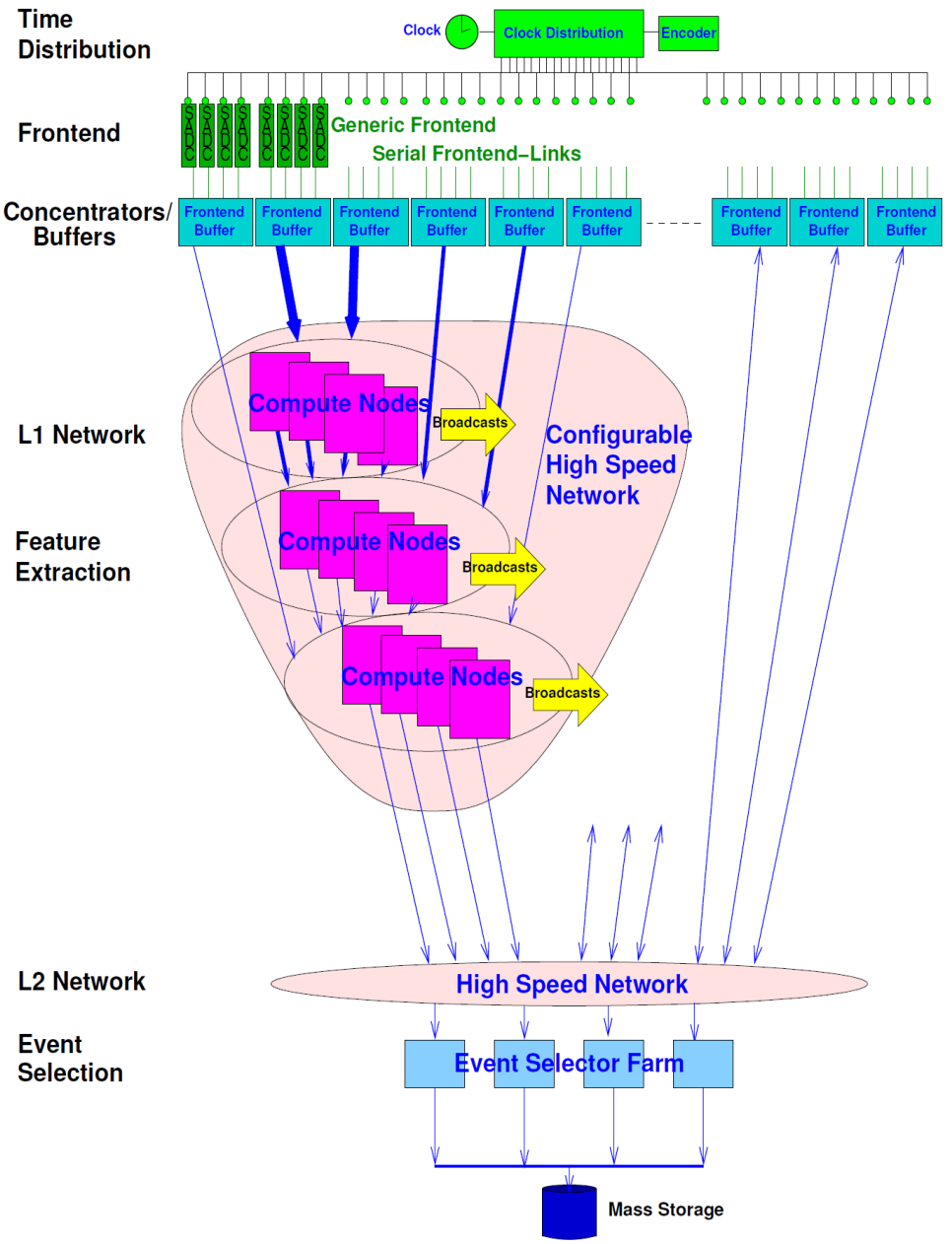




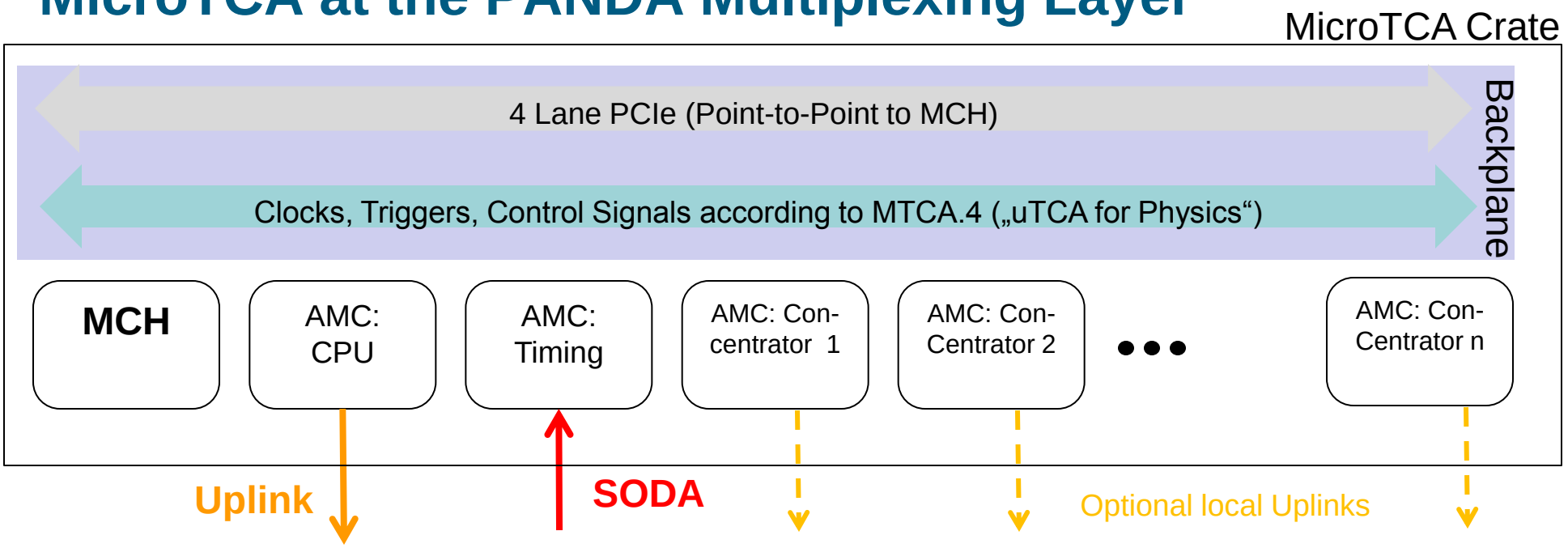
Figures: PANDA TPR

PANDA DAQ

- No hardware trigger
- Free-running system
- L1 trigger: feature extraction on Compute Nodes (ATCA)
- L2 trigger: event selection on PC-farm
- SODA: time distribution and synchronization

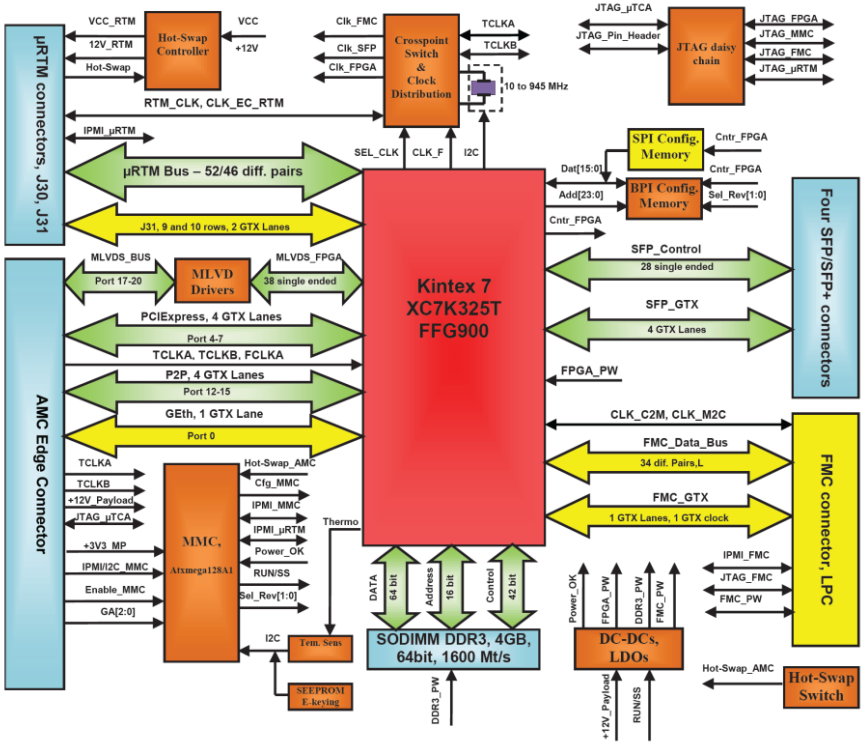


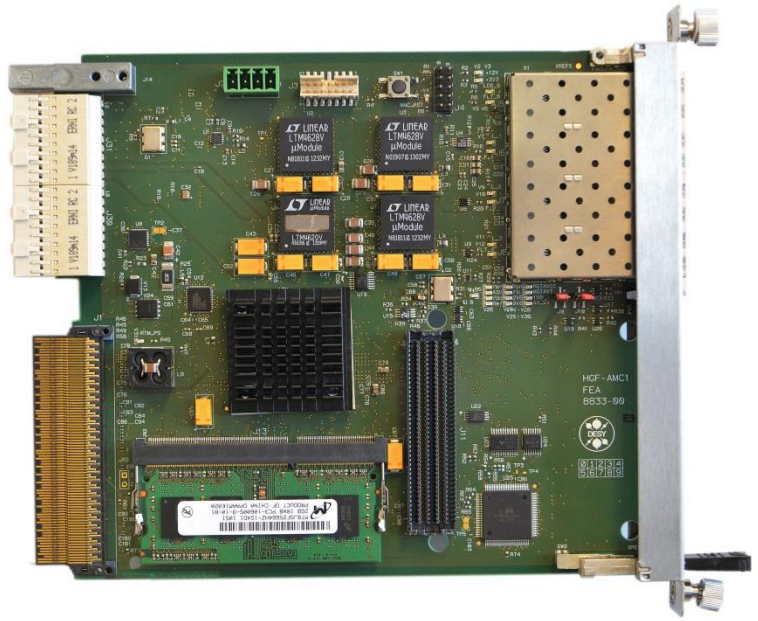
MicroTCA at the PANDA Multiplexing Layer



- Central input for SODA, local distribution on backplane
- Local uplinks on concentrator AMCs for high data rate subsystems
- For intermediate test systems: use digitizer AMCs
- CPU for management + control system + uplink for low data rate subsystems

HGF-AMC: A versatile, powerful module

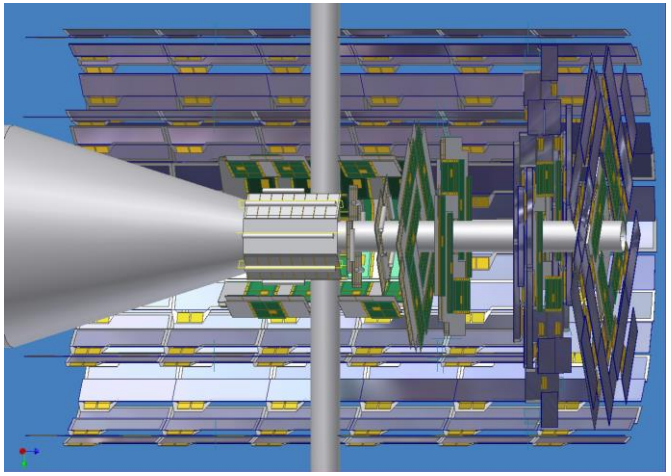




HGF-AMC (DESY/KIT)

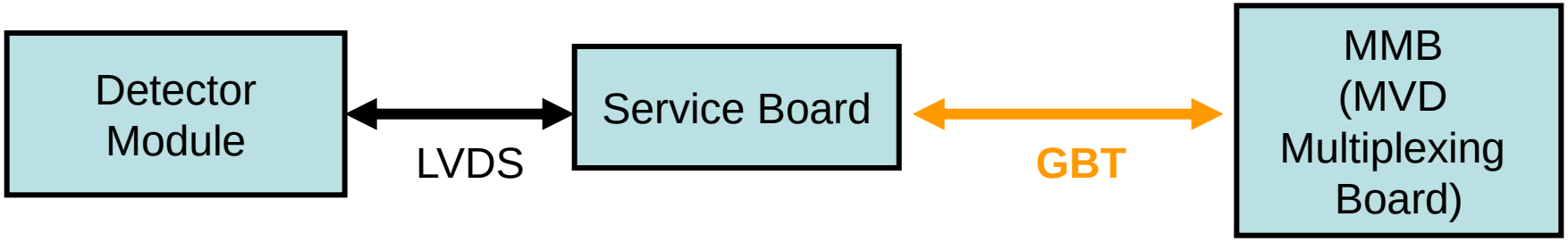
- MicroTCA.4 board developed in HGF Portfolio “Detector Technologies”
- Based on Kintex 7 (4 GTX lanes to Front Panel)
- Flexible Extension by FMCs and RTMs possible
- **Directly usable as concentrator AMC in PANDA!!**

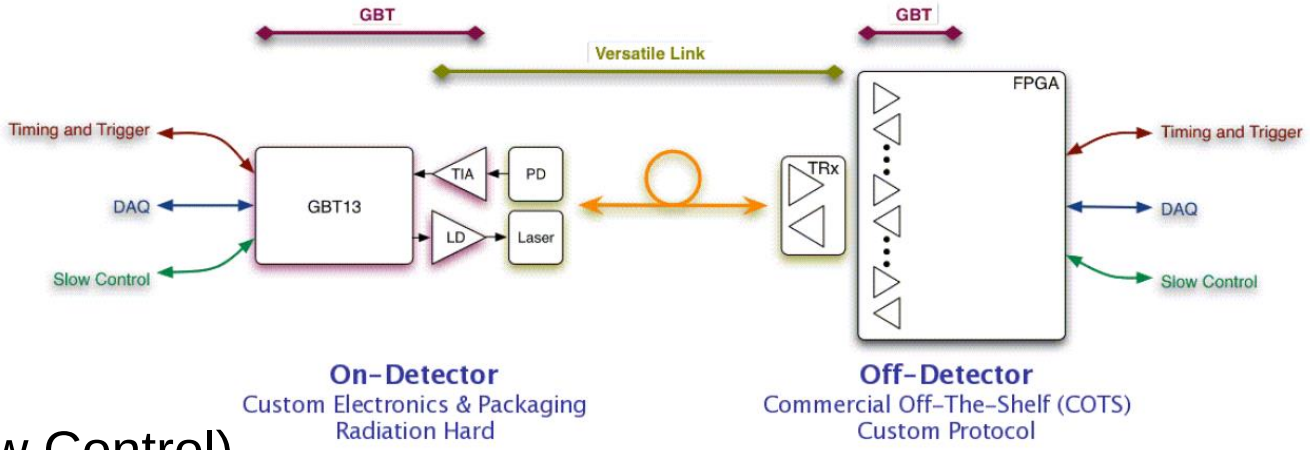
Project 1: PANDA Micro Vertex Detector



- Innermost detector closest to interaction point
- Good spatial and time resolution + energy loss measurement for particle identification
- 4 barrels and 6 disks with Silicon pixel detectors and Silicon strip detectors
- Silicon pixel readout ASIC TOPIX developed by INFN Torino
- Ca. 500 TOPIX ASICs
- Service Board: optical transceiver for link to Compute Node
- Radiation-hard => CERN GBT chipset

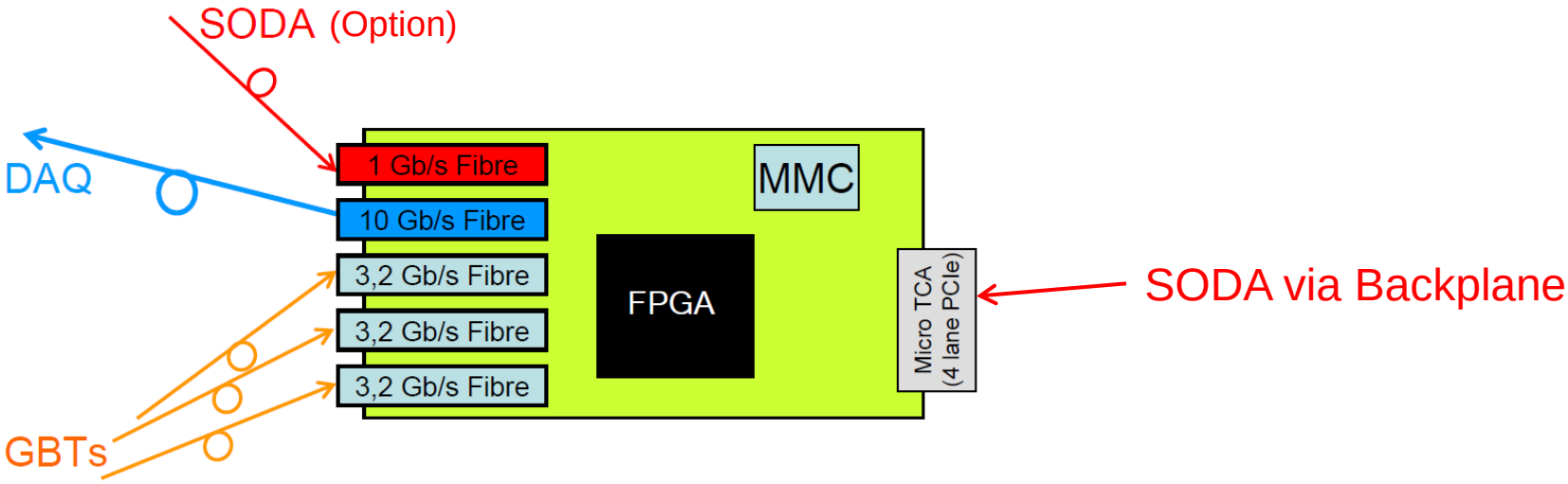
PANDA MVD Readout





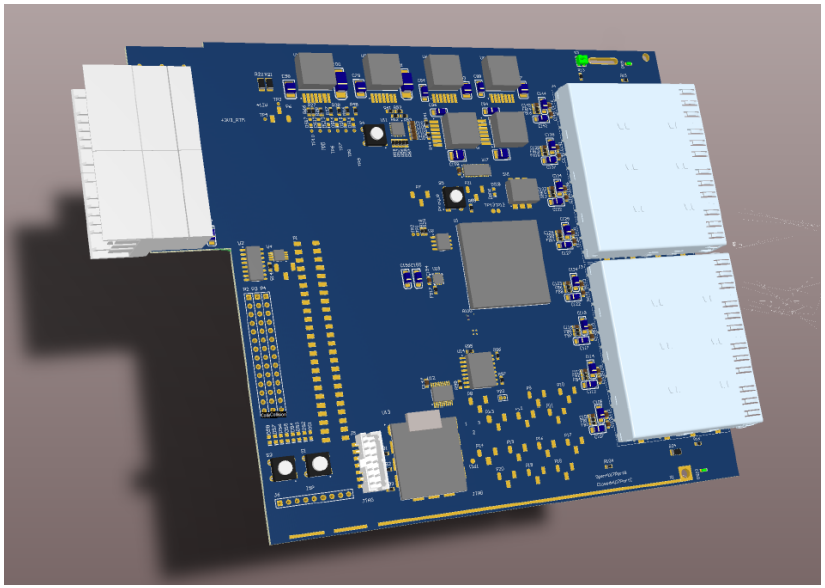
- GBT:
  - Serial optical link
  - 3.36 Gb/s (incl. Slow Control)
  - Line Rate 4.8 Gb/s (Reed-Solomon Encoding)
  - Under development at CERN (Set of 4 ASICs)
  - Implementation of GBT protocol on FPGAs: reference implementation of CERN

PANDA MVD Multiplexing Board (MMB)



- FPGA implementation tasks:
  - GBT protocol
  - Uplink protocol
  - Mapping between both
  - SODA
  - PCIe (for control and montioring tasks)
- HGF-AMC is directly usable for the implementation of the MMB!

Rear IO Module for the HGF-AMC

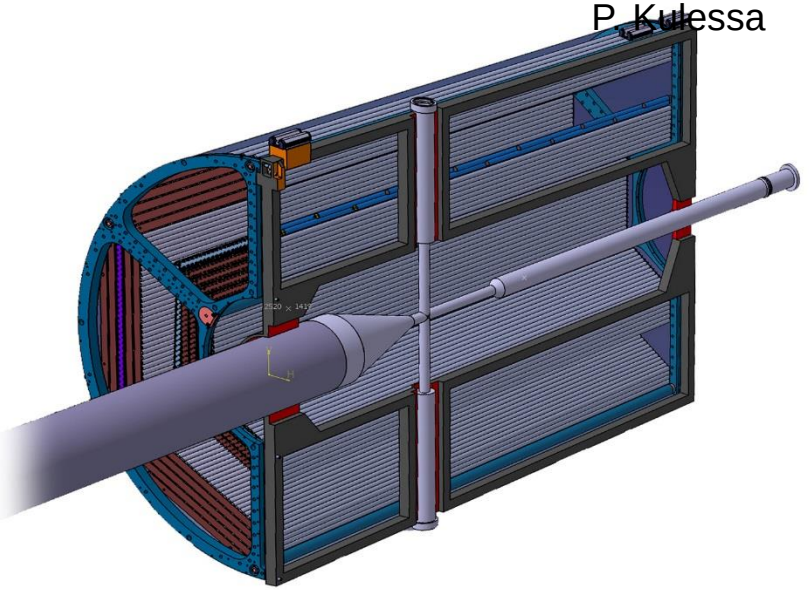


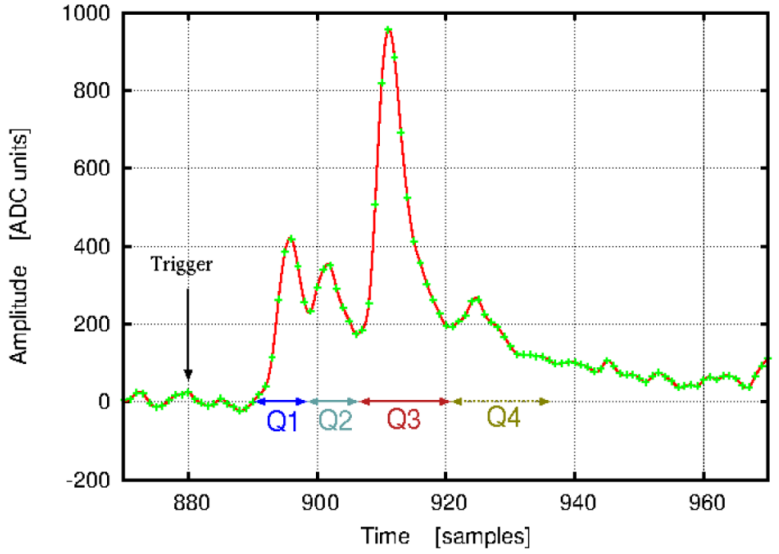
- Increase of multiplexing level
- 8 GTP Transceivers
- Based on Artix7 (XC7A200T) for the mapping to the parallel interface to the HGF-AMC
- Status: Layout finished, must be checked before production
- Common Fund Project: Promotes the HGF-AMC and proves its applicability

Project 2: PANDA Straw Tube Tracker

P. Kulessa

- Central Tracking Detector of PANDA
- Layer around MVD
- Composed out 4636 drift tubes (“Straws”)
- Tracks: Measurement of drift time
- Particle Identification: Measurement of Energy loss => charge measurement
- Cluster Structure of Straw Pulses
  - Sampling ADCs
  - Feature extraction in FPGAs
  - Tests based on old WASA electronics





HGF AMC for the implementation of prototype systems

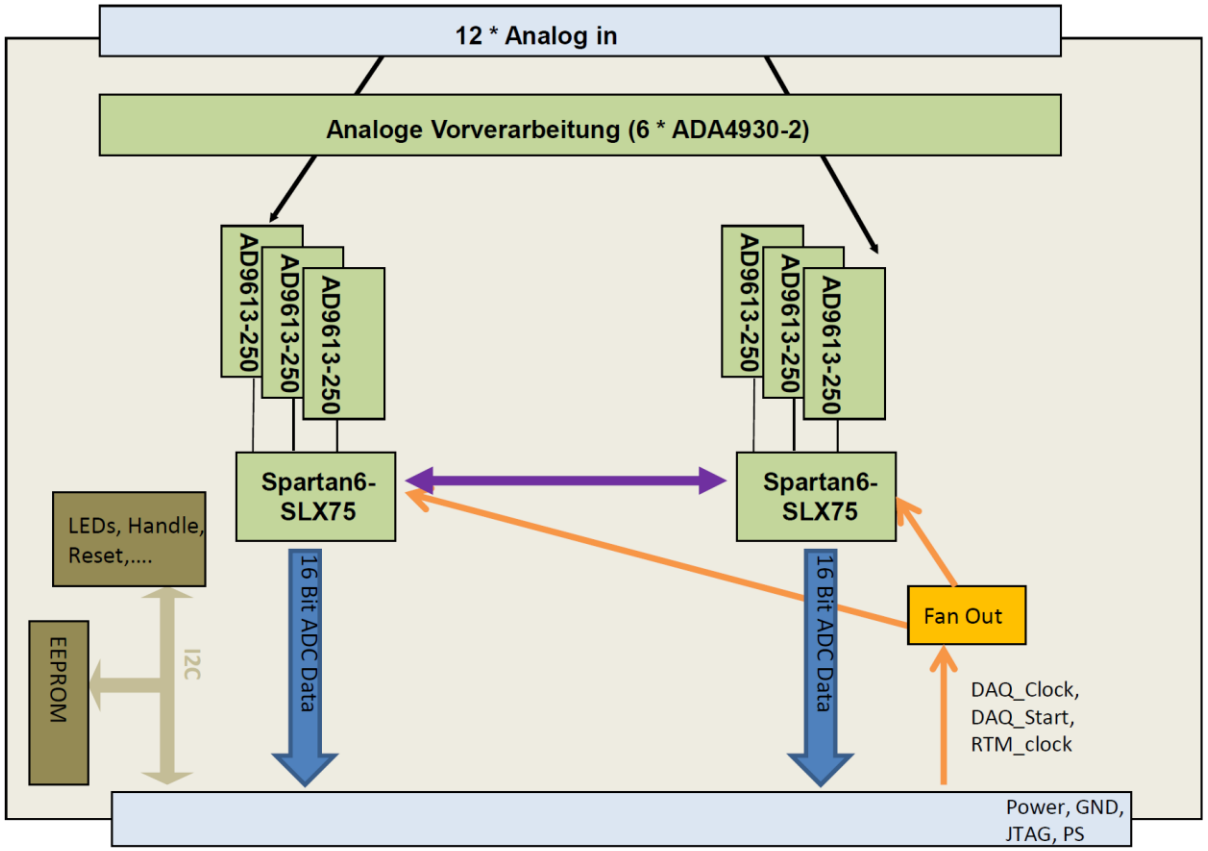
- Existing WASA electronics to slow for free running mode with larger number of straws
- Final System: ATCA with 200 ADC channels/module
  - High development effort and too expensive for test systems

⇒Use MicroTCA as an intermediate system for prototype testing

⇒Development of an RTM for the HGF AMC with sampling ADCs is required

  - 12 channels (Space for SMA connectors + power budget)
  - 250 MHz Sampling Rate
  - Low level feature extraction on Spartan6
  - High Level functions on Kintex7 (HGF-AMC)

12 Channel Sampling ADC RTM for PANDA STT tests



- Common Fund Project: Promotes the HGF-AMC and proves its applicability
- Status: delayed, schematics about 70% finished