JÜLICH
FORSCHUNGSZENTRUM

Modulator Drivers

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Modulators

Mach-Zehnder modulators (as opposed to directly modulated Laser diodes)

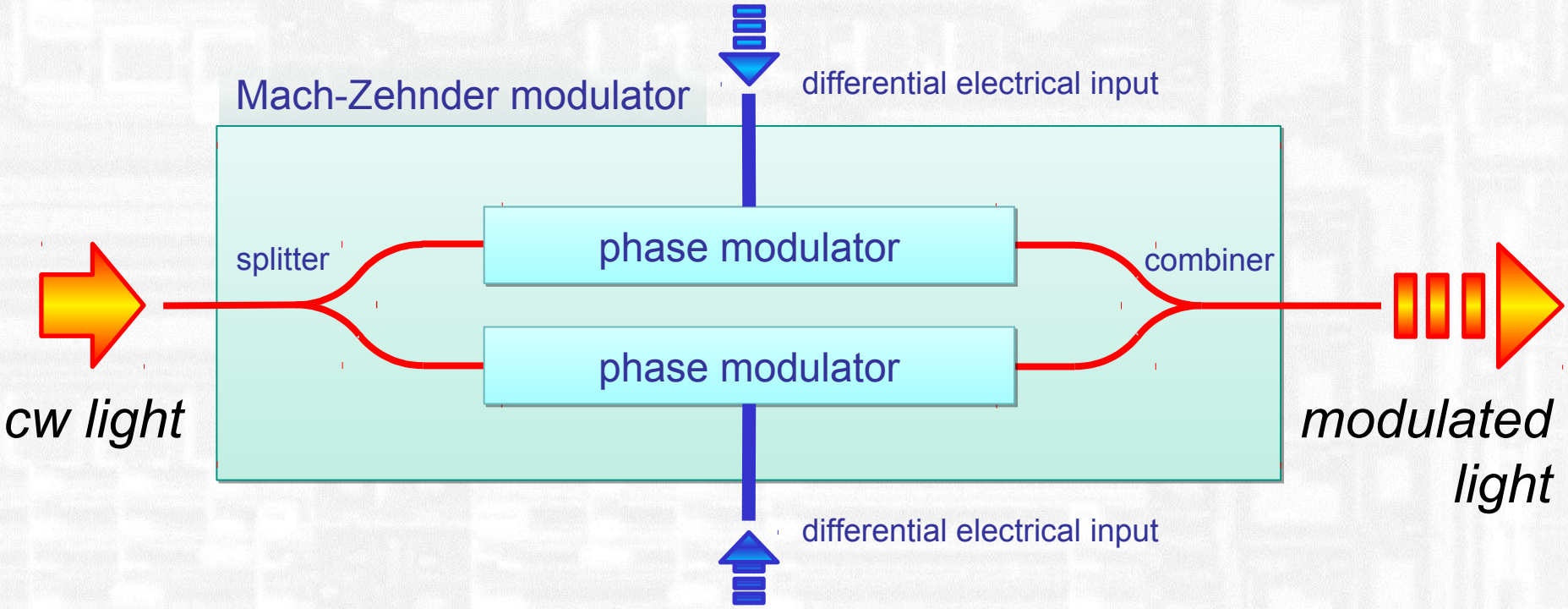
High speeds (up to 40GHz), multiple wavelengths

Target area: detector readout

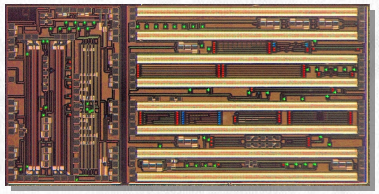
Goal: compact design, integration with frontend ASICs

Mach-Zehnder modulator

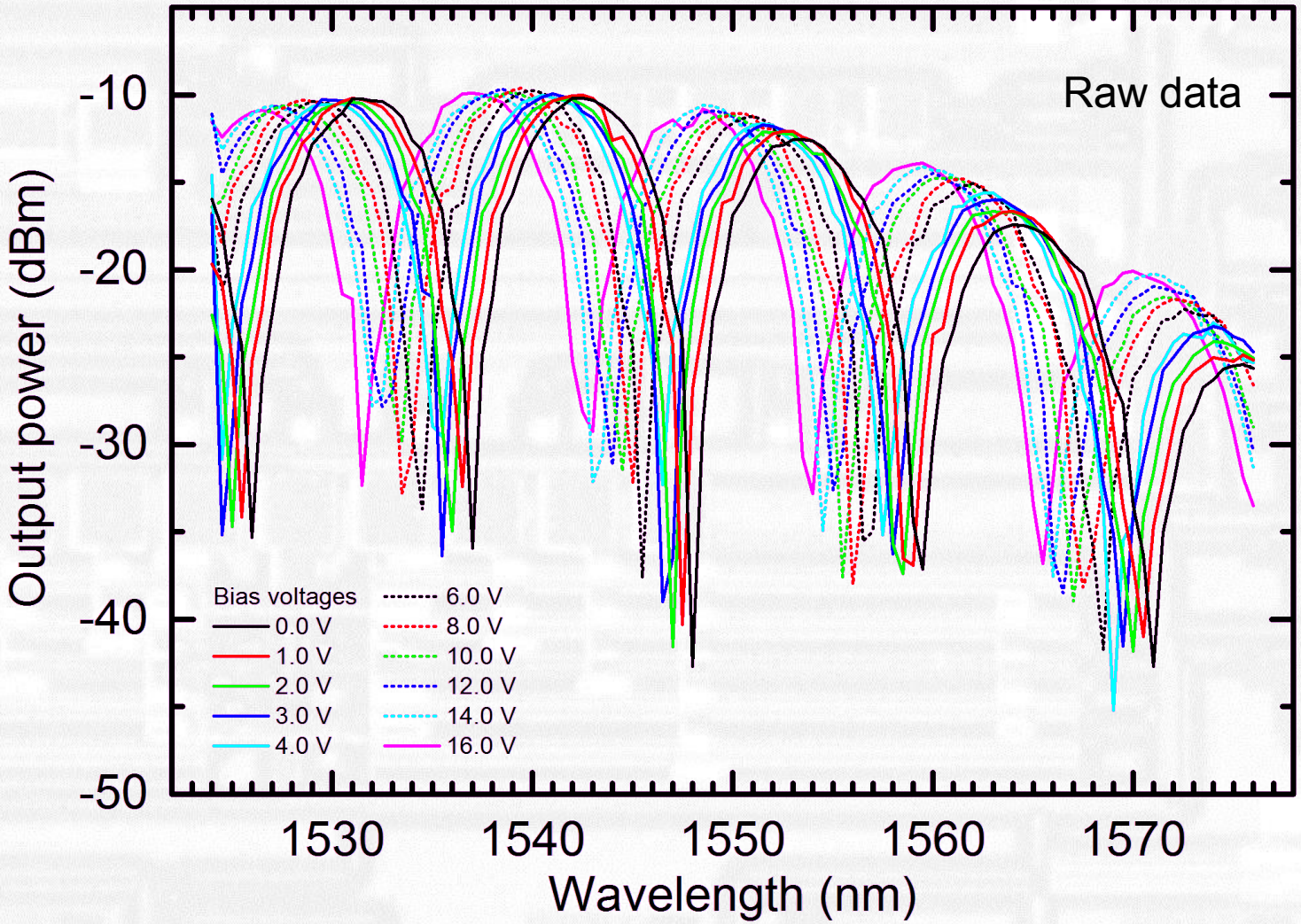
“Classic” Mach-Zehnder modulator



Characterizations



pn-modulators



SOH Modulator?

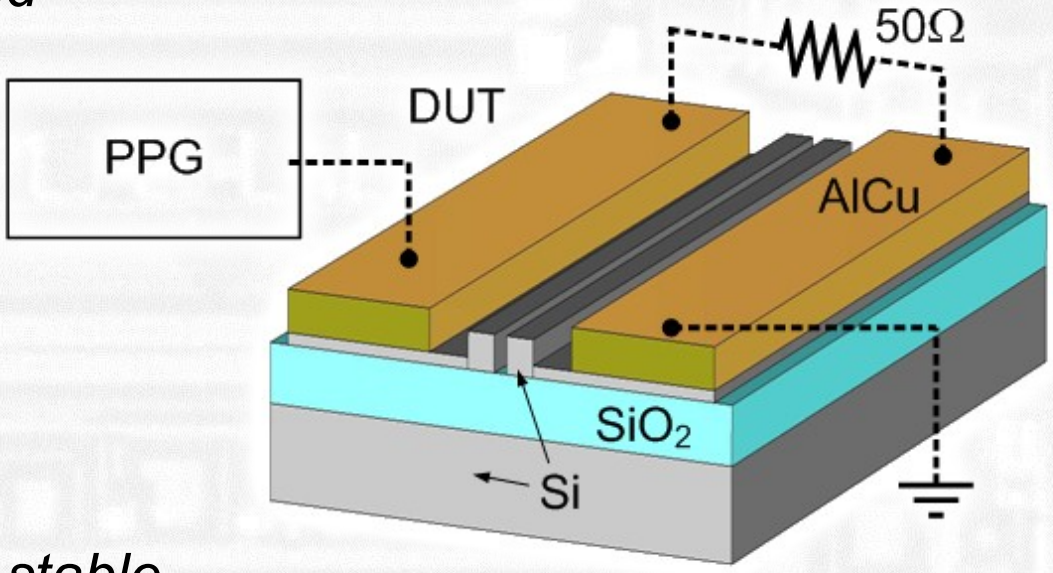
SOH = Silicon Organic Hybrid

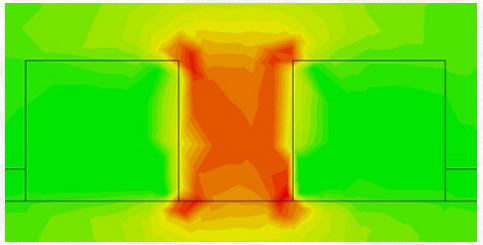
Pros:

- *Fast*
- *Efficient*
- *Simple in principle (single type doping)*

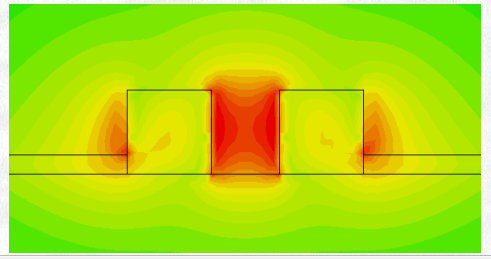
Cons:

- *Polymer not yet long term stable*
- *Polymer not radiation hard (expected)*
- *Deep waveguide slot difficult to fabricate*





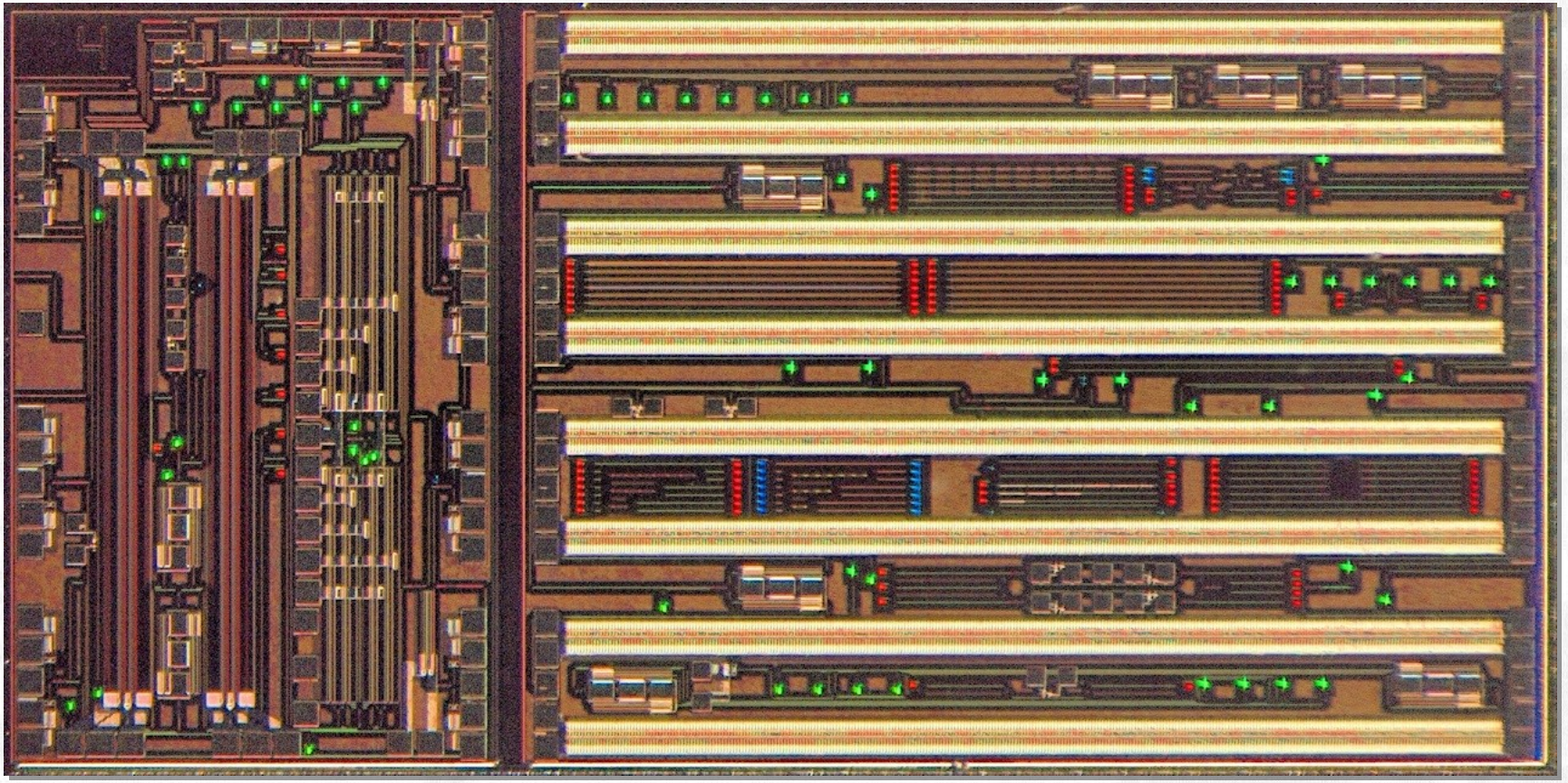
Sim. electr. field



Sim. optical field

Modulator Chip

Chip with different modulator types and Ge-Photodiodes



Real chip

Modulator-Fiber Coupling

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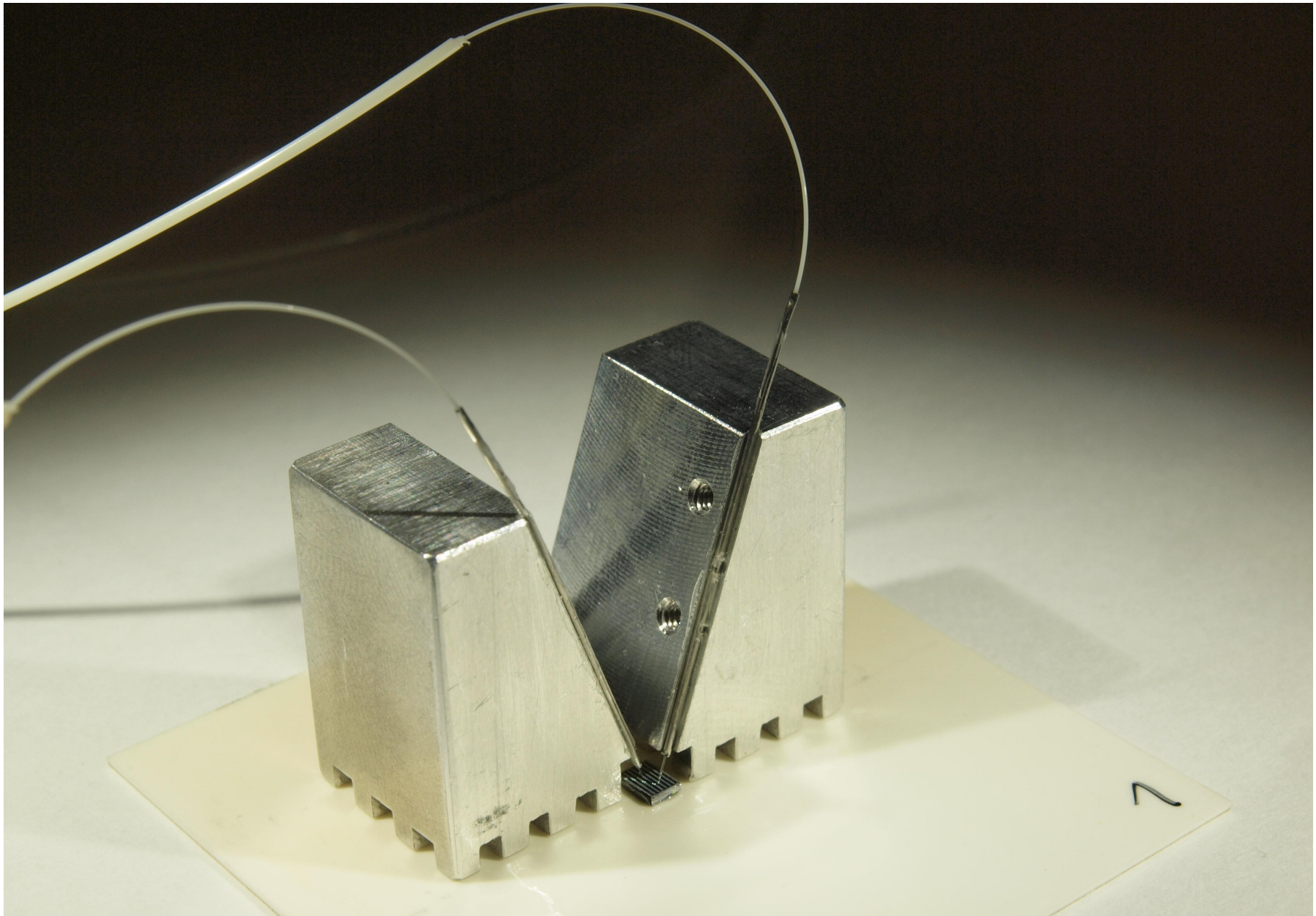
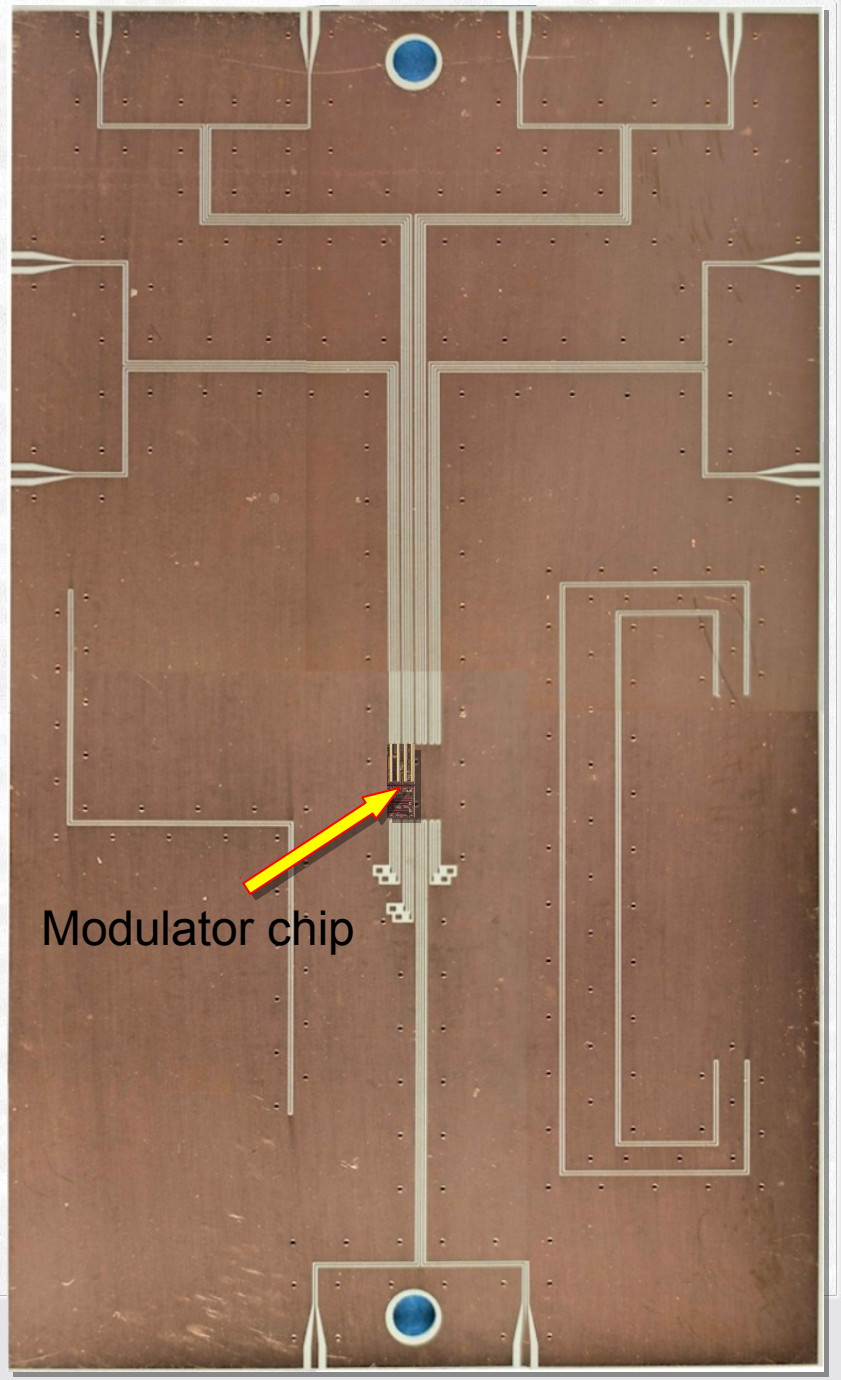


Test System

Modulator chip carrier board with RF transmission lines

- *Grounded coplanar design*
- *50 µm line width*
- *50 µm spacing*
- *Substrate: RT-Duroid 6010LM*
  - *Thickness: 0.63 mm*
  - *Copper thickness: 35 µm*



Modulator Driver Selection Criteria

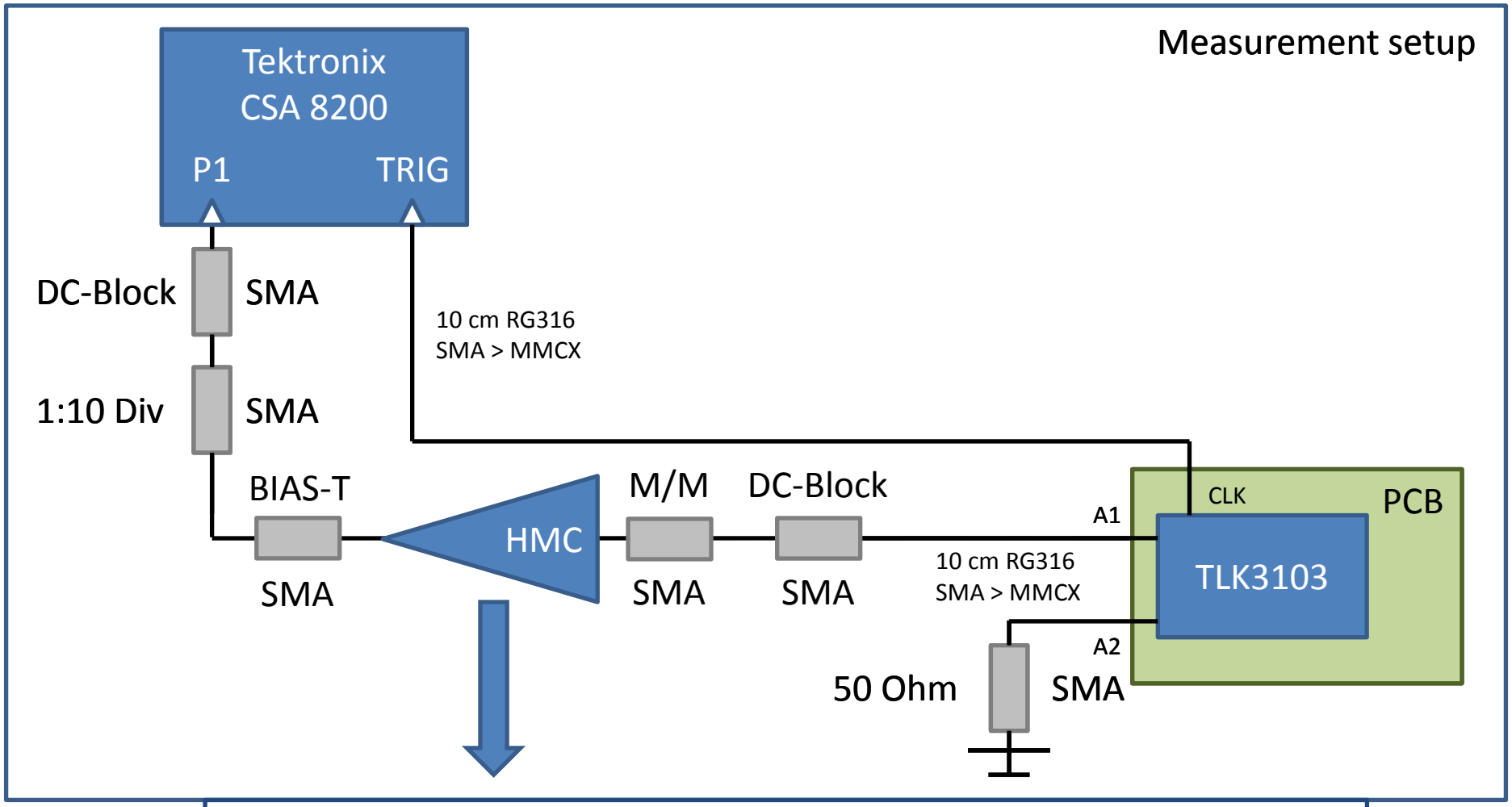
- Output voltage
  (impedance of modulators was uncertain, frequency was no limitation)

- Eval board available
  (3 voltages necessary, one through bias-T, power-up sequence)

- S-parameters available (w/o NDA)

  Chosen: HMC870LC5 (Hittite)

Eyediagramm
TI-PRBS and HMC870LC5

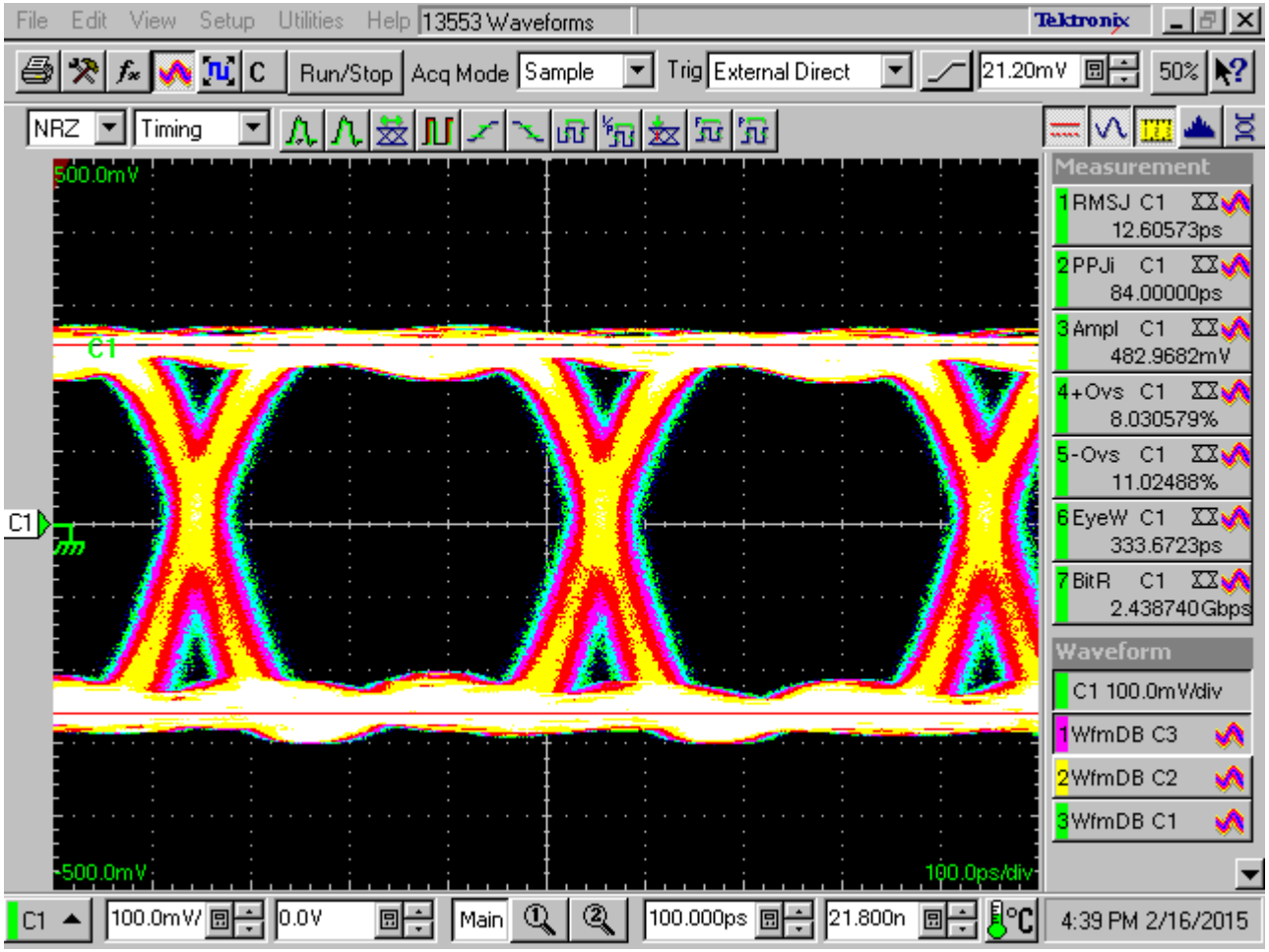


2 Bias Conditions for HMC870LC5:

BIAS 1: VDD = 3.3V, VCRTL = 1V, ID = 100 mA — Datasheet: 3.5V_{PP} output at 0.5 V_{PP} input

BIAS 2: VDD = 5V, VCRTL =1V, ID =140 mA — Datasheet: 7 V_{PP} output at 1.2 V_{PP} input

Eyediagramm
TI-PRBS and HMC870LC5



Eyediagramm, Port TI 3103: A1, Bias Condition: Bias 2, Amplifier #1

TI TLK3103 & HMC870LC5

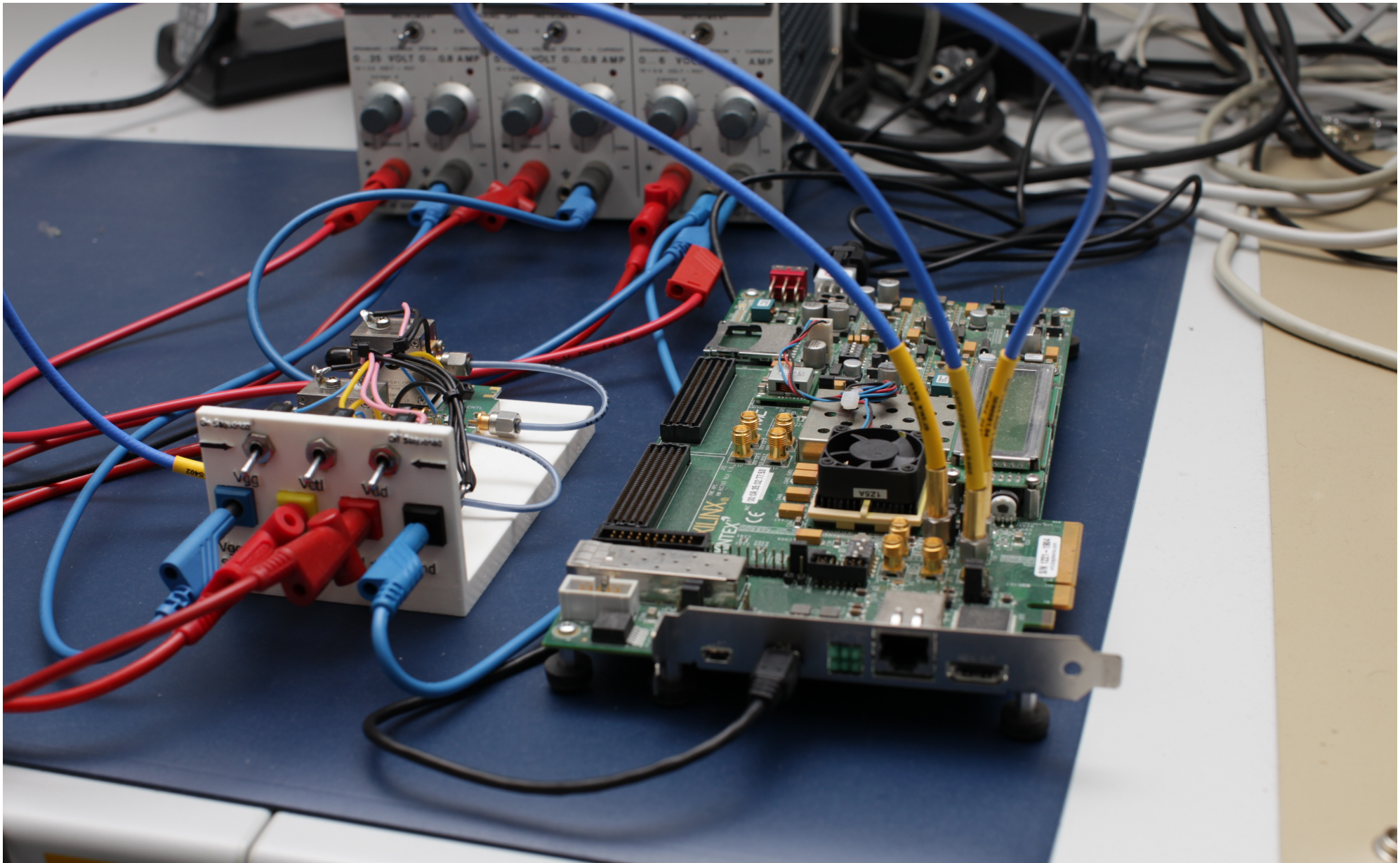
Amplifier #1, Bias 2	A1	A2
RMS Jitter	12.6 ps	12.64 ps
PP Jitter	84 ps	88 ps
Amplitude + overshoot	4.83 V	4.93 V
Overshoot +	8 %	8.2 %
Overshoot -	11 %	8.8 %
Transfer rate	2.5 Gbit/s	1.25 Gbit/s
Amplifier #2, Bias 2		
RMS Jitter	17.5 ps	13.4 ps
PP Jitter	126 ps	92 ps
Amplitude + overshoot	4.63 V	4.64 V
Overshoot +	8.7 %	9.3 %
Overshoot -	11 %	8.5 %
Transfer rate	2.5 Gbit/s	2.5 Gbit/s
	A2 terminated	A1 terminated

Jülich contributions

Modulator technology, assembly and measurements done by KIT

FZJ helped with:
- modulator driver component selection
- initial simulation
- high-speed PCB layout
- verification of electrical measurements

Jülich test 1/2



Jülich test 2/2