PICMG xTCA for Physics

Standard Hardware API (SHAPI)

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for the
Matter and Technologies Kickoff Meeting
DESY Hamburg

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The Goal

Curtesy: Struck Innovative Systems

Who are you?
Which version?
What can you do?
What are you doing?
What functions can you perform?

A standard Hardware API architecture for use in xTCA Community

- structural and methodological approach to device access;
- promote interoperability between hardware and software developed in different institutions;

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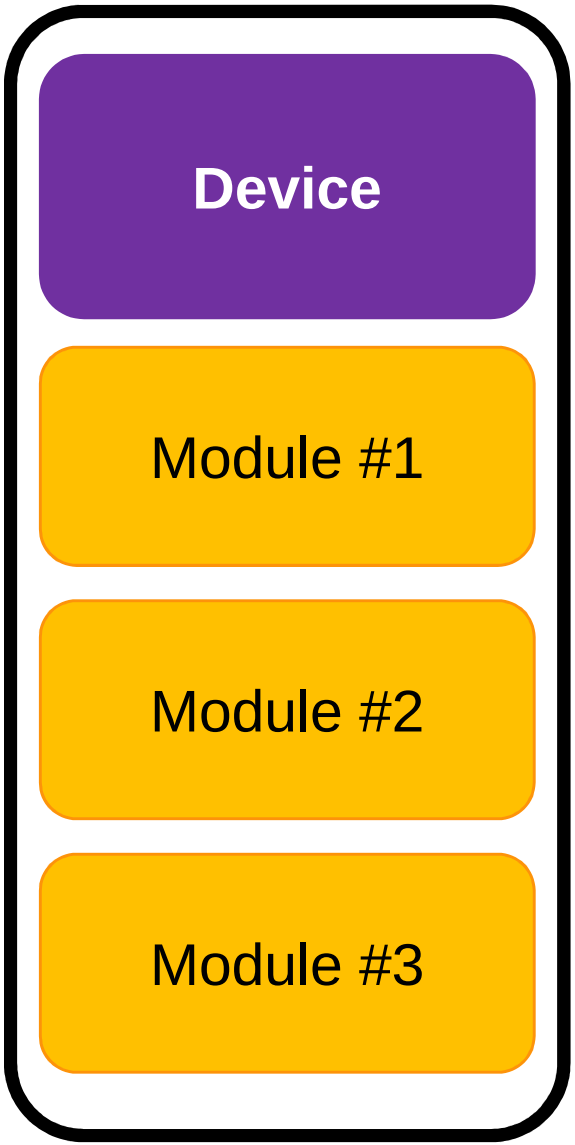
Overview of Addressable I/O space



- Standard set of registers that will
  - Identify the Hardware, Version and Vendor
  - Status and control of capabilities
  - Identify and control of device Interrupts
  - Addresses of all modules implemented
    - ➔ Identify the Module, Version and Vendor
    - ➔ Status and control of capabilities of module
    - ➔ Interrupts it can generate

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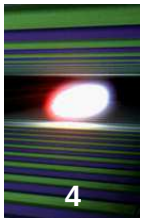
Current XFEL/DESY Standard Register Set



Addressable I/O space through which various devices functions may be managed

- The fundamental data access element is a *register*
- *Registers* are 32 bit wide

Standard registers that identify **Device**

Board Magic Word
Board ID
RESERVED #1
RESERVED #2
HW Version
RESERVED #3
First Project Address

Standard registers for each **Project**

Project Magic Word
Project ID1
Project Version
Project Date
User register
Project Reset
Next Project Address

Board Standard register Set

Board Magic Word
Board ID
RESERVED #1
RESERVED #2
HW Version
RESERVED #3
First Project Address

First Register indicates that Standard register set is being used

Board ID identifies the Board we are communicating with

Hardware Version to identify different Board models

Relative Address to first project in the Device

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Project Standard Set

Project Magic Word
Project ID1
Project Version
Project Date
User register
Project Reset
Next Project Address
Proj. Register #1
Proj. Register #2.1
Proj. Register #2.2
…

First Register indicates that Project follows standard register set

Project ID identifies firmware **OR** special module:

- Which Driver to use
- DMA transfer block
- JTAG firmware uploader
- ….

Version and Date for control and software compatibility

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Project Standard Set

Project Magic Word
Project ID1
Project Version
Project Date
User register
Project Reset
Next Project Address
Proj. Register #1
Proj. Register #2.1
Proj. Register #2.2
…

Soft Reset of Project – reset of state machines and not configurations

Registers that are implemented by developer/vendor (optional)

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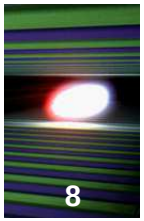
Addresses of Projects



Board Magic Word
Board ID
RESERVED #1
RESERVED #2
HW Version
RESERVED #3
First Project Address

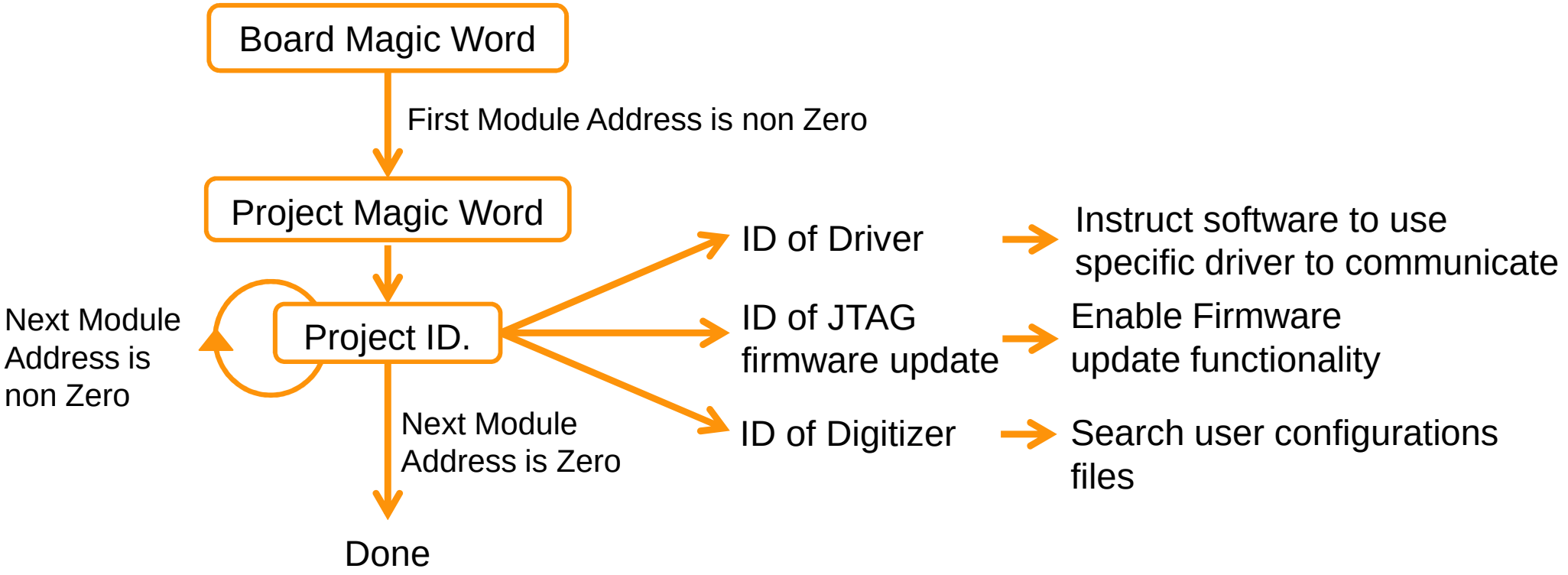
Absolute Offset to first module

Project Magic Word
Project ID1
Project Version
Project Date
User register
Project Reset
Next Project Address
Project User Register #1
Project User Register #2
....

Value Zero – no more modules

Value non Zero – absolute offset to next module

Software communication



- Mapping of all Projects defined on the Device
- Search Project configuration file (based on version and driver name)
- Software functionalities are activated only when certain projects are present in the device

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SHAPI Document

The **SHAPI Design Guide** will convey ideas already in use in different institutions:

- Device and Modules structure
- Register with (relative) addresses to Modules
- Unique group that will assign Device/Standard Modules IDs
  - Online information (manuals/guides/contacts)
- Standard set of Device/Module capabilities
- Standard set to deal with Interrupts

Questions/Suggestions?

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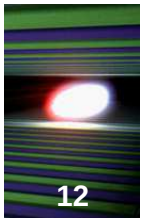
Clip board – copy and paste



Headline

- first level
  - second level
    - ➔ third level

Headline

Text Text
Text Text

Keyword

1. Keyword
2. Keyword

- Keyword
- Keyword

Result Headline

- Text
- Text

Result Headline

Text
Text

Result Headline

- Text
- Text