3D ASIC development

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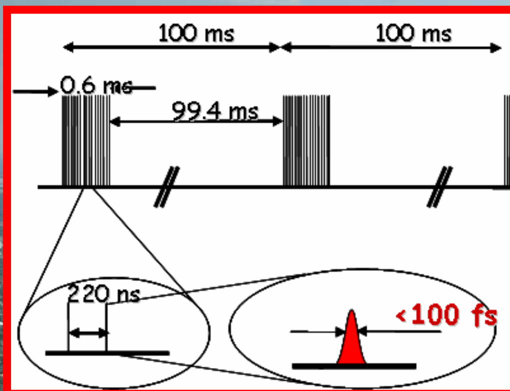
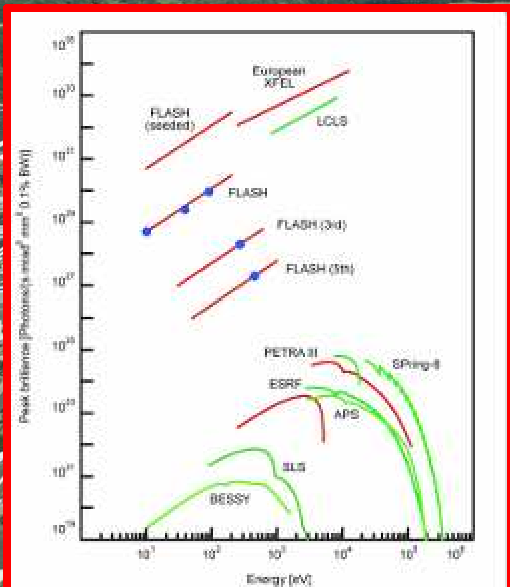
on behalf of the AGIPD collaboration

Outline

- The goal and the obstacles to overcome
  - X-ray sensors for advanced FEL
  - Adaptive Gain Integrating Pixel Detector (AGIPD)
  - 3DIC: a possible path to the solution
- Design and test of 2-tier detector prototype
  - TSVs & tier-to-tier contacts
  - vertically integrated test circuits, matrix prototype
- Conclusion

The Motivation





1Mpixel, 200 µm pitch
Adaptable Gain o(100)
single-photon resolution
10^4 ph dyn rng
Rad tol 100MGy~1GGy
Burst imaging 4.5Mfps
(tested upto 6.5Mfps)
In-pixel Memory (352 img)

The Motivation

2700 pulses
@4.5MHz
every 100ms

352 images
storing
capability

challenging radiation
environment

rad tolerant
design mandatory

spatial resolution
desiderata

200um pixel pitch

A possible solution (long term goal)

1) bump-bond to the detector

tech #1
(CMOS Low Pow)

2) amplification &
double sampling

5) digital
signal
readout

tech #2
(CMOS High Perf)

3) ADConversion

tech #3
(DRAM)

4) store the digitalized signal
in a digital memory cell (on
multiple layers)

The first step

1) bump-bond to the detector

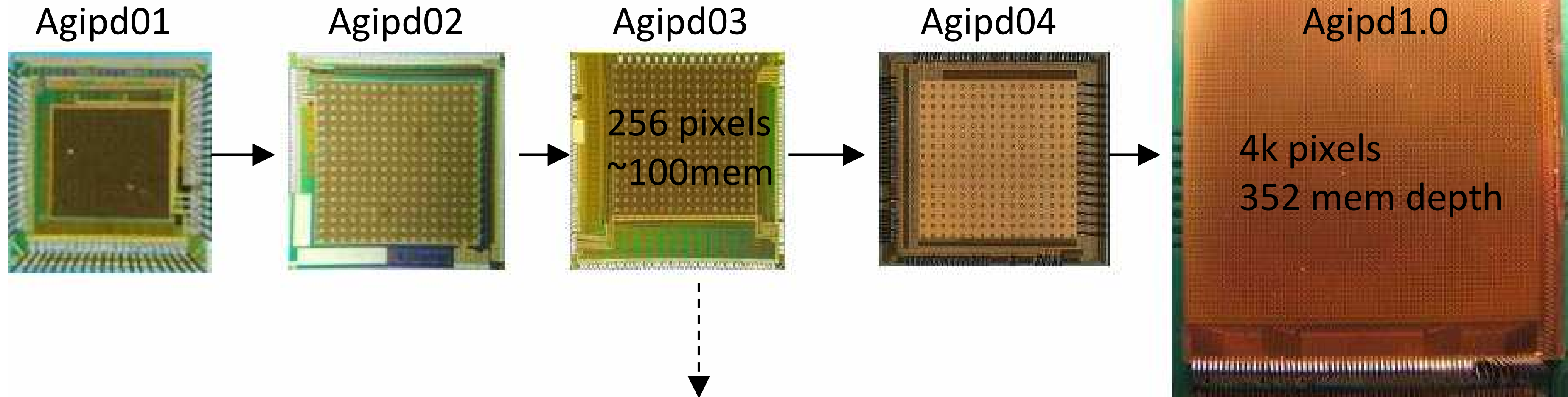
2) amplification & double sampling

3) store the analog signal in a memory cell in the appropriate layer

4) signal readout

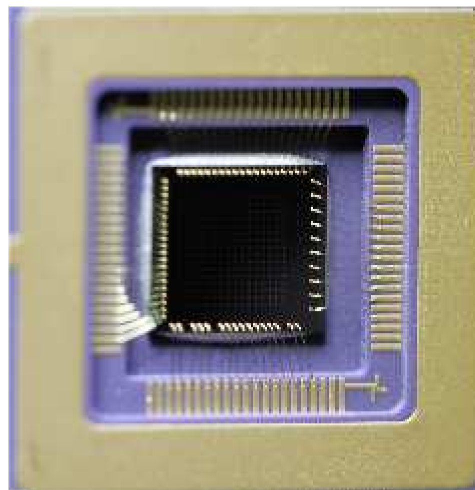
same tech (CMOS Low Pow)

A path toward the solution



GF 130nm CMOS Low Power
ARM SC library
Tezzaron FaStack
double-tier

T13C11 MPWrun, via CMP
submitted 2011
delivered Jan 2014



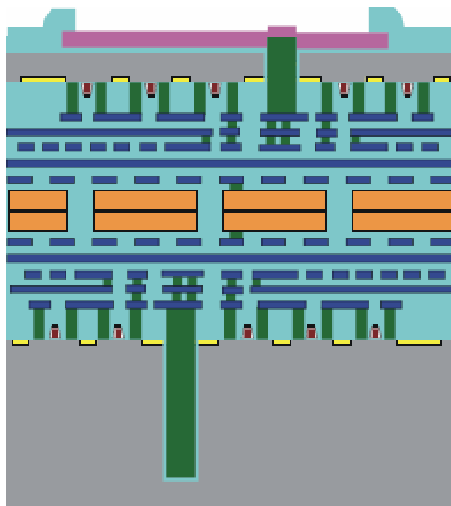
3D-AGIPD0

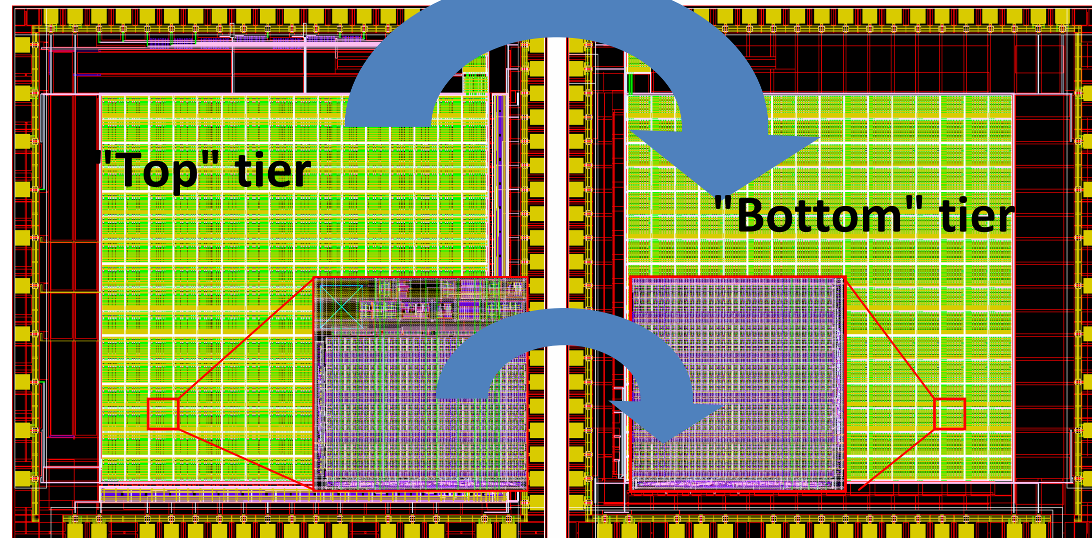
test structures +
256 pixels matrix
200um pitch
544 mem depth

simplified architecture: fixed gain (but reserving the space for multiple-gain circuits; equivalent memcell area)

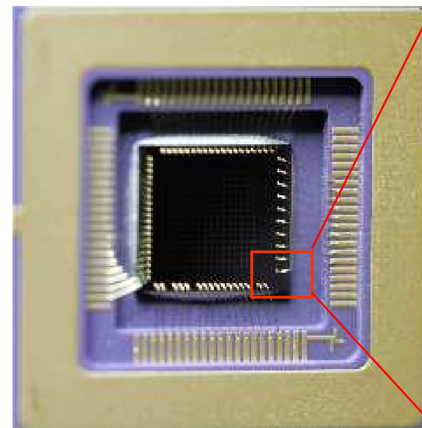
The process at a glance

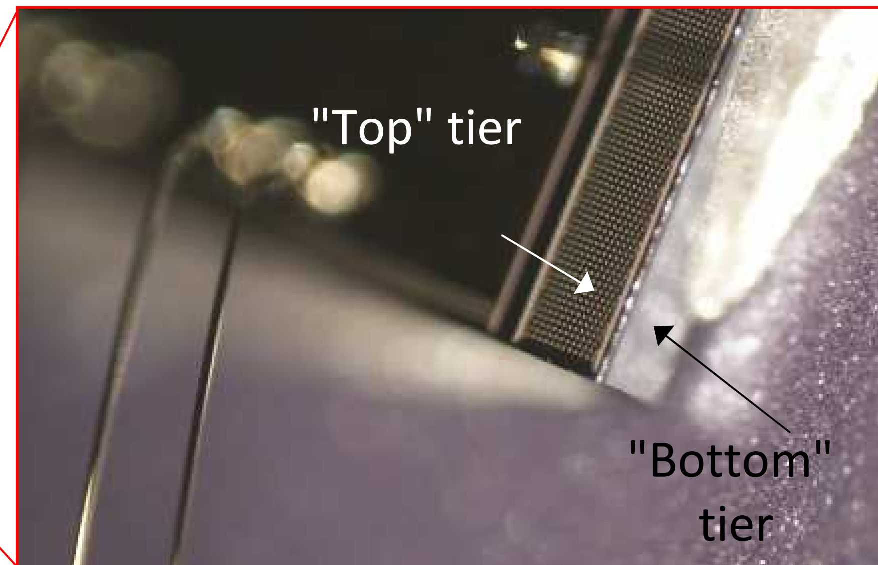
Tezzaron process used





- 2x planar chip manufacture
  - via-middle TSVs
- stacking and face-to-face coupling
- back-grinding of the top tier and exposition of the TSVs
- Pad definition

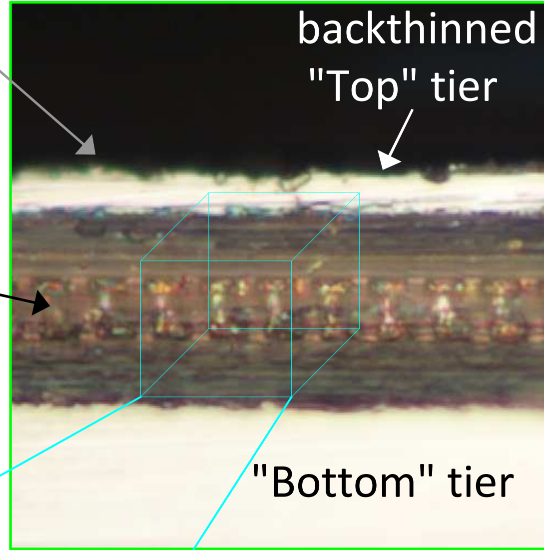


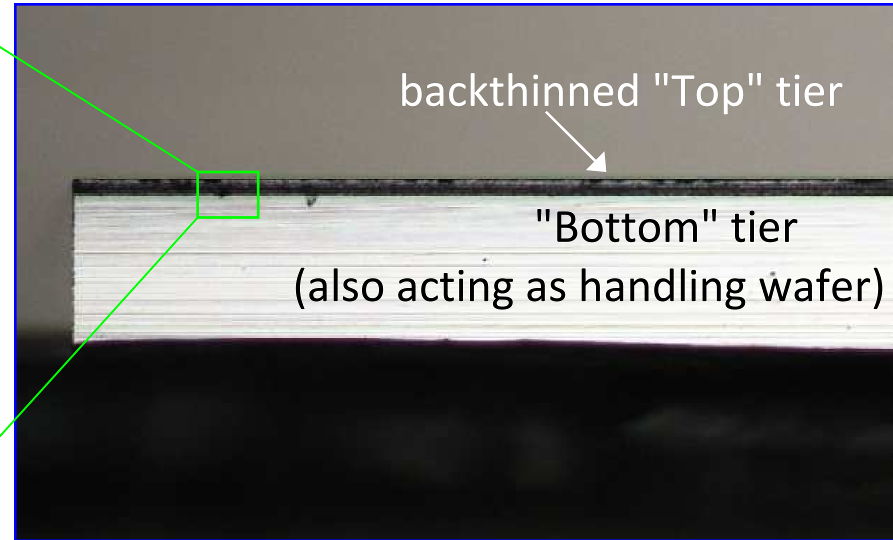


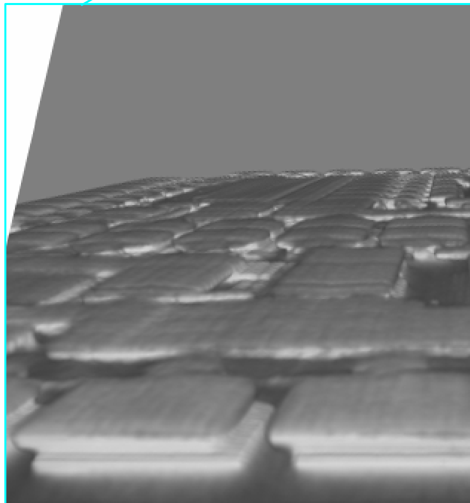
The process at a glance

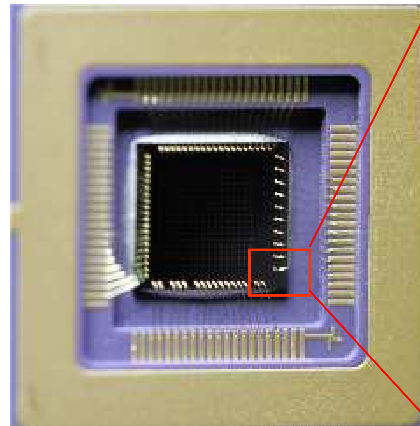
Al wire/bump bonding pads

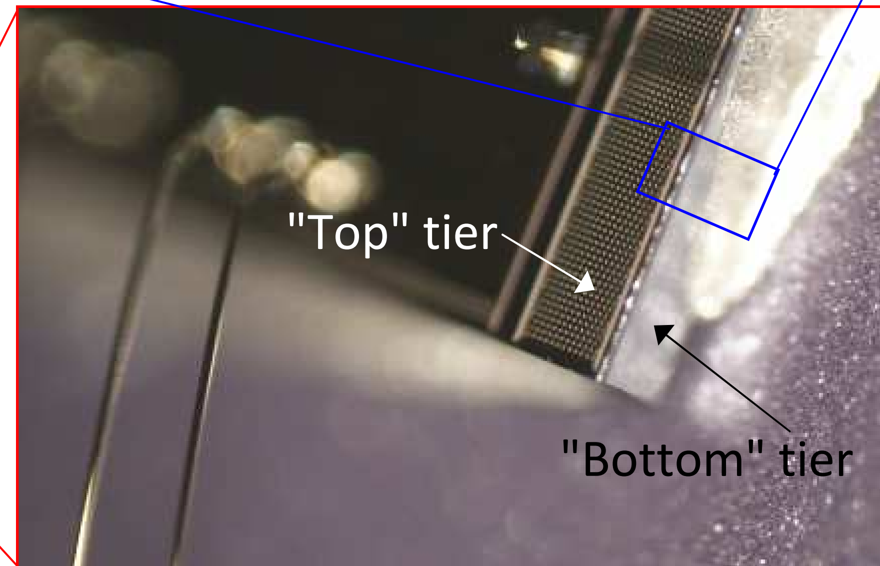
tier-to-tier contacts











pixel architecture

chip architecture

Pads accessible (by TSVs)

2D-test circuits

single pixel structure
(with probe points)

bump-bond pads (accessible by TSVs)

TSV & tier-to tier contact
daisy chains

256-pixel matrix

signal proc.

analog storage

tier-to-tier contacts

analog
storage

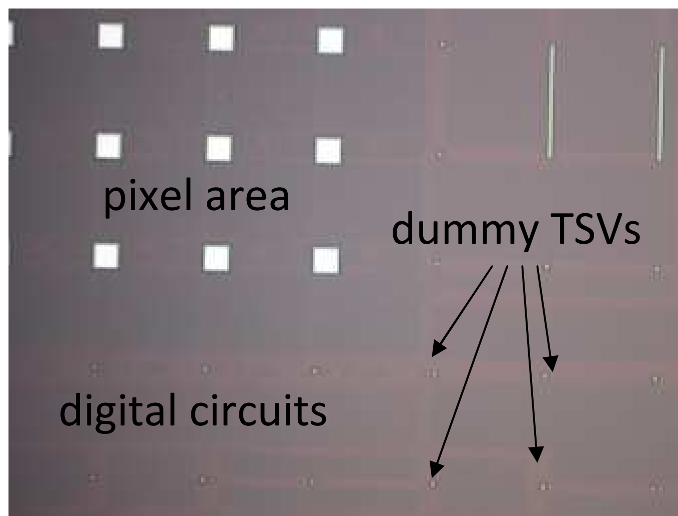
SC-based addressing circuit (distributed on both tiers)
both at the pixel level and at the array level

TSV contacts evaluation

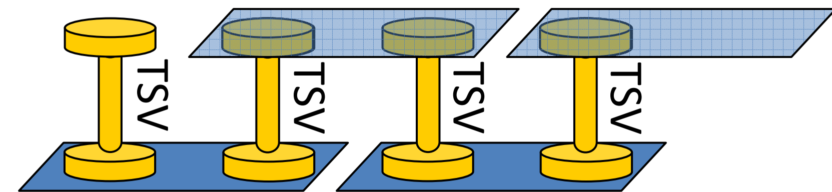
"via middle" TSVs Ø 1.2 um , landing on M1

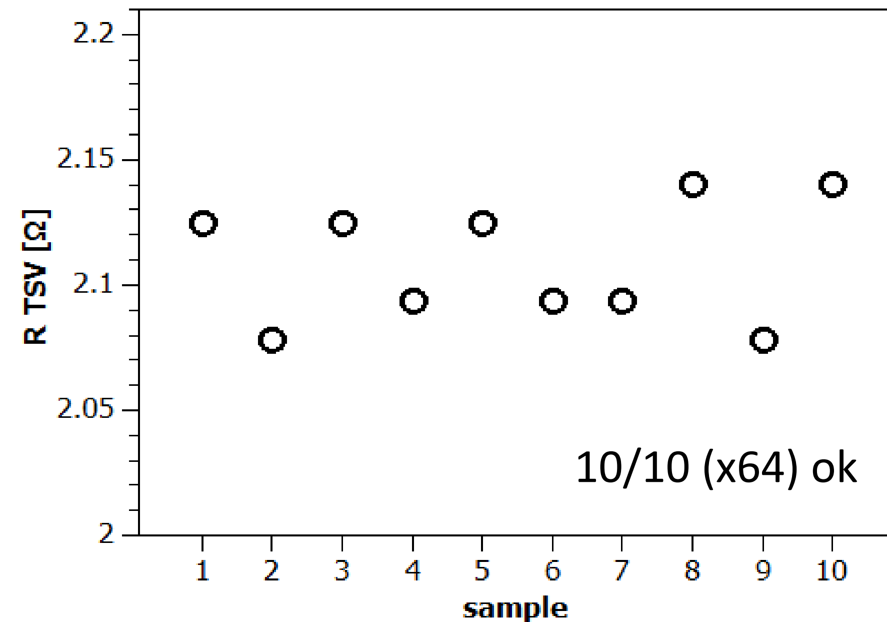
locally: TSV-to-TSV distance down to ~4um
however, globally: "uniform" density of TSVs recommended ($\rightarrow$ uniform resistance to grinding)

$\rightarrow$ designer constraint: dummy TSVs



10x test structure for TSV evaluation: daisy chain of 64 TSVs, by connected M1/backM.



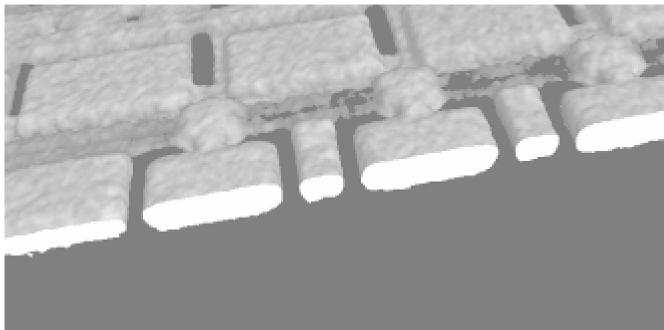


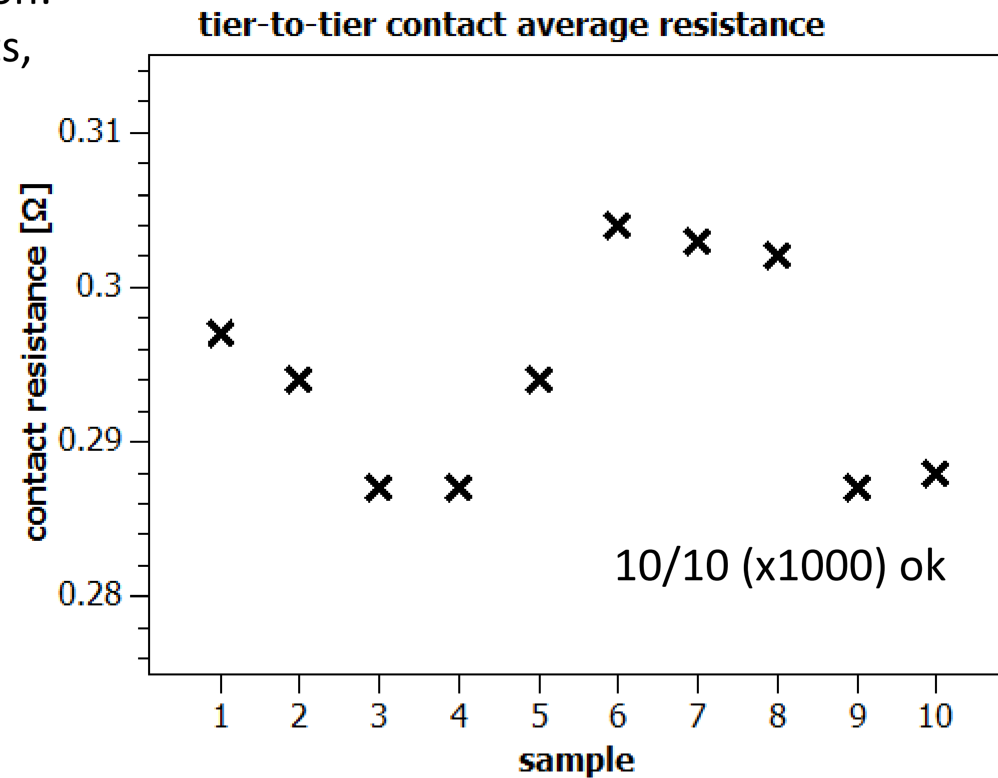
measured on 10 packaged samples
no broken chain, avg R 2.1Ω /TSV

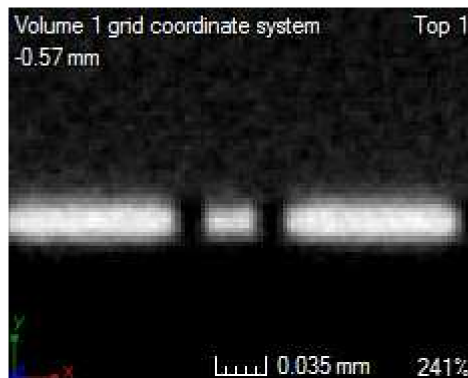
Tier-to-tier contact evaluation

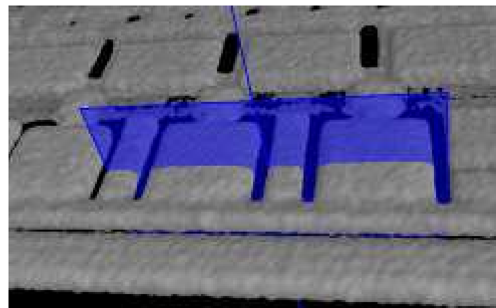
10x test structure for contact evaluation:
daisy chain of 1000 tier-to-tier contacts,
connected in series using M5.

measured independently
on 10 packaged samples
no broken chain



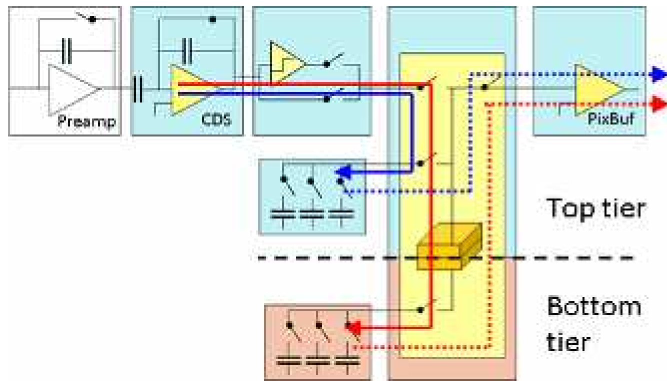


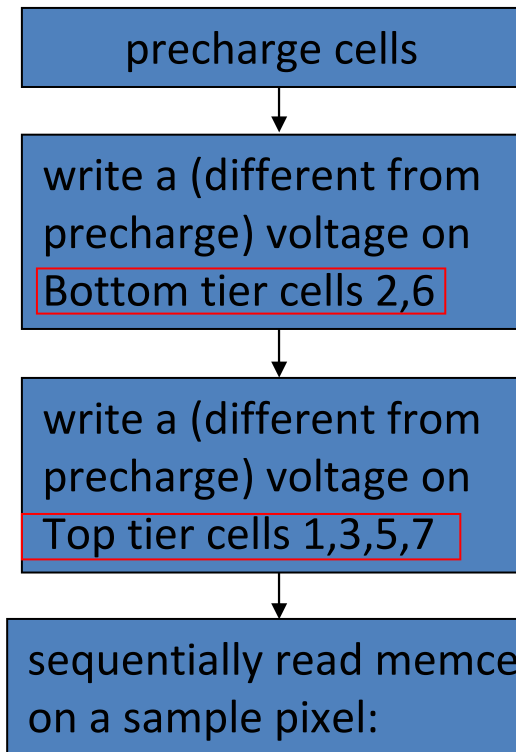


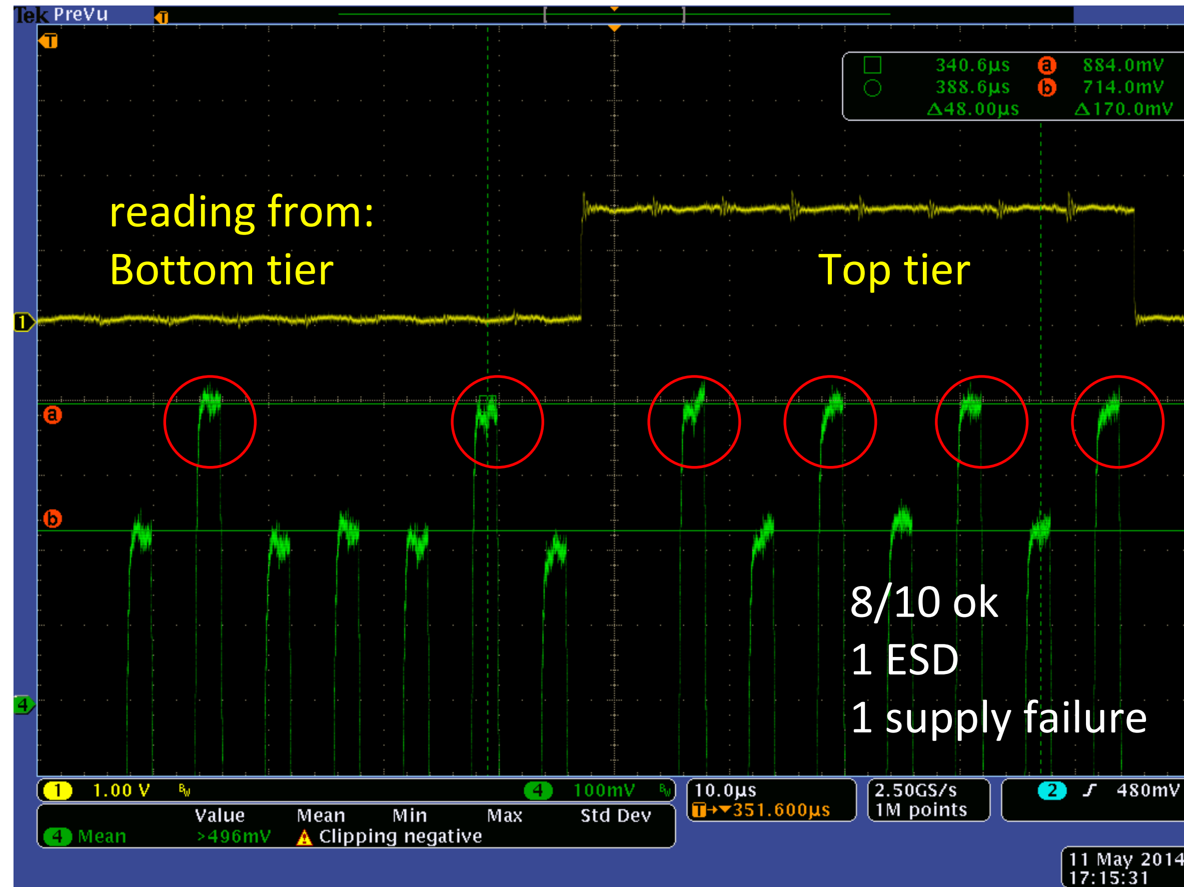


x-ray tomography (F. Beckmann, DESY) also suggest better alignment

Pixel matrix write-read example

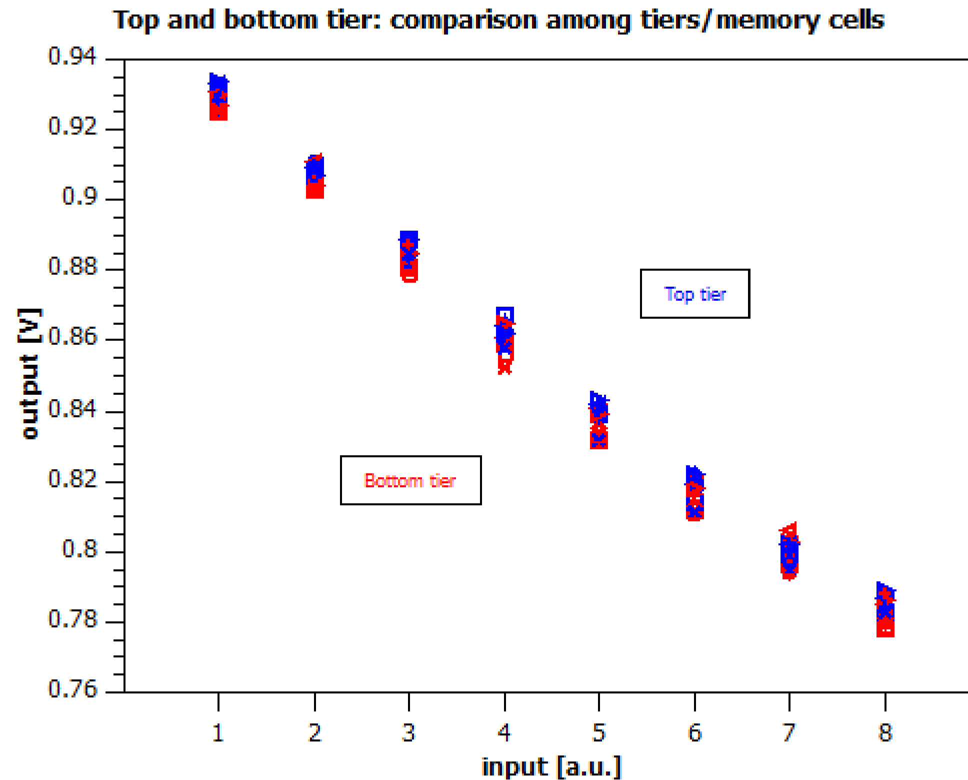




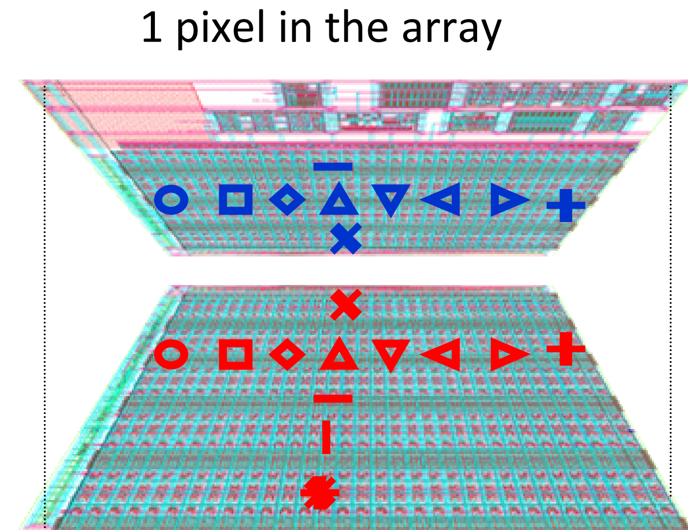


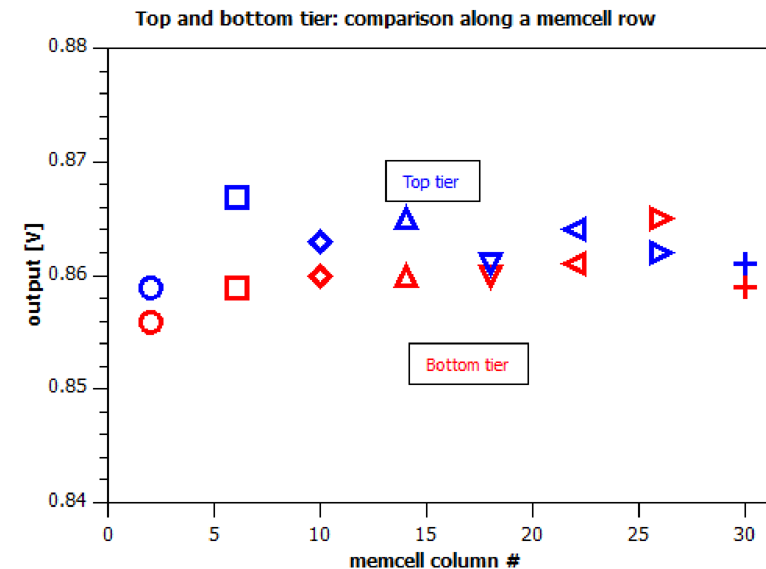
Bottom,1 Bottom,2 Bottom,3 Bottom,4 Bottom,5 Bottom,6 Bottom,7 Top,1 Top,2 Top,3 Top,4 Top,5 Top,6 Top,7

Top/Bottom tier: memory cell-to-memory cell variations



1 pixel in the array





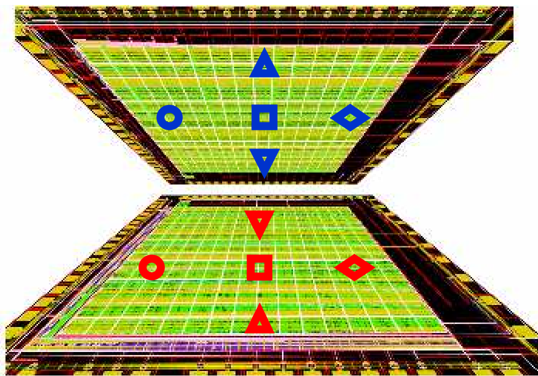
Comparable (linear) detector response

- for charge stored in either in Top/Bottom tier
- for different memory cells in the same pixel

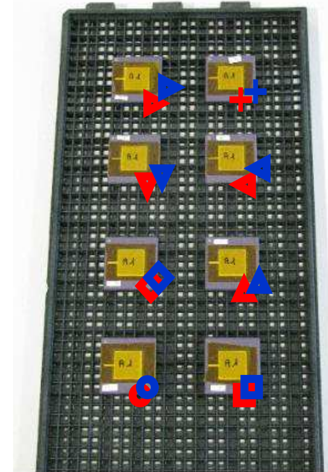
Slight pedestal offset, to be investigated further

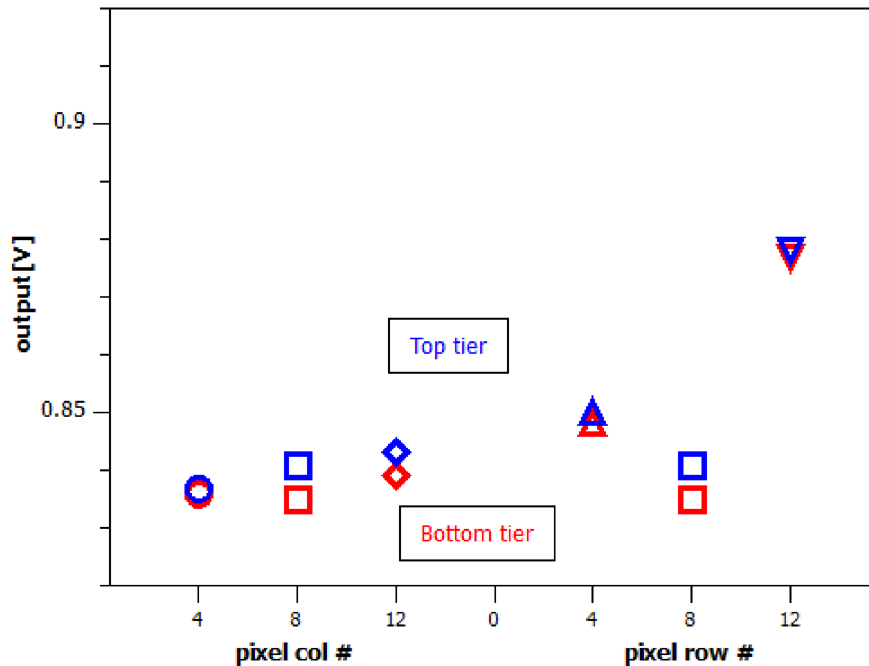
8/10 samples ok

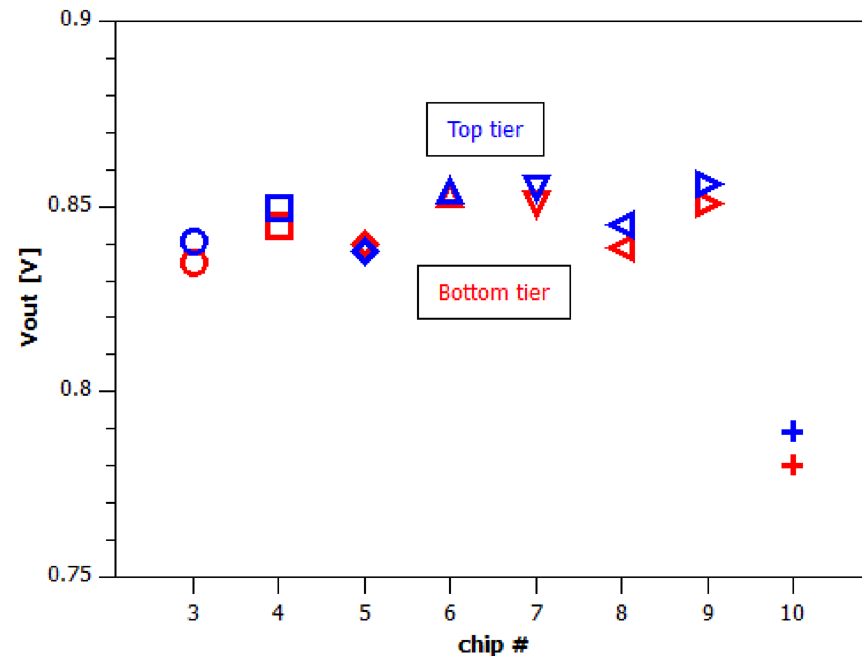
Top/Bottom tier: pixel-to-pixel & chip-to-chip variations



Different pixels/samples: slightly higher variations. However, outputs from memory cells in the Top/Bottom tier of the same pixel remain similar.
Process parameter dispersion in the active pixel circuitry is suspected.
Per-pixel calibration in any case needed.







Conclusion

Extending photon science detectors in the third dimension:

- the 3D-AGIPD case

Prototype produced: T13C11 3DIC MPW run (through CMP)

- GF130nm tech, Tezzaron 3D-process, 2 tiers, face-to-face
- 256 pixel array (200um, 544 images memory depth) + test structures

First evaluations

- good TSV, tier-to-tier contact characteristics (100% of tested)
- 8/10 samples with pixel array working as expected

Experience $\rightarrow$ pros and cons of this approach to vertical integration

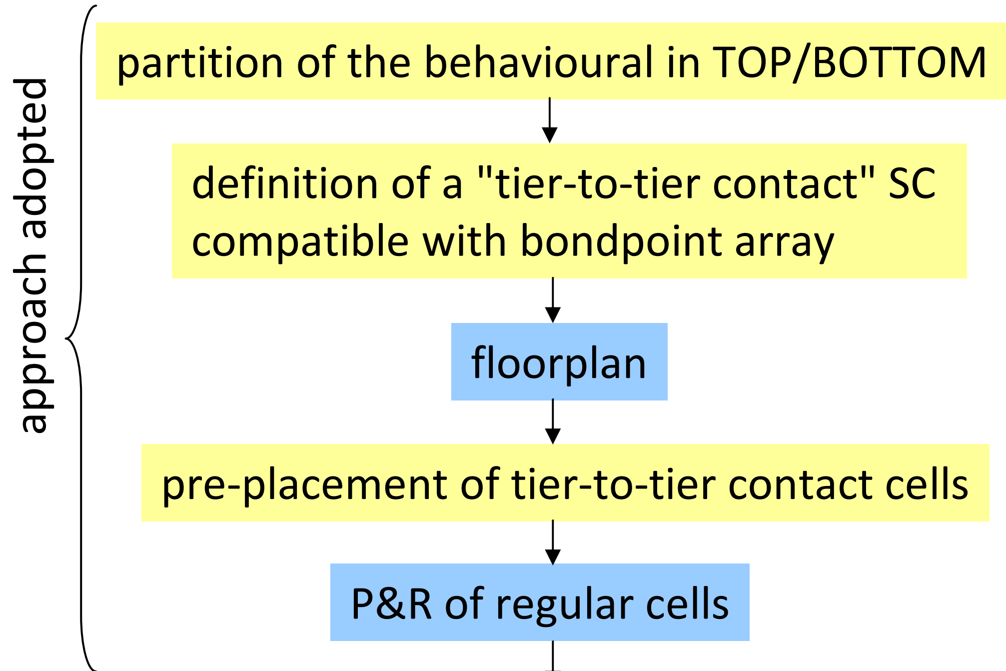
- ➢ long turnover times, delays
- ➢ limited availability out of US
- ➢ presently: 2 tiers

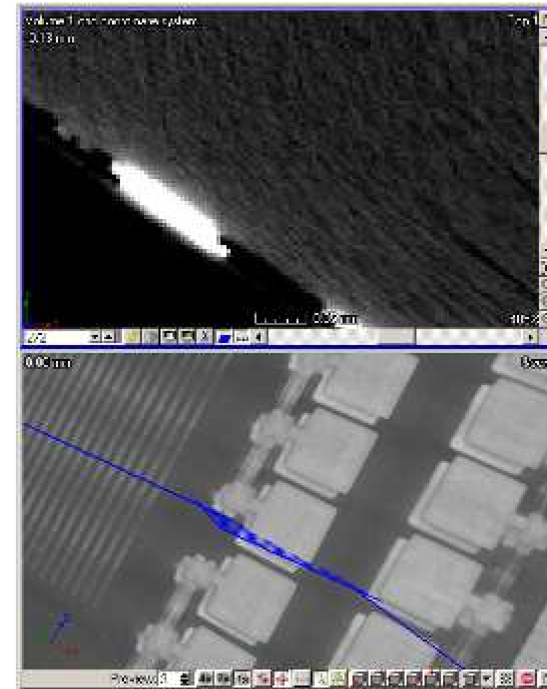
- ✓ it works
- ✓ 2D manufacture, 3D post-processes in one package (transparent to customer)
- ✓ high vert-interconnection density

Backup

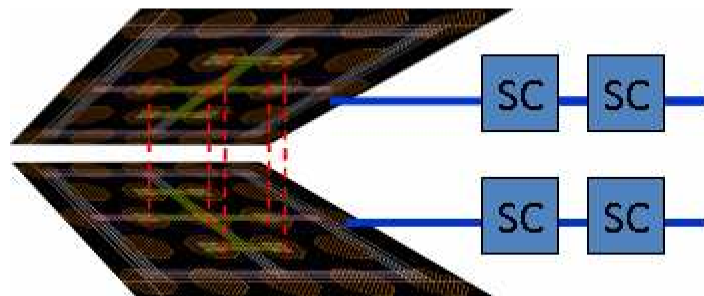
Tier-to-tier contacts

Cu-bondpoints (M6) used for tier-to-tier connectivity

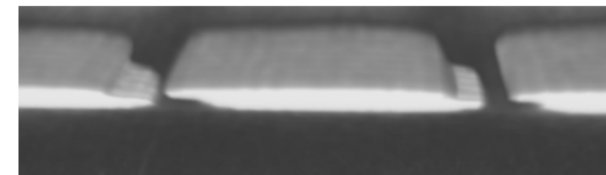




M^3APS (courtesy of INFN-Perugia)
submitted end 2009
Tomography by F. Beckmann (DESY)



tier-to-tier contact redundancy was suggested by 2009 MPW experience, to counter eventual tier misalignment



however ...