Minutes of Strip CMOS sensor progress report meeting, V.0

*2014-10-28*

*Present: A.Blue, D. Muenstermann, D. Bortoletto, I. Mandic, I.Gregor, M.Stanitzki, R. Eber, S.Seidel, V.Fedeyev, J. John, J. Doppke, M. Warren, R. Nickerson, J. Zhang, T. Huffman, Z. Liang, C. Buttar*

*Apologies: A. Grillo*

There was discussion of the AUW session, in particular the interaction with the pixel group, and finalization of the agenda.

The TJ submission final review was held last week, but was poorly attended, possibly due to overlap with Aix-les-Bains. Notes were distributed with a deadline for comments for today.

With regard to the chip distribution from AMS August submission it was agreed that CERN should get the chips initially and they would be distributed from RAL by Jens. Gert will be informed of this.

Sensor Status

It was reported that it would not be possible to produce the architectural AMS submission by the Nov 3rd multi-project deadline. This was already tight, but a computer problem caused a loss of 10 days at UCSC, making it impossible.

There was discussion surrounding how to proceed, which focused on two possibilities, one was to aim at the next multi-project run, which will probably be mid-Feb 2015, the other was to move straight to an engineering run, which would offer significant advantage, particularly in the choice of wafer resistivity and strip length. The possibility of sharing a run with other interested groups, including the pixels, was mooted. It was agreed this should be investigated urgently and the feasibility of funding this investigated.

The status of the chip design is that8-strip region that a design exists which can readout up to 8 hits/BC and the SLAC designers (Angelo and Pietro) have designed a fast LVDS-like driver with signal amplitude tunable in wide range which works in simulation at 320 Mbps BW. They are in process of designing receiver. This work will continue as it is needed in any plan.

The TJ review was reported on. Several different flavors of chip will be submitted on different substrates and collecting either holes or electrons. A summary of these is at:

<https://indico.desy.de/conferenceDisplay.py?confId=11133>

Testing Status

HVStrip1 was reported as working, with four motherboards ‘in the wild’ and two more requests. Extremely nice results were reported, both from a study at the diamond facility near RAL and also at KIT, where a first irradiation to 200Gy was performed with x-rays. The chips were also measured with Fe55 and Sr90 sources. Those involved were praised for the effort. Results are reported in the slides from the meeting. These first results are encouraging, but not yet precise enough to be definitive. The chip works and first results suggest reasonable uniformity between pixels and response within a pixel. At 200kGy the chip remains functional, but some concern was expressed at the apparent degradation in the Fe55 peak.

The status of designing a motherboard for testing the CHESS chip was discussed. This will be done by Oxford with RAL.